H.264 Encoder User Guide

Introduction

H.264 is a popular video compression standard for compression of digital video. It is also known as MPEG-4 Part10 or Advanced Video Coding (MPEG-4 AVC). H.264 uses block-wise approach for compressing the video where the block size is defined as 16 x 16 and is called a macro block. The compression standard supports various profiles that define the compression ratio and complexity of the implementation. The video frames, to be compressed, are treated as I frame, P frame, and B frame. An I frame is an intra-coded frame where compression is done by using the information contained within the frame. No other frames are required to decode an I frame. A P frame is compressed by using the changes with respect to an earlier frame that can be an I frame or a P frame. The compression of B frame is done by using the motion changes with respect to both an earlier frame and an upcoming frame.

The I and P frame compression process has four stages:

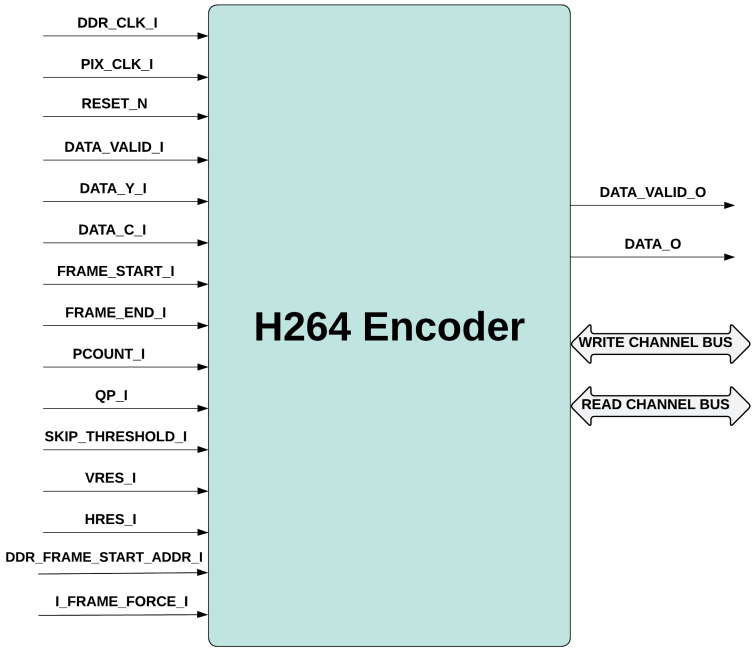
- Intra/Inter prediction
- Integer transformation
- Quantization
- Entropy encoding

H.264 supports two types of encoding:

- Context Adaptive Variable Length Coding (CAVLC)
- Context Adaptive Binary Arithmetic Coding (CABAC)

The current version of H.264 Encoder implements baseline profile and uses CAVLC for entropy encoding. Also, H.264 Encoder supports encoding of I and P frames.

Figure 1. H.264 Encoder Block Diagram



Features

H.264 Encoder has the following key features:

- Compresses YCbCr 420 video format
- Accepts YCbCr 422 video format as input
- Supports 8-bit for each component (Y, Cb, and Cr)
- Supports ITU-T H.264 Annex B compliant NAL byte stream output
- Operates without standalone operation, CPU, or processor assistance not Required
- Supports user configurable Quality Factor (QP)
- Supports P Frame Count (PCOUNT)
- Supports user configurable threshold value for skip block
- Supports computation at the rate of one pixel per clock
- Supports compression up to resolution of 1080p 60 fps
- Uses video arbiter interface for accessing DDR frame buffers
- Minimal latency (252 µs for full HD or 17 horizontal lines)

Supported Families

H.264 Encoder supports the following product families:

- PolarFire® SoC
- PolarFire

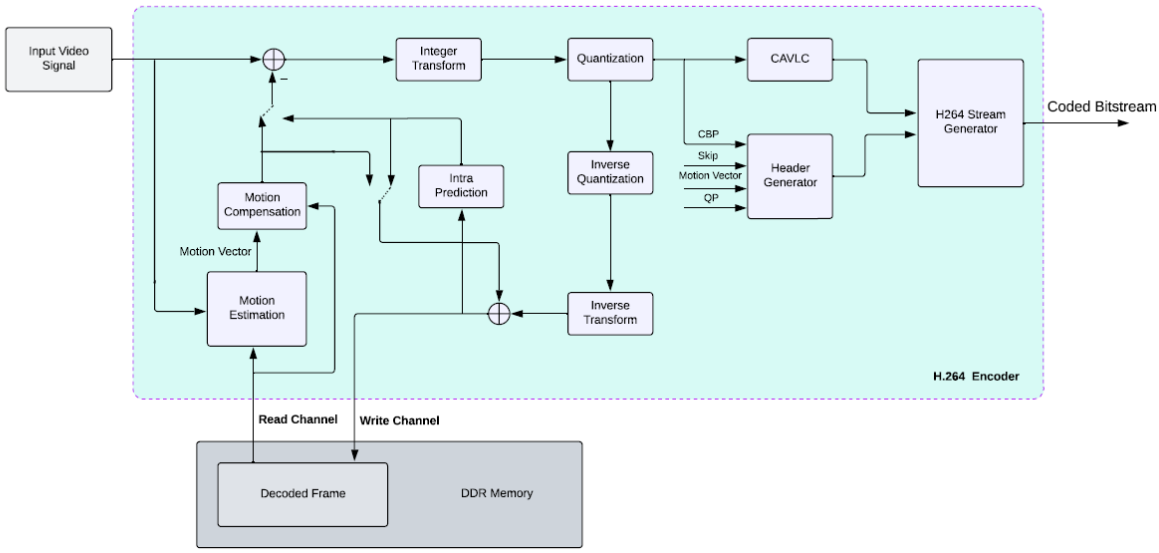
Table of Contents

1. Hardware Implementation

This section describes the different internal modules of the H.264 Encoder. Data input to the H.264 Encoder must be in the form of a raster scan image in the YCbCr 422 format. H.264 Encoder uses 422 formats as input and implements compression in 420 formats.

The following figure shows the H.264 Encoder block diagram.

Figure 1-1. H.264 Encoder - Modules



1.1 Intra Prediction

H.264 uses various intra-prediction modes to reduce the information in a 4 x 4 block. The intra-prediction block in the IP uses only DC prediction on 4 x 4 matrix size. The DC component is computed from the adjacent top and left 4 x 4 blocks.

1.2 Integer Transform

H.264 uses integer discrete cosine transform where the coefficients are distributed across the integer transform matrix and the quantization matrix such that there are no multiplications or divisions in the integer transform. The integer transform stage implements the transformation using shift and add operations.

1.3 Quantization

The quantization multiplies each output of integer transform with a predetermined quantization value defined by the QP user input value. The range of QP value is from 0 to 51. Any value more than 51 is clamped to 51. A lower QP value denotes lower compression and higher quality and vice versa.

1.4 Motion Estimation

The Motion Estimation searches 8 x 8 block of the current frame in the 16 x 16 block of the previous frame and generates motion vectors.

1.5 Motion Compensation

The Motion compensation gets the motion vectors from the Motion Estimation block and finds the corresponding 8 x 8 block in the previous frame.

1.6 CAVLC

H.264 uses two types of entropy encoding—CAVLC and CABAC. The IP uses CAVLC for encoding the quantized output.

1.7 Header Generator

The header generator block generates the block headers, the slice headers, the Sequence Parameter Set (SPS), the Picture Parameter Set (PPS), and the Network Abstraction Layer (NAL) unit depending on the instance of the video frame. Skip block decision logic calculates the Sum of Absolute Difference (SAD) of the current frame 16 x 16 macro block and the previous frame 16 x 16 macro block from the motion vector predicted location. The skip block is decided using the SAD value and the SKIP_THRESHOLD input.

1.8 H.264 Stream Generator

The H.264 stream generator block combines the CAVLC output along with the headers to create the encoded output as per the H.264 standard format.

1.9 DDR Write Channel and Read Channel

H.264 Encoder requires the decoded frame to be stored in DDR memory, which is used in Inter prediction. The IP uses DDR write and read channels to connect with the Video Arbiter IP, which interacts with the DDR memory through the DDR controller IP.

2. Inputs and Outputs

This section describes the inputs and the outputs of the H.264 Encoder.

2.1 Ports

The following tables list the description of the input and the output ports of the H.264 Encoder.

Table 2-1. Inputs and Outputs of H.264 Encoder

Signal Name	Direction	Width	Description
DDR_CLK_I	Input	1	DDR memory controller clock
PIX_CLK_I	Input	1	Input clock with which incoming pixels are sampled
RESET_N	Input	1	Active-low Asynchronous reset signal to the design
DATA_VALID_I	Input	1	Input Pixel data valid signal
DATA_Y_I	Input	8	8-bit Luma pixel input in 422 format
DATA_C_I	Input	8	8-bit Chroma pixel input in 422 format
FRAME_START_I	Input	1	Start of Frame indication The rising edge of this signal is considered as frame start.
FRAME_END_I	Input	1	End of Frame indication
DDR_FRAME_START_ADDR_I	Input	8	DDR memory start address (LSB 24-bits are 0) to store the reconstructed frame. The H.264 IP will store 4 frames and it will use 64 MB of DDR memory.
I_FRAME_FORCE_I	Input	1	User can force to I frame at anytime. It is pulse signal.
PCOUNT_I	Input	8	Number of P frames per every I frame 422 format value ranges from 0 to 255.
QP	Input	6	Quality factor for H.264 quantization 422 fornat value ranges from 0 to 51 where 0 represents highest quality and lowest compression and 51 represents highest compression.
SKIP_THRESHOLD_I	Input	12	Threshold for skip block decision This value represents the SAD value of 16 x 16 Macro block for skipping. The range is from 0 to 1024, with a typical value of 512. Higher threshold produces more skip blocks and low quality.
VRES_I	Input	16	Vertical resolution of input image. It must be multiple of 16.
HRES_I	Input	16	Horizontal resolution of input image. It must be multiple of 16.
DATA_VALID_O	Output	1	Signal denoting encoded data is valid.

.....continued			
Signal Name	**Direction**	**Width**	**Description**
DATA_O	Output	16	H.264 encoded data output that contains NAL unit, slice header, SPS, PPS, and the encoded data of macro blocks.
WRITE_ CHANNEL_BUS	—	—	Write channel bus to be connected with Video arbiter Write channel bus. This is available when the bus interface is selected for Arbiter Interface.
READ_CHANNEL_BUS	—	—	Read channel bus to be connected with Video arbiter Read channel bus. This is available when the bus interface is selected for Arbiter Interface.
DDR Write Native IF—These ports are available when the Native interface is selected for Arbiter Interface.			
DDR_WRITE_ACK_I	Input	1	Write acknowledgment from arbiter write channel.
DDR_WRITE_DONE_I	Input	1	Write completion from arbiter.
DDR_WRITE_REQ_O	Output	1	Write request to arbiter.
DDR_WRITE_START_ADDR_O	Output	32	DDR address to which write has to be made.
DDR_WBURST_SIZE_O	Output	8	DDR write burst size.
DDR_WDATA_VALID_O	Output	1	Data valid to arbiter.
DDR_WDATA_O	Output	DDR_AXI_DATA_WIDTH	Data output to arbiter.
DDR Read Native IF—These ports are available when the Native interface is selected for Arbiter Interface.			
DDR_READ_ACK_I	Input	1	Read acknowledgment from arbiter read channel.
DDR_READ_DONE_I	Input	1	Read completion from arbiter.
DDR_RDATA_VALID_I	Input	1	Data valid from arbiter.
DDR_RDATA_I	Input	DDR_AXI_DATA_WIDTH	Data input from arbiter.
DDR_READ_REQ_O	Output	1	Read request to arbiter.
DDR_READ_START_ADDR_O	Output	32	DDR address from which read has to be made.
DDR_RBURST_SIZE_O	Output	8	DDR read burst size.

3. Clock Constraints

The H.264 Encoder IP uses PIX_CLK_I and DDR_CLK_I clock inputs. Use the clock grouping constraints for place and routing and verify timing as the IP implements the clock domain crossing logic.

4. Installation Instructions

H.264 Encoder core must be installed to the IP Catalog of the Libero® SoC software. This is done automatically through the IP Catalog update function in the Libero SoC software, or the IP core can be manually downloaded from the catalog. Once the IP core is installed in the Libero SoC software IP Catalog, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

5. Testbench

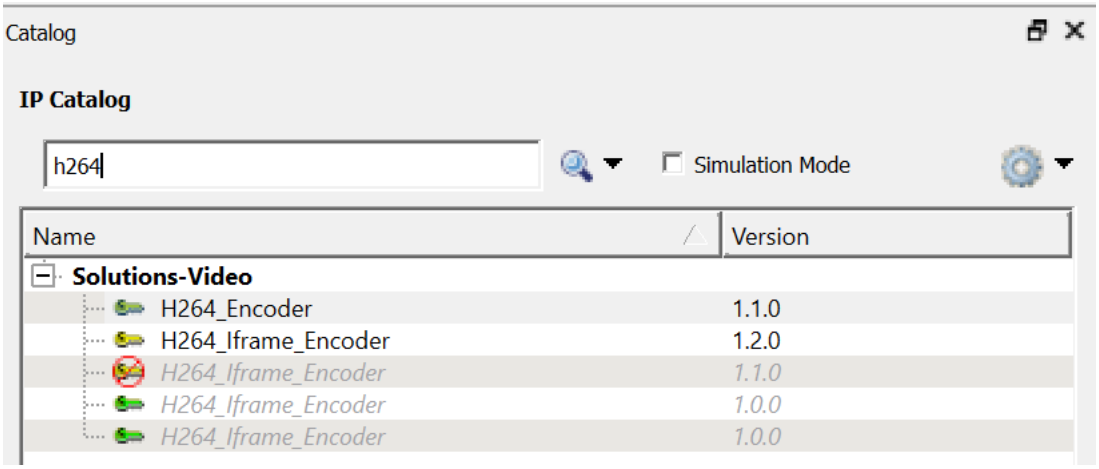
Testbench is provided to check the functionality of the H.264 Encoder IP.

5.1 Simulation

The simulation uses a 432 × 240 image in the YCbCr422 format represented by two files, each for Y and C as input and generates a `H.264` file format containing two frames. The following steps describe how to simulate the core using the testbench.

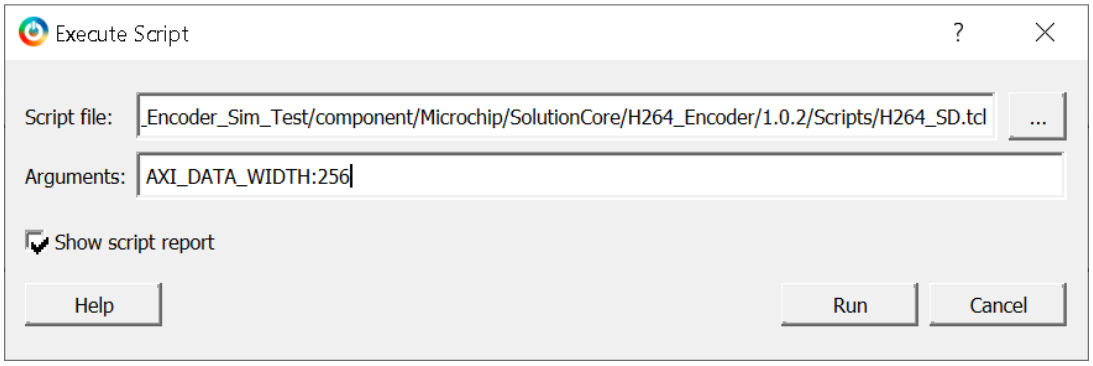
1. Go to Libero SoC **Catalog > View > Windows > Catalog**, and then expand **Solutions-Video**. Double click **H264_Encoder**, and then click **OK**.

   Figure 5-1. H.264 Encoder IP Core in Libero SoC Catalog



2. To generate the required SmartDesign for the H.264 Encoder IP simulation, click Libero **Project > Execute script**. Browse to script `..\<Project_name>\component\Microchip\SolutionCore\H264_Encoder\ <H264 IP version>\scripts\H264_SD.tcl`, and then click **Run** .

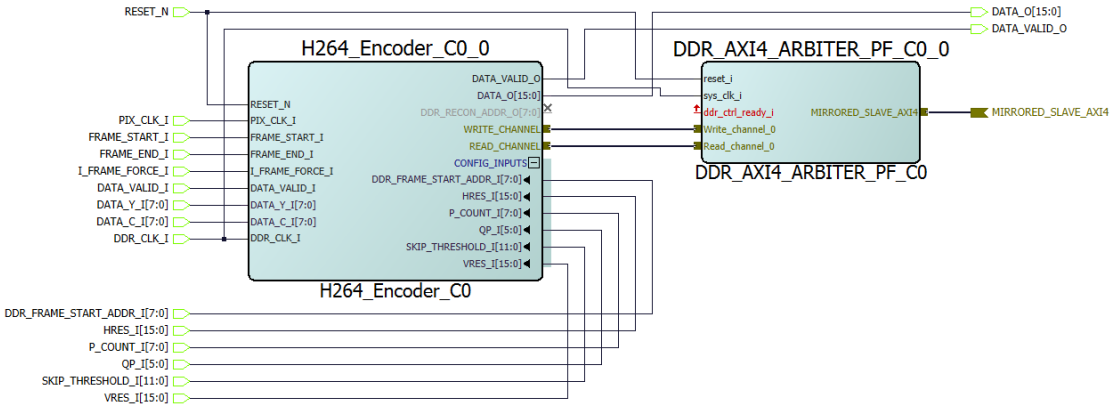
   Figure 5-2. Execute Script Run



   The default AXI data bus width is 512. If the H.264 Encoder IP is configured for 256/128 bus widths, type **AXI_DATA_WIDTH:256** or **AXI_DATA_WIDTH:128** in the **Arguments** field.

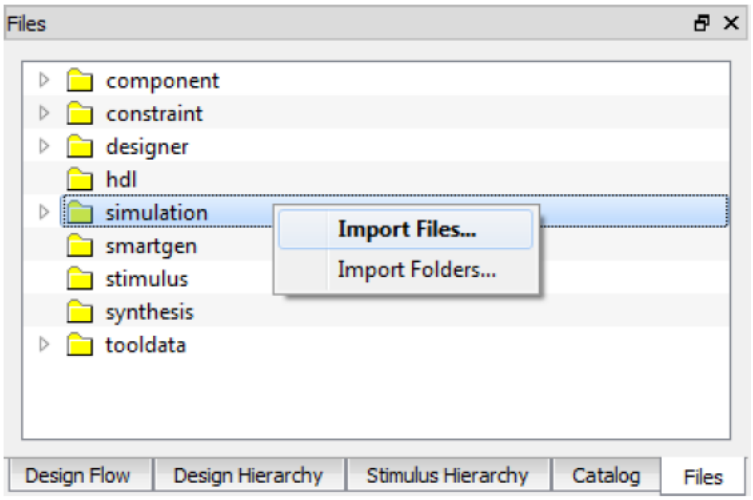
   The SmartDesign appears. See the following figure.

Figure 5-3. Top SmartDesign



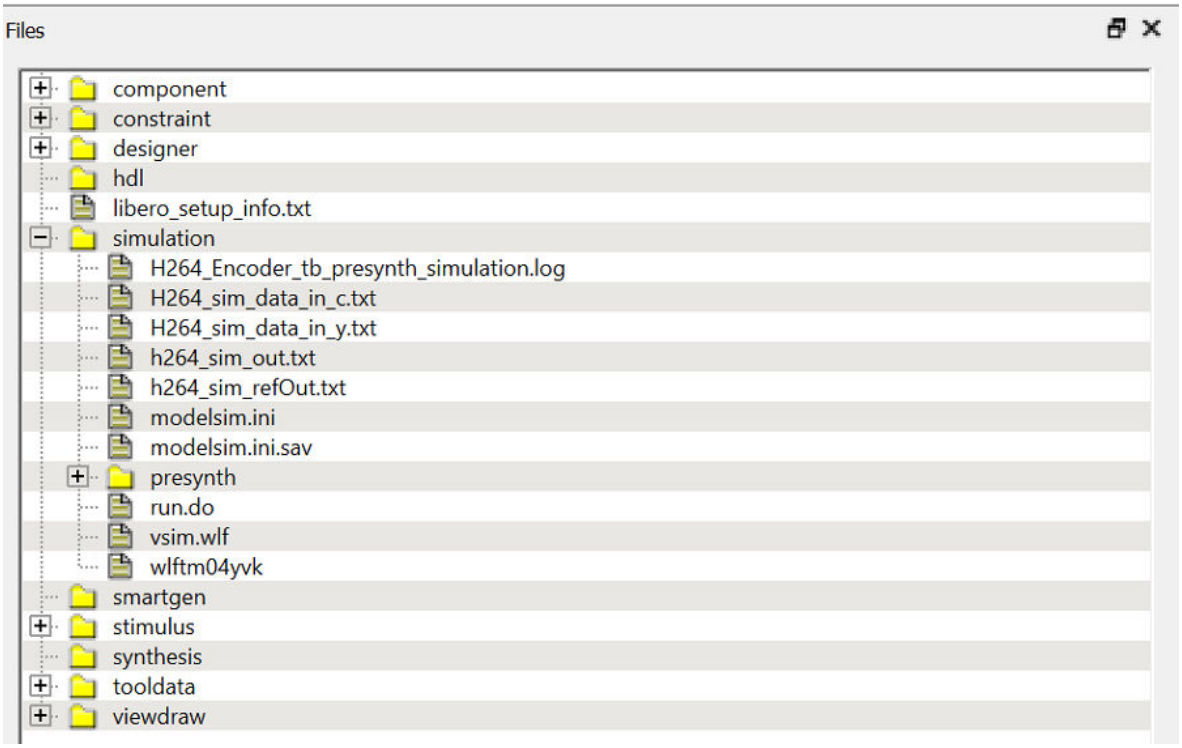
3. On the **Files** tab, click **simulation > Import Files**.

Figure 5-4. Import Files



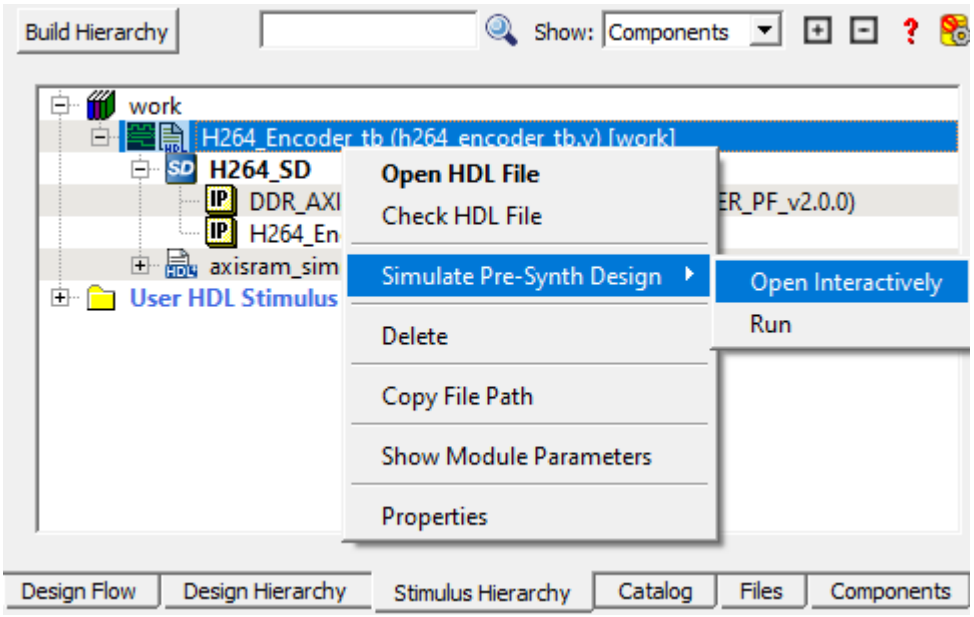
4. Import the `H264_sim_data_in_y.txt, H264_sim_data_in_c.txt` file and the `H264_sim_refOut.txt` file from the following path: `..\<Project_name>\component\Microchip\SolutionCore\ H264_Encoder\<H264 IP version>\Stimulus`.
5. To import a different file, browse the folder that contains the required file, and click **Open**. The imported file is listed under simulation, see the following figure.

Figure 5-5. Imported Files



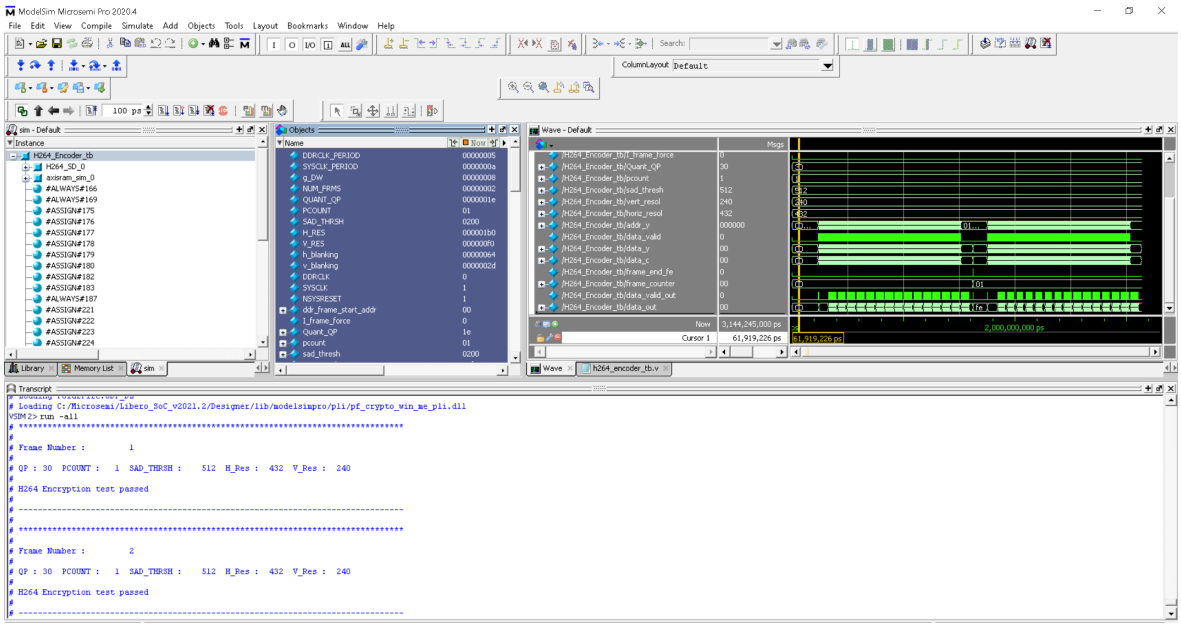
6. On the **Stimulus Hierarchy** tab, click **H264_Encoder_tb** (**H264_Encoder_tb. v**) > **Simulate Pre-Synth Design > Open Interactively**. The IP is simulated for two frames.

Figure 5-6. Simulating Pre-Synthesis Design



ModelSim opens with the testbench file as shown in the following figure.

Figure 5-7. ModelSim Simulation Window



Important: If the simulation is interrupted due to the run time limit specified in the `DO` file, use the `run -all` command to complete the simulation.

6. Resource Utilization

H.264 Encoder is implemented in the PolarFire SoC FPGA (MPFS250T-1FCG1152I package) and generates compressed data by using 4:2:2 sampling of input data.

Table 6-1. Resource Utilization for H.264 Encoder

Resource	Usage
4 Look-Up Tables (LUTs)	69092
D Flip Flops (DFFs)	65522
Static Random Access Memory (LSRAM)	232
uSRAM	30
Math blocks	19
Interface 4-input LUTs	9396
Interface DFFs	9396

7. Configuration Parameters

The following table lists the description of the generic configuration parameters used in the hardware implementation of the H.264 Encoder, which can vary based on the application requirements.

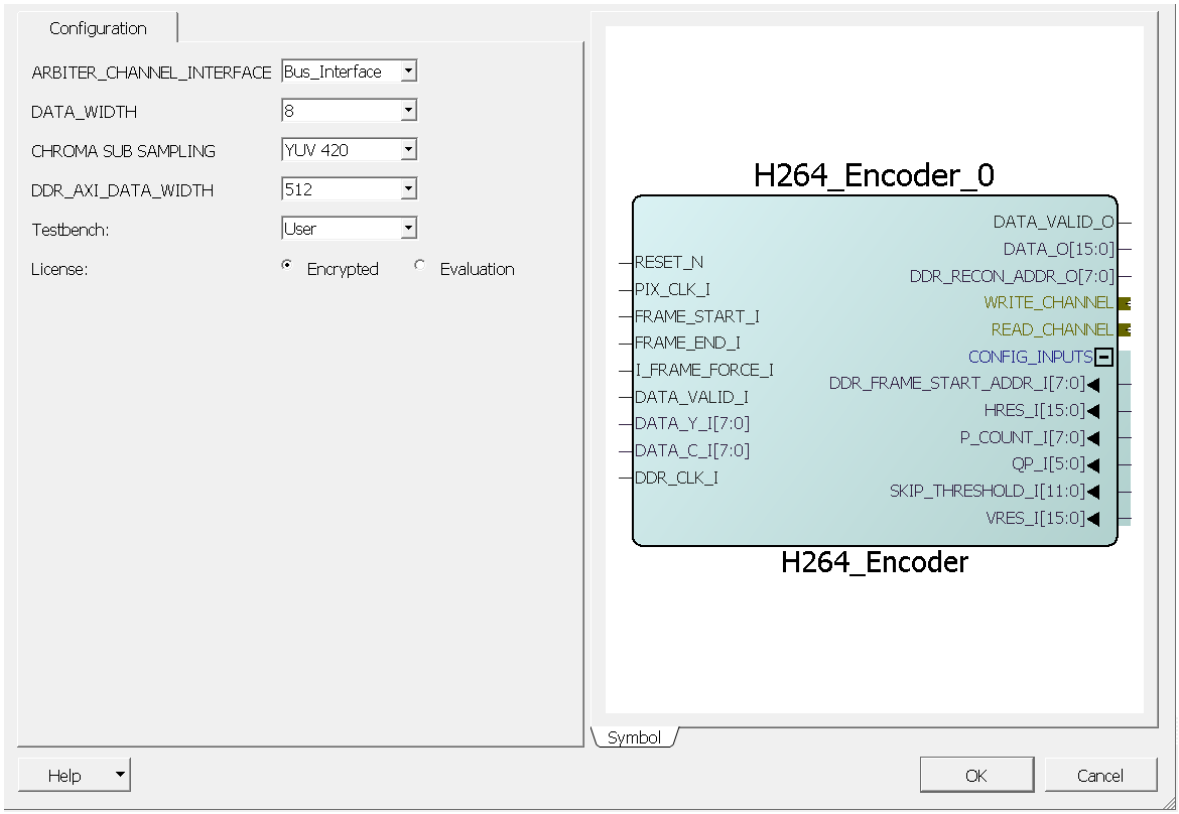
Table 7-1. Configuration Parameters

Name	Description
DDR_AXI_DATA_WIDTH	Defines the DDR AXI data width. It can be 128, 256, or 512
ARBITER_INTERFACE	Option to select the native or bus interface to connect with video arbiter IP

7.1 IP Configurator

The following figure shows the H.264 Encoder IP configuarator.

Figure 7-1. H.264 Encoder Configurator



8. License

H.264 Encoder is provided in encrypted form only under license.

Encrypted RTL source code is license-locked and must be purchased separately. You can perform simulation, synthesis, layout, and program the Field Programmable Gate Array (FPGA) silicon using the Libero design suite.

Evaluation license is provided for free to check the H.264 Encoder features. The evaluation license expires after an hour’s use on the hardware.

9. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 9-1. Revision History

Revision	Date	Description
B	09/2022	• Updated Features section. • Updated the width of DATA_O output signal from 8 to 16, see Table 2-1. • Updated Figure 7-1. • Updated 8. License section. • Updated 6. Resource Utilization section. • Updated Figure 5-3.
A	07/2022	Initial release.

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