AN4229

RT PolarFire®: Building a RISC-V Processor Subsystem

Introduction

Microchip offers the Mi-V processor IP and software toolchain at no cost to develop RISC-V processor based designs. RISC-V is a standard open instruction set architecture (ISA) under the governance of the RISC-V foundation. It offers numerous benefits, which include enabling the open-source community to test and improve cores at a faster pace than closed ISAs.

RT PolarFire FPGAs support Mi-V soft processors to run user applications. This application note describes how to build a Mi-V processor subsystem to execute a user application from the designated TCM memory initialized from the sNVM/µPROM/SPI Flash.

Table of Contents

1. Design Requirements

The following table lists the hardware and software requirements for building a Mi-V processor subsystem.

Design Requirements	Description
Hardware Requirements	
RTPF500TS Evaluation Kit – 12V / 5A AC power adapter and cord – USB 2.0 A to mini-B cable – FlashPro External Programmer	To be released.
Software Requirements	
– Libero® SoC – FlashPro Express – SoftConsole – Tera Term or PuTTY	See the readme.txt file in the design files for all software versions needed to create the Mi-V reference design.

1.1 Design Files

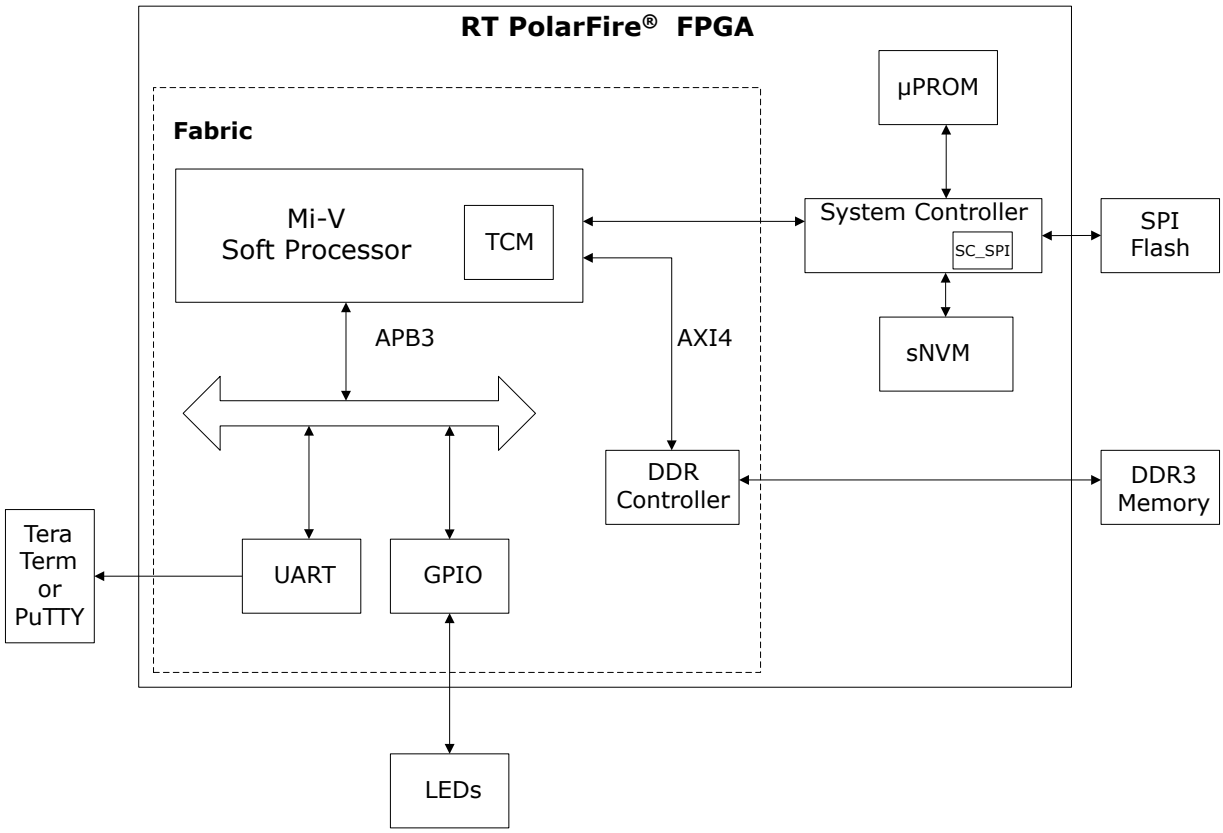
1. Download the reference design files from soc.microsemi.com/download/rsc/?f=rtpf_miv_subsystem_df.
2. Download and install Libero SoC from the following link: www.microsemi.com/product-directory/design-resources/1750-libero-soc#downloads.

2. Design Description

MIV_RV32 is a processor core designed to implement the RISC-V instruction set. The core can be configured to have AHB, APB3, and AXI3/4 bus interfaces for peripheral and memory accesses. Figure 2-1 shows the top-level block diagram of the Mi-V subsystem built on RT PolarFire FPGA.

The user application to be executed on Mi-V processor can be stored in µPROM, sNVM, or an external SPI Flash. At device power-up, the system controller initializes the designated TCM with the user application. The system Reset is released after the TCM initialization is completed. If the user application is stored in SPI Flash, the System Controller uses the SC_SPI interface for reading the user application from SPI Flash. The given user application performs DDR3 memory access and prints the messages to a UART terminal, and blinks user LEDs on the board.

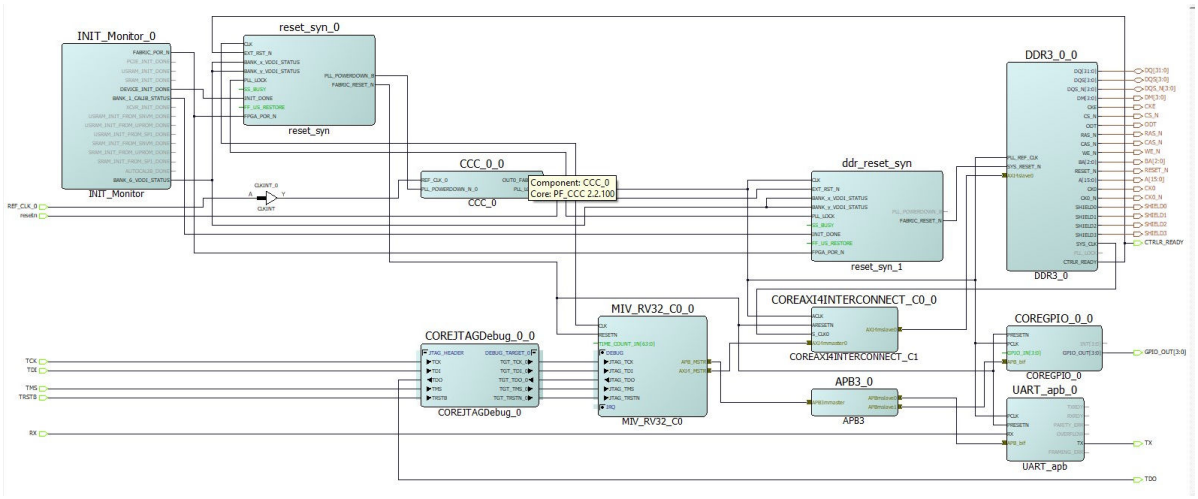
Figure 2-1. Block Diagram



3. Hardware Implementation

The following figure shows the Libero design of the Mi-V processor subsystem.

Figure 3-1. Mi-V Processor Subsystem



Note: Libero SmartDesign screenshot provided in this application note is for illustration purpose only. Open the Libero project to see the latest updates and IP versions.

3.1 IP Blocks

The following table lists the IP blocks used in the Mi-V processor subsystem reference design and their function.

IP Name	Function
INIT_MONITOR	The PolarFire® Initialization Monitor gets the status of device and memory initialization.
reset_syn	This is the CORERESET_PF IP instantiation which generates a system-level synchronous Reset for the Mi-V subsystem.
CCC_0	The PolarFire® Clock Conditioning Circuitry (CCC) block takes an input clock of 50 MHz from the on-board oscillator and generates a 53.3 MHz fabric clock for the Mi-V processor subsystem and other peripherals.
MIV_RV32_C0 (Mi-V Soft Processor IP)	The Mi-V soft processor default Reset Vector Address value is 0x8000_0000. After the device reset, the processor executes the application from 0x8000_0000. TCM is the main memory of the Mi-V processor and is memory mapped to 0x8000_0000. The TCM gets initialized with the user application which stored in the SPI Flash. In the Mi-V processor memory map, the 0x8000_0000 to 8000_FFFF range is defined for TCM memory interface and the 0x6000_0000 to 0x6FFF_FFFF range is defined for the APB interface. The 0x8001_0000 to 8FFF_FFFF range is defined for the AXI interface which is used to interface the external DDR memory.
reset_syn_1	This is the CORERESET_PF IP instantiation which generates a system-level synchronous Reset for DDR3_0.

.....continued	
IP Name	**Function**
DDR3_0 (DDR3 Controller IP)	This IP is used to perform DDR3 read and write operations. The data-width is set to 32-bit and memory clock frequency is set to 533 MHz, which is generated from a reference clock frequency input 53.3 MHz using a clock multiplier (x10) internal to the DDR3 IP. The DDR3 PLL generates a 533 MHz DDR3 memory clock frequency and a 133.25 MHz DDR3 AXI clock frequency.
COREAXI4INTERCONNECT_C1	AXI4 interconnect used to interface the Mi-V soft processor with the DDR3 Controller IP.
COREGPIO_0	The CoreGPIO IP controls the on-board LEDs using GPIOs. It is connected to Mi-V soft processor as an APB slave.
UART_apb	The UART_apb IP controls the UART peripherals used for serial communication.
COREJTAGDebug	Used to debug the Mi-V soft processor.
APB3	APB3 bus interconnect to interface with peripherals.

Note: All the IP user guides and handbooks are available from Libero SoC > Catalog.

3.2 Memory Map

The following table lists the memory map of the memories and peripherals.

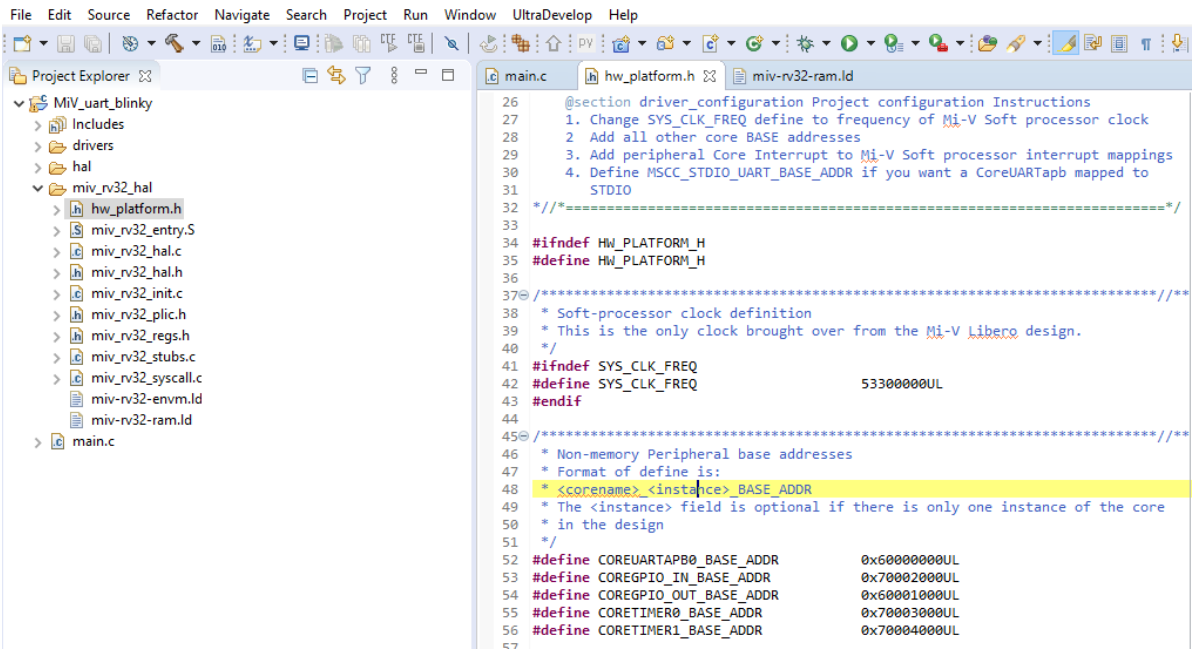
Peripherals	Start Address
TCM	0x8000_0000
DDR3	0x8001_0000
UART	0x6000_0000
GPIO	0x6000_1000

4. Software Implementation

Microchip provides SoftConsole toolchain to build a RISC-V user application executable (.hex) file and debug it. The reference design files include the SoftConsole workspace that contains the MiV_uart_blinky software project. The MiV_uart_blinky user application is programmed on an external SPI Flash using Libero SoC. The user application blinks user LEDs and performs DDR3 read and write operations. The DDR3 read/write status is displayed on the UART terminal.

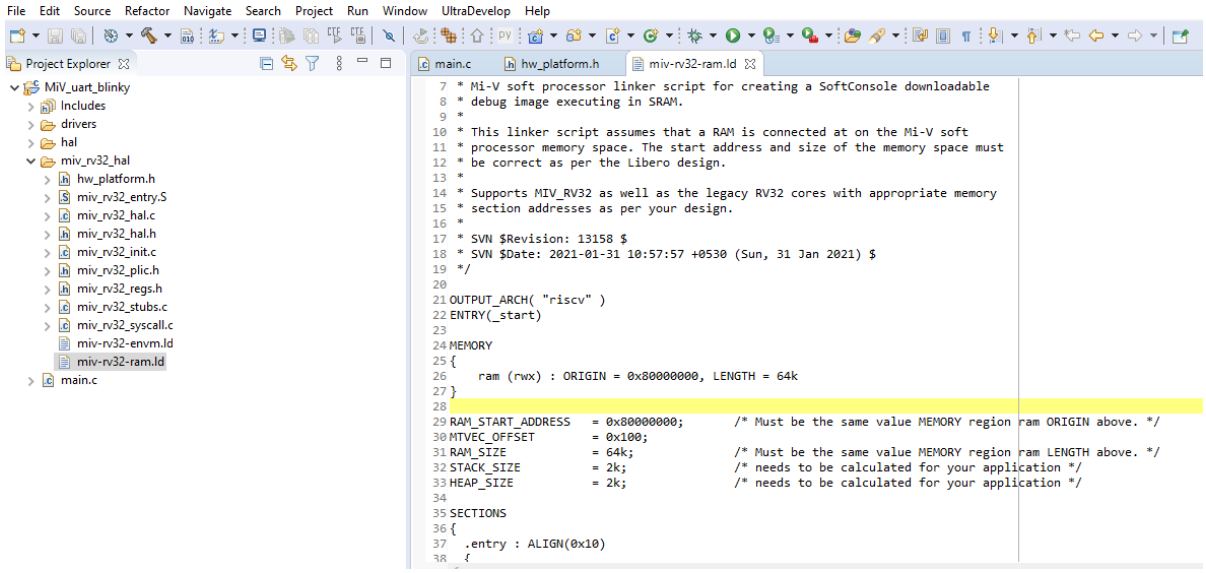
As per the Libero SoC design memory map, the UART and GPIO peripheral addresses are mapped to 0x60000000 and 0x60001000, respectively. This information is provided in the hw_platform.h file as shown in the following figure.

Figure 4-1. Peripheral Mapping



The user application must be executed from the TCM memory (code, data, and stack). Therefore, the RAM address in the linker script is set to the starting address of the TCM memory as shown in the following figure.

Figure 4-2. Linker Script



The linker script (`miv-rv32-ram.ld`) is available in the `SoftConsole_Project\MiV_uart_blinky\miv_rv32_hal` folder of the design files. Building the user application involves the following steps:

1. Creating a Mi-V SoftConsole project
2. Downloading the firmware drivers
3. Importing the firmware drivers
4. Creating the `main.c` file
5. Mapping firmware drivers and the linker script
6. Mapping memory and peripheral addresses
7. Building the application

For more information about these steps, see TU0775: PolarFire FPGA: Building a Mi-V Processor Subsystem Tutorial. The `.hex` file is created after successful build and it is used for design and memory Initialization configuration in Running the Demo.

5. Setting Up the Demo

This involves the following steps:

1. Setting Up the Hardware
2. Setting Up the Serial Terminal (Tera Term)

5.1 Setting Up the Hardware

The following steps describe how to setup the hardware:

1. Power OFF the board using the SW7 switch.
2. Retain the default setting for J31 jumper to use the external FlashPro programmer.
3. Connect the host PC to the J24 connector using the USB cable.
4. Connect the FlashPro programmer to J3 connector (JTAG header) and use another USB cable to connect the FlashPro programmer to the Host PC.
5. Ensure that the USB to UART bridge drivers are automatically detected. Verify it in the device manager of the host PC.
   Note: As shown in Figure 5-1, the port properties of COM8 show that it is connected to USB serial port. Hence, COM8 is selected in this example. The COM port number is system specific. If the USB to UART bridge drivers are not installed, download and install the drivers from www.microsemi.com//documents/CDM_2.08.24_WHQL_Certified.zip.
6. Connect the power supply to J19 connector and switch ON the power supply switch SW7.

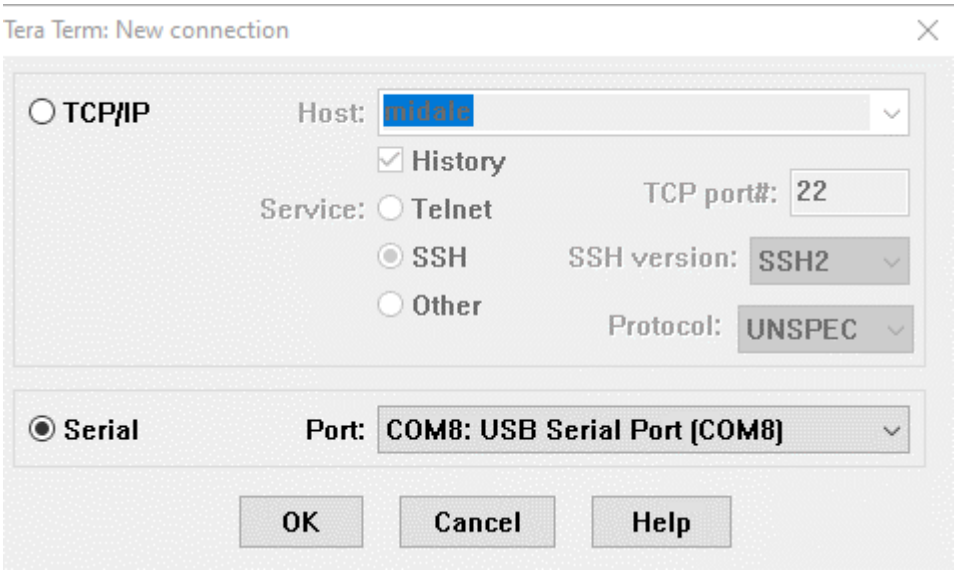
5.2 Setting Up the Serial Terminal (Tera Term)

The user application (`MiV_uart_blinky.hex` file) prints the status of the DDR3 read/write operation on the serial terminal through the UART interface.

Follow these steps to set up the serial terminal:

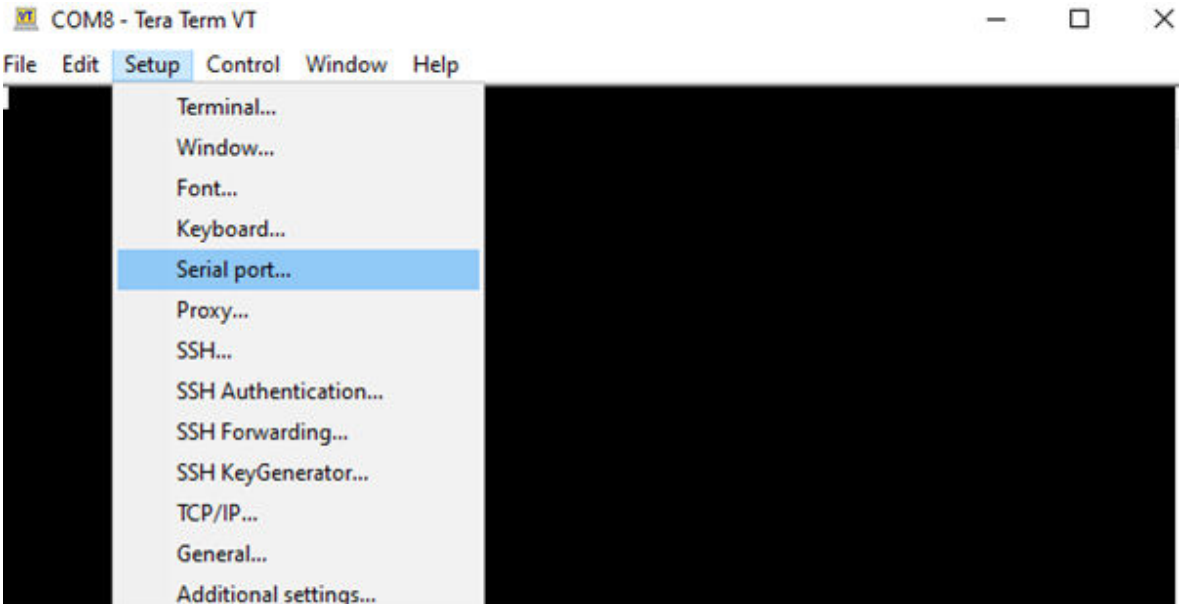
1. Launch Tera Term on the Host PC.
2. Select the identified **COM Port** in Tera Term as shown in the following figure.

Figure 5-1. Identifying the COM Port



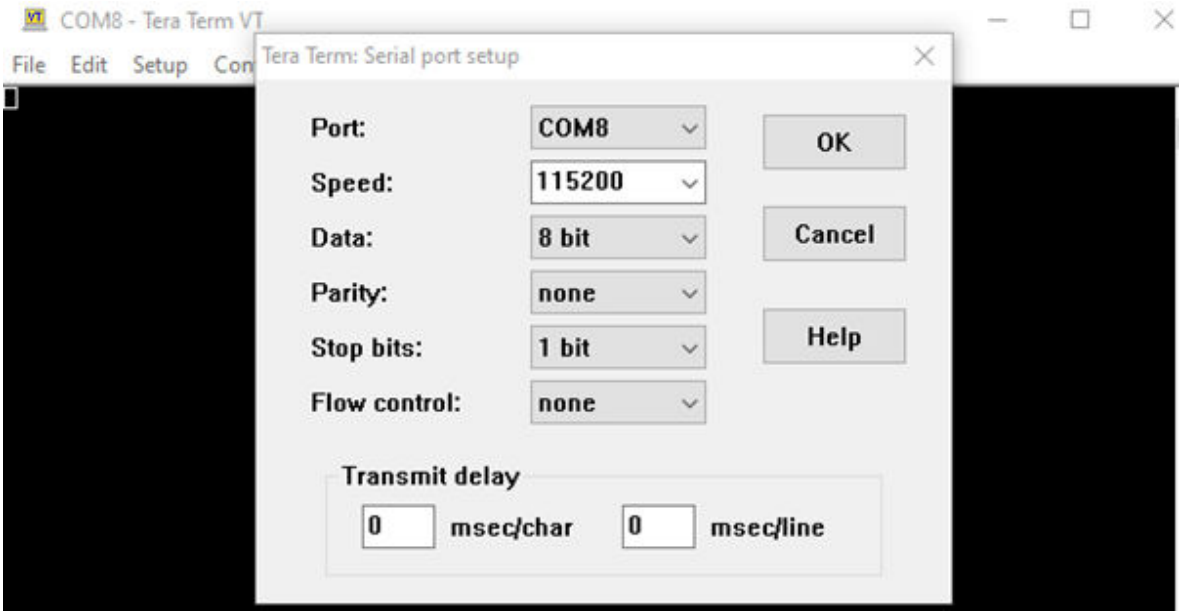
3. From the Menu bar, select **Setup > Serial port...** to set up the COM port.

Figure 5-2. Setting Up the Serial Terminal



4. Set the **Speed** (baud) to **115200** and **Flow Control** to **none** and click **OK** as shown in the following figure.

Figure 5-3. Setting Up the Baud Rate



After the serial terminal is set up, next step is to program the RT PolarFire device.

6. Running the Demo

Running the demo involves the following steps:

1. Generating the TCM Initialization Client
2. Programming the RT PolarFire Device
3. Generating the SPI Flash Image
4. Programming the SPI Flash

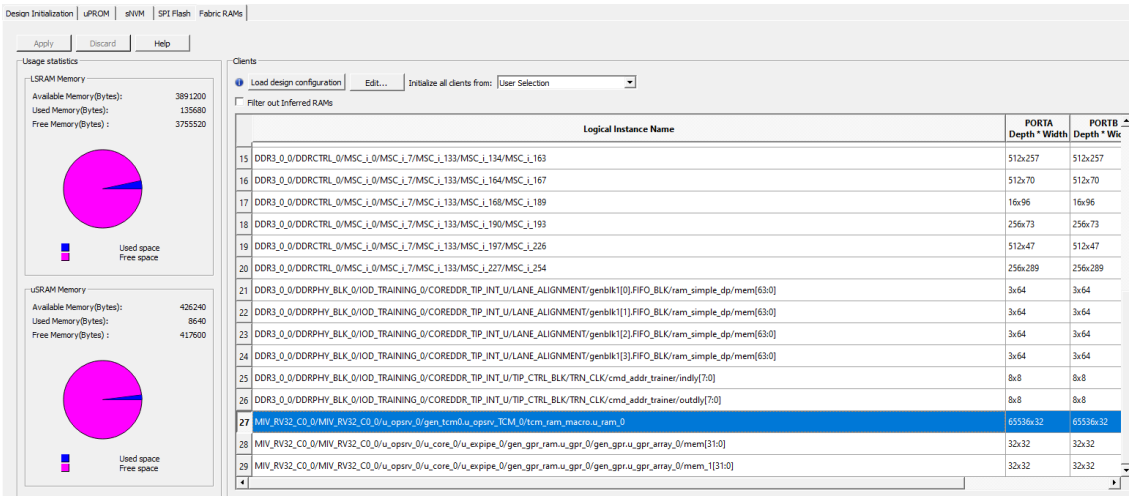
6.1 Generating the TCM Initialization Client

To initialize the TCM in RT PolarFire using the system controller, a local parameter `l_cfg_hard_tcm0_en` in the `miv_rv32_opsrv_cfg_pkg.v` file must be changed to `1'b1` before Synthesis. For more information, see the the *MIV_RV32 Handbook*.

In Libero SoC, the **Configure Design Initialization Data and Memories** option generates the TCM initialization client and adds it to sNVM, µPROM, or an external SPI Flash, based on the type of non-volatile memory selected. In this application note, the TCM initialization client is stored in the SPI Flash. This process requires the user application executable file (`.hex` file). The hex file (`*.hex`) is generated using SoftConsole application project. A sample user application is provided along with the design files. The user application file (`.hex`) is selected for creating the TCM initialization client using the following steps:

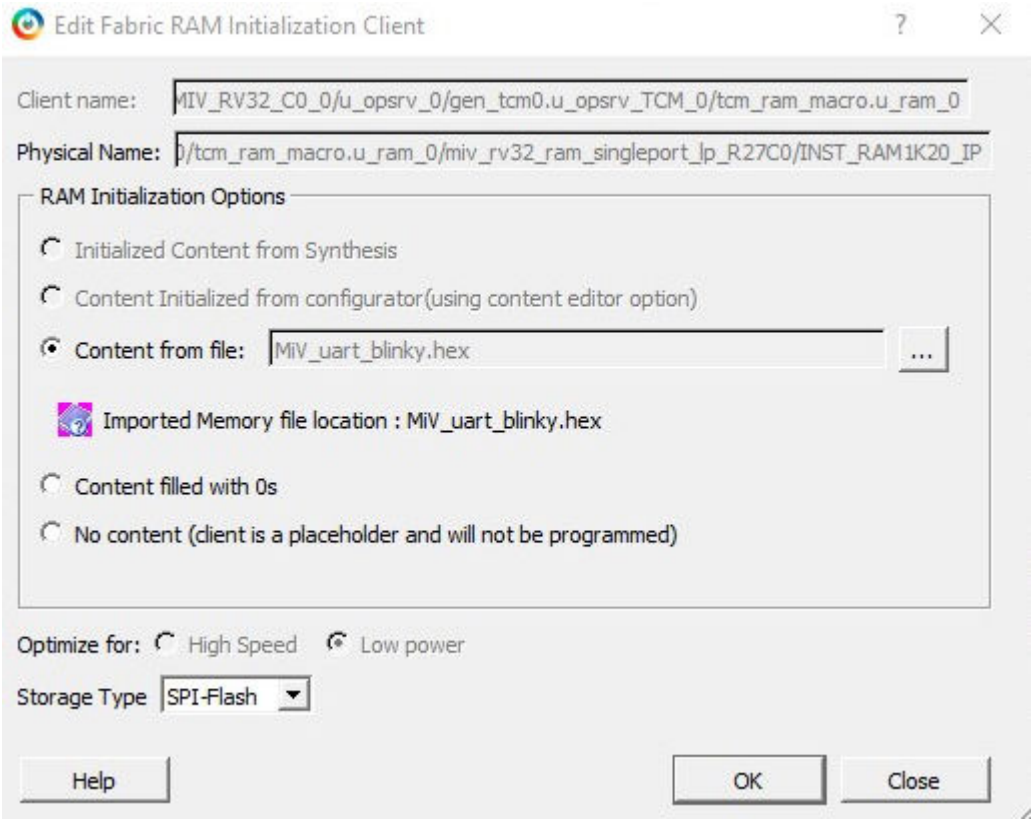
1. Launch Libero SoC.
2. Select **Configure Design Initialization Data and Memories** from **Libero Design Flow**.
3. On the **Fabric RAMs** tab, select the TCM instance as shown in the following figure.

Figure 6-1. Selecting the TCM Instance



4. In the **Edit Fabric RAM Initialization Client** dialog box, set **Storage type** to **SPI-Flash**. Then, select **Content from file** and click the **Import (...)** button as shown in the following figure.

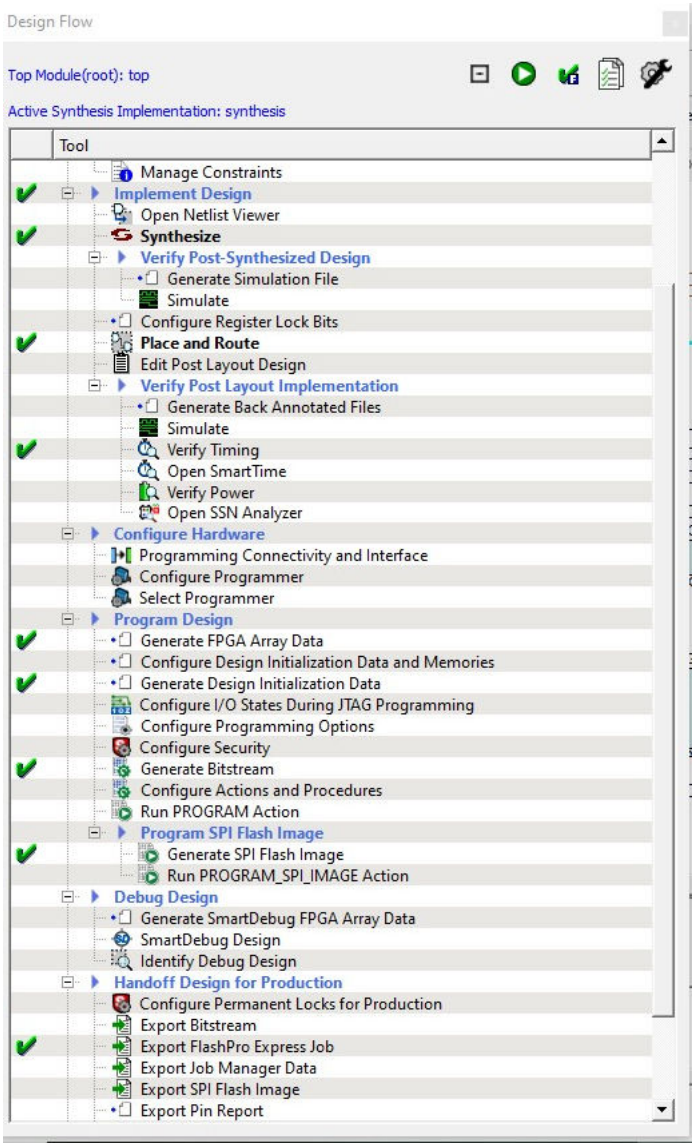
Figure 6-2. Importing the TCM Initialization Client



6.2 Programming the RT PolarFire Device

The reference design files include the Mi-V processor subsystem project created using Libero SoC. The RT PolarFire device can be programmed using Libero SoC. The Libero SoC design flow is shown in the following figure.

Figure 6-3. Libero SoC Design Flow



To program the RT PolarFire device, open the Mi-V processor subsystem project in Libero SoC and double click **Run Program Action** .

6.3 Generating the SPI Flash Image

To generate the SPI Flash image, double click **Generate SPI Flash Image** on the **Design Flow** tab.

When the SPI Flash image is generated successfully, a green tick mark appears next to **Generate SPI Flash Image**.

6.4 Programming the SPI Flash

To program the SPI Flash image:

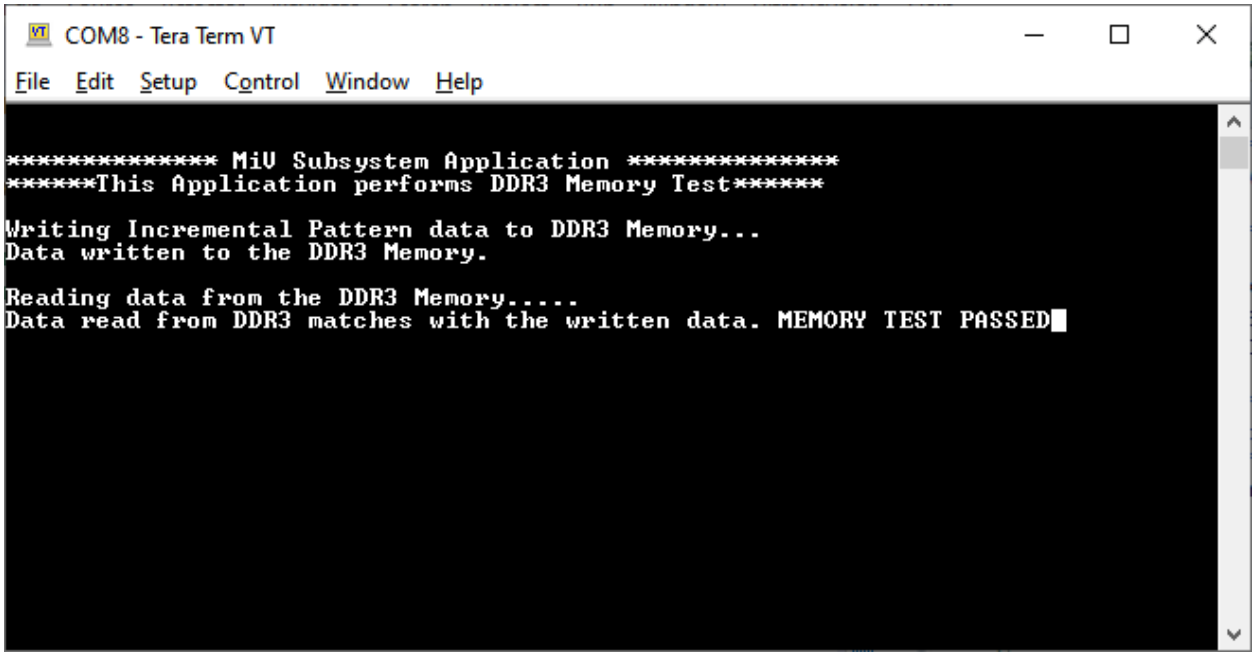
1. Double click **Run PROGRAM_SPI_IMAGE** on the **Design Flow** tab.

2. Click **Yes** in the dialog box.

When the SPI image is successfully programmed on to the device, a green tick mark appears next to **Run PROGRAM_SPI_IMAGE**.

After SPI Flash programming is completed, the TCM is ready and executes the user application. As a result, LEDs 1, 2, 3, and 4 blink, and the 256 MB DDR3 memory write and read access is performed and verified, then prints are observed on the serial terminal, as shown in the following figure.

Figure 6-4. UART Terminal



This concludes the demo.

The on-board RT PolarFire device and the SPI Flash can also be programmed using FlashPro Express, see 7. Appendix: Programming the RT PolarFire Device Using FlashPro Express.

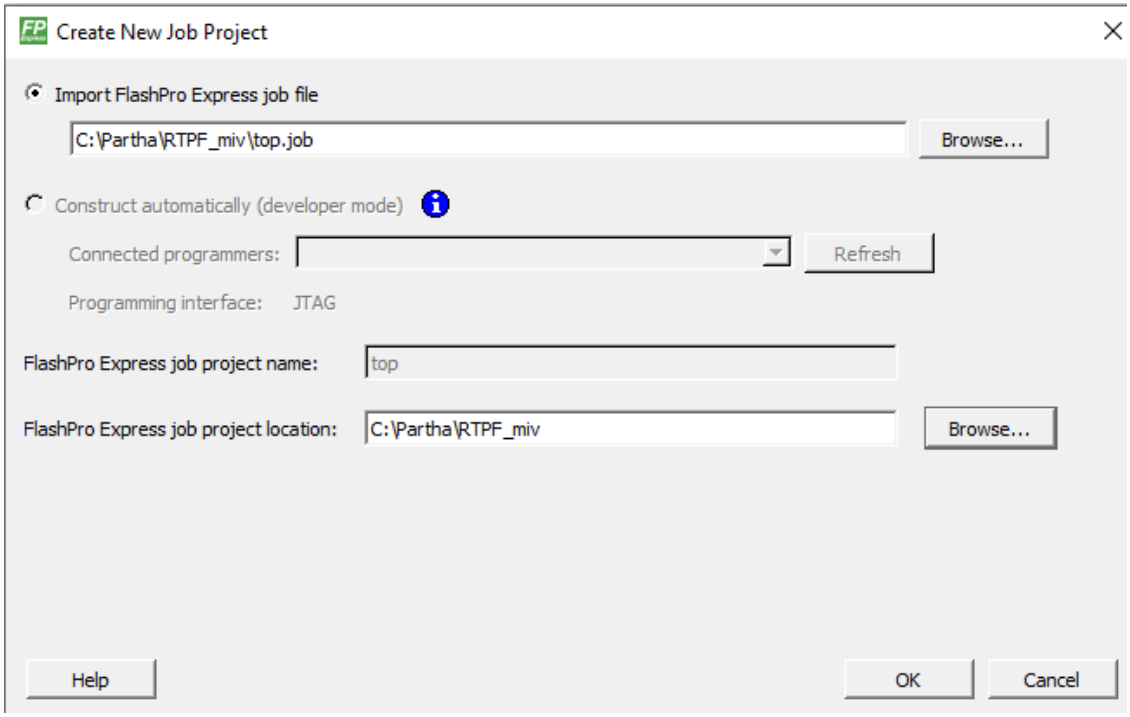
7. Appendix: Programming the RT PolarFire Device Using FlashPro Express

The reference design files include a programming job file for programming the RT PolarFire device using FlashPro Express. This job file also includes the SPI Flash image, which is the TCM initialization client. FlashPro Express programs both the RT PolarFire device and the SPI Flash with this programming `.job` file. This section describes how to program the RT PolarFire device with the programming file using FlashPro Express. The programming `.job` file is available at `DesignFiles_directory\Programming_Job`.

Follow these steps:

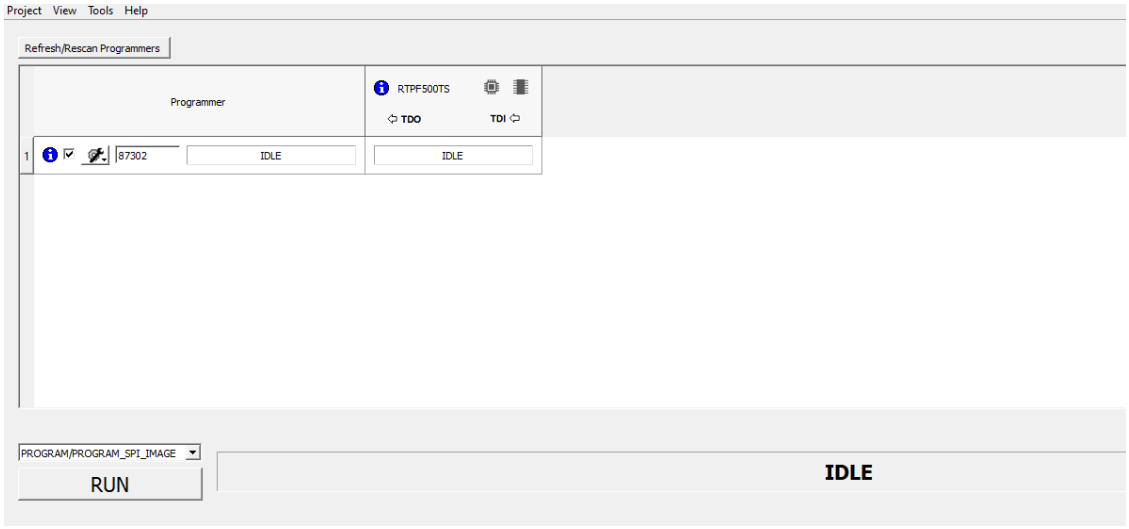
1. Set up the hardware, see Setting Up the Hardware.
2. On the host PC, launch the FlashPro Express software.
3. Click **New** or select **New Job Project from FlashPro Express Job** from the Project menu to create a new job project.
4. In the dialog box, enter the following:
   - Programming job file: Click **Browse** and navigate to the location where the `.job` file is located and select the file. The .job file is available at `DesignFiles_directory\Programming_Job`.
   - **FlashPro Express job project location**: Click **Browse** and navigate to the location where you want to save the project.

   Figure 7-1. New Job Project from FlashPro Express Job



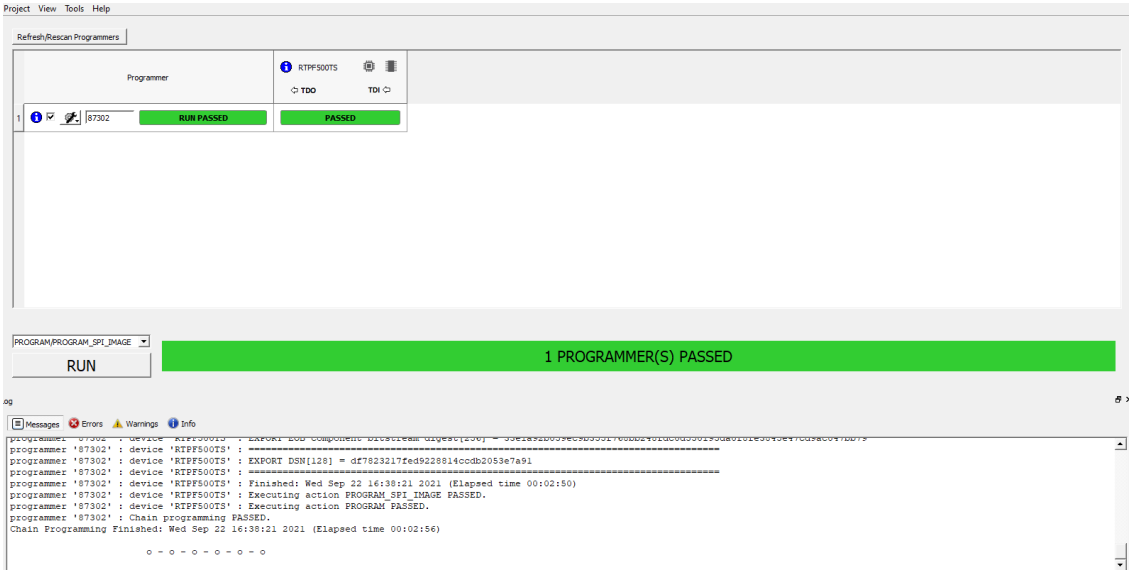
5. Click **OK**. The required programming file is selected and ready to be programmed.
6. The FlashPro Express window appears as shown in the following figure. Confirm that a programmer number appears in the Programmer field. If it does not, check the board connections and click **Refresh/Rescan Programmers**.

Figure 7-2. Refresh/Rescan Programmers



7. Click **RUN**. When the device is programmed successfully, a **RUN PASSED** status is displayed as shown in the following figure.

Figure 7-3. FlashPro Express—RUN PASSED



This concludes the RT PolarFire device and the SPI Flash programming. Power-cycle the board to view the status of DDR3 memory write and read operation in the UART terminal and observe the blinking user LEDs.

8. Revision History

The revision history table describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	10/2021	The first publication of this document.

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