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Total Ionizing Dose Test Report

No. 21T-RT4G150-CQ352- K3QR1

June 16, 2021

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I. SUMMARY TABLE

Table. 1. Summary

Parameter	Tolerance
1. Gross Functionality	Passed 125 krad(SiO_2)
2. Power Supply Current	Passed 125 krad(SiO_2)
3. Input Threshold (VIL/VIH)	Passed 125 krad(SiO_2)
4. Output Drive (VOL/VOH)	Passed 125 krad(SiO_2)
5. Propagation Delay	Passed 125 krad(SiO_2) for 10% degradation criterion
6. Transition Time	Passed 125 krad(SiO_2)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the basis of an extensive database of TID testing for Radiation-Tolerant FPGAs including flash-based FPGAs. Microsemi TID reports can be found at http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/military-aerospace-radiation-reliability-data#tid-reports

Electrical parameters are measured pre-irradiation and post-irradiation using the burn in design and the Automatic Test Equipment (ATE) program. The report summarizes sample pins.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters.

Table. 2. DUT and Irradiation Parameters

Part Number	RT4G150
Package	CQ352
Foundry	United Microelectronics Corp.
Technology	65 nm
DUT Design	Burn in design with inverter string
Die Lot Number	K3QR1
Quantity Tested	6
Serial Number (Dose)	15736 (125 krad), 15737 (125 krad), 15745 (125 krad), 15749 (125 krad), 15750 (125 krad), 15802 (125 krad)
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	5 krad (SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias	Static at 1.2V/2.5V/3.3V/3.3V
IO Configuration	Single ended Differential Pair

B. Test Method

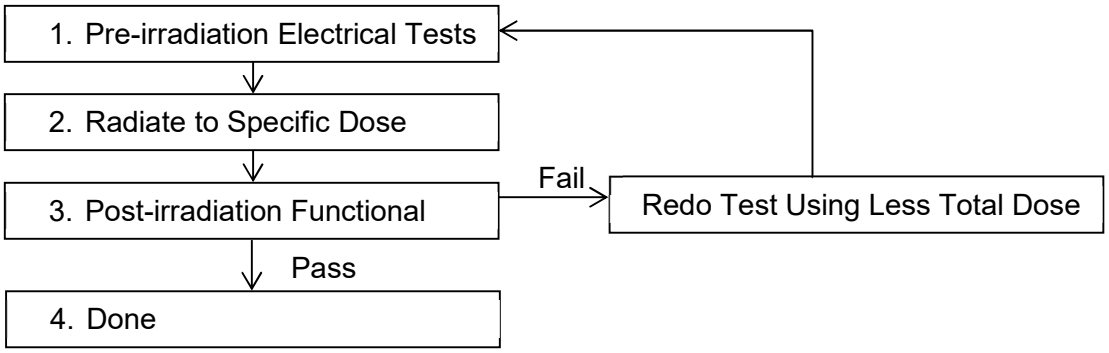

Fig. 1. Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 shows the flow chart describing the steps for the functional and parametric tests.

C. Design and Parametric Measurements

RTG4 FPGA devices have different types of I/Os, such as MSIO and MSIOD, double data rate I/Os (DDRIO), and dedicated I/Os based on functional usage. For more information on I/O naming conventions and I/O description, refer to the RTG4 FPGA Pin Description. All I/Os are tested pre and post-irradiation.

Fabric functionality coverage performed by the burn in design is summarized in table 2 below. In addition to the fabric coverage the supplemental test of propagation delay is also used to determine DUT functionality. These tests are performed pre and post-irradiation and recorded as a pass/fail.

Refer to appendix A for a graphical representation of fabric functional coverage blocks used to perform the functional tests.

Table. 3. Fabric Functional Coverage

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	Maximum output toggle rate(checker board) compared to reference
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 µRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
I/O Block	I/O utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

The core power supply current IDD, the I/Os power supply currents (IDDI_2.5/IDDI_3.3) and the charge pump and PLL power supply current (IPP_PLL) are also monitored during irradiation in real time.

The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential inputs, and is reported as a pass or fail, as part of the ATE test program. The output-drive voltage (VOL/VOH) is also measured on all pins on the MSIO MSIOD and DDRIO. This report contains the output-drive voltage measurements on selected IO pins used in the burn in design. LVTTL and LVCMOS 2.5V standard at different sourcing and sinking currents are reported.

A 2000 stage inverter string is used to measure the propagation delay. The propagation delay is defined as the time delay from the triggering edge at the Clock input to the switching edge at the output. The propagation delay is monitored real time during irradiation and the time difference between positive switching edges of the clock and output are reported. Additionally, the transition characteristics (rise and fall) at the output of the inverter chain are measured pre and post-irradiation. Oscilloscope screen captures are shown in section III. F.

III. TEST RESULTS

A. Functionality

Every DUT passed the pre-irradiation and post-irradiation functional tests mentioned in section II.C.

B. Power Supply Current

The core power supply current (IDD) is 1.2 V, the I/O bank power supply currents (IDDI) are 2.5 V (IDDI_2.5) and 3.3 V (IDDI_3.3). The charge pump and PLL power supply current (IPP_PLL) is 3.3 V. Figures 2-25 illustrate the plot of in-flux standby IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL versus total dose for every DUT. Tables 3-6 summarize the pre-irradiation and post-irradiation total current (static & dynamic) IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL.

Table. 4. Pre-irradiation and Post-irradiation I_{DD}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
15736	125 krad	0.2950	0.3174	7.59
15737	125 krad	0.2620	0.2934	11.98
15745	125 krad	0.2235	0.2490	11.41
15749	125 krad	0.2740	0.3100	13.14
15750	125 krad	0.2409	0.2746	13.99
15802	125 krad	0.2190	0.2460	12.33

Table. 5. Pre-irradiation and Post-irradiation $I_{DDI\_2.5}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
15736	125 krad	0.0056	0.0061	8.93
15737	125 krad	0.0054	0.0066	22.22
15745	125 krad	0.0053	0.0067	26.42
15749	125 krad	0.0054	0.0069	27.78
15750	125 krad	0.0053	0.0066	24.53
15802	125 krad	0.0052	0.0066	26.92

Table. 6. Pre-irradiation and Post-irradiation $I_{DDI\_3.3}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
15736	125 krad	0.0207	0.0223	7.73
15737	125 krad	0.0203	0.0218	7.39
15745	125 krad	0.0200	0.0216	8.00
15749	125 krad	0.0202	0.0218	7.92
15750	125 krad	0.0199	0.0214	7.54
15802	125 krad	0.0193	0.0207	7.25

Table. 7. Pre-irradiation and Post-irradiation I_{PP_PLL}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
15736	125 krad	0.0030	0.0032	6.67
15737	125 krad	0.0032	0.0032	0.00
15745	125 krad	0.0031	0.0031	0.00
15749	125 krad	0.0032	0.0031	-3.13
15750	125 krad	0.0032	0.0035	9.37
15802	125 krad	0.0032	0.0031	-3.13

The following figures (2-25) show the in-beam monitoring of the currents mentioned above as a function of TID for the available DUTs.

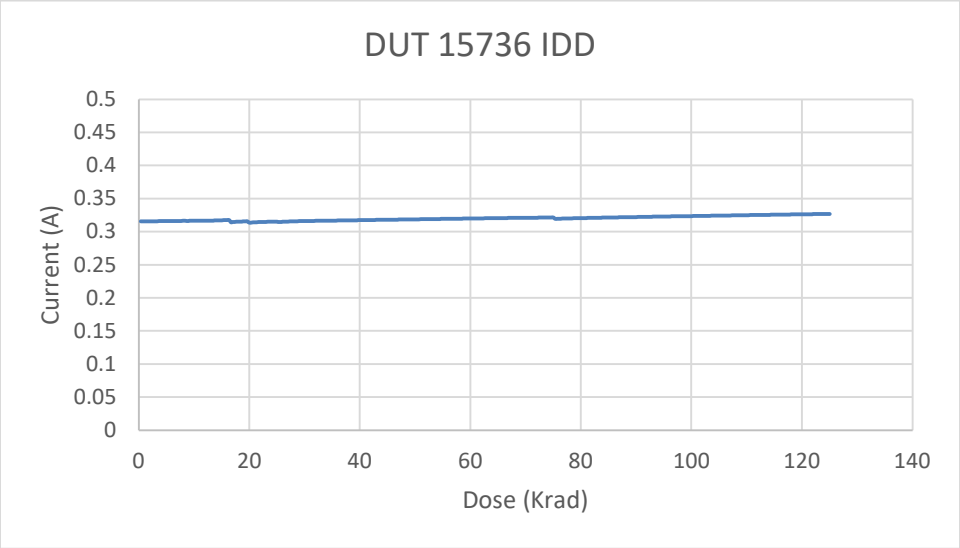

Fig. 2. DUT 15736 core power supply current (I_{DD}) versus TID

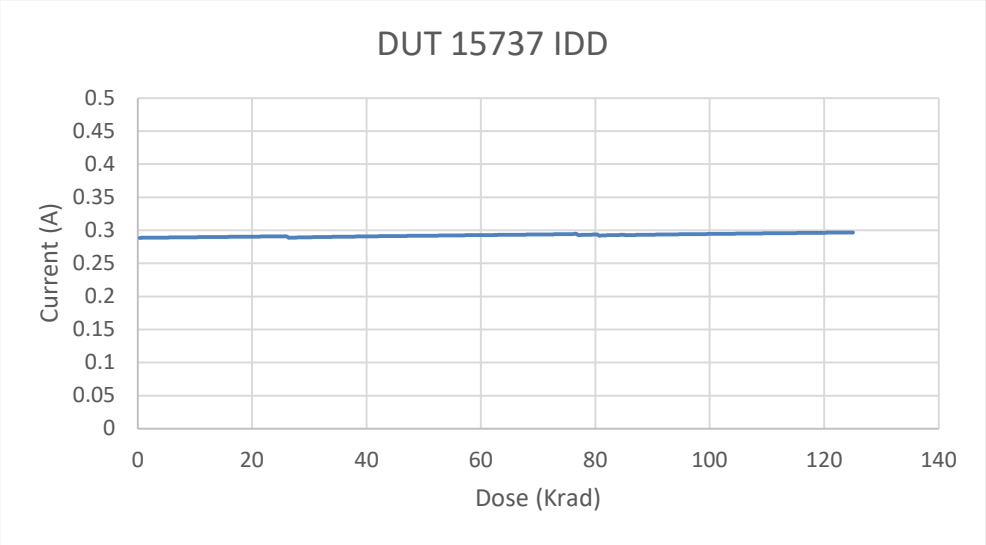

Fig. 3. DUT 15737 core power supply current (I_{DD}) versus TID

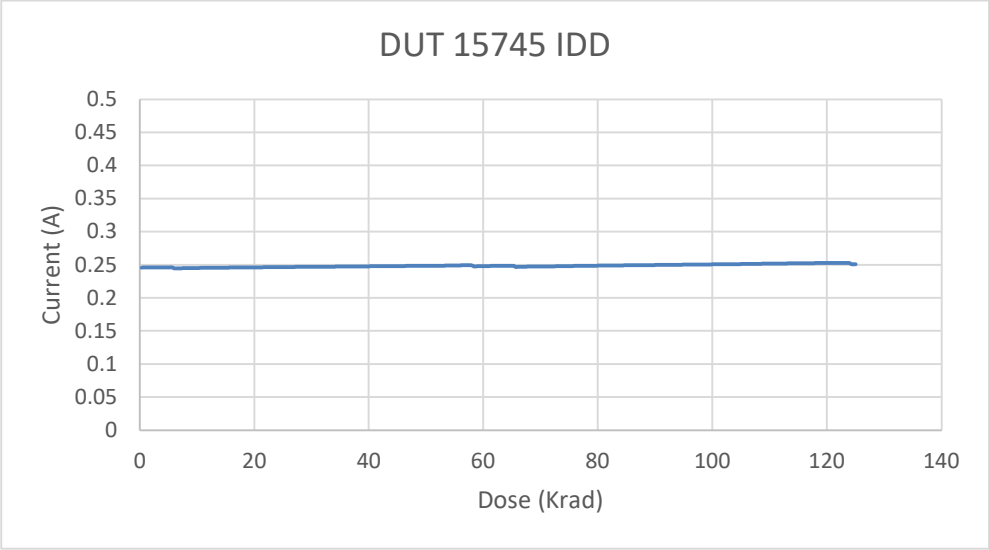

Fig. 4. DUT 15745 core power supply current (I_{DD}) versus TID

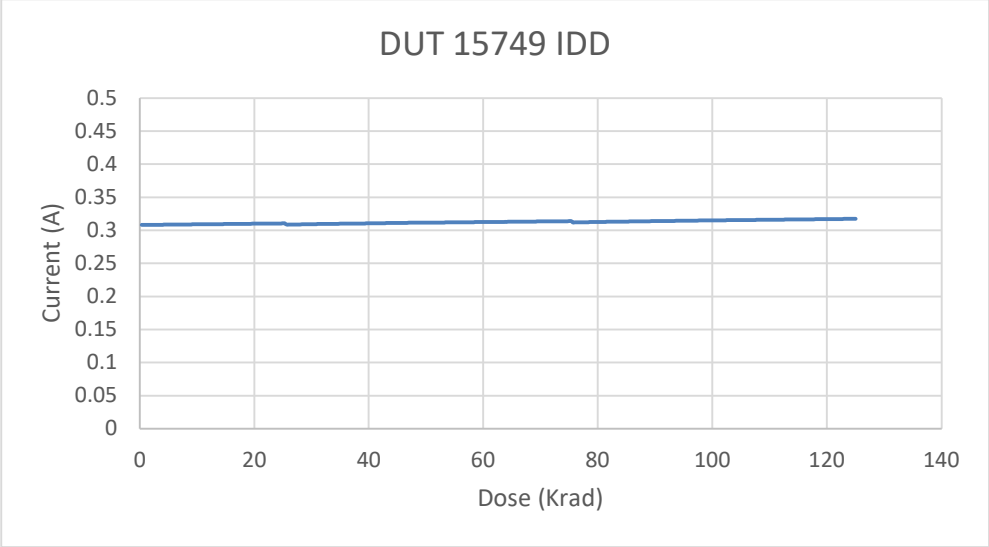

Fig. 5. DUT 15749 core power supply current (I_{DD}) versus TID

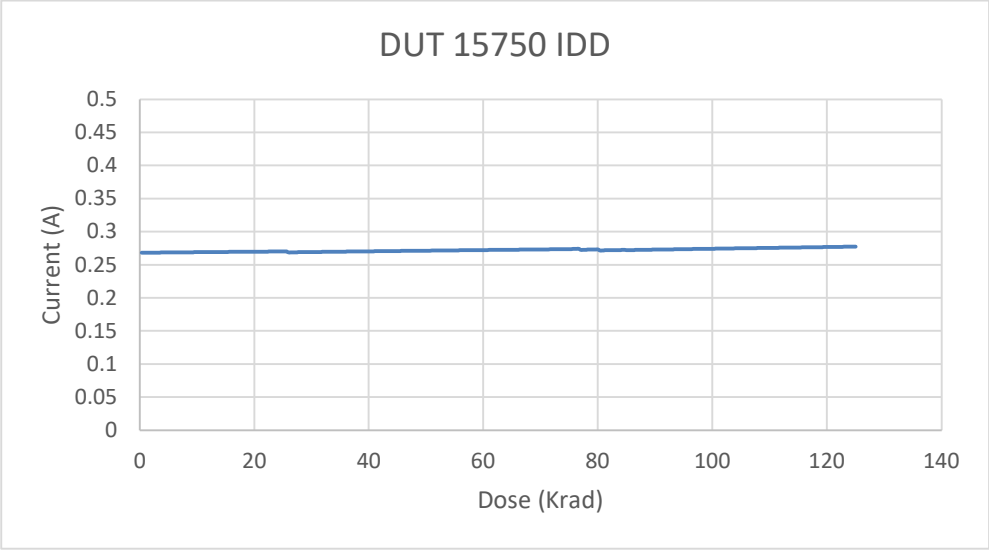

Fig. 6. DUT 15750 core power supply current (I_{DD}) versus TID

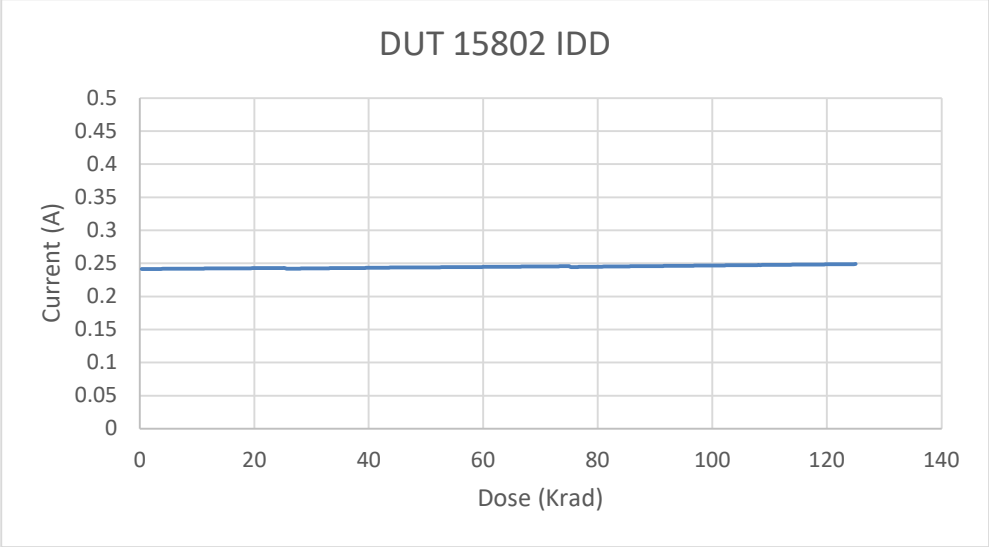

Fig. 7. DUT 15802 core power supply current (I_{DD}) versus TID

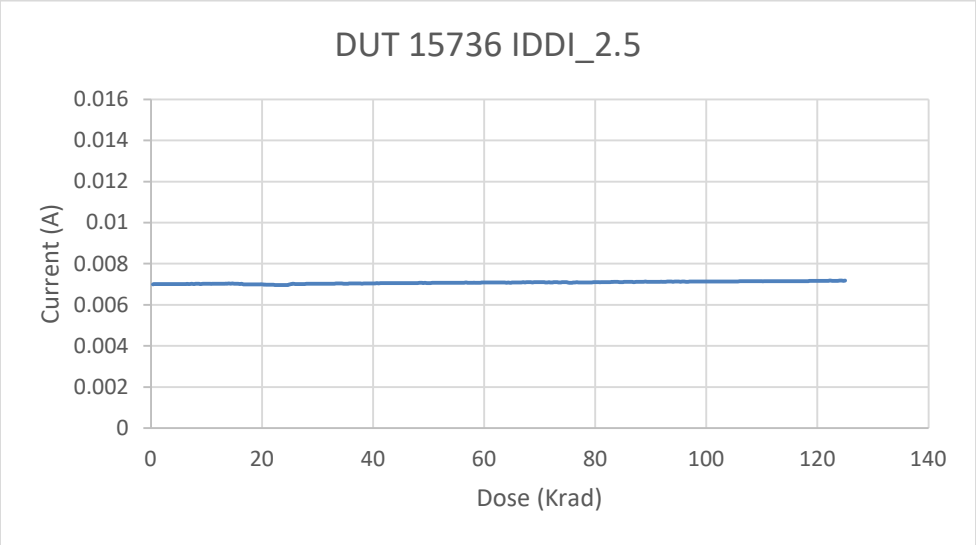

Fig. 8. DUT 15736 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

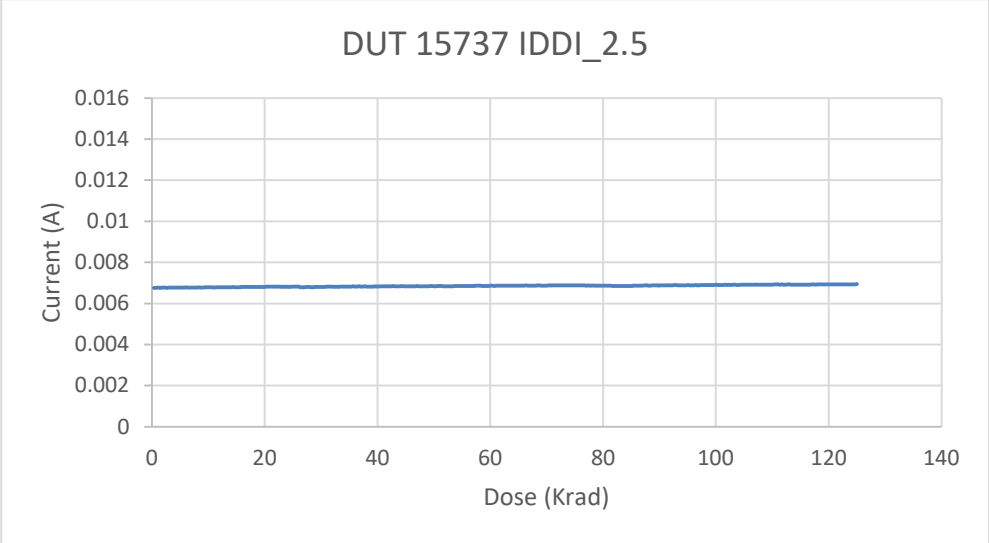

Fig. 9. DUT 15737 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

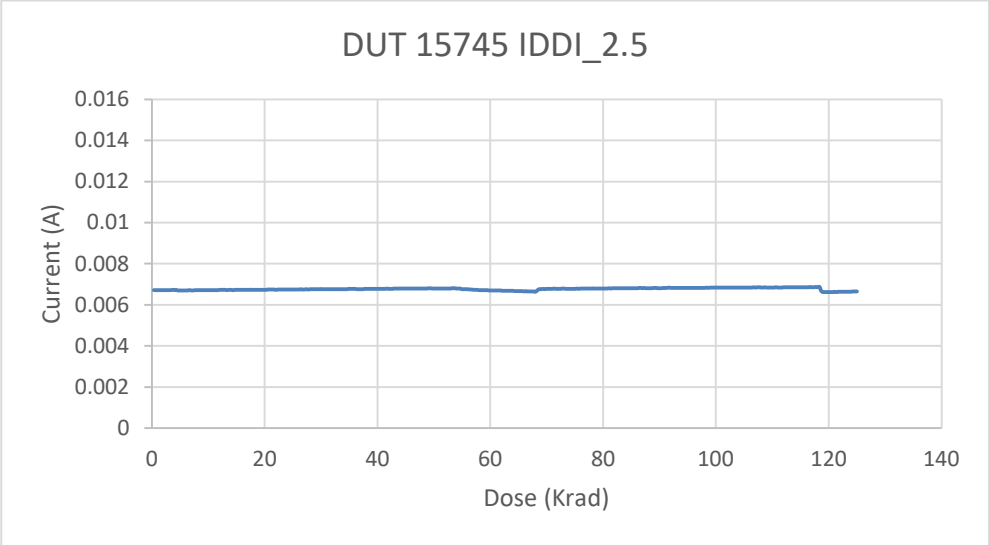

Fig. 10. DUT 15745 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

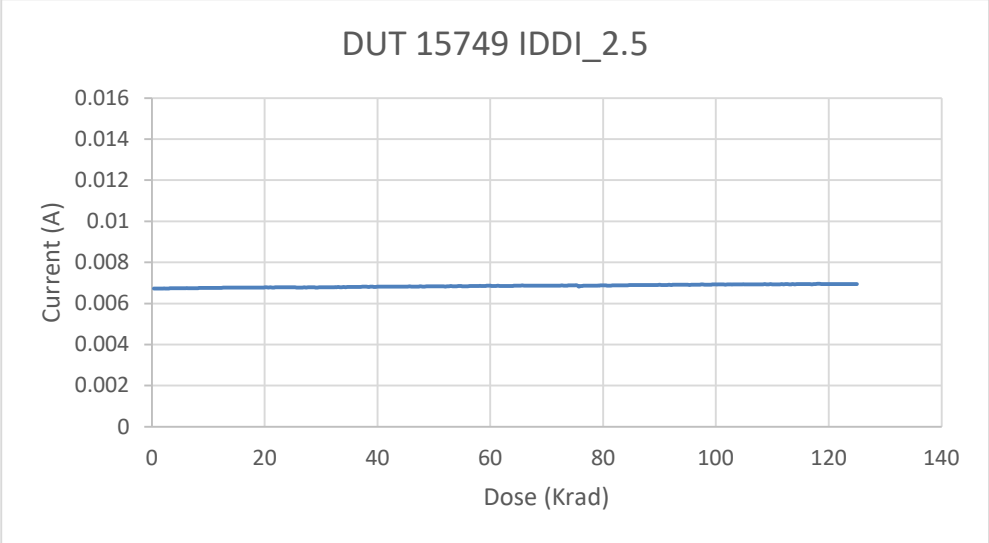

Fig. 11. DUT 15749 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

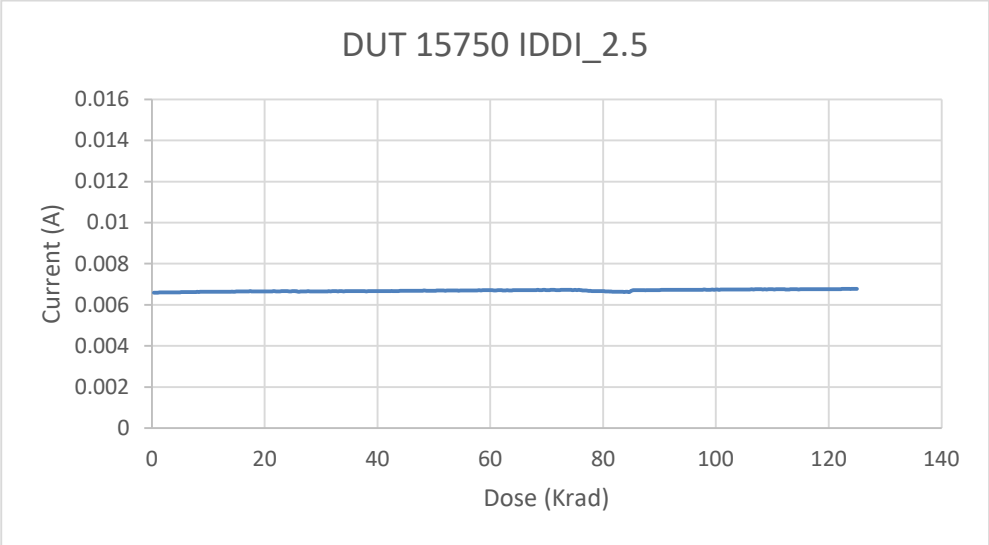

Fig. 12. DUT 15750 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

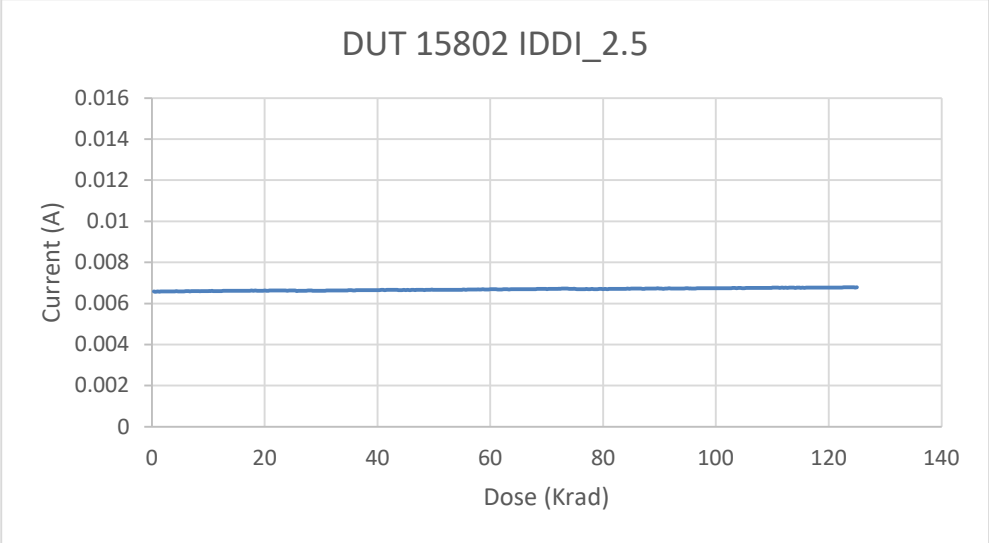

Fig. 13. DUT 15802 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

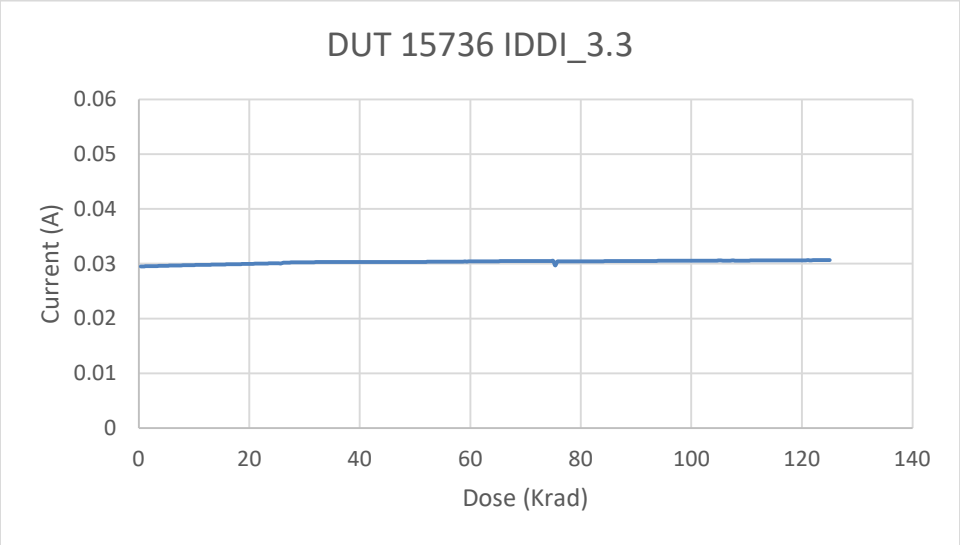

Fig. 14. DUT 15736 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

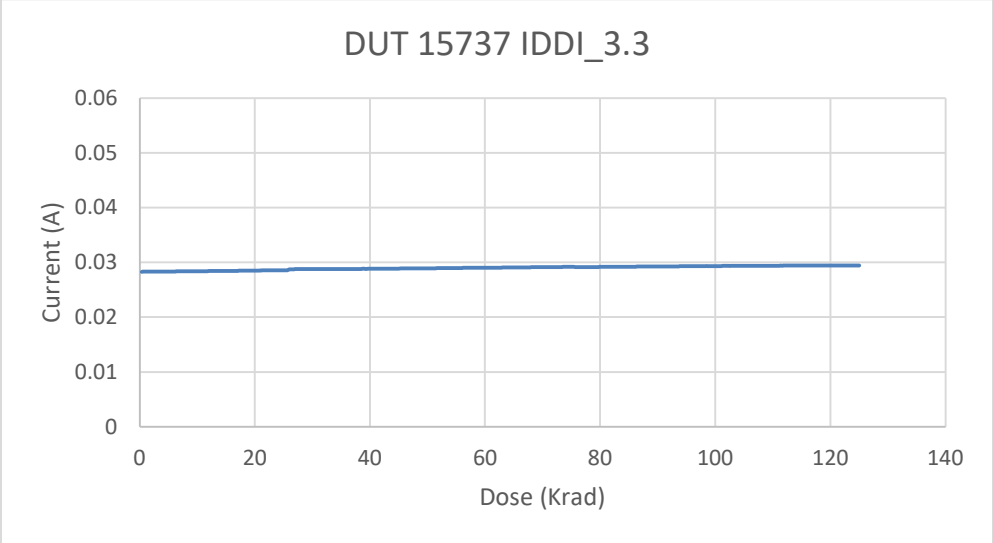

Fig. 15. DUT 15737 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

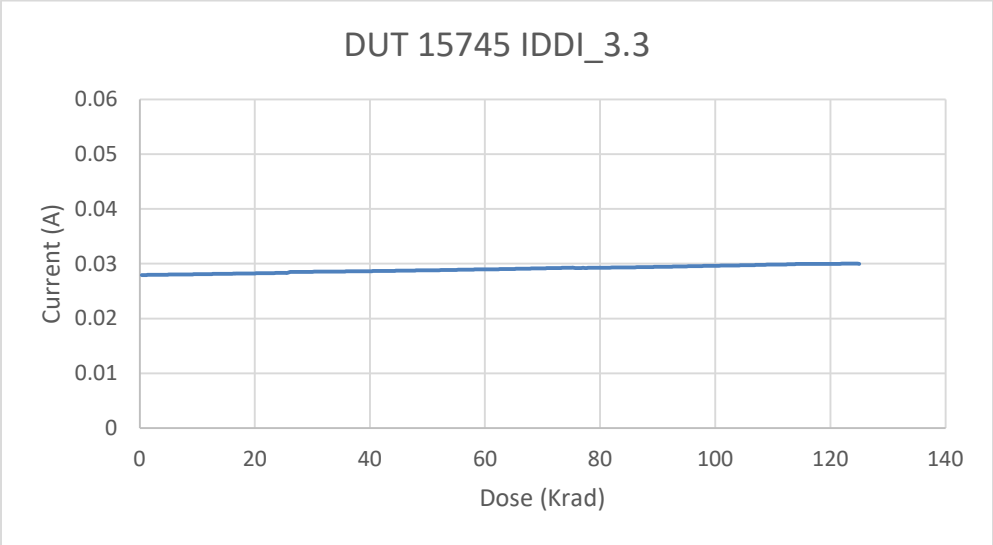

Fig. 16. DUT 15745 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

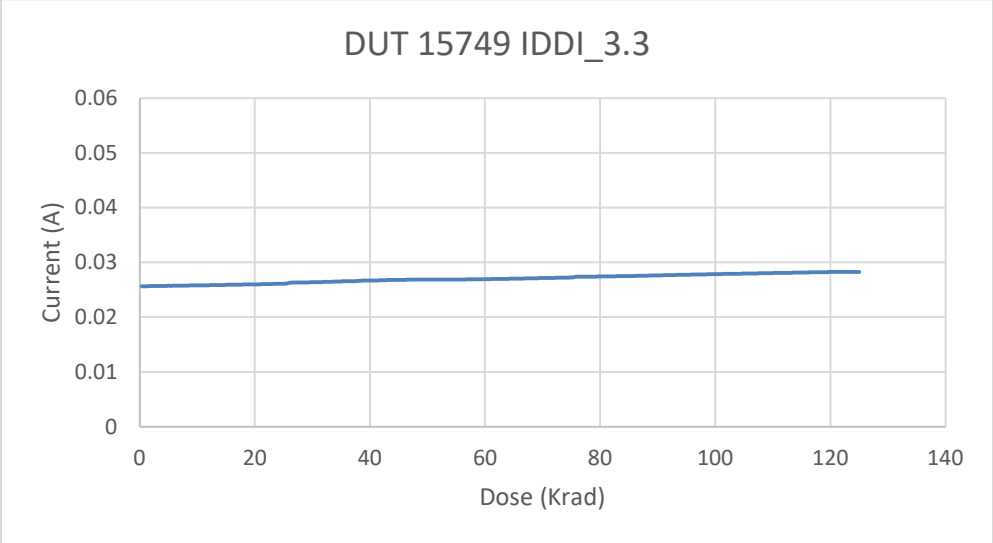

Fig. 17. DUT 15749 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

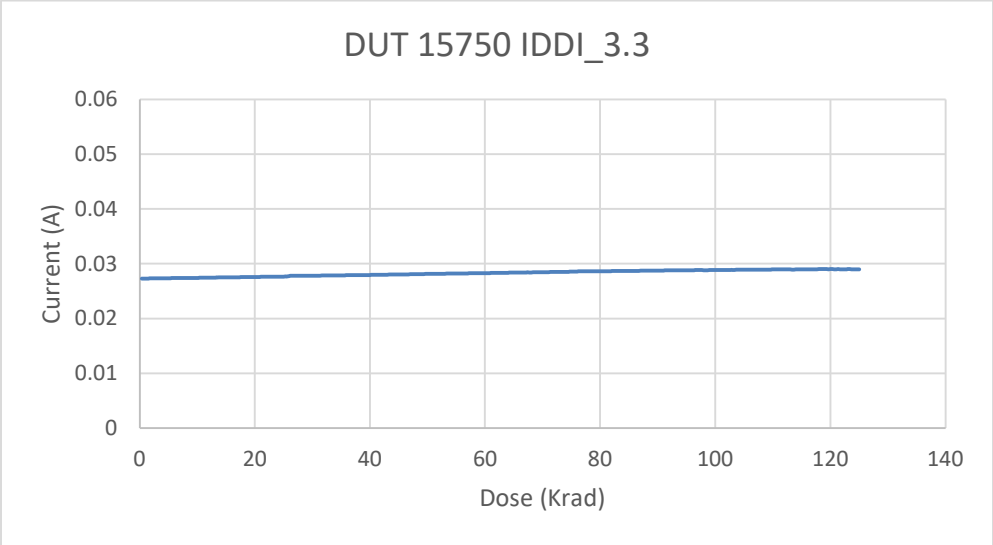

Fig. 18. DUT 15750 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

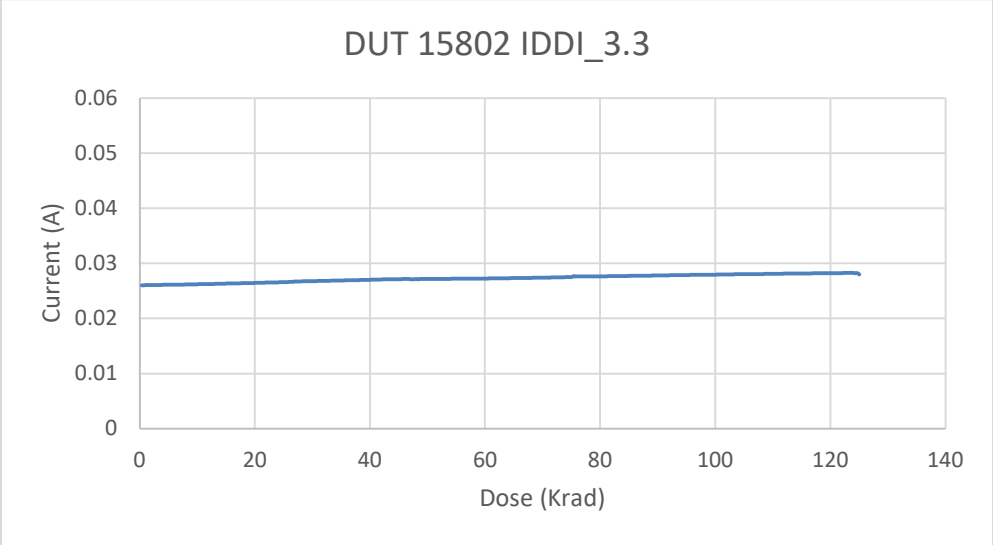

Fig. 19. DUT 15802 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

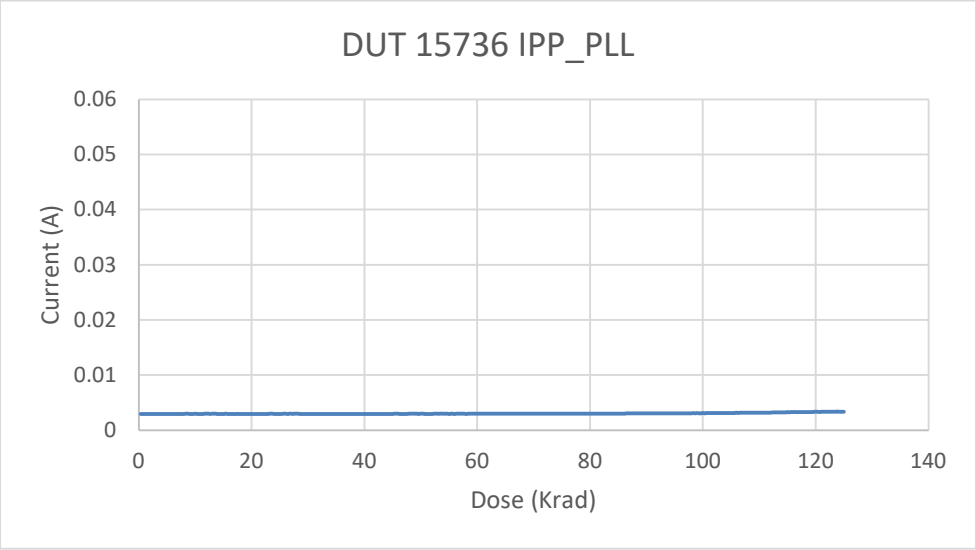

Fig. 20. DUT 15736 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

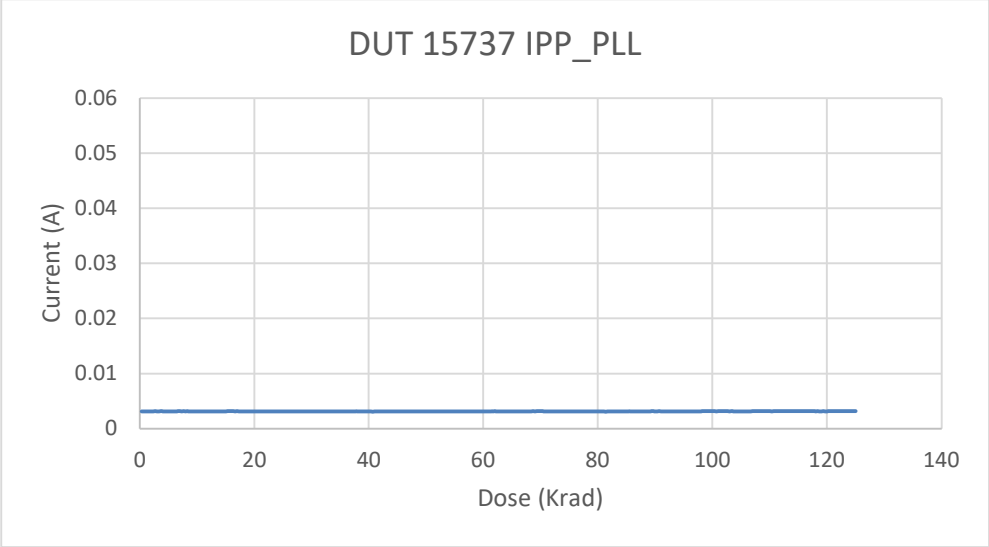

Fig. 21. DUT 15737 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

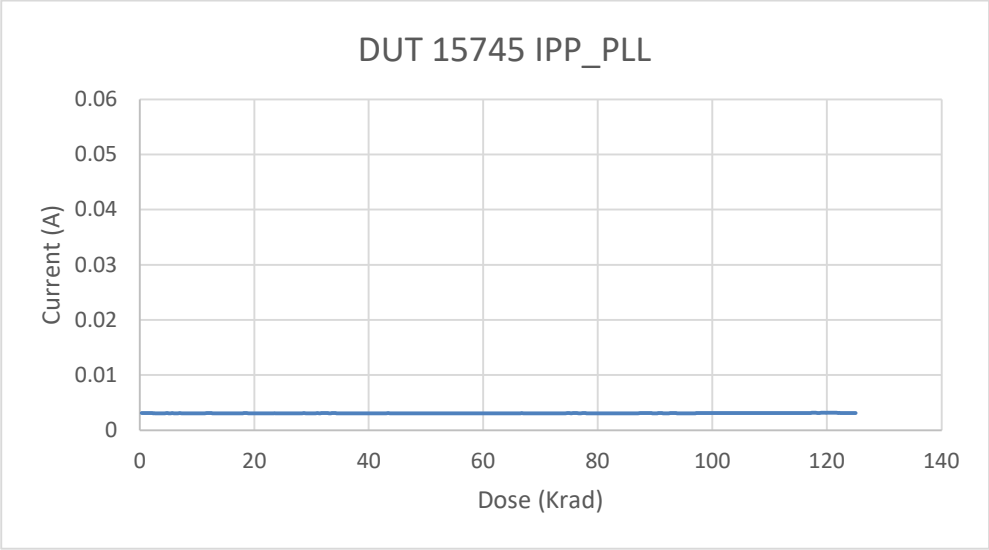

Fig. 22. DUT 15745 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

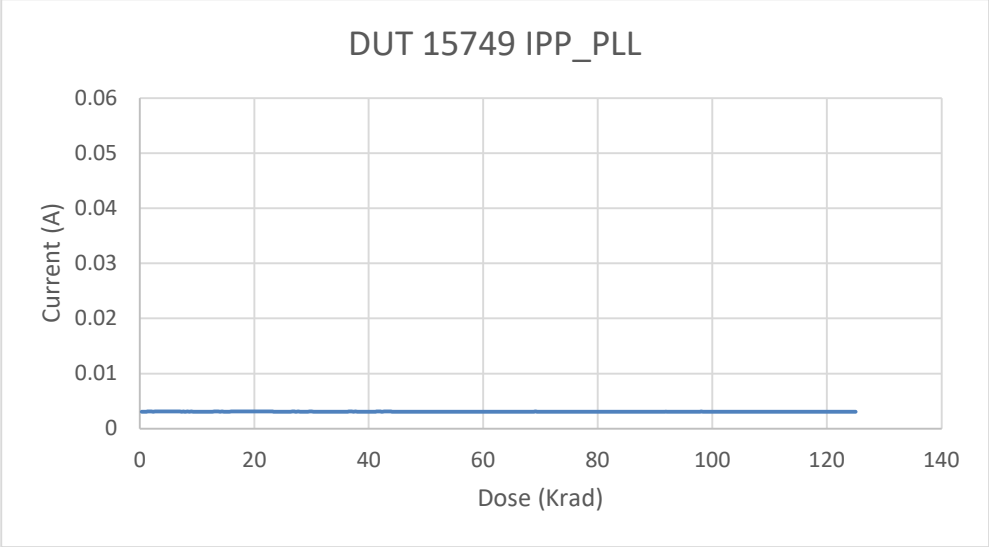

Fig. 23. DUT 15749 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

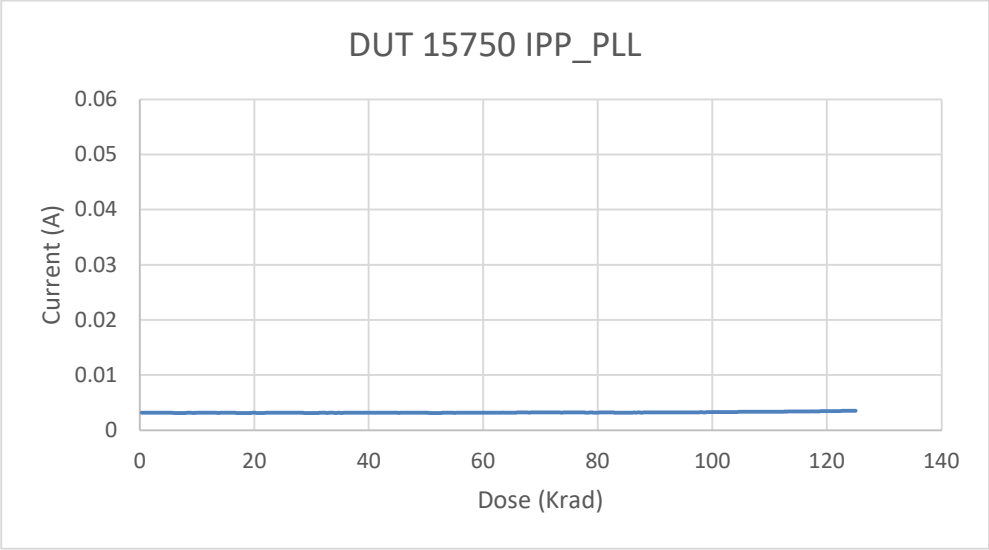

Fig. 24. DUT 15750 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

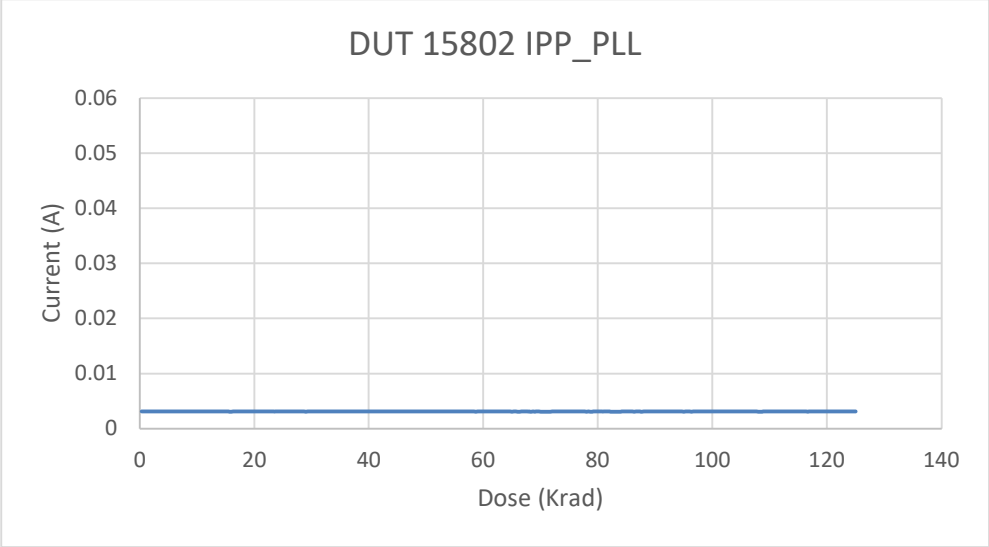

Fig. 25. DUT 15802 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

C. Single-Ended Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design starts to switch. VIH is the input trip point when the input is going high to low and VIL is the input trip point when the input is going low to high. The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential input and recorded as pass or fail. All I/Os are tested at their respective I/O standards and are compliant to the JEDEC specs. Refer to http://www.microsemi.com/document-portal/doc_view/135193-ds0131-rtg4-fpga-datasheet for more information.

The 3 DUTs tested passed with respect to the testing specification pre and post-irradiation. This pass/fail is determined as part of the ATE test program used to perform pre and post-irradiation electrical parametric measurements.

Table. 8. VIH Summary

DUT	Pre-irradiation	Post-irradiation
15736	Passed	Passed
15737	Passed	Passed
15745	Passed	Passed
15749	Passed	Passed
15750	Passed	Passed
15802	Passed	Passed

Table. 9. VIL Summary

DUT	Pre-irradiation	Post-irradiation
15736	Passed	Passed
15737	Passed	Passed
15745	Passed	Passed
15749	Passed	Passed
15750	Passed	Passed
15802	Passed	Passed

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-irradiation output-drive voltages (VOL/VOH) are performed on all available IOs. The measurements performed pre and post irradiation are within the specification limits; in each case, the radiation-induced degradation is within 10%. For the purpose of this report, the measurements presented below in tables 10 through 33 are sampled on several pins used in the burn in design.

Table. 10. LVCMOS 25 VOH – DUT 15736

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.137	2.136	2.208	2.208	2.183	2.181	2.163	2.162	2.137	2.136	2.126	2.126
PLL_MON	81	2.134	2.132	2.203	2.202	2.173	2.173	2.152	2.151	2.120	2.119	2.107	2.105
TID_BUF_OUT	92	2.133	2.132	2.202	2.201	2.173	2.172	2.151	2.150	2.118	2.117	2.104	2.103
TOGGLE_MON	97	2.134	2.134	2.204	2.204	2.176	2.174	2.155	2.154	2.124	2.123	2.111	2.109
MONITOR	104	2.133	2.132	2.202	2.202	2.174	2.172	2.152	2.151	2.120	2.119	2.107	2.105

Table. 11. LVCMOS 25 VOH – DUT 15737

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.138	2.137	2.209	2.208	2.182	2.181	2.164	2.163	2.137	2.136	2.126	2.125
PLL_MON	81	2.135	2.134	2.203	2.203	2.174	2.173	2.152	2.151	2.119	2.119	2.107	2.106
TID_BUF_OUT	92	2.134	2.134	2.203	2.202	2.173	2.172	2.151	2.150	2.118	2.117	2.104	2.103
TOGGLE_MON	97	2.135	2.134	2.204	2.204	2.177	2.175	2.155	2.155	2.124	2.124	2.111	2.110
MONITOR	104	2.134	2.133	2.203	2.202	2.174	2.173	2.152	2.152	2.120	2.118	2.105	2.104

Table. 12. LVCMOS 25 VOH – DUT 15745

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.137	2.136	2.208	2.208	2.182	2.182	2.164	2.163	2.136	2.136	2.126	2.125
PLL_MON	81	2.133	2.133	2.203	2.202	2.174	2.173	2.152	2.151	2.120	2.119	2.106	2.105
TID_BUF_OUT	92	2.133	2.133	2.202	2.202	2.173	2.172	2.151	2.150	2.118	2.118	2.104	2.103
TOGGLE_MON	97	2.135	2.134	2.204	2.204	2.176	2.175	2.155	2.154	2.124	2.123	2.111	2.110
MONITOR	104	2.133	2.133	2.202	2.203	2.174	2.173	2.152	2.151	2.119	2.119	2.105	2.105

Table. 13. LVCMOS 25 VOH – DUT 15749

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.139	2.138	2.210	2.209	2.184	2.183	2.166	2.164	2.139	2.138	2.128	2.127
PLL_MON	81	2.135	2.135	2.204	2.203	2.175	2.174	2.154	2.153	2.122	2.120	2.107	2.106
TID_BUF_OUT	92	2.134	2.134	2.203	2.203	2.174	2.174	2.152	2.152	2.119	2.119	2.106	2.105
TOGGLE_MON	97	2.136	2.136	2.206	2.205	2.178	2.177	2.157	2.156	2.126	2.126	2.113	2.112
MONITOR	104	2.136	2.135	2.204	2.204	2.175	2.174	2.154	2.153	2.121	2.120	2.107	2.106

Table. 14. LVCMOS 25 VOH – DUT 15750

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.137	2.136	2.208	2.208	2.183	2.182	2.164	2.164	2.137	2.137	2.126	2.125
PLL_MON	81	2.134	2.133	2.203	2.202	2.174	2.174	2.153	2.152	2.120	2.120	2.107	2.106
TID_BUF_OUT	92	2.133	2.132	2.202	2.202	2.173	2.172	2.151	2.151	2.118	2.118	2.104	2.103
TOGGLE_MON	97	2.135	2.134	2.204	2.204	2.176	2.176	2.155	2.155	2.124	2.124	2.112	2.111
MONITOR	104	2.134	2.133	2.203	2.202	2.174	2.174	2.152	2.152	2.120	2.120	2.107	2.106

Table. 15. LVCMOS 25 VOH – DUT 15802

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.140	2.140	2.211	2.210	2.185	2.185	2.167	2.166	2.140	2.140	2.129	2.129
PLL_MON	81	2.137	2.137	2.205	2.204	2.176	2.176	2.155	2.155	2.123	2.122	2.110	2.109
TID_BUF_OUT	92	2.137	2.136	2.205	2.205	2.175	2.175	2.154	2.153	2.121	2.120	2.107	2.107
TOGGLE_MON	97	2.138	2.138	2.207	2.206	2.179	2.179	2.158	2.157	2.127	2.127	2.114	2.114
MONITOR	104	2.137	2.136	2.205	2.204	2.176	2.176	2.156	2.155	2.123	2.123	2.109	2.108

Table. 16. LVCMOS 25 VOL – DUT 15736

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	236.0	236.6	165.1	165.5	190.7	190.9	208.5	208.7	235.1	235.5	246.0	246.2
PLL_MON	81	239.8	239.8	171.0	171.0	199.3	199.5	220.0	220.2	251.7	252.0	265.2	265.6
TID_BUF_OUT	92	239.7	239.4	171.4	171.3	200.2	200.1	221.1	221.2	253.7	253.9	267.8	267.7
TOGGLE_MON	97	238.7	238.5	169.3	169.3	196.8	197.1	217.1	217.3	247.8	247.9	260.9	261.1
MONITOR	104	239.9	239.7	170.7	171.1	199.2	199.3	220.1	220.4	251.9	252.3	265.8	266.4

Table. 17. LVCMOS 25 VOL – DUT 15737

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	235.3	235.6	164.3	164.5	190.0	190.1	208.2	208.3	234.8	234.9	245.6	246.0
PLL_MON	81	238.5	238.4	170.5	170.6	198.7	198.8	219.6	219.5	251.8	251.6	265.0	265.1
TID_BUF_OUT	92	238.5	238.3	170.8	170.6	199.5	199.3	220.9	220.5	253.6	253.1	267.3	267.1
TOGGLE_MON	97	237.0	236.5	168.5	168.4	196.2	195.8	216.4	216.2	247.2	247.3	260.1	260.3
MONITOR	104	238.4	238.2	170.2	170.3	198.9	199.0	219.6	219.6	252.0	251.9	265.9	266.1

Table. 18. LVCMOS 25 VOL – DUT 15745

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	235.6	235.2	164.1	164.4	189.7	189.9	207.9	208.0	234.2	234.6	245.1	245.4
PLL_MON	81	238.5	238.2	169.9	170.0	198.3	198.1	218.9	218.7	250.8	250.6	264.6	264.5
TID_BUF_OUT	92	238.1	237.6	170.3	170.3	199.2	198.8	220.2	220.2	252.8	252.7	266.8	266.5
TOGGLE_MON	97	237.1	236.6	168.4	168.2	195.9	195.9	216.3	215.8	246.6	246.7	259.9	259.8
MONITOR	104	238.1	237.9	170.0	169.9	198.6	198.6	219.2	219.2	251.5	251.8	265.3	265.5

Table. 19. LVCMOS 25 VOL – DUT 15749

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	235.1	234.9	164.1	163.8	189.6	189.6	207.4	207.7	233.9	233.8	244.5	244.9
PLL_MON	81	238.5	238.0	170.0	169.9	198.3	198.2	218.9	218.8	250.9	250.8	264.5	264.4
TID_BUF_OUT	92	238.7	238.4	170.7	170.2	199.2	198.7	220.2	220.0	252.9	252.4	267.0	266.4
TOGGLE_MON	97	236.6	236.0	168.0	167.7	195.6	195.3	215.7	215.4	246.1	246.2	259.2	259.1
MONITOR	104	237.9	237.3	169.8	169.5	198.3	198.4	219.0	218.9	251.1	251.2	265.1	264.9

Table. 20. LVCMOS 25 VOL – DUT 15750

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	234.8	235.2	163.8	163.9	189.1	189.4	207.2	207.4	233.4	233.5	244.4	244.8
PLL_MON	81	238.0	237.8	169.6	169.3	198.0	197.9	218.6	218.6	250.3	250.3	263.9	264.1
TID_BUF_OUT	92	239.0	238.5	170.4	170.5	198.9	199.0	220.1	219.9	252.7	252.3	266.4	266.5
TOGGLE_MON	97	237.1	236.5	168.2	167.9	195.6	195.3	215.8	215.6	246.0	246.2	259.1	259.3
MONITOR	104	238.1	237.9	169.8	169.7	198.2	197.9	219.1	218.9	250.9	251.2	264.9	264.9

Table. 21. LVCMOS 25 VOL – DUT 15802

		2mA		4mA		6mA		8mA		12mA		14mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	232.3	232.2	162.0	161.9	187.3	187.7	205.3	205.4	231.5	231.9	242.2	242.6
PLL_MON	81	235.4	235.0	167.9	167.8	195.7	195.6	216.1	216.1	247.7	247.4	261.3	261.1
TID_BUF_OUT	92	235.4	234.6	168.4	168.4	197.0	196.7	217.9	217.5	250.4	249.9	264.3	263.9
TOGGLE_MON	97	233.7	233.2	166.2	165.8	193.3	193.2	213.6	213.3	244.0	243.8	257.1	256.9
MONITOR	104	235.0	234.4	167.5	167.7	195.7	195.6	216.5	216.4	248.2	248.0	261.8	261.8

Table. 22. LVTTL VOH – DUT 15736

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.923	2.923	2.916	2.915	2.903	2.902	2.889	2.888	2.876	2.875
PLL_MON	81	2.920	2.918	2.910	2.909	2.891	2.890	2.872	2.871	2.853	2.853
TID_BUF_OUT	92	2.919	2.918	2.910	2.909	2.889	2.889	2.870	2.869	2.850	2.850
TOGGLE_MON	97	2.920	2.920	2.911	2.911	2.894	2.893	2.876	2.875	2.859	2.857
MONITOR	104	2.919	2.918	2.910	2.909	2.891	2.890	2.872	2.871	2.853	2.852

Table. 23. LVTTL VOH – DUT 15737

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.923	2.924	2.917	2.916	2.903	2.902	2.889	2.888	2.875	2.874
PLL_MON	81	2.921	2.920	2.911	2.910	2.892	2.891	2.872	2.871	2.853	2.852
TID_BUF_OUT	92	2.920	2.920	2.910	2.909	2.891	2.890	2.871	2.870	2.851	2.850
TOGGLE_MON	97	2.922	2.921	2.912	2.911	2.894	2.894	2.877	2.876	2.859	2.858
MONITOR	104	2.920	2.920	2.911	2.910	2.892	2.891	2.872	2.871	2.853	2.851

Table. 24. LVTTL VOH – DUT 15745

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.923	2.922	2.917	2.916	2.902	2.902	2.889	2.888	2.876	2.875
PLL_MON	81	2.920	2.919	2.911	2.910	2.892	2.891	2.872	2.872	2.853	2.853
TID_BUF_OUT	92	2.920	2.920	2.910	2.909	2.890	2.890	2.870	2.870	2.850	2.850
TOGGLE_MON	97	2.921	2.921	2.912	2.911	2.894	2.893	2.877	2.876	2.859	2.858
MONITOR	104	2.920	2.920	2.910	2.909	2.891	2.890	2.872	2.872	2.853	2.852

Table. 25. LVTTL VOH – DUT 15749

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.925	2.924	2.918	2.917	2.904	2.903	2.891	2.889	2.878	2.876
PLL_MON	81	2.921	2.921	2.912	2.911	2.893	2.892	2.874	2.873	2.854	2.854
TID_BUF_OUT	92	2.921	2.920	2.911	2.910	2.891	2.890	2.871	2.872	2.853	2.852
TOGGLE_MON	97	2.923	2.922	2.914	2.913	2.896	2.895	2.878	2.877	2.861	2.860
MONITOR	104	2.921	2.921	2.912	2.911	2.892	2.892	2.874	2.873	2.855	2.854

Table. 26. LVTTL VOH – DUT 15750

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.923	2.922	2.917	2.916	2.903	2.902	2.889	2.889	2.877	2.875
PLL_MON	81	2.920	2.920	2.911	2.910	2.892	2.891	2.873	2.872	2.854	2.853
TID_BUF_OUT	92	2.919	2.919	2.909	2.909	2.890	2.890	2.871	2.870	2.851	2.851
TOGGLE_MON	97	2.921	2.921	2.912	2.912	2.894	2.894	2.877	2.877	2.860	2.859
MONITOR	104	2.920	2.920	2.911	2.910	2.892	2.891	2.873	2.872	2.853	2.853

Table. 27. LVTTL VOH – DUT 15802

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	2.926	2.926	2.919	2.918	2.906	2.905	2.892	2.891	2.879	2.878
PLL_MON	81	2.923	2.922	2.914	2.913	2.895	2.894	2.876	2.875	2.857	2.856
TID_BUF_OUT	92	2.923	2.922	2.913	2.912	2.893	2.893	2.873	2.874	2.853	2.854
TOGGLE_MON	97	2.924	2.924	2.915	2.915	2.898	2.897	2.880	2.879	2.862	2.861
MONITOR	104	2.923	2.923	2.914	2.913	2.894	2.894	2.876	2.875	2.856	2.856

Table. 28. LVTTL VOL – DUT 15736

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	216.4	216.2	222.5	222.5	235.4	235.5	248.4	248.5	261.5	262.0
PLL_MON	81	219.7	219.6	228.6	228.7	246.9	247.1	265.2	265.5	283.8	284.1
TID_BUF_OUT	92	219.4	219.5	228.9	228.8	248.0	248.1	267.2	267.2	286.6	286.4
TOGGLE_MON	97	218.6	218.7	226.6	226.4	243.6	243.9	261.1	261.1	278.8	279.2
MONITOR	104	219.6	219.5	228.2	228.5	246.7	246.7	265.2	265.8	284.1	284.8

Table. 29. LVTTL VOL – DUT 15737

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	215.5	215.5	221.7	221.4	234.7	234.6	247.7	248.0	261.2	261.6
PLL_MON	81	218.6	218.2	227.4	227.4	246.1	246.0	264.9	265.0	283.9	283.9
TID_BUF_OUT	92	218.4	218.1	227.9	227.5	247.3	247.1	266.9	266.6	286.2	286.1
TOGGLE_MON	97	216.9	216.5	225.3	224.7	242.9	242.6	260.3	260.4	278.2	278.1
MONITOR	104	218.4	217.9	227.4	227.3	246.2	246.3	265.0	265.2	284.4	284.6

Table. 30. LVTTL VOL – DUT 15745

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	215.4	215.4	221.1	221.4	234.3	234.4	247.7	247.6	260.8	260.9
PLL_MON	81	218.5	217.8	227.2	226.8	245.5	245.2	264.1	263.9	283.0	283.1
TID_BUF_OUT	92	218.0	217.5	227.4	227.1	246.5	246.4	266.0	265.8	285.9	285.0
TOGGLE_MON	97	217.0	216.5	225.3	225.0	242.4	242.4	259.7	259.7	277.5	277.5
MONITOR	104	218.2	217.6	227.5	227.1	245.8	245.7	264.7	264.7	284.1	284.0

Table. 31. LVTTL VOL – DUT 15749

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	214.9	215.1	221.2	221.6	233.8	234.2	247.2	247.5	260.5	260.9
PLL_MON	81	218.3	218.2	227.2	227.2	245.5	245.4	264.2	264.2	282.9	283.2
TID_BUF_OUT	92	218.8	218.4	227.9	227.4	246.7	246.3	266.1	265.8	285.6	285.3
TOGGLE_MON	97	216.5	216.3	224.7	224.7	241.8	241.8	259.4	259.4	277.0	276.9
MONITOR	104	217.9	217.7	226.6	226.6	245.5	245.7	264.1	264.4	283.2	283.6

Table. 32. LVTTL VOL – DUT 15750

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	215.2	215.2	221.0	221.1	233.8	233.7	246.7	246.7	260.1	259.9
PLL_MON	81	218.1	217.7	226.9	226.3	245.1	244.8	263.8	263.4	282.7	282.5
TID_BUF_OUT	92	219.1	218.3	228.0	227.7	246.7	246.2	265.7	265.6	285.5	284.9
TOGGLE_MON	97	217.2	216.7	225.5	224.7	242.3	241.8	259.6	259.1	277.1	276.8
MONITOR	104	218.1	217.8	226.8	226.5	245.5	245.2	264.3	264.1	283.4	283.3

Table. 33. LVTTL VOL – DUT 15802

		2mA		4mA		8mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
EPCSRST_N	74	212.6	212.7	218.8	218.9	231.8	231.3	244.9	244.6	258.4	258.3
PLL_MON	81	216.0	215.3	224.5	223.8	242.9	242.1	260.9	260.6	279.9	279.6
TID_BUF_OUT	92	215.8	215.2	224.8	224.4	244.4	244.0	263.7	263.2	283.8	282.8
TOGGLE_MON	97	214.3	213.6	222.6	221.8	239.9	239.4	257.4	256.9	275.0	274.6
MONITOR	104	215.5	214.8	224.0	223.7	242.9	242.3	261.3	261.3	280.5	280.2

E. Propagation Delay

Table 34 lists the pre-irradiation and post-irradiation propagation delay measurements. It shows that the change due to radiation on each DUT is not significant and every DUT passes the 10% degradation criterion.

Table. 34. Pre-irradiation and Post-irradiation Propagation Delay Change

DUT	Total Dose	Pre-irradiation (µs)	Post-irradiation (µs)	Change Degradation (%)
15736	125 krad	0.421	0.427	1.43
15737	125 krad	0.425	0.433	1.88
15745	125 krad	0.432	0.436	0.93
15749	125 krad	0.427	0.436	2.11
15750	125 krad	0.435	0.442	1.61
15802	125 krad	0.432	0.44	1.85

F. Transition Time

The figures below show the pre-irradiation and post-irradiation transitions edges. In each case the radiation induced transition degradation is not observable.

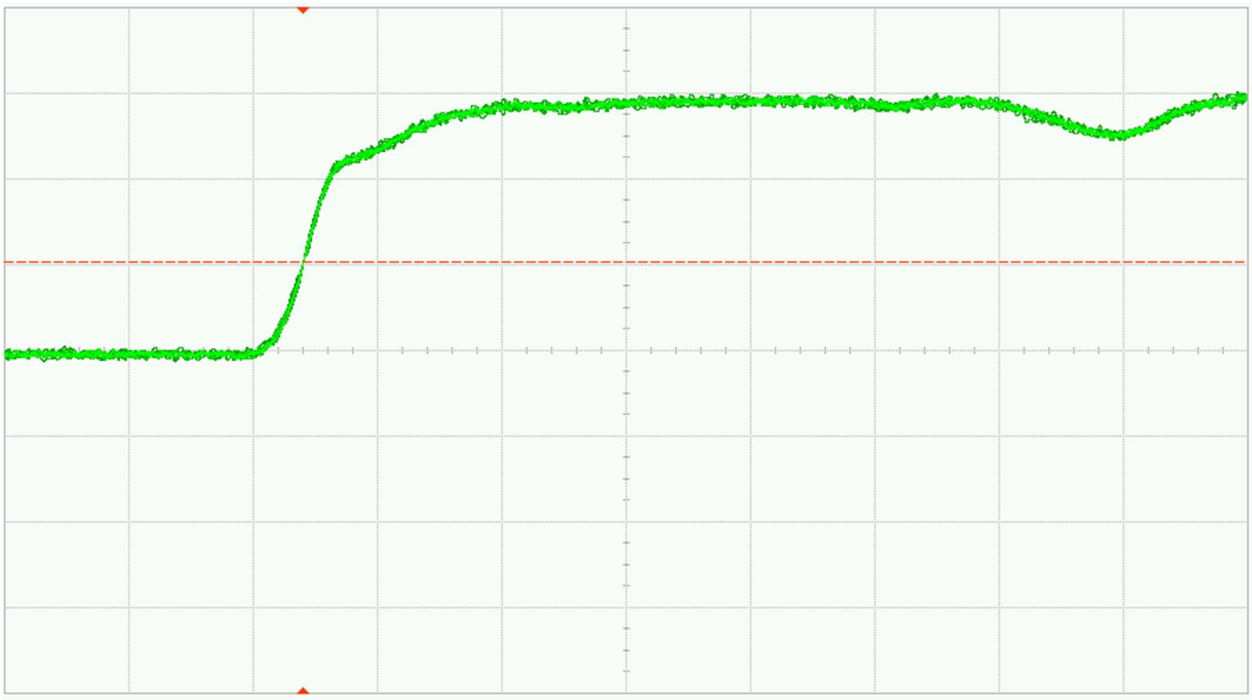

Fig. 26 (a). DUT 15736 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

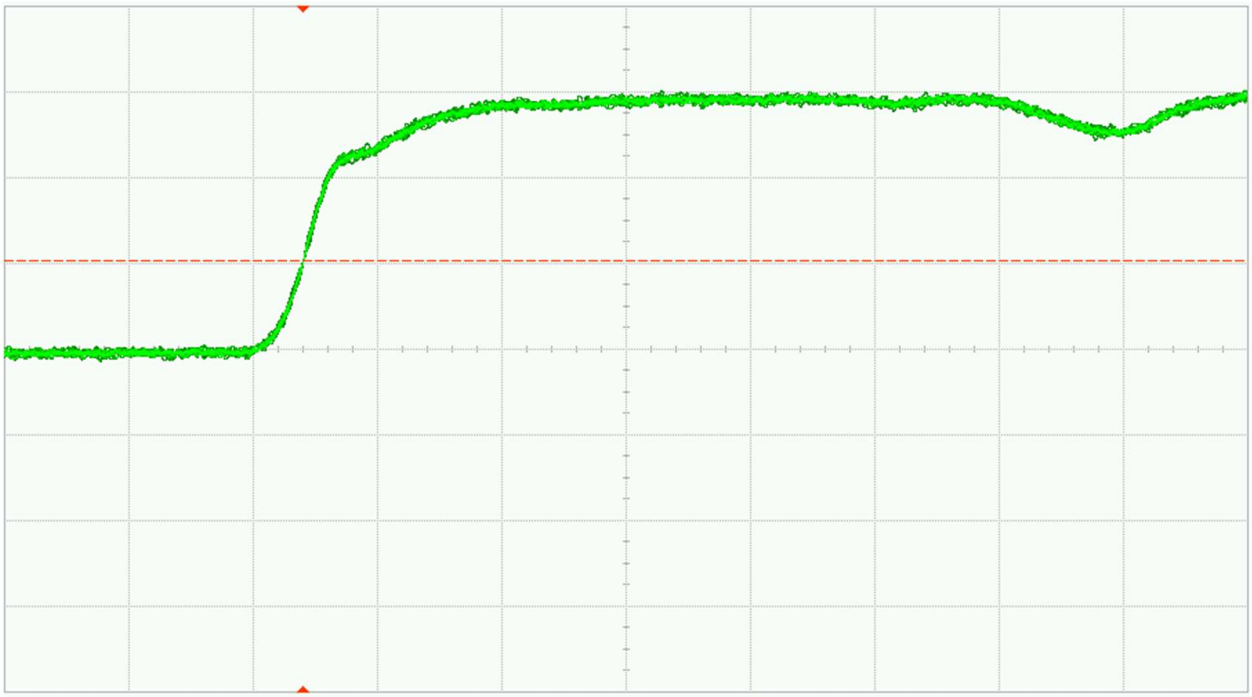

Fig. 26 (b). DUT 15736 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

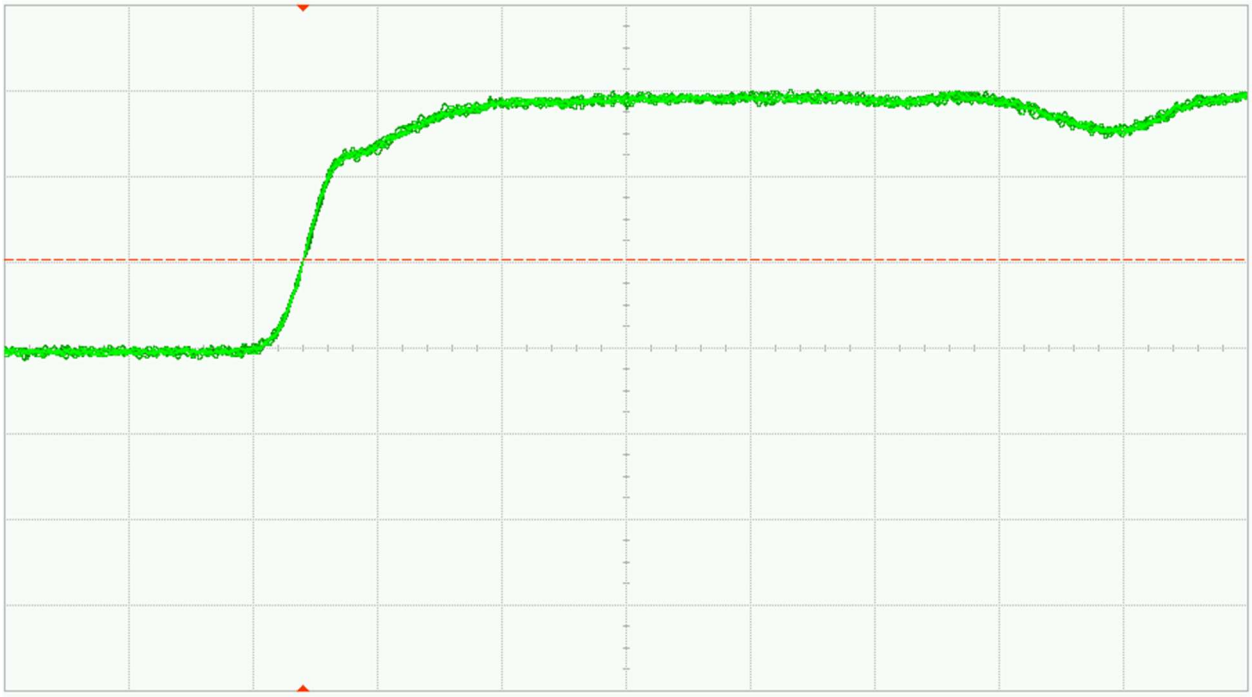

Fig. 27 (a). DUT 15737 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

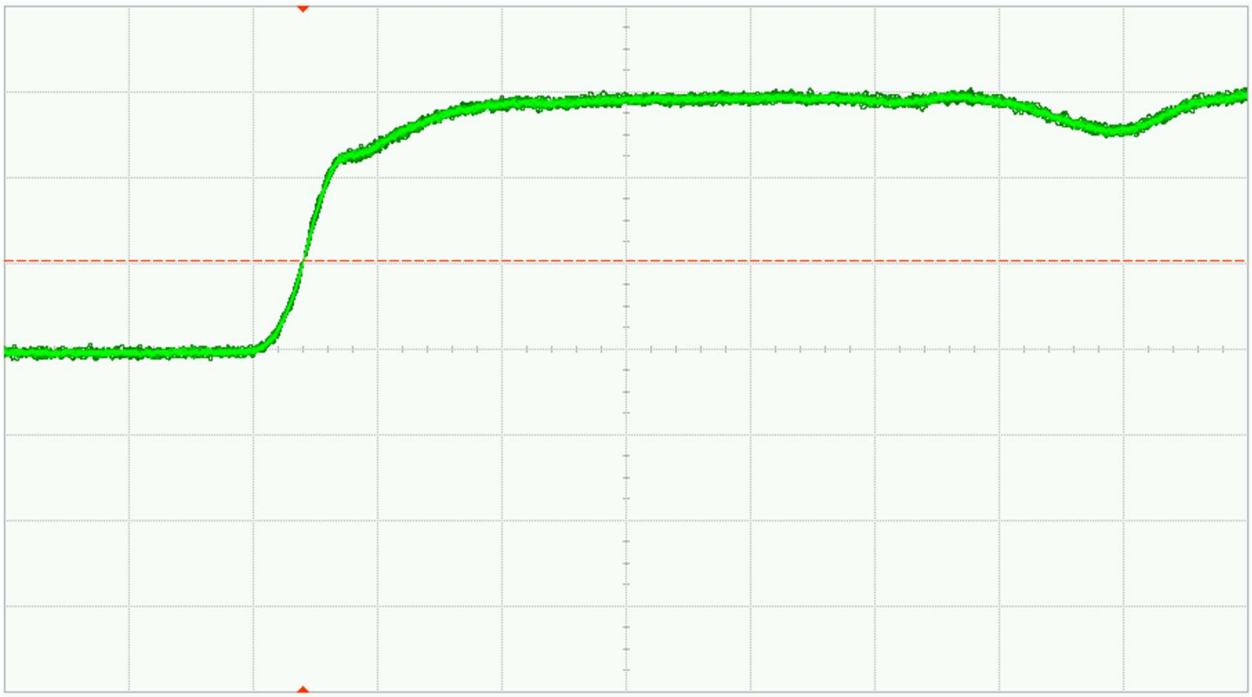

Fig. 27 (b). DUT 15737 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Fig. 28 (a). DUT 15745 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

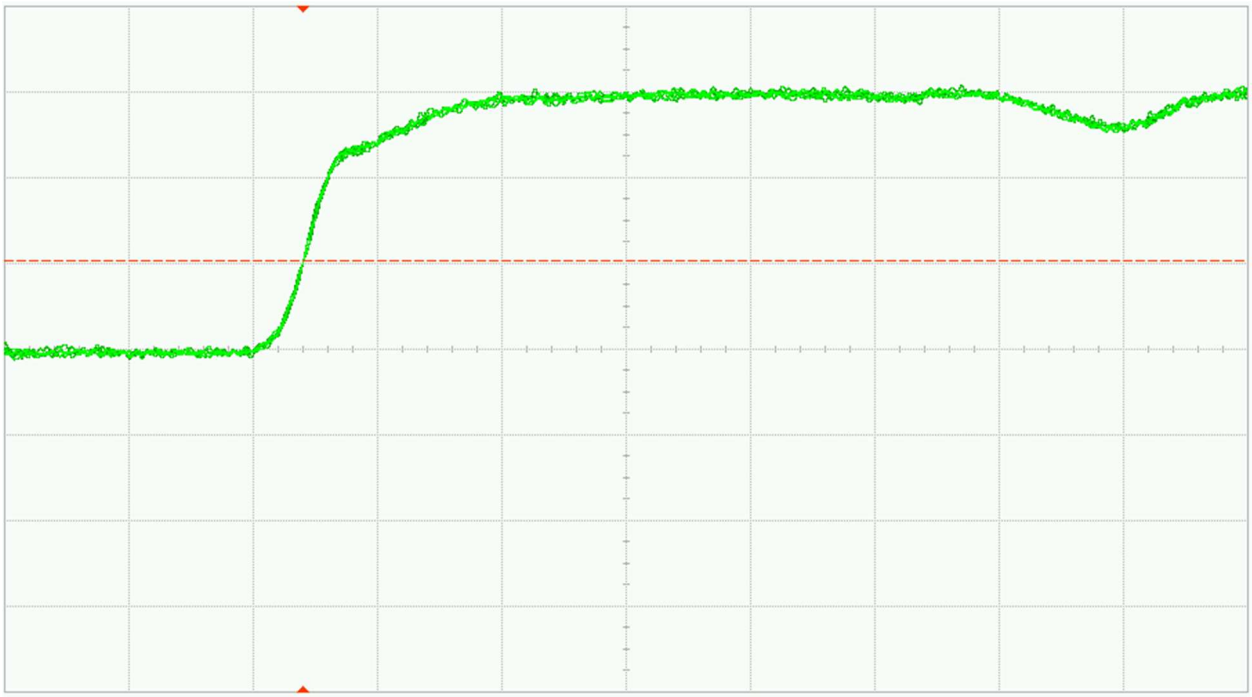

Fig. 28 (b). DUT 15745 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

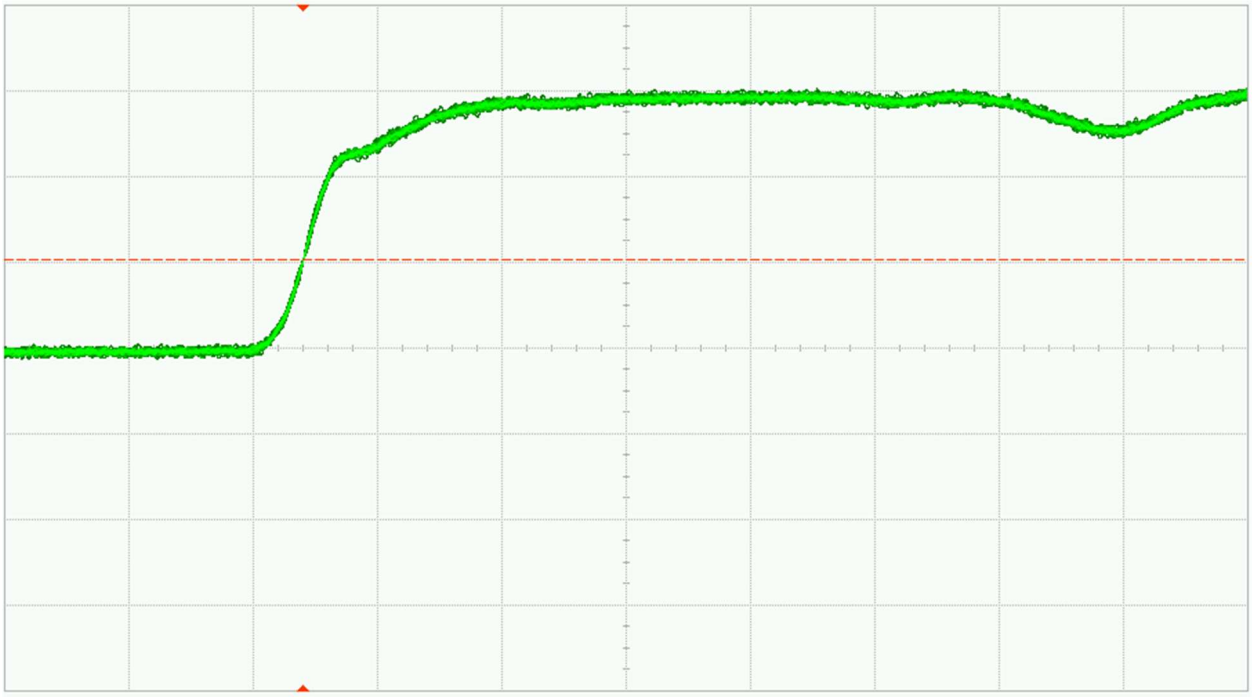

Fig. 29 (a). DUT 15749 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

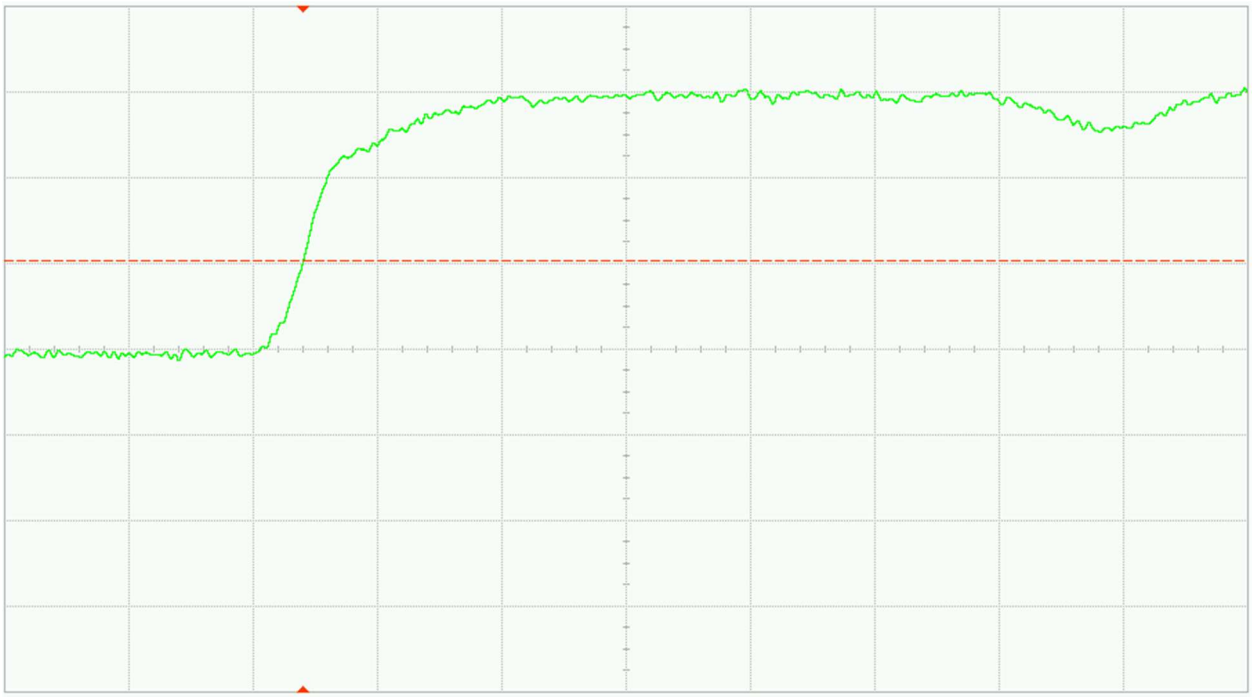

Fig. 29 (b). DUT 15749 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

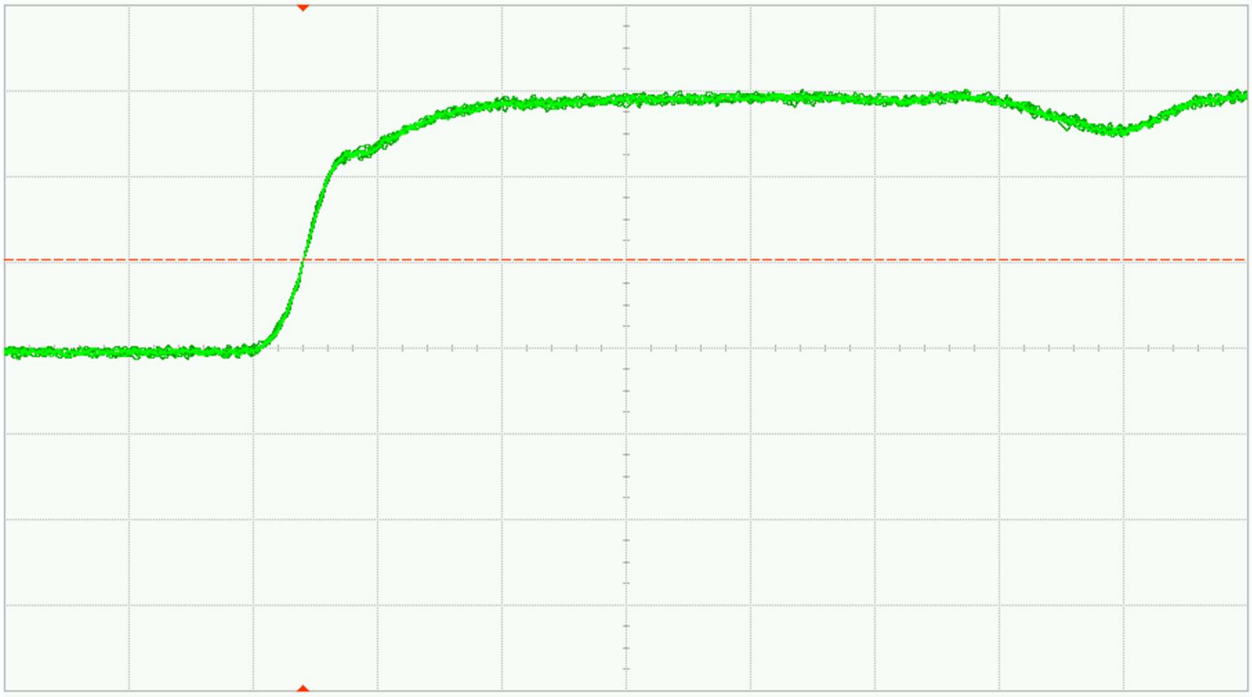

Fig. 30 (a). DUT 15750 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

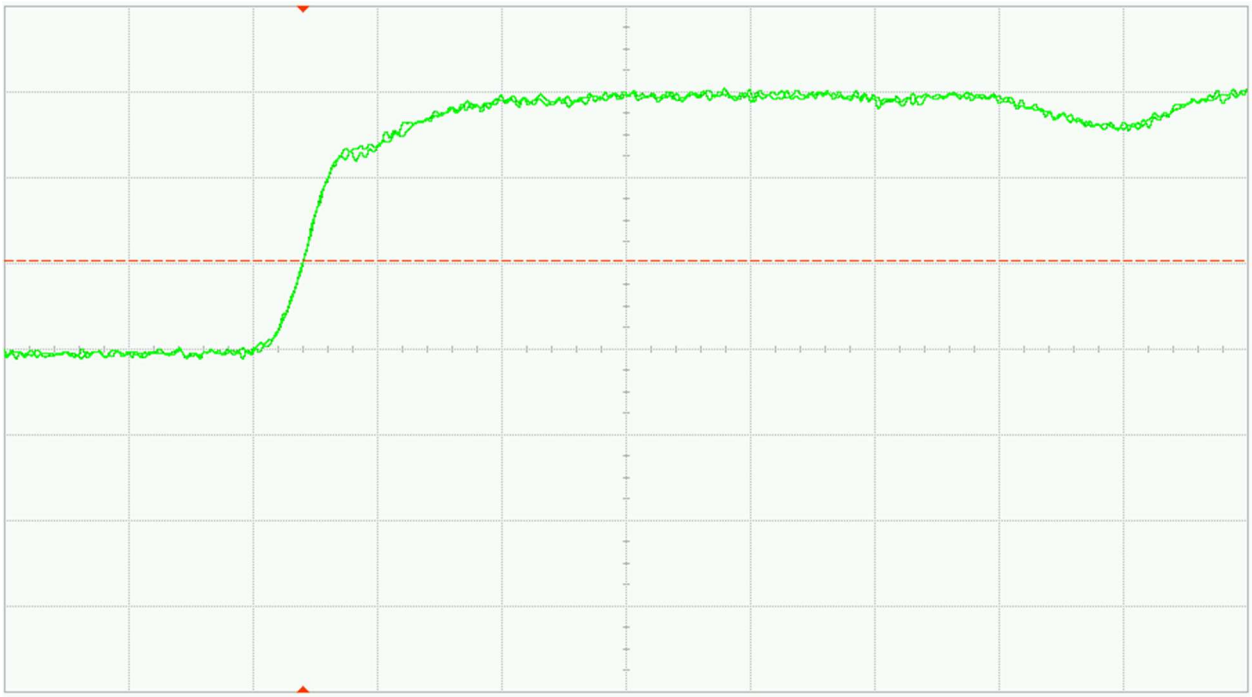

Fig. 30 (b). DUT 15750 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

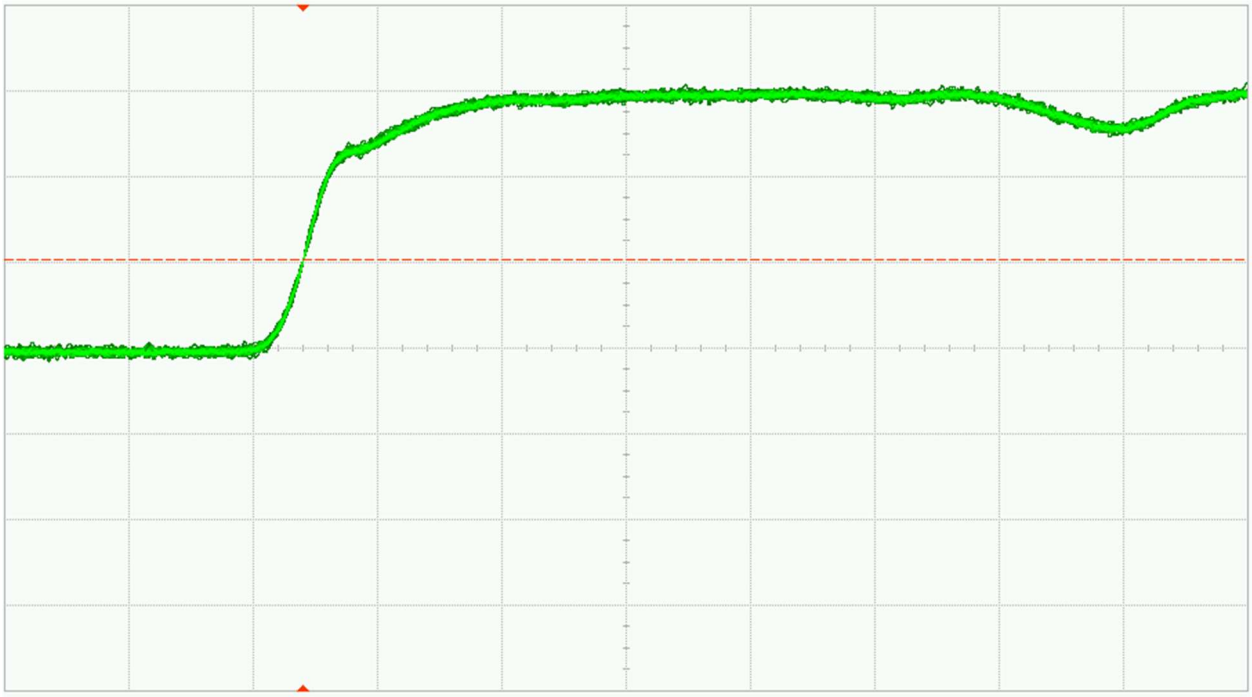

Fig. 31 (a). DUT 15802 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Fig. 31 (b). DUT 15802 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

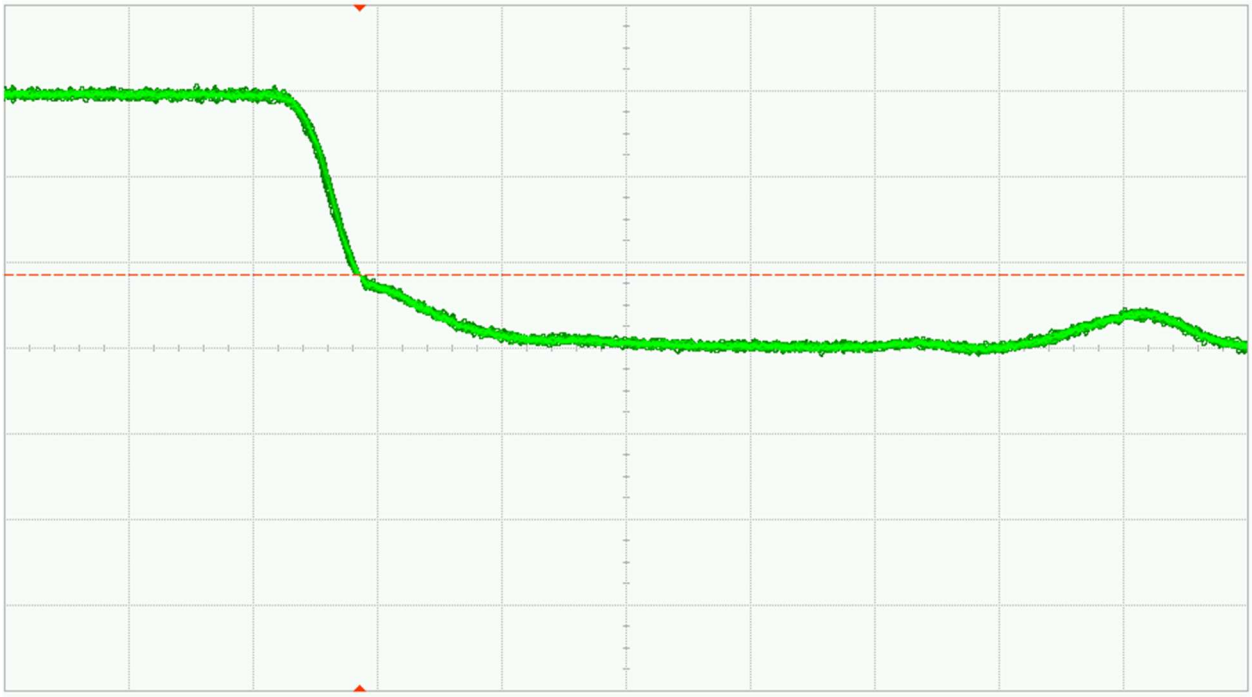

Fig. 32 (a). DUT 15736 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

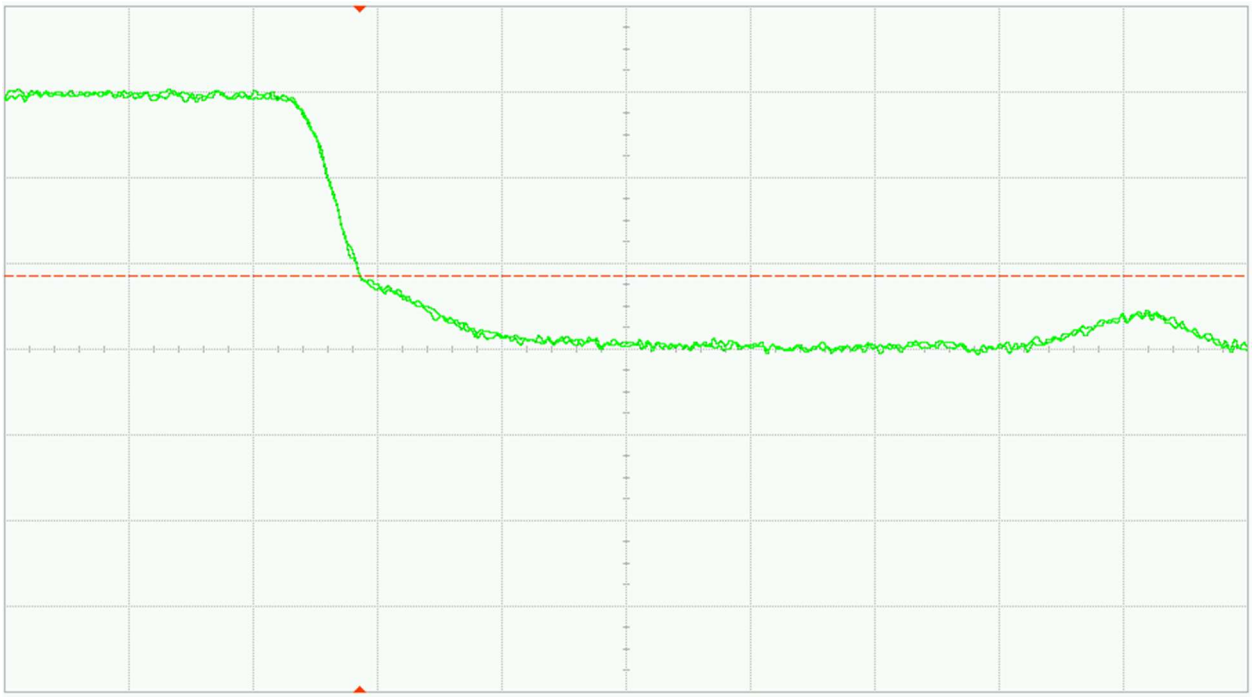

Fig. 32 (b). DUT 15736 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

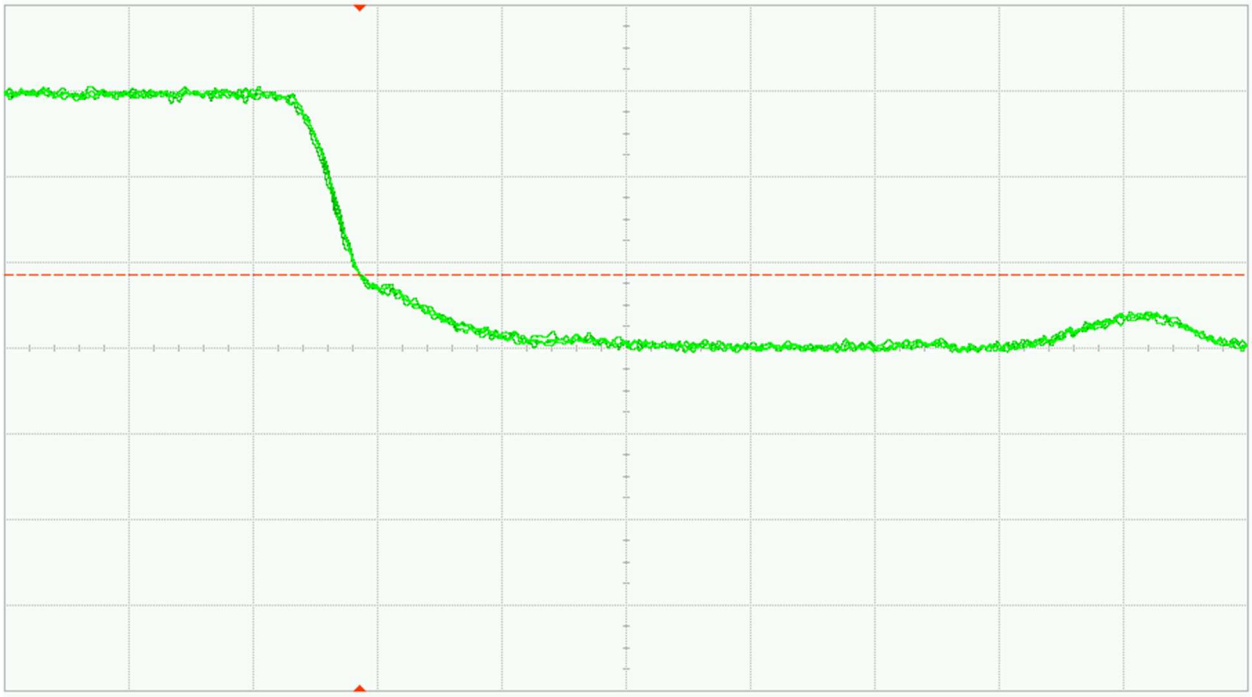

Fig. 33 (a). DUT 15737 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

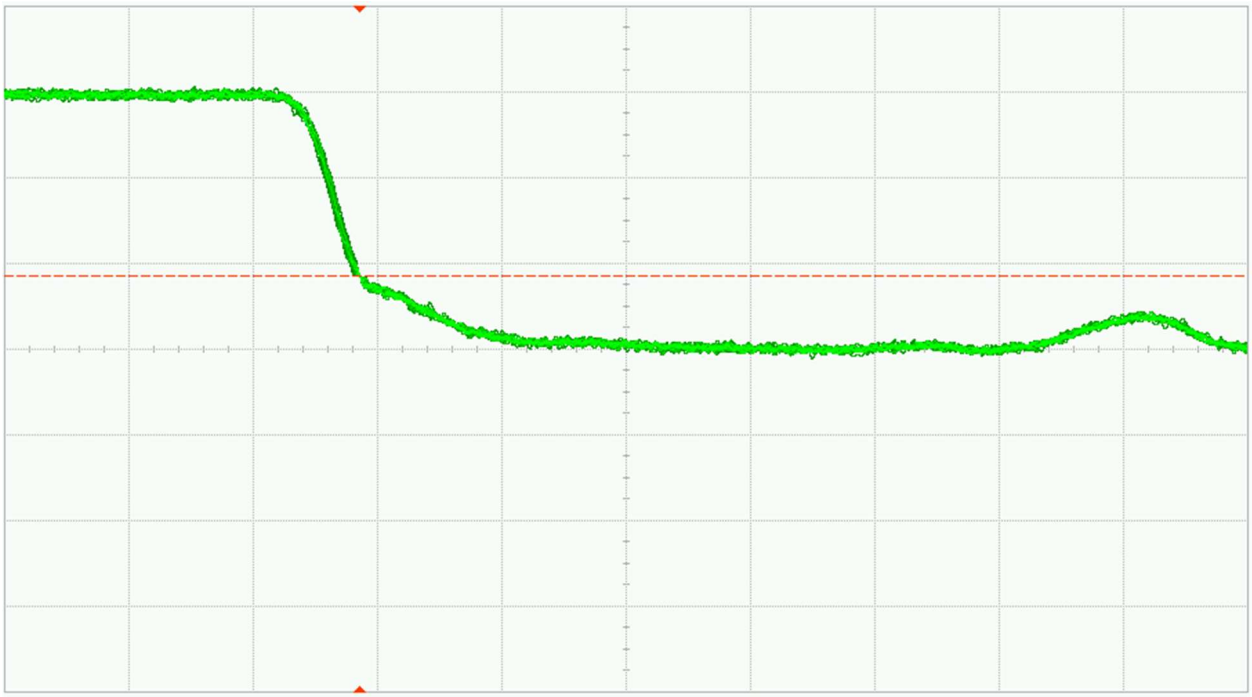

Fig. 33 (b). DUT 15737 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

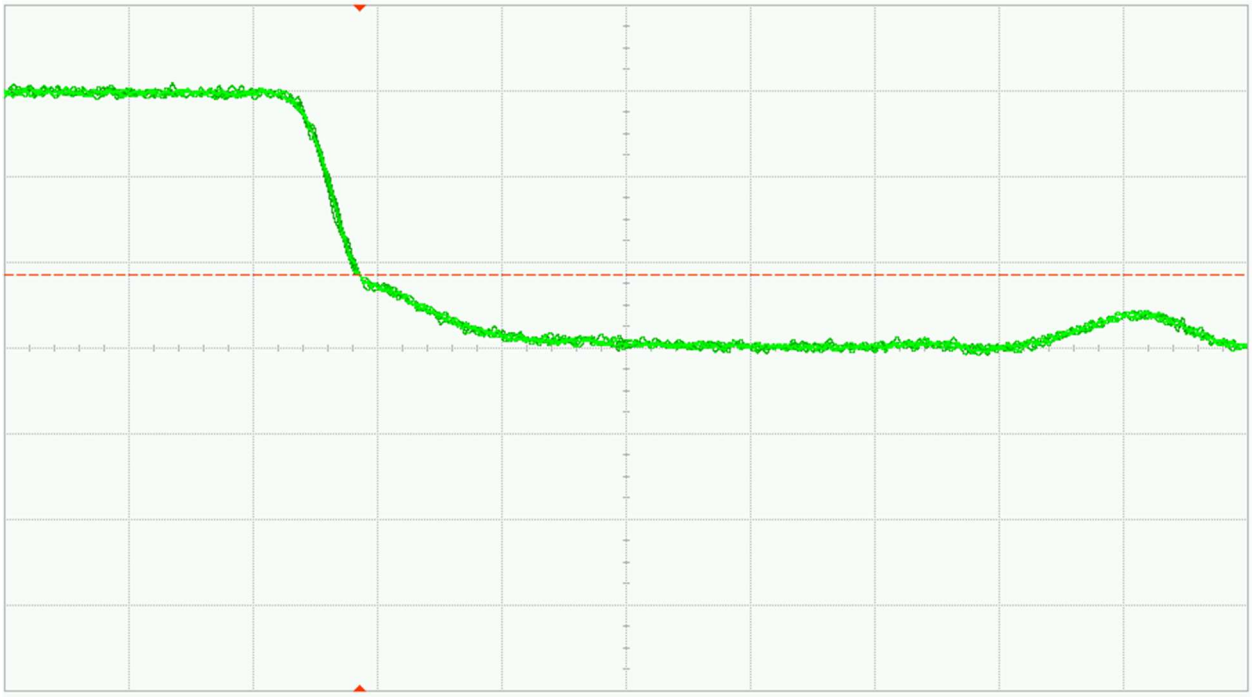

Fig. 34 (a). DUT 15745 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

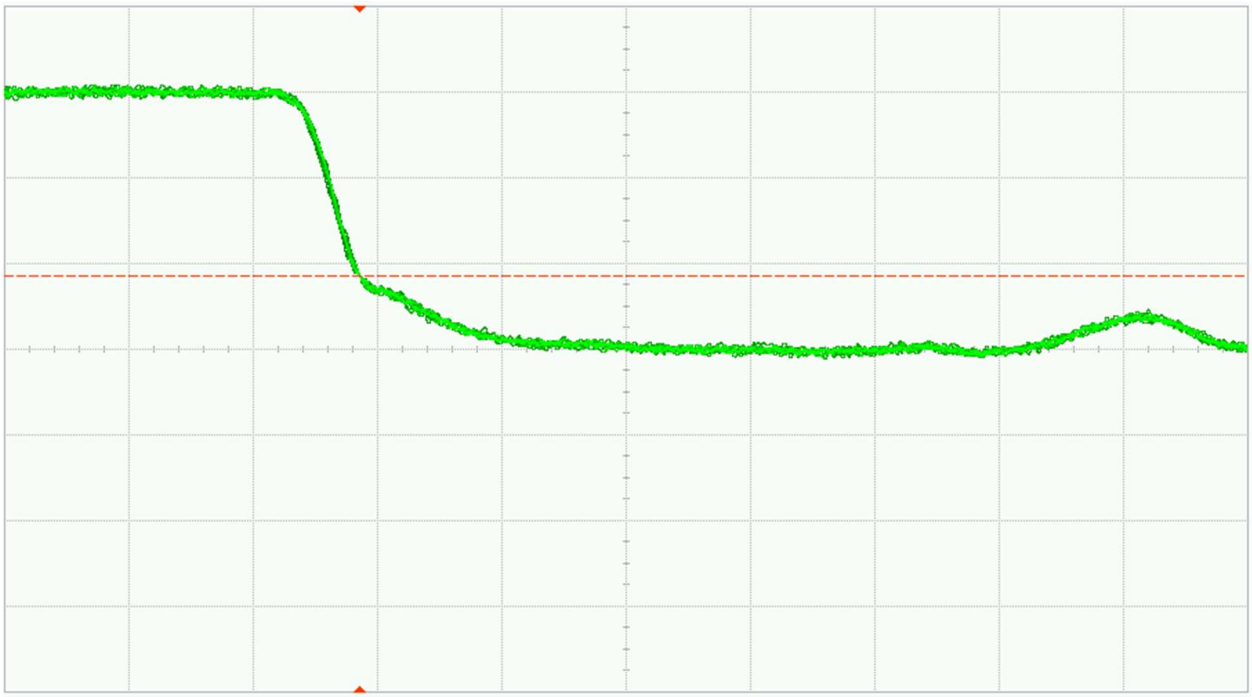

Fig. 34 (b). DUT 15745 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

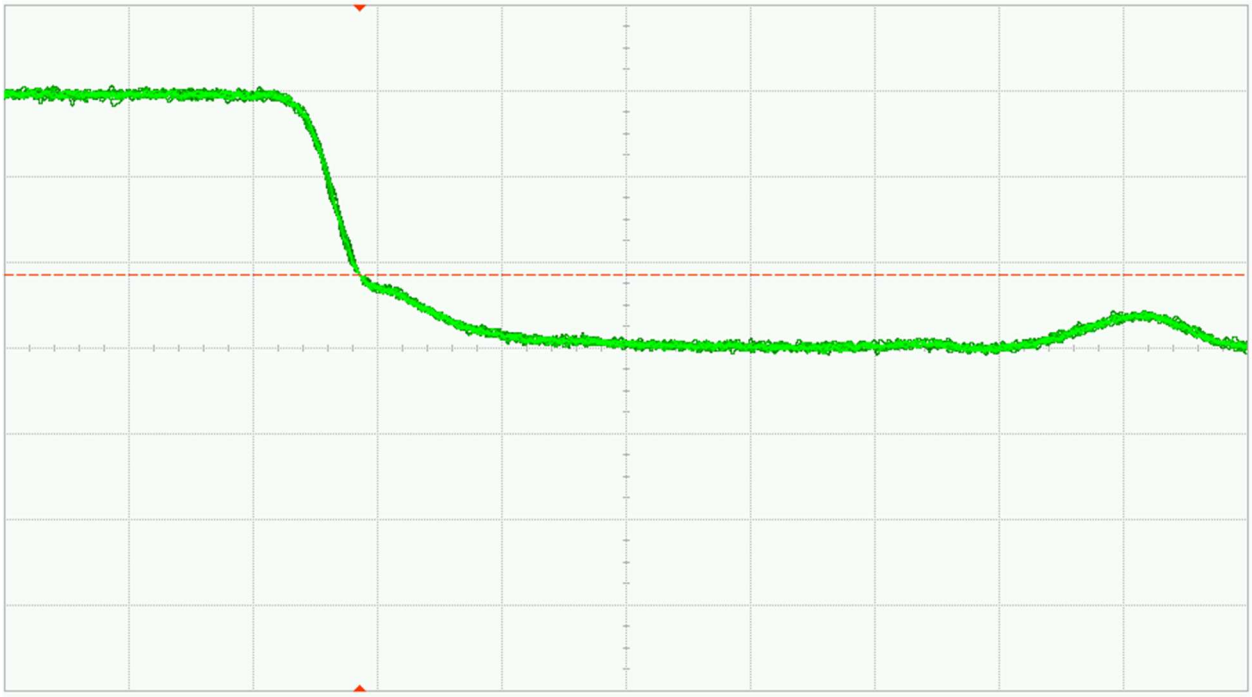

Fig. 35 (a). DUT 15749 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

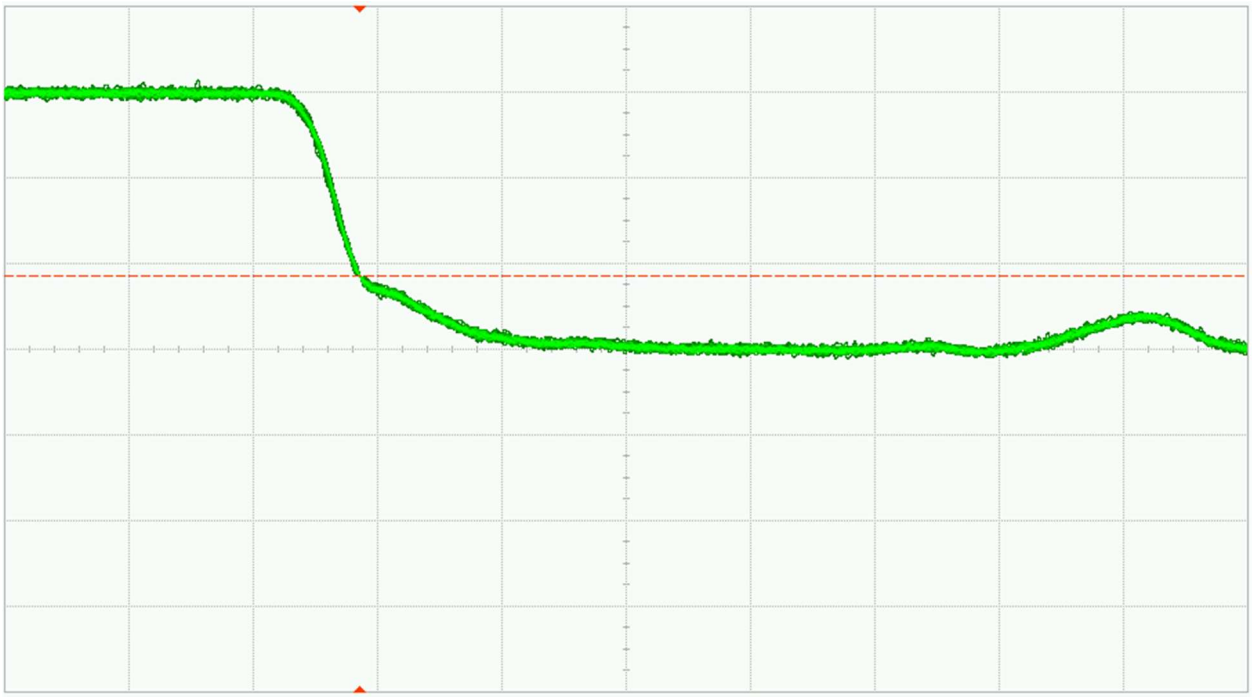

Fig. 35 (b). DUT 15749 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Fig. 36 (a). DUT 15750 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

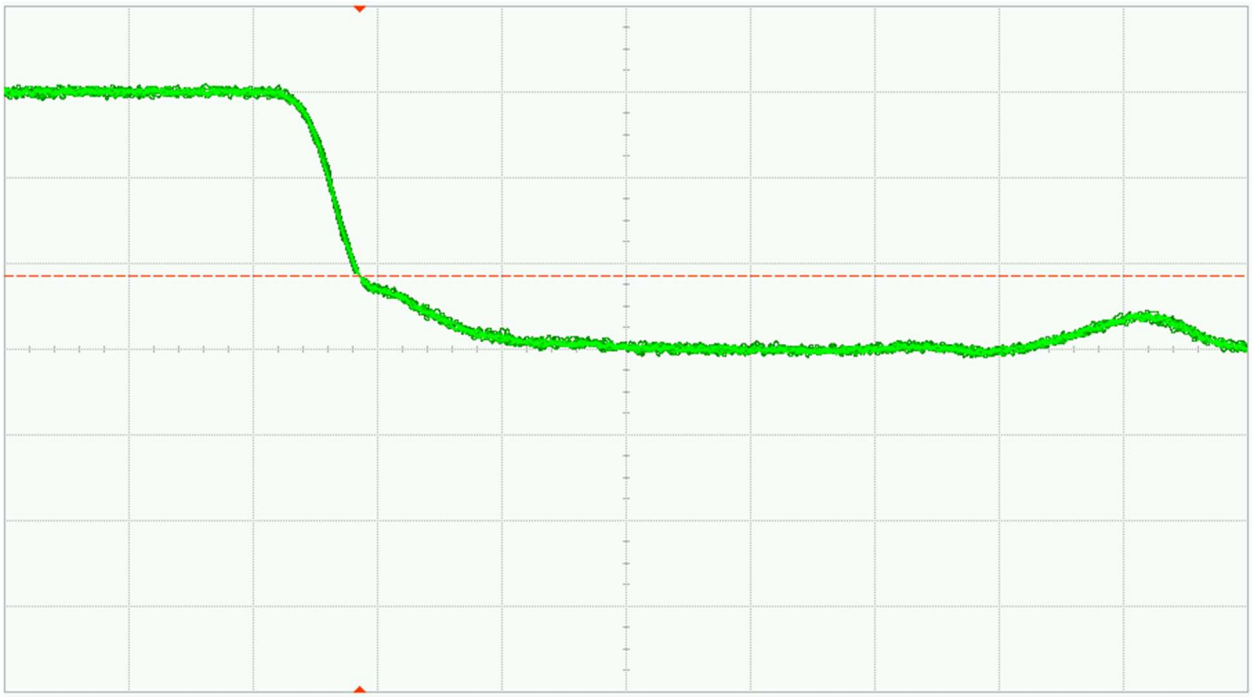

Fig. 36 (b). DUT 15750 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

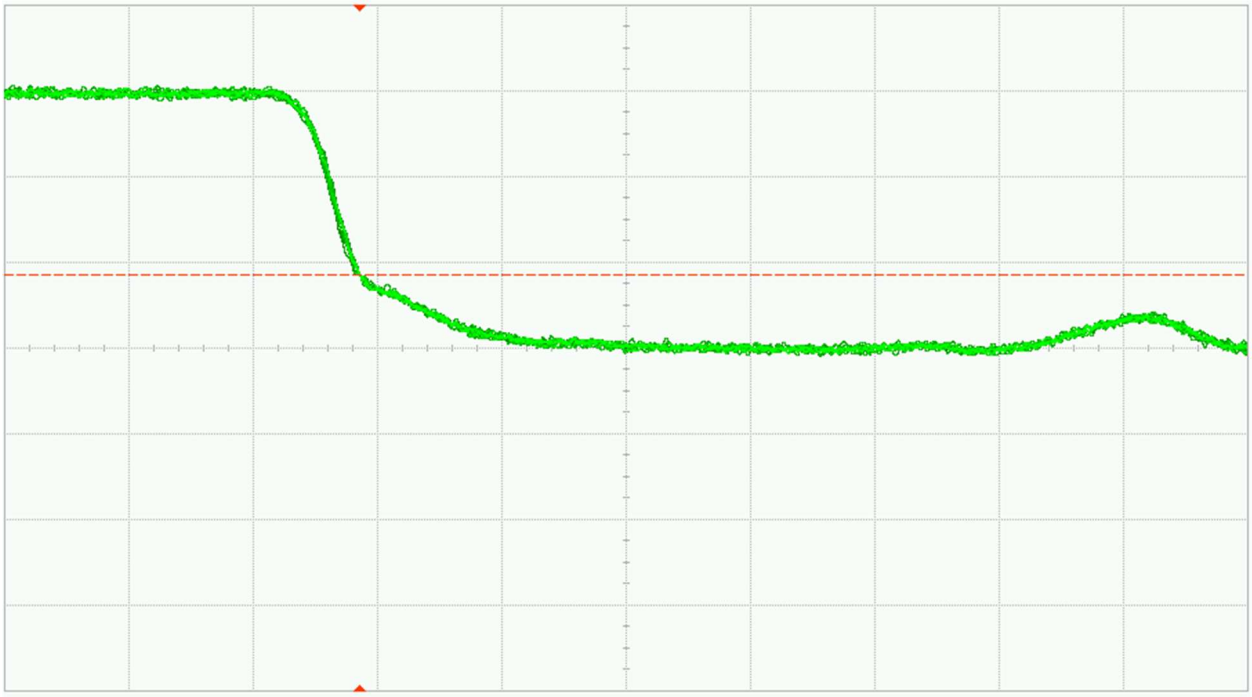

Fig. 37 (a). DUT 15802 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

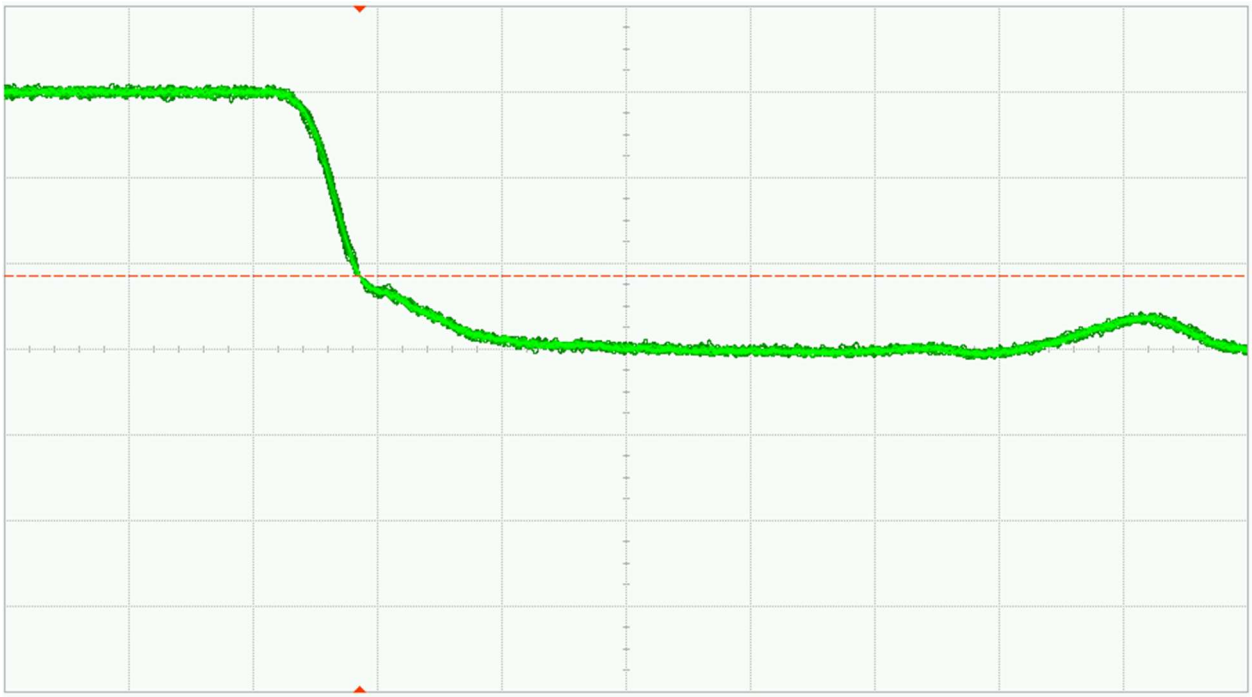

Fig. 37 (b). DUT 15802 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Appendix A

Table. 35. High level block diagrams of blocks used to perform fabric functional coverage pre and post-irradiation

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 µRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
IO Block	IO utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

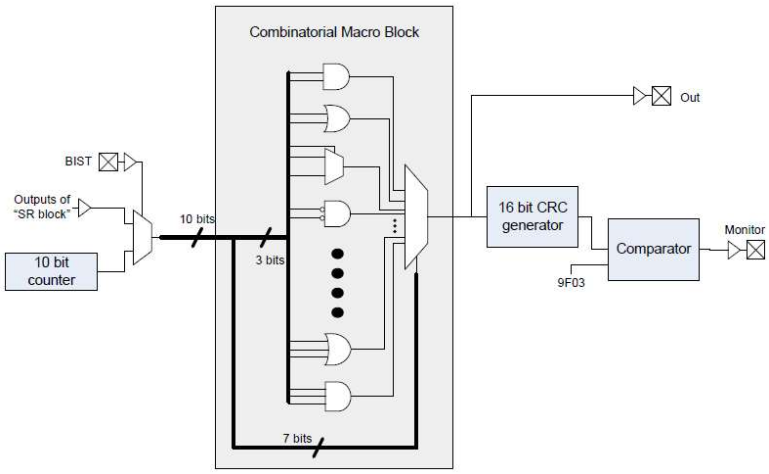

Fig. 38. Combo Block

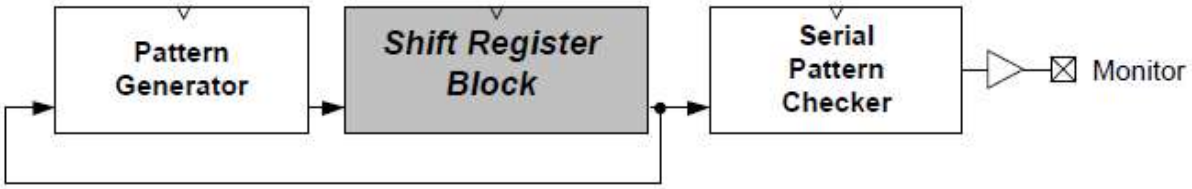

Fig. 39. Shift Register Block

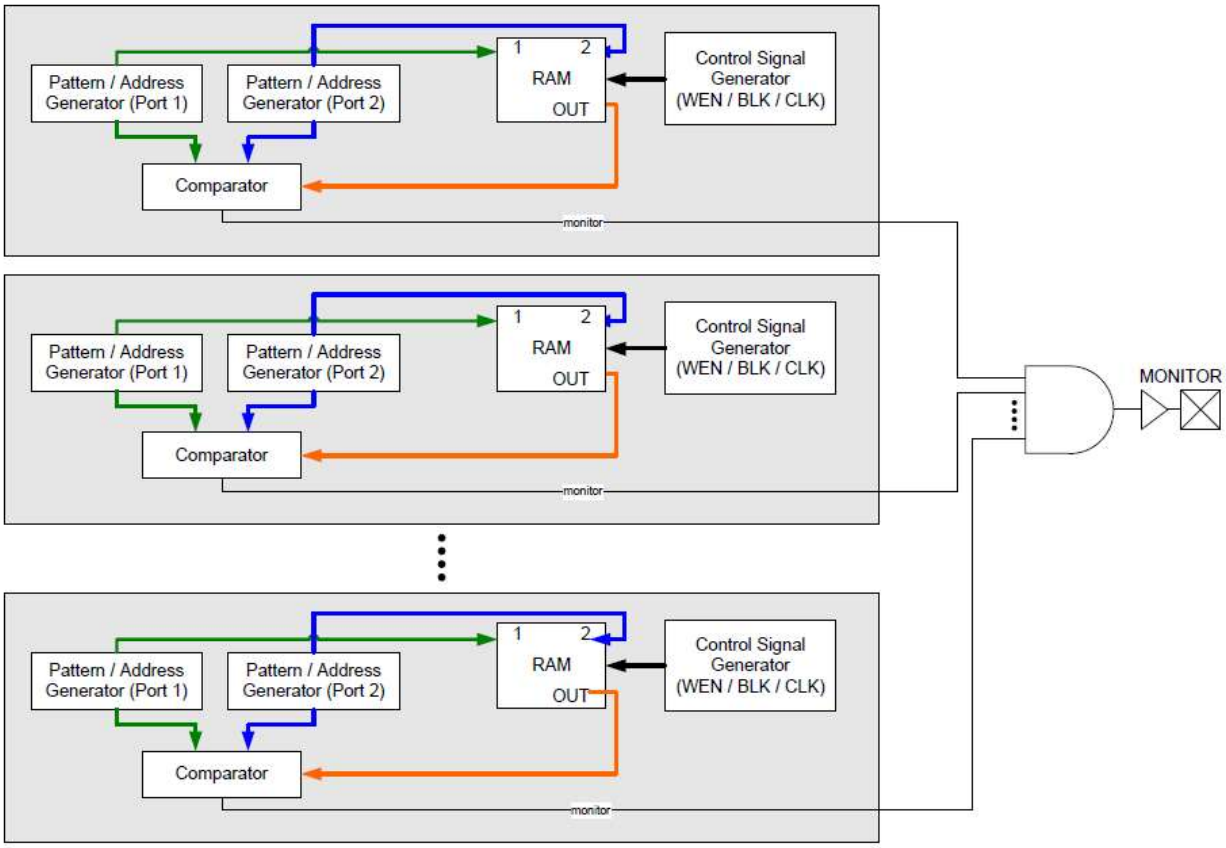

Fig. 40. Embedded Ram Blocks

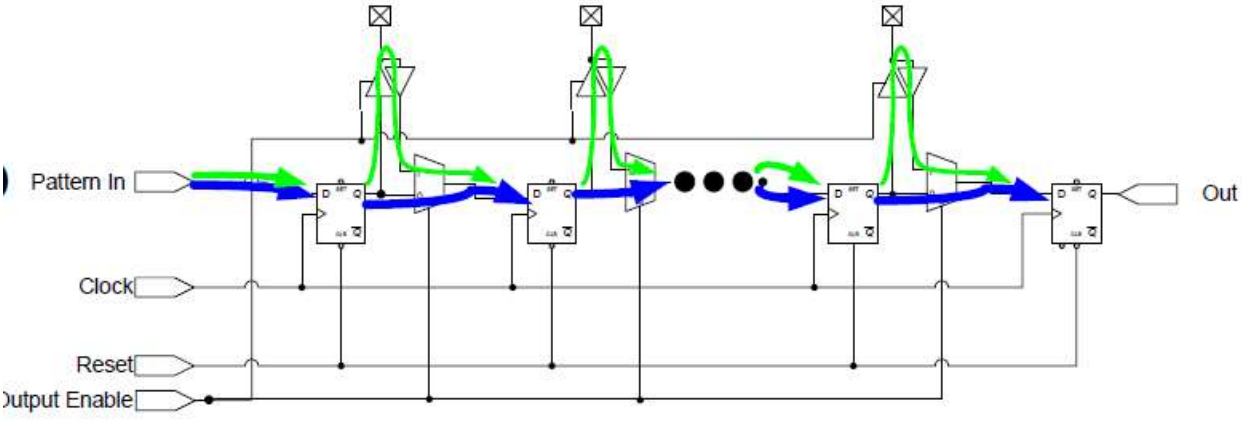

Fig. 41. IO Block

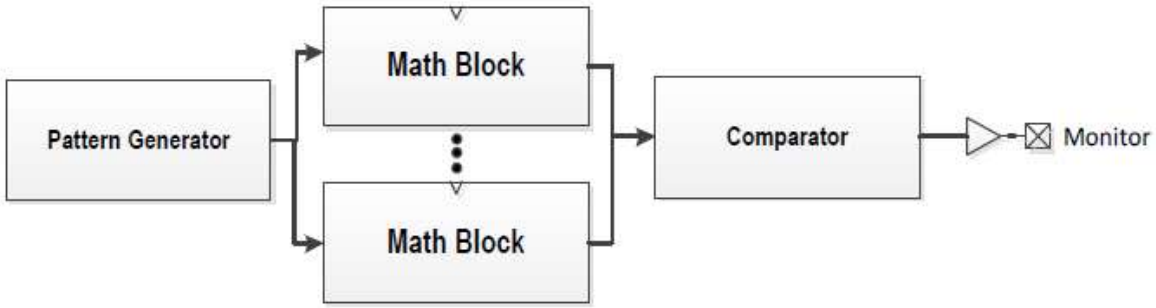

Fig. 42. Math Block

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