RT PolarFire FPGA Packaging and Pin Descriptions

Introduction (Ask a Question)

This guide provides pin and packaging information (such as, bank assignments and mechanical information) for RT PolarFire® Field Programmable Gate Arrays (FPGAs).

RT PolarFire FPGAs feature a flexible I/O structure that supports a range of mixed voltages through bank selection. The High Speed Input/Output (HSIO) and General-Purpose Input/Output (GPIO) are configured as differential I/Os or two single-ended I/Os. For more information about HSIO, GPIO, and supported I/O standards, see RT PolarFire FPGA User I/O User Guide.

Important: Some of the protocol standard uses the terminology Master and Slave. The equivalent Microchip terminology used in this document is **Initiator** and **Target**, respectively.

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1. Packaging Overview (Ask a Question)

RT PolarFire FPGAs are available in three variations of a hermetically sealed ceramic land grid array with 1509 contacts. For flight and engineering development applications, FPGAs are available with gold-plated land pads (LG1509) or with solder columns (CG1509). For engineering development applications only, FPGAs are available with solder balls (CB1509). Each package (device variant) has various I/O banks to allow the flexibility of using different I/O standards. This document refers to the CG1509 package designator. The information presented is also applicable to the LG1509 (ceramic land grid array with no solder termination) and the CB1509 (ceramic ball grid array with solder ball termination, for prototyping purposes).

The following table lists the RT PolarFire FPGA variant, with user I/O and XCVR lanes.

Table 1-1. RT PolarFire FPGA Product Family

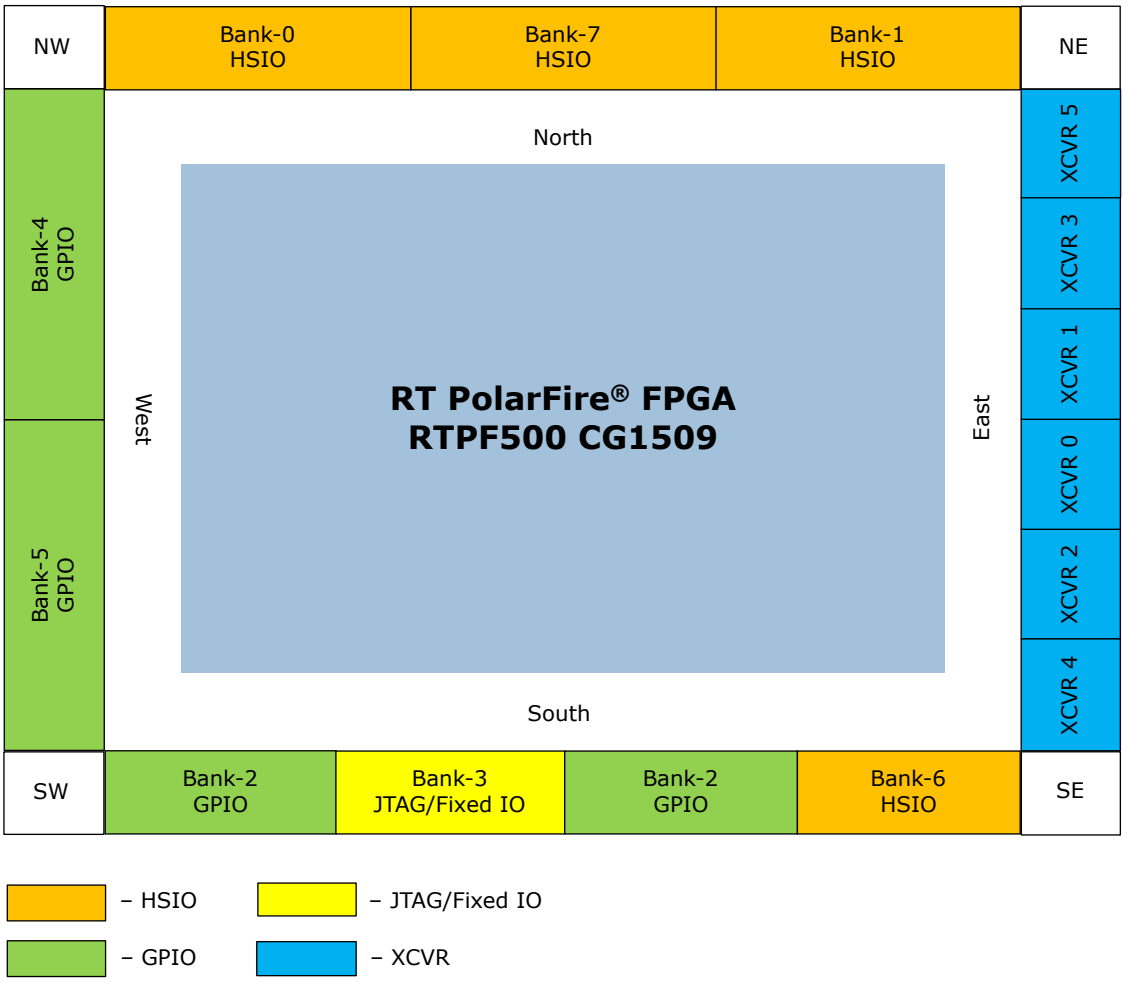
Features		RTPF500T
FPGA Fabric	Logic Elements (4 LUT + DFF)	481
	Math Blocks (18 × 18 MACC)	1480
	LSRAM Blocks (20 kbit)	1520
	µSRAM Blocks (64 × 12)	4440
	Total RAM (Mbits)	33
	µPROM (Kbits 9-bit bus)	513
	User DLLs/PLLs	8
High-Speed I/O	250 Mbps to 12.7 Gbps Transceiver Lanes	24
	PCIe® Gen2 End Points/Root Ports	2
Total I/Os	Total User I/Os	632
Packaging	Type/Size/Pitch	—
	CG1509 (40 mm × 40 mm, 1.0 mm)	—

2. Bank Locations (Ask a Question)

RT PolarFire FPGA I/Os are grouped based on I/O voltage standards and I/O capabilities. Each I/O bank has dedicated I/O supplies and ground voltages. Because of these dedicated supplies, only I/O with compatible standards are assigned to the same I/O voltage bank.

The following illustration shows the bank locations for the RTPF500T device with available package combinations.

Figure 2-1. RT PolarFire® RTPF500T-CG1509 I/O Bank Locations



The following table lists the organization of the I/O banks in RT PolarFire FPGAs. Each XCVR supports four lanes in every package. In all the packages, PCIe® is supported only in XCVR0.

Table 2-1. Organization of I/O Banks

Bank Number	CG1509
	RTPF500T
Bank 0	HSIO
Bank 1	HSIO
Bank 2	GPIO
Bank 3	JTAG/FIXED I/O
Bank 4	GPIO

.....continued	
Bank Number	**CG1509**
	RTPF500T
Bank 5	GPIO
Bank 6	HSIO
Bank 7	HSIO
XCVR 0	Included
XCVR 1	Included
XCVR 2	Included
XCVR 3	Included
XCVR 4	Included
XCVR 5	Included

Each I/O bank supports multiple DDR lanes. If CDR/SGMII interface is connected to the I/O bank, the Tx and Rx signal must be within the same DDR Lane. Only one CDR/SGMII is allowed per DDR lane.

For more information about DDR lanes for each package in Package Pin Assignment Table (PPAT), see RT PolarFire FPGA Product Overview.

The following table lists the XCVR channels for RT PolarFire device/package.

Table 2-2. Serial Transceiver Channels

Device	CG1509
RTPF500T	24

3. Packaging Pin Assignment (Ask a Question)

The PPAT information is available in the Packing section. For more information, see RT PolarFire FPGAs Documentation web page. PPAT contains information about recommended DDR pin-outs, PCI Express capability for XCVR-0, DDR Lane information for I/O CDR, and generic IOD interface pin placement.

4. Pin Descriptions (Ask a Question)

RT PolarFire device has user I/O (GPIO/HSIO) pins, dedicated I/O bank pins, memory interface, XCVR interface, clocking pins, and supply pins.

4.1 User I/O (Ask a Question)

RT PolarFire FPGA I/Os are paired up to meet the differential I/O standards and grouped into lanes of 12 buffers with a lane controller for memory interfaces. For more information about the memory controller, see PolarFire Family Memory Controller User Guide.

Two types of I/O buffers are available—HSIO and GPIO. HSIO is optimized for 1.2 Gbps (DDR4) operation with operating supplies between 1.1V and 1.8V. GPIO buffers support a wider range of I/O interfaces with speeds of up to 1066 Mbps when using single-ended standards and 1.25 Gbps when using differential standards. GPIO supports multiple standards with an integrated Clock Data Recovery (CDR) to high-speed serial interfaces such as 1 GbE.

Each RT PolarFire FPGA user I/O uses an IOxyBz naming convention, where:

- IO = the type of I/O.
- x = the I/O pair number in bank z
- y = P (positive) or N (negative). In single-ended mode, the I/O pair operates as two separate I/O—P and N. Differential mode is implemented with a fixed I/O pair and cannot be split with an adjacent I/O
- B = bank (refer note in 4.1.1. Supported I/O Features)
- z = bank number

GPIOxyBz and HSIOxyBz are bi-directional user I/O pins that are capable of differential signaling.

4.1.1 Supported I/O Features (Ask a Question)

The following table lists the I/O features supported on HSIO and GPIO.

Table 4-1. Supported I/O Features

I/O Feature	HSIO	GPIO	Additional Information
Programmable ON/OFF clamp	—	Yes	—
Hot-plug	—	Yes	—
Cold sparing	Yes	Yes	—
True differential output driver	—	Yes	—
Programmable ON/OFF 100Ω differential termination	—	Yes	—
PVT-compensated output drive	Yes	Yes	—
Programmable slew control	—	Yes	—
PVT compensated slew control	Yes	—	—
Programmable input hysteresis	Yes	Yes	—
Mobile industry processor interface (MIPI) (input)	—	Yes	High-speed and low-power
MIPI (output)	—	Yes	High-speed

Important: HSIO is pseudo-cold spare, that is, it requires the spare device to have its HSIO VDDI banks powered up to prevent I/O leakage through the ESD diodes.

4.2 Supply Pins (Ask a Question)

The following table lists multiple power supply pins required for proper device operation. For more information about unused conditions and power sequence, see RT PolarFire FPGA Board Design User Guide.

Table 4-2. Supply Pins

Name	Description	Operating Voltage
XCVR_VREF	Voltage reference for transceiver	0.9V/1.25V
VDD_XCVR_CLK	Provides common power to all transceiver reference clock buffers	2.5V/3.3V
VDDA25	Transceiver PLL power	2.5V
VDDA	Power for transceiver Tx and Rx lanes 0, 1, 2, 3	1.0V/1.05V
VSS	Core digital ground	—
VDD	Device core digital supply	1.0V/1.05V
VDDIx (JTAG Bank)	Supply for I/O circuits in a bank	1.8V/2.5V/3.3V
VDDIx (GPIO Banks)	Supply for I/O circuits in a bank	1.2V/1.5V/1.8V/2.5V/3.3V
VDDIx (HSIO Banks)	Supply for I/O circuits in a bank	1.2V/1.5V/1.8V
VDD25	Power for corner PLLs and PNVM	2.5V
VDD18	Power for programming and HSIO receiver. HSIO auxiliary power supply	1.8V
VDDAUXx	Auxiliary supply for I/O circuits. Auxiliary supply voltage must be set to 2.5V or 3.3V and must be always equal to or higher than VDDIx of GPIO banks	Greater than or equal to VDDI

Important: SSTL25 (stub series terminated logic) I/O standard for 1.25V V_{REF}, SSTL18 I/O standard for 0.9V, and HSUL18 I/O standard for 0.9V.

Important: Designers should be familiar with the latest Single Event Latch-Up radiation test data before choosing GPIO supply voltages.

4.2.1 Packaging Decoupling Capacitors (Ask a Question)

RT PolarFire 1.0 mm pitch package contains decoupling capacitors to support high-speed I/O operation.

The following table lists the packaging decoupling capacitors contained in the LG1509/CB1509/CG1509 packages.

Table 4-3. Packaging Decoupling Capacitors

Power Supply	1 mm Pitch	
	Caps available	Value
VDDI0	3	0.18 µF (x3)
VDDI1	2	0.18 µF (x2)
VDDI2	3	0.18 µF (x3)
VDDI4	4	0.18 µF (x4)
VDDI5	4	0.18 µF (x4)
VDDI6	3	0.18 µF (x3)
VDDI7	3	0.18 µF (x3)

.....continued		
Power Supply	1 mm Pitch	
	Caps available	Value
VDD	7	0.18 µF (x7)
VDD18	2	0.18 µF (x2)
VDDA	4	4.7 nF (x1) 2.2 nF (x2) 1.0 nF (x1)

4.3 Memory Interface (Ask a Question)

Valid locations for DDR memory interfaces are shown in PPAT, see RT PolarFire FPGA Product Overview.

By using the Libero® SoC RT PolarFire configurator, all individual DDR interface pins are identified from the macro. For more information about the memory interface, see PolarFire Family Memory Controller User Guide.

The following table lists the reference receiver modes of I/O standards.

Table 4-4. Reference Receiver Modes

I/O Standard	VDDIx	VREF	On-Die Termination (ODT) (in Ω)	Bank Type	Application
SSTL18	1.8V	0.9V	40/50/60/80/120/240	GPIO, HSIO	RLDRAM2
SSTL15	1.5V	0.75V	40/50/60/80/120/240	GPIO, HSIO	DDR3
SSTL135	1.35V	0.68V	20/30/40/60/120	HSIO	DDR3L
HSTL15	1.5V	0.75V	40/50/60/80/120/240	GPIO, HSIO	QDRII+
HSTL135	1.35V	0.68V	20/30/40/60/120	HSIO	RLDRAM3
HSUL12	1.2V	0.6V	60/120/40	HSIO	LPDDR3
HSTL12	1.2V	0.6V	60/120/240	HSIO	QDRII+
POD12	1.2V	0.6V	20/30/40/60/120	HSIO	DDR4

4.4 DDR Interface (Ask a Question)

The DDR subsystems are hardened ASIC blocks for interfacing the LPDDR3, DDR3, and DDR4 memories. It supports 16-, 32-, and 64-bit data bus width modes with ECC support. The DDRIO uses fixed impedance calibration for different drive strengths. These values are programmed using Libero SoC RT PolarFire software for the selected I/O standard. The values are fed to the pull-up or pull-down reference network to match the impedance with an external resistor. For more information about DDR signals, see PolarFire Family Memory Controller User Guide.

4.5 Clocking Pins (Ask a Question)

Clock Conditioning Circuit (CCC) blocks, located at each corner of the RT PolarFire FPGAs, contain two PLLs and two DLLs that provide flexible on-chip and off-chip clock management and synthesis capabilities. CCCs are labeled according to their locations in the core. For example, the CCC located in the northeast corner is labeled as CCC_NE. For more information about clocking pins, see PolarFire Family Clocking Resources User Guide. Preferred clock inputs (CLKIN) are located on three sides of the device, with eight preferred clock inputs on the west side, twelve on the north side, and either 12 or 16 inputs on the south side, depending on the package. The following table lists the clocking pin names and descriptions. For more information about CCC pin voltage, see Table 4-2.

Table 4-5. Clocking Pins

Name	Description	When Unused
CCC_NW_PLL0_OUT[0:1]	Dedicated PLL output clock pins used to drive high-performance clocks in DDR3 and DDR4 applications located in the corners of RT PolarFire device to route the clocks to and from the PLLs and DLLs.	Do not connect (DNC)
CCC_NW_PLL1_OUT[0:1]		
CCC_NE_PLL0_OUT[0:1]		
CCC_NE_PLL1_OUT[0:1]		
CCC_SE_PLL0_OUT[0:1]		
CCC_SE_PLL1_OUT[0:1]		
CCC_SW_PLL0_OUT[0:1]		
CCC_SW_PLL1_OUT[0:1]		
CCC_SE_CLKIN_S_[8:15]	Preferred clock inputs that connect external clock signals to the CCCs and the global clock network through low-latency paths. It is recommended to use these preferred clock inputs for connecting external clocks to the clock inputs of PLLs, DLLs, and fabric logic.	DNC
CCC_SW_CLKIN_S_[0:3]		
CCC_SW_CLKIN_W_[0:3]		
CCC_NW_CLKIN_W_[4:7]		
CCC_NW_CLKIN_N_[0:3]		
CCC_NE_CLKIN_N_[8:11]		
CLKIN_S_[4:7]	Preferred clock inputs directly routed to internal global buffers through MUXes.	DNC
CLKIN_N_[4:7]		

Important: Some of the preferred clock inputs have connections to feedback clock input of the PLL/DLL present in the CCC. It is required to choose a preferred clock input which has connection to the PLL reference clock input for clock frequency synthesis. For preferred clock inputs connectivity to PLLs/DLLs and global clock network, see PolarFire Family Clocking Resources User Guide.

4.6 Dedicated I/O Bank Pins (Ask a Question)

JTAG, SPI, and DEVRST_N signals share the same bank 3 supply and are not directly available to the fabric. SPI I/O are, however, dynamically switched over to be used by the fabric whenever the RT PolarFire controller is not using them. Dedicated I/O bank supplies must be powered up above their operational threshold and enabled before the RT PolarFire controller negates the main power-on reset to the FPGA fabric. The following tables list the JTAG, SPI, and DEVRST_N pin names and descriptions. Libero configures unused user I/O as input buffer disabled, output buffer tri-stated with weak pull-up. For more information about unused conditions, see RT PolarFire FPGA Board Design User Guide.

The JTAG bank voltages can be set to operate at 1.8V, 2.5V, or 3.3V. The following table lists the JTAG pins.

Table 4-6. JTAG Pins

Pin Names	Direction	Weak Pull-Up/Unused Condition	Description
TMS	Input	Yes/DNC	JTAG test mode select
TRSTB	Input	Yes	JTAG test reset. Must be held low during device operation
TDI	Input	Yes/DNC	JTAG test data in In ATPG or test mode, when using a 4-bit tdi bus, this I/O is used as tdi[0].
TCK	Input	No	JTAG test clock
TDO	Output	No/DNC	JTAG test data out

Important: If FPGA is in System Controller Suspend Mode and TRSTB is unused, either an external 1 kΩ pull-down resistor should be connected to TRSTB to override the weak internal pull-up, or TRSTB should be driven low from the external source.

Important: In unused condition, TCK must be connected to VSS through 10 kΩ resistor.

Table 4-7. Device Reset Pins

Name	Direction	Weak Pull-up	Description
DEVRST_N	Input	22 KΩ	Device reset (asserted low).

Table 4-8. SPI Interface Pins

Name	Direction	Description
SCK	Bi-directional	SPI clock
SS	Bi-directional	SPI target select
SDI	Input	SDI input for the shared SPI interface.
SDO	Output	SDO output for the shared SPI interface.
SPI_EN	Input	Pulled up or down through a resistor or driven dynamically from an external source to enable or tri-state the SPI I/O.
IO_CFG_INTF	Input	Pulled up or down through a resistor or driven dynamically from an external source to indicate whether the shared SPI interface is an initiator or a target. Dedicated to the system controller. 0: SPI target interface 1: SPI initiator interface

Table 4-9. Special Pins

Name	Direction	Description	Unused Condition
NC	—	No connect pin. This pin indicates that it is not connected within the circuitry. NC pins can be driven by any voltage or can be left floating with no effect on the operation of the device.	—
DNC	—	Do not connect pin. DNC pins must not be connected to any signals on the PCB, and they must be left unconnected.	—
LPRB_A	Output	Specifies an internal signal for probing (oscilloscope-like feature). The two live probe I/O cells function as either of the following: • Live probe • User I/O (GPIO)	Libero-defined DNC
LPRB_B	Output		Libero-defined DNC
FF_EXIT_N	Input	Reserved	—
Shield Signal	Output	Shield signal is required for each DDR data byte signal. It must be driven with maximum drive strength to improve the signal integrity.	Only when DDR controller is in use

4.7 XCVR Interface (Ask a Question)

The transceiver I/O available in the RT PolarFire device is dedicated for high-speed serial communication protocols. Libero Defined DNC pins are pulled up internally when not used in the Libero design.

Table 4-10. XCVR Interface Pins

Name	Direction	Description	Unused Condition
XCVR_xy_REFCLK_P XCVR_xy_REFCLK_N	Input	Differential serial reference clock xy - location x - transceiver number (0, 1, 2, 3) y - lane number (0, 1, 2, 3)	DNC

.....continued			
Name	**Direction**	**Description**	**Unused Condition**
XCVR_x_TXy_P XCVR_x_TXy_N	Output	Differential serial transmit pins. x - transceiver number (0, 1, 2, 3) y - lane number (0, 1, 2, 3)	Libero-defined DNC.
XCVR_x_RXy_P XCVR_x_RXy_N	Input	Differential serial receive pins. x - transceiver number (0, 1, 2, 3) y - lane number (0, 1, 2, 3)	Libero-defined DNC, see PolarFire Family Transceiver User Guide.

5. Package Pin-outs (Ask a Question)

The following table lists the packaging pin-outs of the RT PolarFire device. Detailed PPAT is available for download, and it contains revision history, device specification, power supplies, pin-outs, and BGA graphic. For more information about PPAT, see RT PolarFire FPGA Ceramic 1509-Pin Package Pin Assignment Table.

Table 5-1. Package Pin Outs

Device	Package
	CG1509
RTPF500T	Yes

5.1 Pin Compatibility Between Devices (Ask a Question)

The following table lists the pin compatible packages of RT PolarFire device.

Table 5-2. Pin Compatible Packages

Package	Devices
CG1509	RTPF500T
CB1509	
LG1509	

6. Mechanical Drawings (Ask a Question)

The following illustrations show the top, bottom, and side views and dimensions for the RT PolarFire FPGAs.

Figure 6-1. RTPF500T-CG1509 Package Top-View and Side-View

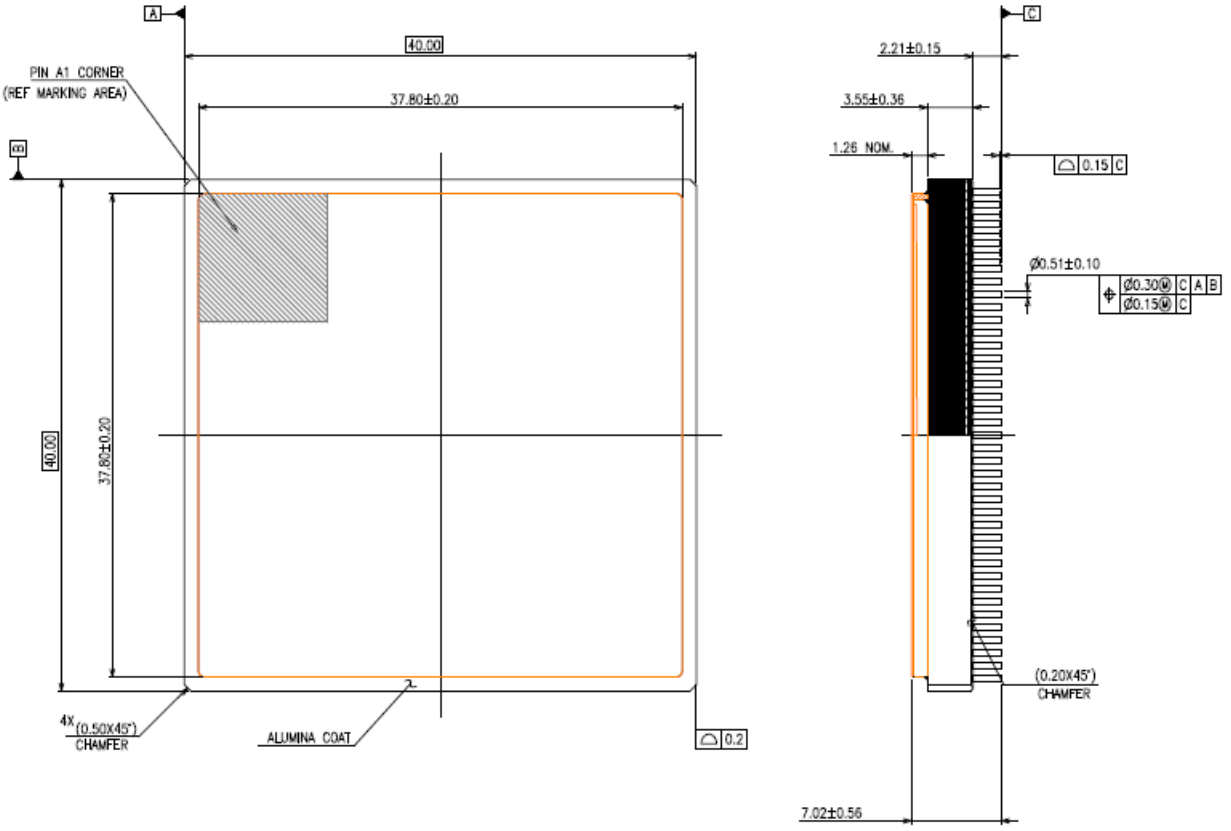


Figure 6-2. RTPF500T-CG1509 Package Bottom-View

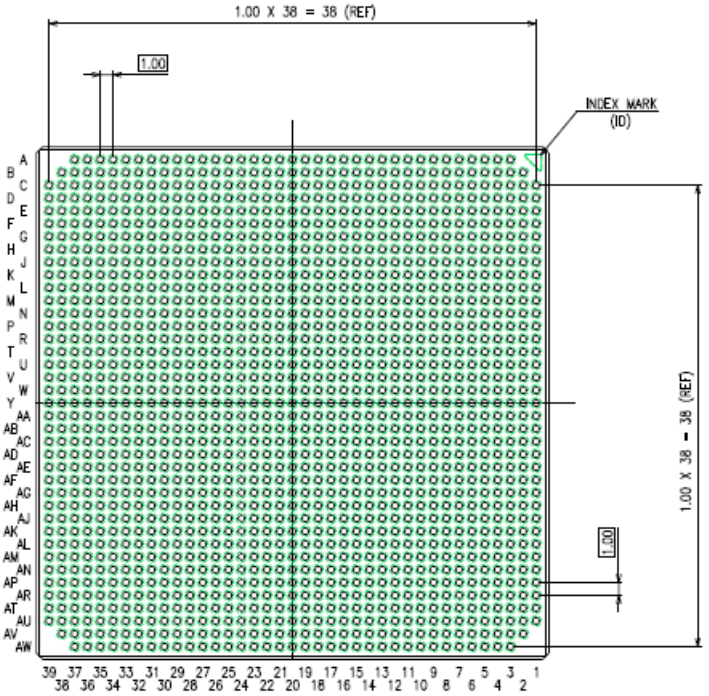


Figure 6-3. RTPF500T-CB1509 Package Top-View and Side-View

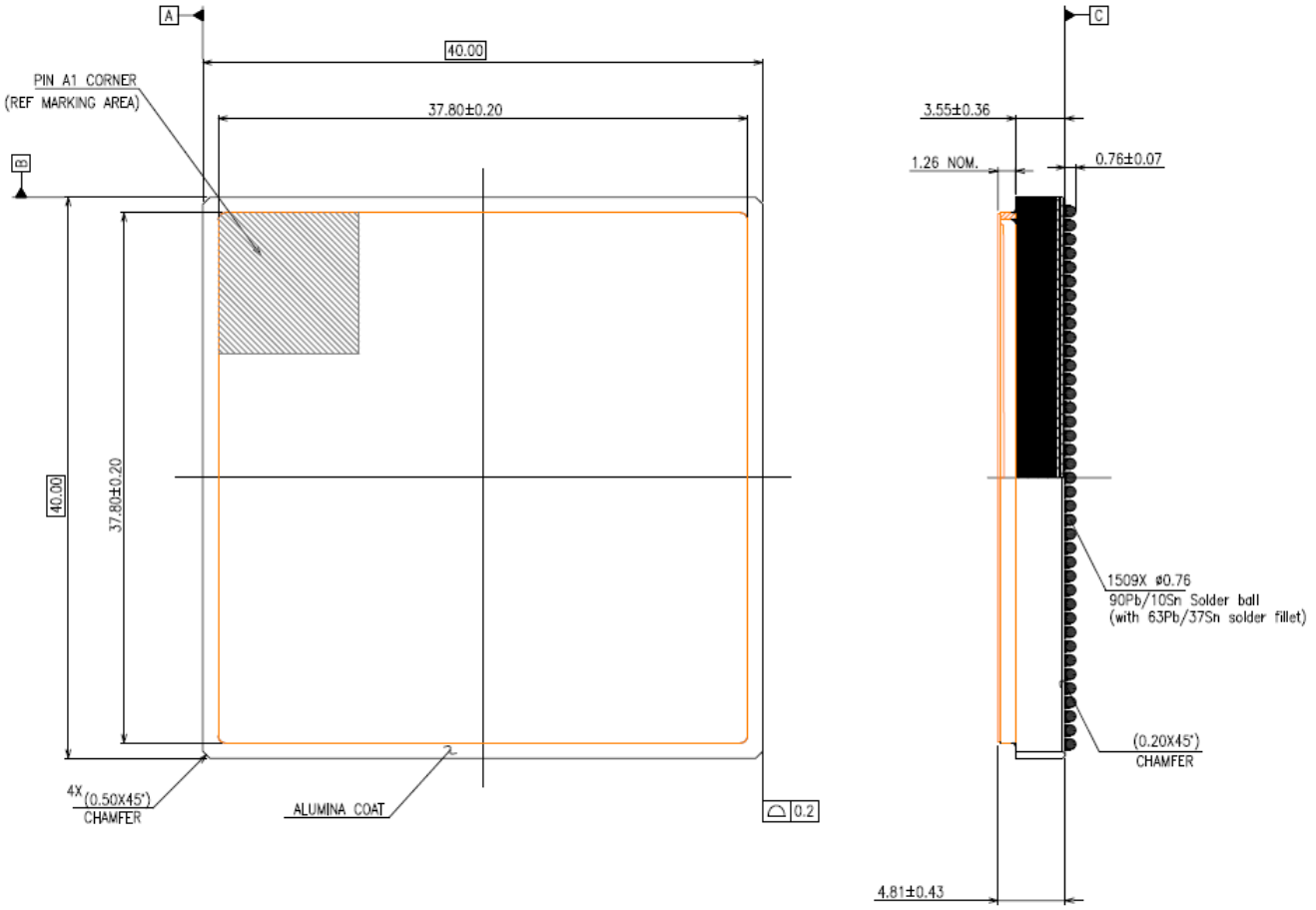
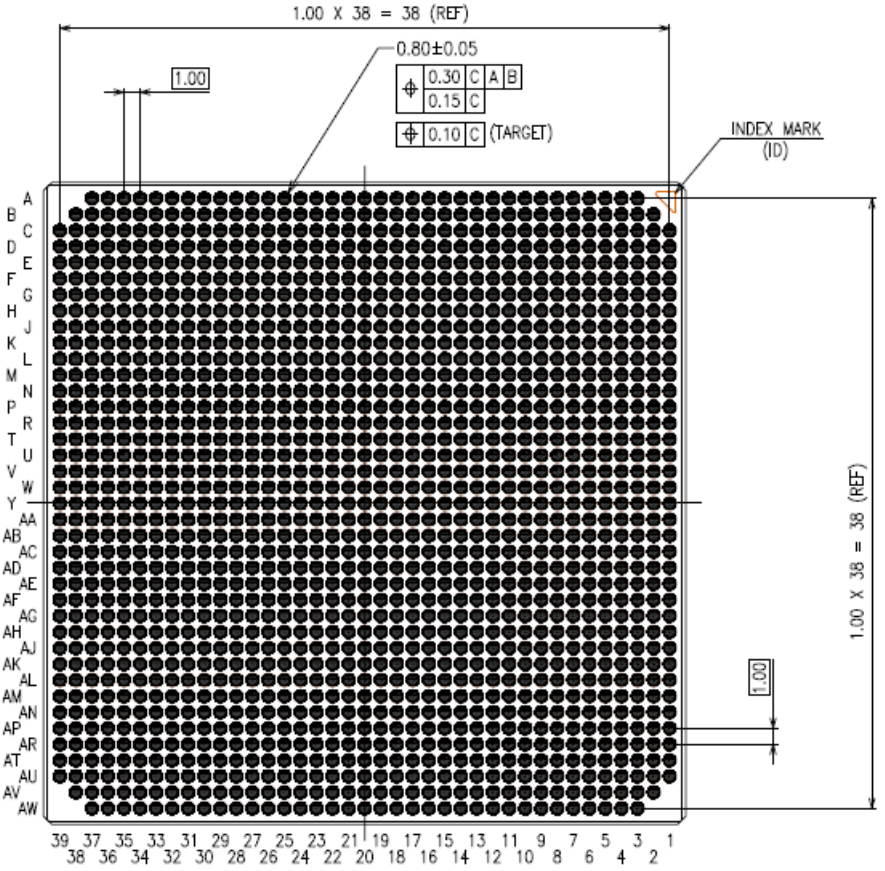


Figure 6-4. RTPF500T-CB1509 Package Bottom-View



7. Package Material Information (Ask a Question)

The following table lists the RT PolarFire ball grid array leaded packages.

Table 7-1. RT PolarFire® Ball Grid Array Leaded Package

Package	CB1509
Package Pitch	1 mm
Substrate Material	Alumina
Solder Ball Composition	Sn20/Pb80
Solder Bump Material	Sn98.2/Ag1.8

Table 7-2. RT PolarFire® Column Grid Array Leaded Package

Package	CG1509
Package Pitch	1 mm
Substrate Material	Alumina
Solder Column Composition	Sn20/Pb80 columns with copper spiral
Solder Bump Material	Sn98.2/Ag1.8

Table 7-3. RT PolarFire® Land Grid Array Leaded Package

Package	LG1509
Package Pitch	1 mm
Substrate Material	Alumina
Land Pad Composition	Gold Plated Land Pads
Solder Bump Material	Sn98.2/Ag1.8

8. Thermal Specifications (Ask a Question)

The following table lists the thermal resistances of the RT PolarFire FPGA package device.

Table 8-1. RT PolarFire® Package Thermal Resistance

Package	Environment	Theta-JA	Theta-JB	Theta-JC	Psi-JB	Psi-JT	Unit
RTPF500T-CG1509	Still Air	8.15 C/W	3.42 C/W	0.54 C/W	3.2 C/W	0.014 C/W	C/W

9. Package Mass (Ask a Question)

The following table lists the package mass information.

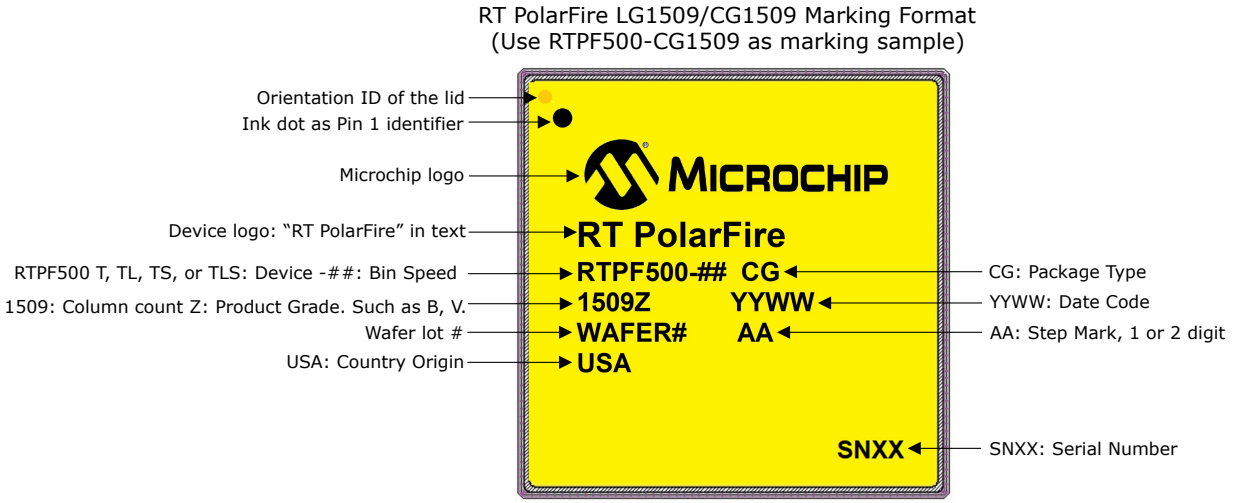
Table 9-1. Package Mass Information

Package Name	Mass Value
LG1509	28.40g
CB1509	32.71g
CG1509	34.50g

10. Package Marking (Ask a Question)

Microchip marks the full ordering part number on the top of each device. The following figure provides details for each character code present on Microchip's RT PolarFire FPGA device.

Figure 10-1. RT PolarFire® LG1509/CG1509 Package Marking Format



11. Packing and Shipping (Ask a Question)

The RT PolarFire series device is packed in trays, which are used to pack most of the Microchip surface-mount devices. Trays provide excellent protection from mechanical damage. In addition, they are manufactured using the anti-static material to provide limited protection against ESD damage.

Table 11-1. Standard Device Counts per Tray and Carton

Package	Maximum Number of Devices Per Jewel Box
CG1509	1
CB1509	1
LG1509	1

12. PCB Design (Ask a Question)

For more information about PCB design rules for CCGA packages, see AC190: Ceramic Column Grid Array Application Note.

13. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 13-1. Revision History

Revision	Date	Description
A	07/2023	The following is a summary of the changes made in revision A of this document. • Document migrated from Microsemi template to Microchip template. • Document number was changed to DS50003552A from UG0933. • Added CB1509 package mechanical drawing Figure 6-3. • Added CB1509 package mechanical drawing Figure 6-4.
1	10/2022	Initial release

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