TR0067
Test Report
RTG4 FPGA SerDes Interoperability with TI TLK2711

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

The document was update with minor enhancements.

1.2 Revision 1.0

The first publication of this document.

2 RTG4 FPGA SerDes Interoperability with TI TLK2711

Microchip® provides an interoperability solution for interfacing RTG4™ FPGA SerDes with Texas Instrument (TI) TLK2711 transceiver device. RTG4 FPGAs integrate Microchip's fourth-generation flash-based FPGA fabric and high-performance interfaces such as serialization/deserialization (SerDes) on a single-chip while maintaining the resistance to radiation-induced configuration upsets in the harshest radiation environments, such as space flight, high altitude aviation, medical electronics, and nuclear power plant control. The TLK2711-SP is a member of the Wizard Link transceivers family of multi-gigabit transceivers. It is intended for use in ultra-high-speed bidirectional point-to-point data transmission systems and supports speed of 1.6 Gbps to 2.5 Gbps, providing up to 2 Gbps of data bandwidth.

The intent of the TLK2711 Interoperability report is to demonstrate that the RTG4 device can interface and operate with the TLK2711. This report provides the interoperability test results performed with the TLK2711 device. The interoperability test results describe the hardware and software requirements for TLK2711 and RTG4 device, complete hardware test setup, equipment used, and final test report results of RTG4-TLK2711 interoperability.

2.1 References

- *UG0567: RTG4 FPGA High-Speed Serial Interfaces User Guide*
- *RTG4 FPGA Datasheet*
- *https://www.ti.com/lit/pdf/sgls307*
- *http://www.ti.com/lit/pdf/sglu001*
- *https://www.silabs.com/timing/clock-generators/general-purpose/device.si5338a*
- *https://www.silabs.com/documents/public/user-guides/Si5338-EVB.pdf*

2.2 Test Requirements

The following are the hardware and software requirements for the interoperability tests.

2.2.1 Hardware Requirements

- RTG4 Development Kit
- Two USB A to mini-B cables
- TLK2711 EVM
- Si5338 EVB
- 110 V to 240 V AC to 12 V DC power adapter for RTG4 Development kit
- Keysight 2.5 V DC power supply for TLK2711
- 7 SMA cables
- Keysight scope

2.2.2 Software Requirements

- Libero® System-on-Chip (SoC) v12.6
- Clock builder Pro v3.1

2.2.3 Source Files

For design files, contact Microchip Tech Support Team at *soc_tech@microsemi.com*.

2.3 Interoperability Test Setup

The interoperability test is performed on the RTG4 Development kit board with RTG4150-1CG1657M device as shown in Figure 1, page 4 and Texas Instruments TLK2711 EVM shown in Figure 2, page 5. The design for the test is developed using the Libero SoC v12.6 software by instantiating the PCIE_SERDES IP and other IP cores like SYSRESET, RTG4FCCC, RCOSC_50MHz, and RTG4FCCCECALIB in the SmartDesign. Clocks to both RTG4 and TLK2711 devices are provided from Si5338 EVB. Si5338 is selected as clock generator for interoperability test because its specification meets the 0 ppm and Tj (peak to peak jitter) requirement for both the TLK2711 and RTG4 device. For more information, see *RTG4 FPGA Datasheet and TI TLK2711-SP Datasheet*.

Except for the changes related to the AC coupling capacitors and resistors, no additional components are required in order to perform this test.

The jumper settings for TI TLK2711 EVM is done as per the *TI TLK2711 EVM user guide*. Before performing the interoperability tests, make sure the following changes are completed to the RTG4, TLK2711, and Si5338 EVB, both on the hardware and the software side.

For RTG4

1. Ensure that the 100 nF AC coupling capacitors is placed on the Tx data path at the RTG4 Development kit.
2. Provide Low jitter 125 MHz LVDS 2.5 reference clock with 0 ppm.
3. Remove 0 Ω resistors at R102 and R104 on the RTG4 Development kit as 125 MHz reference clock from the on-board crystal oscillator is not used.
4. Install 0 Ω resistors at R97 and R106 on the RTG4 Development kit as differential clock is supplied from Si5338 card through J48 and J57 SMA ports on the RTG4 Development kit.
5. In the RTG4 PCIE_SERDES_IF_INIT IP core configurator, click **Signal Integrity** options and set the parameters as follows:
    - Set the Transmit deemphasis settings for SerDes to 1200 mV amplitude, 0 dB for Pre-Transmit and -3.5 dB for Post-Transmit.
    - Set the channel characteristics to predefined settings ‘1’ in the receive CTLE settings for SerDes.

For TLK2711

1. Ensure that the 10 nF AC coupling capacitors is placed on the Tx data path at the TLK2711 EVM, which serve as required AC coupling for the RTG4 receiver. For AC coupling specification, see *TI TLK2711-SP Datasheet*.
2. To configure the TLK2711 in normal operation mode, keep the Jumper settings as default except for the following:
    - TESTEN(J7) - Closed
    - PRBSEN(J7) - Open
    - LCKREFEN(J7) - Open
    - ENABLE(J7) - Open
    - LOOPEN - Closed

    For more information about TLK2711 EVM kit set up and usage, see *http://www.ti.com/lit/pdf/sglu001.*
3. The TLK2711-SP generates 2.5 Gbps PRBS-7 data, which is used for interoperability test. To achieve this serial rate, provide GTX_CLK with LVCMOS 2.5, 125 MHz clock with 0 ppm, and peak to peak jitter within 40 ps.

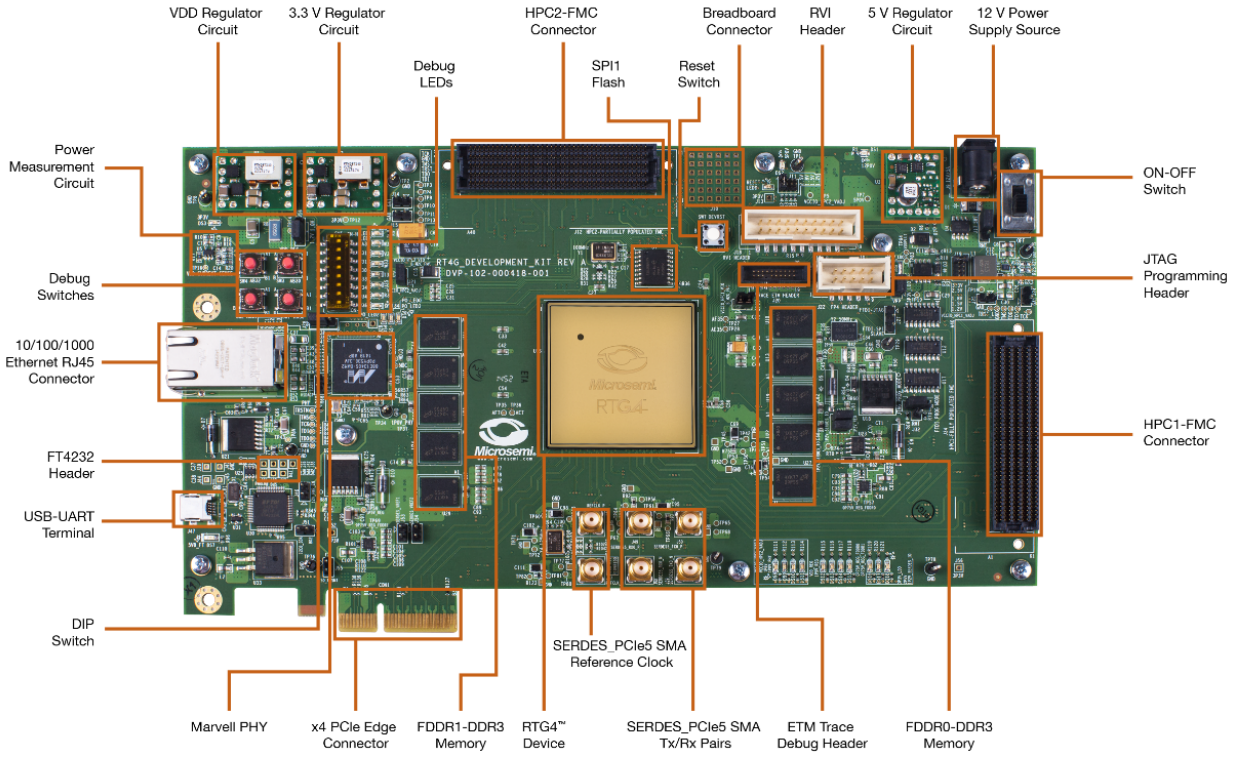
For Si5338

1. Remove 10 nF AC coupling capacitors at the clock output ports from which you can supply clocks to the TLK2711 and RTG4 devices. This is done to meet the VIL, VIH, and common-mode voltage specifications of the TLK2711 and RTG4 devices, respectively.
2. In the clock builder Pro GUI, set the input clock to 25 MHz from the crystal oscillator and output clocks to 125 MHz.
3. In the clock builder Pro GUI, select the clock format for both the output clocks from the drop down:
    - Single ended clock to TI TLK2711 - CMOS single only, 2.5 V
    - Differential clock to RTG4 - LVDS 2.5 V

In the TLK2711 EVM, J13 and J14 SMA ports are used to transmit the differential serial data to the RTG4 device, while J17 and J23 SMA ports are used to receive the differential serial data from the RTG4 device. In the RTG4 Development kit, J49 and J58 SMA ports are used to receive the differential serial data from the TLK2711 device, while J50 and J59 is used to transmit the differential serial data to the TLK2711 device. A single-ended LVCMOS clock is provided at the J8 SMA port on the TLK2711 EVM, while a differential LVDS clock is provided at J48 and J57 SMA ports on the RTG4 Development kit.

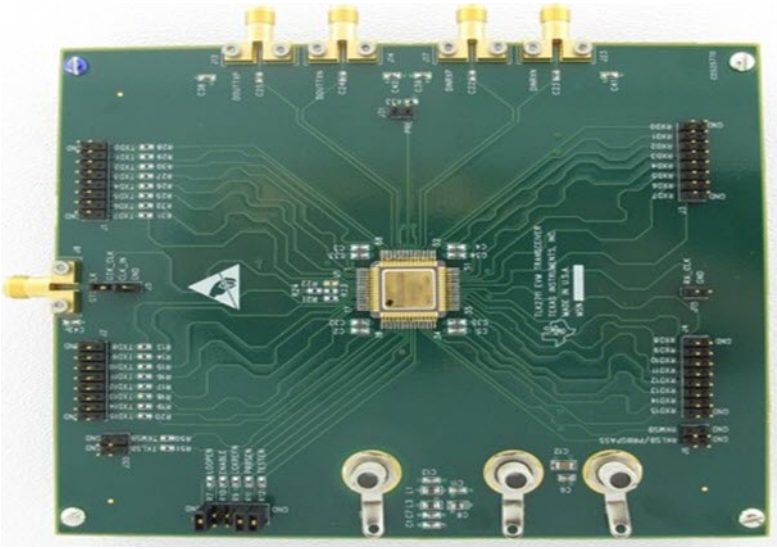
The following figure shows the RTG4 Development kit.

Figure 1 • **RTG4 Development Kit**



The following figure shows the TI TLK2711 EVM evaluation board.

Figure 2 • **TI TLK2711 EVM**



In the following figure, TLK2711 transceiver built-in PRBS generator generates PRBS-7 data, which is transmitted to the RTG4 device through the SMAs. The received data at the RTG4 SerDes is deserialized, looped back, and further serialized before sending it back to the TLK2711 device through the SMAs. Built-in PRBS checker at the TLK2711 device verifies the PRBS data and asserts the PRBS_PASS signal when the PRBS verification reports zero error. The clocks to both TLK2711 and RTG4 devices are provided by Si5338 card.

The following figure shows the block diagram of Interoperability test.

Figure 3 • **Block Diagram of Interoperability Test**

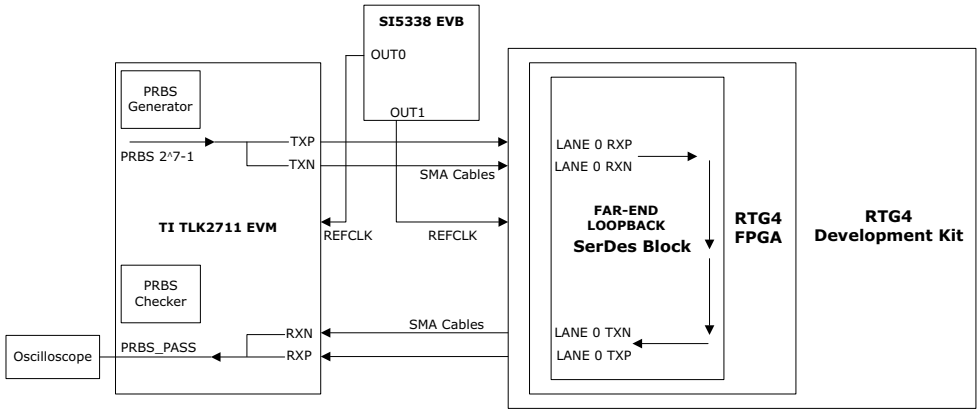
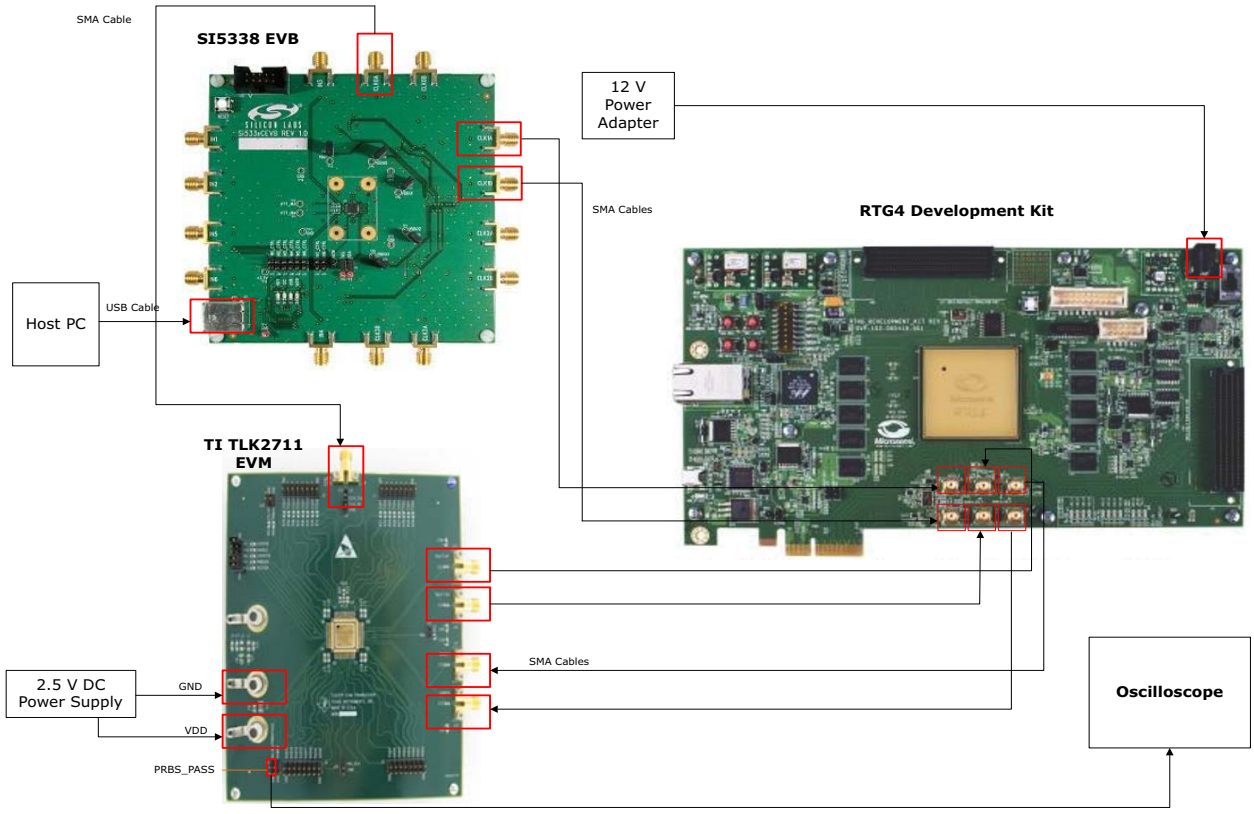


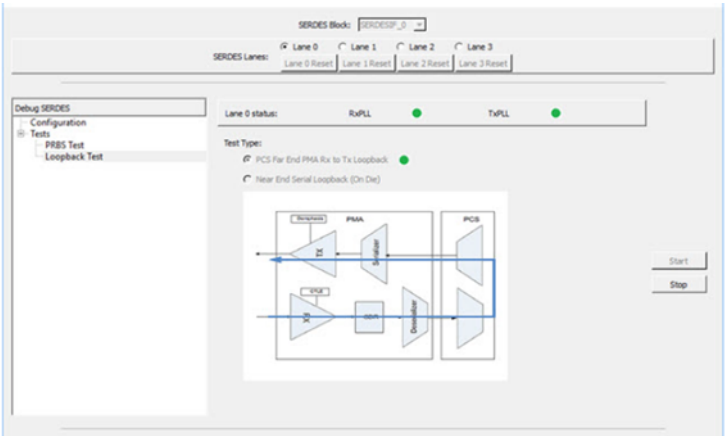
Figure 4 • **Hardware Setup for Interoperability Testing of TLK2711 with RTG4 Device**



2.4 RTG4-TLK2711 Interoperability Test Results

Microchip's SmartDebug tool complements design simulation by allowing verification and troubleshooting at the hardware level. SmartDebug provides access to non-volatile memory (eNVM), SRAM, SerDes, and probe capabilities. The following figure depicts the successful execution of the Far End loopback test using SmartDebug SerDes utility, where PRBS-7 data is transferred from the TLK2711 device to RTG4 device. SerDes PMA deserializes and serializes the data before sending it off-chip back to the TLK2711 device. This loopback requires 0 ppm clock variation between the Tx and Rx SerDes clocks.

Figure 5 • **SmartDebug GUI for Far End Loopback**



To perform interoperability tests that is serial number 3, 4, and 5 as listed in Table 1, follow:

1. Power-on the Si5338 card and program it for necessary clock settings with the help of Clock Builder Pro GUI.
2. Power-on the RTG4 Development kit.
3. Open Libero SoC software and program the RTG4 device with the design.
4. Open the SmartDebug. In the SmartDebug window, click **Debug SerDes**.
   - Select **PRBS test** > **Serial data (off die)** for tests 3 and 4.
   - Select **Loopback test** > **PCS Far End PMA Rx to Tx Loopback** for test 5.
   - Click **Start**.
5. Power-on the TI TLK2711 EVM.

For test 3, when selecting PRBS test serial data (off die), PRBS checker in the RTG4 SerDes compares and verify the PRBS data sent from TLK2711 device. Based on its output, **RXPLL** and **Lock to data** LED indicators turn green or red, and cumulative error count show the errors.

For test 4, when selecting PRBS test serial data (off die), PRBS generator in the RTG4 SerDes generates the PRBS data and send this data off die to the TLK2711 device. **TXPLL** LED indicator turns green indicating successful lock of TXPLL in the RTG4 device. The TLK2711 checks the received pattern and indicates the status on its PRBS_PASS output pin.

For test 5, when selecting PCS Far End PMA Rx to Tx loopback, PRBS data from the TLK2711 device is looped back at the RTG4 SerDes and sent to TLK2711 device. **RXPLL**, **TXPLL,** and **PCS Far End PMA Rx to Tx Loopback** LED indicators turn green indicating successful configuration of the SerDes registers and successful lock of RXPLL and TXPLL. The TLK2711 checks the received pattern and indicates the status on its PRBS_PASS output pin.

Note: RTG4 PRBS-7 is bit-wise inverted relative to other devices or visa-versa. Hence, switching the P/N wiring is required to properly communicate between the devices using the same PRBS-7 polynomial. For test 3 where TLK2711 is a transmitter and RTG4 is a receiver, ensure to connect the Txp SMA port of TLK2711 EVM with the Rxn SMA port of RTG4 Development kit and the Txn port of TLK2711 EVM with the Rxp port of RTG4 development kit. Ensure to have the same connections for test 4 where RTG4 acts as transmitter and TLK2711 as the receiver. For RTG4 SerDes Far End loopback test, the inversion of P and N channels is not required since the RTG4 SerDes is acting as a pass-through device.

The following table lists the Interoperability test results.

Table 1 • **Interoperability Test Results**

Sr. no.	Test	Status
1.	TLK2711 internal loopback	Pass (PRBS_PASS high)
2.	TLK2711 SMA loopback	Pass (PRBS_PASS high)
3.	TLK2711 Tx to RTG4 Rx simplex	Pass (**TXPLL**, **RXPLL**, and **Lock to data** LED indicators on the SmartDebug GUI turns green. **Cumulative Error Count** is 0)
4.	RTG4 Tx to TLK2711 Rx simplex	Pass (PRBS_PASS high)
5.	RTG4 SerDes Far End loopback test	Pass (PRBS_PASS high)

2.5 Conclusion

This interoperability test shows successful transmission of PRBS-7 data from the TI TLK2711 transceiver device to the RTG4 FPGA device using RTG4 SerDes's Far End loopback feature for looping back the data to the TLK2711 device. TLK2711 receiver receives the data successfully with PRBS_PASS signal indicating high. The test has been performed under room temperature with 12 V and 2.5 V power supply to the RTG4 Development kit and TI TLK2711 EVM, respectively.