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Errata
PolarFire SoC FPGA: Engineering Samples (ES) Devices

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Contents

Figures

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 1.0

The first publication of this document.

2 Errata for PolarFire SoC Engineering Samples

The PolarFire® SoC FPGA family engineering samples (ES) are subject to the limitations described in this errata document. This document contains updated information about any known engineering sample-specific issues and provides the available limitations and workarounds. Engineering sample issues identified in this document will be corrected in subsequent production revision of the devices listed in the following table. Contact *Microchip Technical Support* for more information.

2.1 Sample Revisions

The following table lists the sample revisions released. If not specified, the errata items impact all ES revisions listed in the table.

Table 1 • **Sample Revisions**

Device	Packages	Revision
MPFS250T	FCVG484EES	1
	FCG1152EES	
	FCSG536EES	
	FCVG784EES	

The following table lists the operating conditions for the PolarFire-SoC engineering samples. The operating conditions for production devices follow datasheet specifications. These operating conditions are for engineering samples only. See *DS0147: PolarFire SoC Advanced Datasheet* for production specifications.

Table 2 • **PolarFire SoC ES Operating Conditions**

Operation Temperature Range	VDD Core Voltage (Programming Voltage Only)	Program / Erase
20 °C to 50 °C[1]	1.0 ± 0.03 V[2]	20 °C to 50 °C

1. T_J = Junction Temperature
2. VDD = 1.05 V ± 0.03 V is not supported on PolarFire SoC ES silicon but will be supported for Production silicon. However, VDDA is supported at both 1.0 V and 1.05 V ± 0.03 V on ES silicon.

2.2 PCB Designs

For information about how to determine proper signal pinout, see *UG0901: PolarFire SoC FPGA Board Design Guidelines User Guide*. The proper signal pinout is required for all clocking, transceiver, and FPGA pin recommendations.

2.3   ES Device Identification

PolarFire SoC FPGA engineering samples can be identified by the temperature grade field in the lower left-hand corner. As the following illustration shows, an ES annotation will appear in the temperature grade field indicating device is engineering sample and revision marking is shown along right side of code mark.

Figure 1 •   **ES Identification Markings**
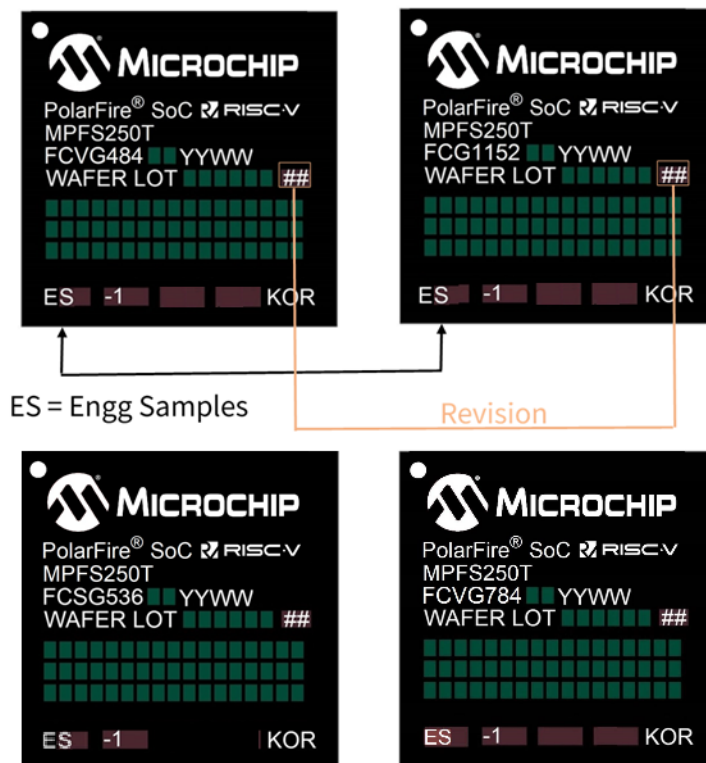
3   Errata Descriptions and Workarounds

The following sections describe device errata and the workarounds wherever applicable.

The following table lists the ES specific device errata and the affected PolarFire SoC ES device revision. For die revision part marking specification, see ES Identification Markings, page 3.

Table 3 •   **Summary of PolarFire SoC ES FPGA Errata**

Description	Silicon Revisions	Details
Microprocessor Subsystem (MSS) cannot Access System Controller SPI Flash, **page 4**	1	Applicable to all PolarFire SoC ES versions.
AXI Switch Memory Protection Unit (MPU) is not Operational, **page 5**.		
MSS I2C peripheral will Work only with MSS Core Version 2.0.108 and above, **page 5**.		
In Worst-case Scenario, MSS CPU's Frequency is Limited to 600 MHz, **page 5**		
When MSS Works as a Master, DRI Interrupt Line should not be Used, **page 6**		
DRI Error and DRI Fault Interrupts are not Connected to the Maintenance Interrupt, **page 6**		
MSS GPIO Configuration Registers should only be Reset by the CPU's, **page 6**		
Fabric APB DRI's Slow Writes Corrupt the SmartDebug JTAG/SPI Read Data, **page 6**		
System Controller Suspend Mode is not Supported, **page 6**		
PolarFire SoC MSS GEM (Gigabit Ethernet MAC) has Issue with 'Undersize Frame Counter' in Ethernet Statistics, **page 6**		
Auto-program or Auto-Update of eNVM should not be Used, **page 7**		Only Applicable to PolarFire SoC ES Revision 1 silicon.
Auto-update System Service will Allow SPI Master Mode to be Used Incorrectly Configured for SPI Slave Mode, **page 7**		

3.1   Microprocessor Subsystem (MSS) cannot Access System Controller SPI Flash

PolarFire SoC ES silicon has an issue in system controller between the analog dynamic reconfiguration interface (DRI) register block and SPI block that results in incorrect data during reads from the RXFIFO. Writes and reads to other SPI registers (for example, control, frame count, Tx data and direct access) work correctly.

Due to this issue, the MSS cannot directly access the PolarFire SOC external flash device via the SPI controller attached to the system controller using DRI bus.

This limitation will be fixed in production silicon.

3.2 AXI Switch Memory Protection Unit (MPU) is not Operational

PolarFire SoC ES parts have silicon bug that may cause AXI bus issues when illegal messages are rejected by PolarFire SoC memory protection unit (MPU). For this reason, MPU is currently disabled as part of system start-up firmware. This means that the MPU's are inactive and will not generate access warnings or interrupts.

This limitation will be fixed in production silicon.

3.3 MSS I2C peripheral will Work only with MSS Core Version 2.0.108 and above

In PolarFire SoC ES parts, MSS I2C clock and data signals are pulled low after MSS initialization. MSS core in Libero 12.4 has the required workaround for this MSS I2C issue in ES device. Use MSS core version 2.0.108 or above for Libero 12.4 or use Libero 12.5 and above where workaround will be automatically applied when the user selects an ES part. Note that the workaround fix in Libero is using the fabric in all cases and the user will need to program the FPGA portion to have the MSS I2C working.

This limitation will be fixed in production silicon. User designs using MSS I2C in ES silicon can not be ported to production silicon. Users need to regenerate the MSS configurator and bitstream when porting design to production silicon and make sure to target the correct device.

3.4 In Worst-case Scenario, MSS CPU's Frequency is Limited to 600 MHz

In PolarFire SoC ES, maximum achievable MSS CPU frequency is 625 MHz for both STD and -1 speed grades. The eMMC/SD controller requires a fixed 200 MHz clock, fed from the same PLL as the CPU. The CAN controller requires a clock, which is a multiple of 8 MHz, also fed from the same PLL as the CPU. However, in engineering samples, the following limitations applies for these clock frequencies:

1. If the eMMC/SD controller is being used in the system, the maximum MSS CPU clock frequency is 600 MHz.
2. If the CAN controller is being used in the system (but not the eMMC/SD controller), the maximum MSS CPU clock frequency is either 624 MHz (with 100 MHz reference clock) or 620 MHz (with 125 MHz reference clock). There is a general restriction in the available MSS CPU frequency:

- If using 100 MHz reference clock for MSS PLL:
  When no eMMC/SD or CAN is being used, the MSS CPU frequencies are—all integer values from 2 through 625
  - When eMMC/SD being used (with or without CAN), the MSS CPU frequencies are:
    2, 4, 5, 6, 8, 10, 12, 15, 16, 20, 24, 25, 30, 32, 40, 48, 50, 60, 75, 80, 100, 120, 125, 150, 160, 200, 240, 250, 300, 400, 500, 600.
  - When CAN being used (without eMMC/SD), the MSS CPU frequencies are:
    All integer values from 2 through 156,
    Every 2nd value from 158 through 312
    Every 4th value from 316 through 624
- If using 125 MHz reference clock for MSS PLL:
  - When no eMMC/SD or CAN is being used, the MSS CPU frequencies are—all integer values from 2 through 250 and every 5th value from 255 through 625.
  - When eMMC/SD being used (with or without CAN), the MSS CPU frequencies are:
    2, 4, 5, 6, 8, 10, 12, 15, 16, 20, 24, 25, 30, 32, 40, 48, 50, 60, 75, 80, 100, 120, 125, 150, 160, 200, 240, 250, 300, 400, 500, 600
  - When CAN being used (without eMMC/SD), the MSS CPU frequencies are:
    2 – 32, 34, 35, 36, 38, 40, 42, 44, 45, 46, 48, 50, 52, 54, 55, 56, 58, 60, 62, 64, 65, 68, 70, 72, 75, 76, 80, 84, 85, 88, 90, 92, 95, 96, 100, 104, 105, 108, 110, 112, 115, 116, 120, 124, 125, 128, 130, 135, 136, 140, 144, 145, 150, 152, 155, 160, 168, 170, 176, 180, 184, 190, 192, 200, 208, 210, 216, 220, 224, 230, 232, 240, 248, 250, 260, 270, 280, 290, 300, 310, 320, 340, 360, 380, 400, 420, 440, 460, 480, 500, 520, 540, 560, 580, 600, 620.

Note: The User Crypto may also get its clock from the MSS PLL but has the option of getting its clock from the FPGA fabric. This does not place the same limitations on MSS CPU frequency.

This limitation will be fixed in production silicon.

3.5 When MSS Works as a Master, DRI Interrupt Line should not be Used

The DRI interrupt system should not be used with the PolarFire SOC ES silicon device. If enabled, the interrupt input to the fabric and MSS from the DRI system cannot be cleared without a device reset. As a workaround, few events that DRI interrupts may have been used for are also available as status signals to the fabric.

This limitation will be fixed in production silicon.

3.6 DRI Error and DRI Fault Interrupts are not Connected to the Maintenance Interrupt

DRI Error and DRI Fault interrupt bits in the Maintenance Register function as expected but will not cause a CPU interrupt—the interrupt enable is effectively disabled in ES silicon.

This limitation will be fixed in production silicon.

3.7 MSS GPIO Configuration Registers should only be Reset by the CPU's

The three MSS GPIO blocks do not support the fabric reset functionality in PolarFire SoC ES silicon. The GPIO blocks should be configured so that the byte resets use the internal MSS reset, that is, the GPIO_CR configuration register 'soft_reset_select' bits should not be set to 0.

This limitation will be fixed in production silicon.

3.8 Fabric APB DRI's Slow Writes Corrupt the SmartDebug JTAG/SPI Read Data

A fabric DRI write operation to one of the PCIe subsystem (PCIESS) controllers APB configuration blocks may corrupt a SmartDebug JTAG/SPI read operation; the read will return zero. If this is suspected, the SmartDebug operation should be carried out again until the expected data is received.

This limitation will be fixed in production silicon.

3.9 System Controller Suspend Mode is not Supported

System controller suspend mode is not supported in PolarFire SoC ES silicon parts. This limitation will be fixed in production silicon.

3.10 PolarFire SoC MSS GEM (Gigabit Ethernet MAC) has Issue with 'Undersize Frame Counter' in Ethernet Statistics

In the Polarfire SoC, for 1Gbps half-duplex mode, Ethernet statistics "undersize_frames" counter within the GEM increments for received frame sizes less than 512 bytes instead of incrementing for less than 64 bytes. Subsequent transition to 1Gbps full-duplex mode does not resolve the issue. User should note that 'Undersize Frame counter' reports correctly for all other speeds and duplex modes, including 1Gbps full-duplex if not transitioning from half-duplex.

3.11 Auto-program or Auto-Update of eNVM should not be Used

Boot initiated auto-program/auto-update of eNVM will fail. Auto-program/update of eNVM should not be used on PolarFire SoC ES silicon. This limitation will be fixed in production silicon.

3.12 Auto-update System Service will Allow SPI Master Mode to be Used Incorrectly Configured for SPI Slave Mode

In PolarFire SoC ES silicon, auto-update system service will allow SPI master mode to be used on a PolarFire SoC ES silicon device configured in SPI slave mode. Ideally, it should throw an error. If this service is used on device configured in slave mode, there is a possibility of contention on the SPI flash pins. Fix for this issue is that auto-update system service should not be used if the PolarFire SoC ES silicon device is configured for slave mode.

This limitation will be fixed in production silicon.

4 Fabric Transceiver Protocols and DDR Memory Interfaces

Supported transceiver protocols and DDR memory interfaces are reused features from PolarFire FPGA. These are currently in plan for validation and these features are in the process of being validated. These features are expected to work with similar robustness as in PolarFire FPGAs.

5 Libero SoC Software Errata

For more Libero SoC related "known Issues and limitations", see *Libero SoC Release Notes* document.

6 Embedded Software Errata

See the "Known Issues and useful tips" section in *SoftConsole Release Notes* document.

These SoftConsole known issues are under active investigation to ascertain the root cause and to resolve the underlying problems with the intention that these are resolved in a future release.