

**Getting Started with the RISC-V Based PolarFire® SoC
FPGA Webinar Series**
Session 14 The PolarFire SoC Icicle Kit Model in Renode



A Leading Provider of Smart, Connected and Secure Embedded Control Solutions



SMART | CONNECTED | SECURE

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Thursday June. 11, 2020

Supporting Content

www.microsemi.com/Mi-V “Renode Webinar Series”

The screenshot shows the Microsemi website's product directory for FPGA SoC. The URL in the address bar is `product-directory/fpga-soc/5210-mi-v-embedded-ecosystem#renode-webinar-series`. The navigation bar includes links for Ordering, Company, Partners, and Support. A search bar is present with the text "Search Microsemi.com". Below the navigation bar, there is a banner for "Libero SoC Design Suite v12.0" with bullet points: "Unified design suite for PolarFire, IGLOO2, SmartFusion2 and RTG4 families", "60% runtime reduction for Timing and 20% runtime reduction for Power", and "25% runtime improvement for Place and Route". Below the banner, a breadcrumb trail reads "Home / Products & Services / FPGA & SoC / Mi-V RISC-V Ecosystem". The main heading is "Mi-V RISC-V Ecosystem". Below this, there is a horizontal menu with links: Overview, Mi-V Partners, Tutorials, Renode Webinar Series (highlighted with a red box), and Articles and News. The section title is "Getting Started with the RISC-V Based PolarFire™ SoC FPGA Webinar Series". The text below reads: "Learn how to get started with the PolarFire SoC FPGA, the world's first RISC-V based SoC FPGA, to create fully deterministic, real-time systems alongside the Linux® operating system. We are holding a series of webinars to introduce you to the free Renode™ development platform from Mi-V partner Antmicro that is available with our SoftConsole v6.0 software development environment. You will see demo applications, learn how to create projects, and find out how to set up and configure your own systems targeting the new SoC FPGA architecture." Below this text, there is a link "Click here to register." and logos for Mi-V and Antmicro. The section title for the first webinar is "Webinar 1 (May 2): Discover Renode for PolarFire™ SoC Design and Debug". The text below reads: "In this introductory session, we will provide you with an overview of SoftConsole 6.0 with Renode™ integration. We will introduce you to the Renode development framework and provide an overview of the platform and its features. You will also learn about the PolarFire™ SoC architecture and how to use Renode to develop your application."

Webinar 1: Discover Renode for PolarFire® SoC Design and Debug

Webinar 2: How to Get Started with Renode for PolarFire SoC

Webinar 3: Learn to Debug a Bare-Metal PolarFire SoC Application with Renode

Webinar 4: Tips and Tricks for Even Easier PolarFire SoC Debug with Renode

Webinar 5: Add and Debug PolarFire SoC Models with Renode

Webinar 6: Add and Debug Pre-Existing Model in PolarFire SoC

Webinar 7: How to Write Custom Models

Webinar 8: What's New in SoftConsole v6.2

Webinar 9: Getting Started with PolarFire SoC

Webinar 10: Introduction to the PolarFire SoC Bare-Metal Library

Webinar 11: Handling Binaries

Webinar 12: Simple Peripheral as Software Stimulus

Webinar 13: Two Baremetal Applications on PolarFire SoC

Agenda

- **SoftConsole v6.3**
- **Renode Icicle Kit Model**

SoftConsole v6.3

SoftConsole v6.3

- SoftConsole v6.3 released July 2020
- Renode v1.9.0 will be included in SoftConsole v6.3, which includes the Icicle Kit model
- Model names all updated to MPFS naming convention

```
RENODE™
Renode, version 1.8.2.16245 (b2ae449e-201911210859)

(monitor) $GDB_SERVER_PORT=3333
(monitor) path add @C:\Microsemi\SoftConsole_v6.2_\renode-microchip-mods/
Current 'PATH' value is: C:\Microsemi\SoftConsole_v6.2_\renode;C:\Microsemi\SoftConsole_v6.2_\renode\bin;C:\Microsemi\SoftConsole_v6.2_\renode-microchip-mods\
(monitor) include @scripts\polarfire-soc-generic-board.resc
Starting GDB server on port: 3333
(machine-0) peripherals
Available peripherals:

sysbus (SystemBus)
├── can0 (PSE_CAN)
│   ├── <0x2010C000, 0x2010CFFF>
├── can1 (PSE_CAN)
│   ├── <0x2010D000, 0x2010DFFF>
├── clint (CoreLevelInterruptor)
│   ├── <0x02000000, 0x0200FFFF>
├── ddr (MappedMemory)
│   ├── <0x80000000, 0xBFFFFFFF>
├── e51 (RiscV64)
│   ├── Slot: 0
```










```
RENODE™
Renode, version 1.9.0.12492 (3a684b41-202005270653)

(monitor) $GDB_SERVER_PORT=3333
(monitor) path add @C:\Microchip\SoftConsole-v6.3.0.375\renode-microchip-mods/
Current 'PATH' value is: C:\Microchip\SoftConsole-v6.3.0.375\renode;C:\Microchip\SoftConsole-v6.3.0.375\renode\bin;C:\Microchip\SoftConsole-v6.3.0.375\renode-microchip-mods\
(monitor) include @scripts\polarfire-soc-generic-board.resc
Starting GDB server on port: 3333
(machine-0) peripherals
Available peripherals:

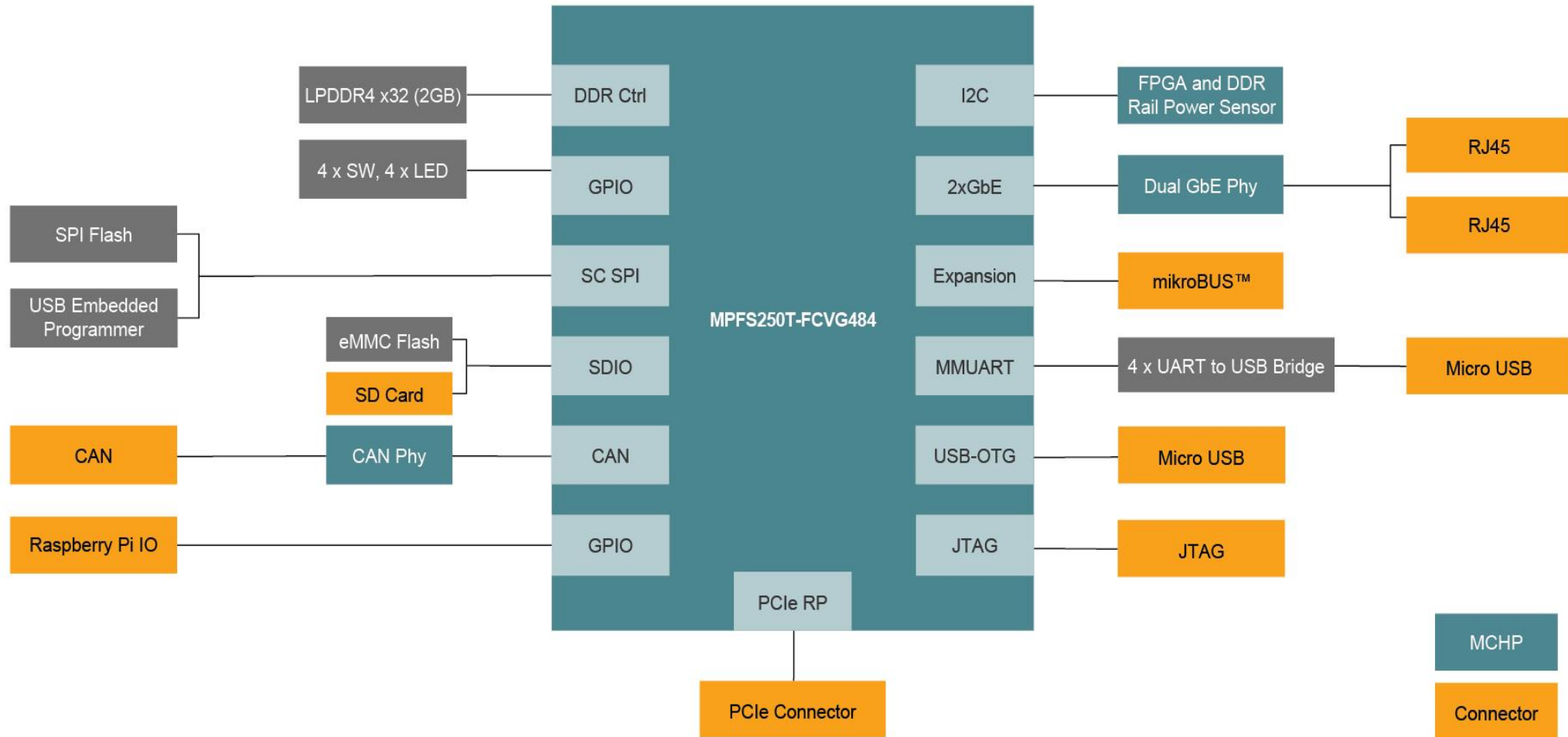
sysbus (SystemBus)
├── can0 (MPFS_CAN)
│   ├── <0x2010C000, 0x2010CFFF>
├── can1 (MPFS_CAN)
│   ├── <0x2010D000, 0x2010DFFF>
├── clint (CoreLevelInterruptor)
│   ├── <0x02000000, 0x0200FFFF>
├── ddr (MappedMemory)
│   ├── <0x80000000, 0xBFFFFFFF>
├── e51 (RiscV64)
│   ├── Slot: 0
```

Renode Icicle Kit Model

Renode Icicle Kit Model

<div>🏠 Renode - documentation</div> <div>RENODE™</div> <div>INTRODUCTION</div> <div>Installing Renode</div> <div>Using Renode</div> <div>Running your first demo</div> <div>Supported boards</div> <div>Troubleshooting</div> <div>BASIC USAGE</div> <div>Working with machines</div> <div>Describing platforms</div> <div>Basic execution control</div> <div>Using the logger</div> <div>State saving and loading</div> <div>Environment</div> <div>DEBUGGING</div> <div>Debugging with GDB</div> <div>NETWORKING</div> <div>Setting up a wired network</div> <div>Setting up a wireless network</div> <div>Connecting to the host network</div> <div>Inspecting the traffic with Wireshark</div> <div>TUTORIALS</div> <div>Microsemi Mi-V example</div> <div>Testing Zephyr PTP support</div> <div>Renode, Fomu and EtherBone bridge example</div> <div>USB/IP support</div> <div>ADVANCED TOPICS</div>	tegra3.resc	vegaboard_riscv.resc	quark_c1000.resc
			
	Fomu	LiteX/VexRiscv on Digilent Arty	Xilinx ZedBoard
	renode_etherbone_fomu.resc	arty_litex_vexriscv.resc	zedboard.resc
			
	ST Micro STM32F103 Blue Pill	Kendryte K210	Zolertia Firefly
	stm32f103.resc	kendryte_k210.resc	zolertia.resc
			
	QuickFeather Development Kit	OpenPOWER Microwatt on Digilent Nexys Video	Microchip PolarFire SoC Icicle Kit
	quickfeather.resc	microwatt.resc	mpfs-icicle-kit.repl

Renode Icicle Kit Model



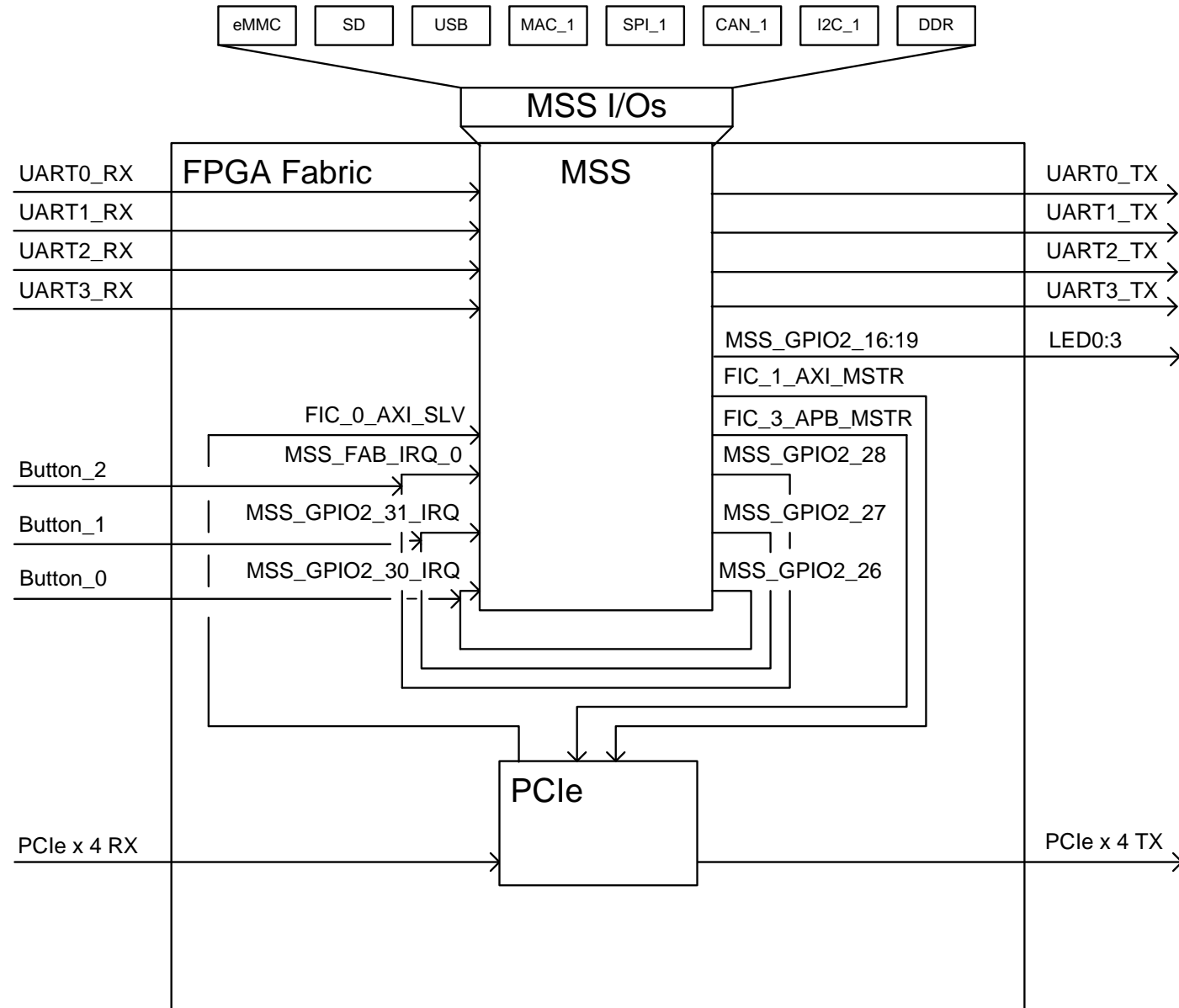
Renode Icicle Kit Model

- Expands on the original PolarFire SoC Icicle Kit Renode model

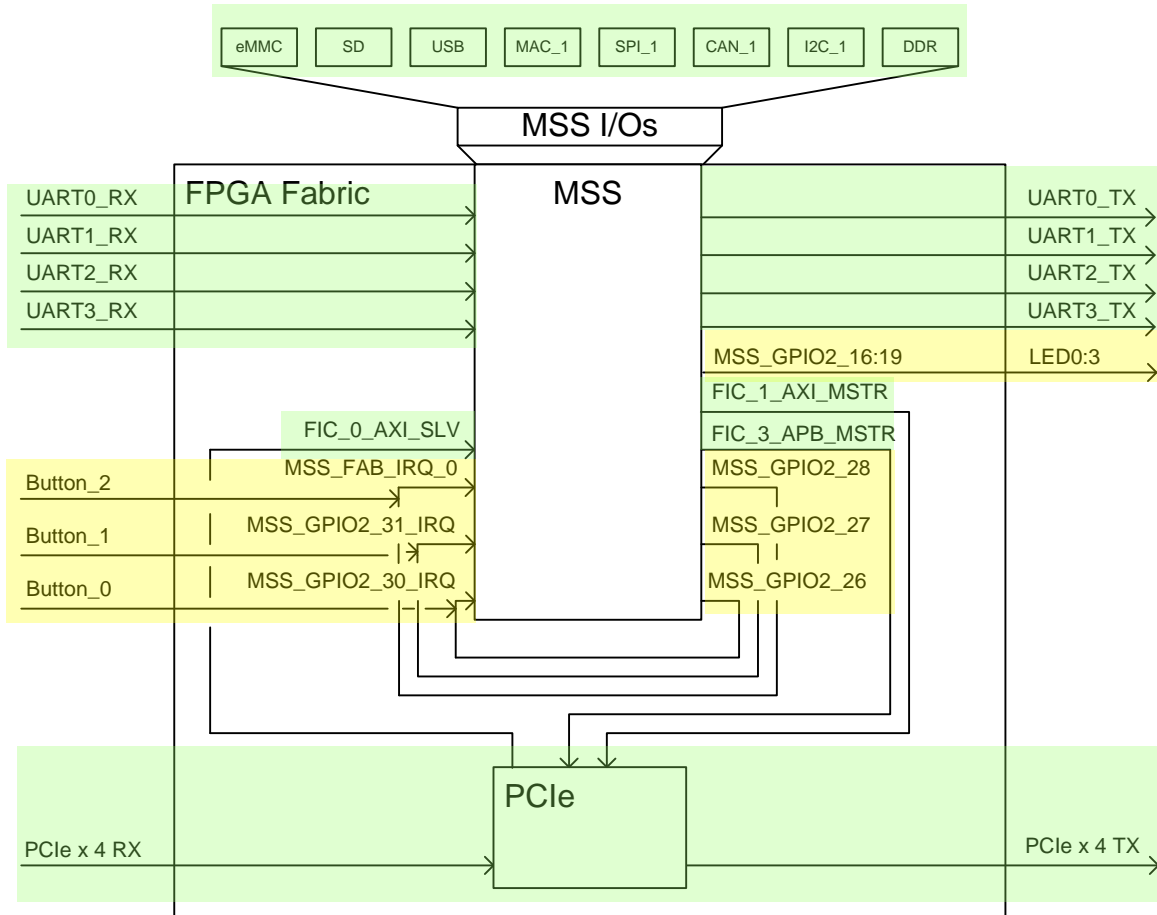
```
1 :name: PolarFire SoC Icicle
2 :description: This is a sample script prepared to create a PolarFire SoC Icicle platform
3
4 include @scripts/polarfire-soc-generic-board.resc
5
```

```
1 :name: PolarFire SoC Icicle
2 :description: This is a sample script prepared to create a PolarFire SoC Icicle platform
3
4 include @scripts/macros-pfsoc.resc
5
6 logLevel 3
7
8 using sysbus
9 mach create
10
11 machine LoadPlatformDescription @platforms/cpus/polarfire-soc.repl
12 machine LoadPlatformDescriptionFromString
13 """
14 gpio0: @ none
15
16 gpio1: @ none
17
18 gpio2:
19     16 -> led000
20     17 -> led100
21     18 -> led200
22     19 -> led300
23     26 -> gpio2@30
24     27 -> gpio2@31
25     28 -> plic@118
26
27 pseFlash: @ none
28
29 led0: Miscellaneous.LED @ gpio2 16
30
31 led1: Miscellaneous.LED @ gpio2 17
32
33 led2: Miscellaneous.LED @ gpio2 18
34
35 led3: Miscellaneous.LED @ gpio2 19
36
37 button1: Miscellaneous.Button @ gpio2 30
38     -> gpio2@30
39
40 button2: Miscellaneous.Button @ gpio2 31
41     -> gpio2@31
42
43 button3: Miscellaneous.Button @ gpio2 28
44     -> plic@118
45 """
46
47 logLevel 3 sysbus.e51
48 logLevel 3 sysbus.u54_1
49 logLevel 3 sysbus.u54_2
50 logLevel 3 sysbus.u54_3
51 logLevel 3 sysbus.u54_4
52
53 # Before invoking this script the GDB port has to be set, example:
54 # $GDB_SERVER_PORT=3333
55 # When this script (or its children) are invoked from the SoftConsole external
56 # launcher then the GDB port can be set by adding the following argument before
57 # the platform script is invoked:
58 # -e "$GDB_SERVER_PORT=3333"
59 echo -n "Starting GDB server on port: "
60 echo $GDB_SERVER_PORT
61 machine StartGdbServer `echo $GDB_SERVER_PORT`
```

Renode Icicle Kit Model



Renode Icicle Kit Model



```

1 :name: PolarFire SoC Icicle
2 :description: This is a sample script prepared to create a PolarFire SoC Icicle platform
3
4 include @scripts/macros-pfsoc.resc
5
6 logLevel 3
7
8 using sysbus
9 mach create
10
11 machine LoadPlatformDescription @platforms/cpus/polarfire-soc.repl
12 machine LoadPlatformDescriptionFromString
13 """
14 gpio0: @ none
15
16 gpio1: @ none
17
18 gpio2:
19     16 -> led0@0
20     17 -> led1@0
21     18 -> led2@0
22     19 -> led3@0
23     26 -> gpio2@30
24     27 -> gpio2@31
25     28 -> plic@118
26
27 pseFlash: @ none
28
29 led0: Miscellaneous.LED @ gpio2 16
30
31 led1: Miscellaneous.LED @ gpio2 17
32
33 led2: Miscellaneous.LED @ gpio2 18
34
35 led3: Miscellaneous.LED @ gpio2 19
36
37 button1: Miscellaneous.Button @ gpio2 30
38     -> gpio2@30
39
40 button2: Miscellaneous.Button @ gpio2 31
41     -> gpio2@31
42
43 button3: Miscellaneous.Button @ gpio2 28
44     -> plic@118
45 """
46
47 logLevel 3 sysbus.e51
48 logLevel 3 sysbus.u54_1
49 logLevel 3 sysbus.u54_2
50 logLevel 3 sysbus.u54_3
51 logLevel 3 sysbus.u54_4
52
53 # Before invoking this script the GDB port has to be set, example:
54 # $GDB_SERVER_PORT=3333
55 # When this script (or its children) are invoked from the SoftConsole external
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58 # -e "$GDB_SERVER_PORT=3333"
59 echo -n "Starting GDB server on port: "
60 echo $GDB_SERVER_PORT
61 machine StartGdbServer `echo $GDB_SERVER_PORT`

```

Renode Icycle Kit Model


polarfire-soc.repl

E51	U54_1	U54_2	U54_3	U54_4
CLINT	PDMA	PLIC	MMUART0	MMUART1
MMUART2	MMUART3	MMUART4	eMMC	SPI0
SPI1	I2C0	I2C1	CAN0	CAN1
MAC0	MAC1	PHY	GPIO0	GPIO1
GPIO2	WDOG0	WDOG1	WDOG2	WDOG3
WDOG4	RTC	MSTIMER	eNVM	USB
DDR	PCIe0	PCIe1	QSPI	

Renode Icycle Kit Model

- The current sensor model is still a work in progress
- It will be available at the end of June
- When its released the model can be downloaded and added as JiT
- Watch webinar 6 “Add and Debug Pre-Existing Model in PolarFire SoC”
- Watch webinar 12 “Simple Peripheral as Software Stimulus”

Icicle Kit Model

 [renode](#) / [renode-infrastructure](#)


Used by ▼ 18


Watch ▼ 6


Star 4


Fork 15

<> Code

 Pull requests 2


 Actions

 Security 0

 Insights






Branch: master ▼ [renode-infrastructure](#) / [src](#) / [Emulator](#) / [Peripherals](#) / [Peripherals](#) / [Sensors](#) /

Create new fileUpload filesFind fileHistory

 **mateusz-holenko** [#18461] Add ADXL345 model

Latest commit d13a15b on Mar 26

..

 ADXL345.cs	[#18461] Add ADXL345 model	2 months ago
 DummySensor.cs	[#9650] Update copyright headers.	3 years ago
 MAX6682MUA.cs	[#9650] Update copyright headers.	3 years ago
 SI70xx.cs	[#9650] Update copyright headers.	3 years ago
 TI_LM74.cs	[#9650] Update copyright headers.	3 years ago

workspace.examples - mpfs-gpio/src/application/hart0/e51.c - SoftConsole v6.3.0.376

File Edit Source Refactor Navigate Search Project Git Run Window Help

Project Explorer

mpfs-blinky

mpfs-freertos-lwip

mpfs-gpio

- Binaries
- Includes
- src
 - application
 - demos
 - hart0
 - e51.c
 - hart1
 - hart2
 - inc
 - modules
 - platform
 - Debug
 - renode
 - mpfs-gpio hw Debug.launch
 - mpfs-gpio Renode Debug.launch
 - mpfs-gpio Renode Start-platform-and-d
 - README.html
 - README.md

e51.c

```
137 * Application code running on HART0 is placed here.
138 * U54 HARTs are not used and they are kept in WFI
139 */
140 void e51 (void)
141 {
142     /*Reset UART0 */
143     SYSREG->SOFT_RESET_CR &= ~(0x01UL << 5);
144
145     /* all clocks on */
146     SYSREG->SUBBLK_CLOCK_CR = 0xffffffff;
147
148     PLIC_init();
149
150     PLIC_SetPriority_Threshold(0);
151     PLIC_SetPriority(GPIO1_BIT16_or_GPIO2_BIT30_PLIC_30, 2);
152     PLIC_SetPriority(GPIO1_BIT17_or_GPIO2_BIT31_PLIC_31, 2);
153     PLIC_SetPriority(GPIO0_NON_DIRECT_PLIC, 2);
154     PLIC_SetPriority(GPIO1_NON_DIRECT_PLIC, 2);
155     PLIC_SetPriority(GPIO2_NON_DIRECT_PLIC, 2);
156     PLIC_SetPriority(FABRIC_F2H_0_PLIC, 2);
157
158     PLIC_EnableIRQ(GPIO1_BIT16_or_GPIO2_BIT30_PLIC_30);
159     PLIC_EnableIRQ(GPIO1_BIT17_or_GPIO2_BIT31_PLIC_31);
160     PLIC_EnableIRQ(GPIO2_NON_DIRECT_PLIC);
161     PLIC_EnableIRQ(FABRIC_F2H_0_PLIC);
162     PLIC_EnableIRQ(MMUART0_PLIC_77);
163
164     __disable_local_irq((int8_t) MMUART0_E51_INT);
165     __enable_irq();
166
167     /* GPIO2 */
168     MSS_GPIO_init(GPIO2_L0);
```

Outline Expressions Disassembly

stdio.h

string.h

../inc/common.h

mpfs_hal/mss_hal.h

drivers/mss_gpio/mss_gpio.h

drivers/mss_uart/mss_uart.h

mpfs_hal/mss_clint.h

uart_lock : uint64_t

uart_buf : char[]

gpio1_bit16_or_gpio2_bit30_plic_30_IRQHandler(void) : uint8_t

gpio1_bit17_or_gpio2_bit31_plic_31_IRQHandler(void) : uint8_t

fabric_f2h_0_plic_IRQHandler(void) : uint8_t

SysTick_Handler(uint32_t) : void

rx_size : uint8_t

rx_buff : uint8_t[]

uart0_rx_handler(mss_uart_instance_t*) : void

e51(void) : void

Variables Registers

Name	Type	Value
------	------	-------

Problems Markers Console Terminal Search Debugger Console

CDT Build Console [mpfs-mustein-julia]

Renode Icicle Kit Mode

- Available in SoftConsole v6.3
- Current sensor model will be available from
- Add the model to your SoftConsole project
- Add the path to the model in your external tools
- Add your launch script to your SoftConsole project and add it to the external tool configurations
- Watch webinar 6 “Add and Debug Pre-Existing Model in PolarFire SoC”
- Watch webinar 12 “Simple Peripheral as Software Stimulus”

Agenda

- **SoftConsole v6.3**
- **Renode Icicle Kit Model**

Thank you!

Any questions?

Second Thursdays

July 9 - Webinar 15: Linux® on Renode

Aug. 13 - Webinar 16: Building Applications for Linux on PolarFire SoC

Sep. 10 - Webinar 17: Real-Time (AMP Mode) on PolarFire SoC