

LX7720DB to SAMRH71EVB Connector Kit

1 Description

This is a connector kit connecting an [LX7720 Daughter Board](#) to a [SAMRH71F20-EK Evaluation Kit](#) for radiation hardened variable-frequency drives (Figure 1). Demonstration firmware is available.

The design operates a 3-phase permanent magnet synchronous motor (PMSM) using an LX7720 for motor driver and phase currents measurement, and a [SAMRH71F20](#) (200 DMips Cortex M7 with 100krad TID capability) as the PI loop controller (Figure 2).



Figure 1. LX7720DB and SAMRH71EVB Setup

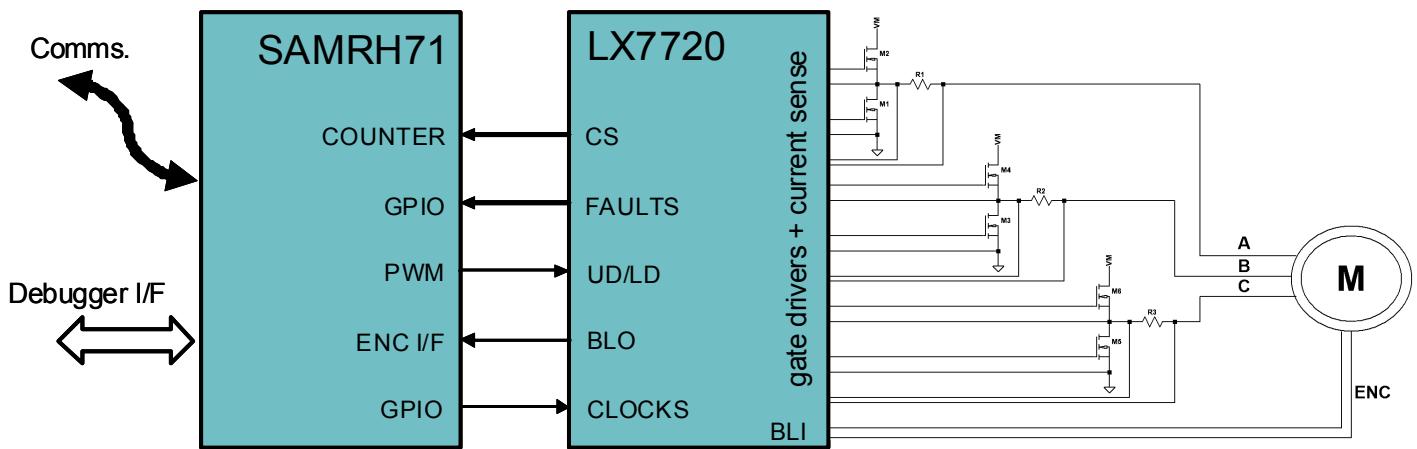


Figure 2. LX7720DB and SAMRH71EVB Motor Driver Top Level Block Diagram

The firmware implements Field Oriented Control (FOC) algorithm using two D/Q space current PI loops, and a speed regulation loop using a two-channel quadrature optical encoder. The current sense processing and the FOC algorithm sustaining a 20kHz PWM (fast) loop and 4kHz torque (slow) loop bring the SAMV71 CPU to < 55% loading.

1.1 LX7720 Operations

- The LX7720 drives 3 MOSFET half-bridges for the 3 motor phases, and senses motor phase currents
 - The LX7720 current sense outputs are 25Mbit/s $\Delta\Sigma$ modulator output streams
- The LX7720 monitors the motor's two-channel quadrature optical encoder via the BLI1 and BLI2 comparator inputs, and provides the corresponding BLO1 and BLO2 logic outputs

1.2 SAMRH71 Operations

- The SAMRH71 generates 6 PWM waveforms for the LX7720's half-bridges (independent high and low drives)
- The SAMRH71 generates the LX7720's 25MHz $\Delta\Sigma$ modulator clock and charge pump clock
- The SAMRH71 senses rotor position using the encoder interface via GPIO monitoring the LX7720 BLO1, BLO2 outputs
- The SAMRH71 calculates motor currents using digital filters on the LX7720 $\Delta\Sigma$ modulator output streams:
 - Integrator using a timer/counter
 - SINC3 decimation filter
 - Median filter
- The SAMRH71 monitors LX7720 fault outputs via GPIO

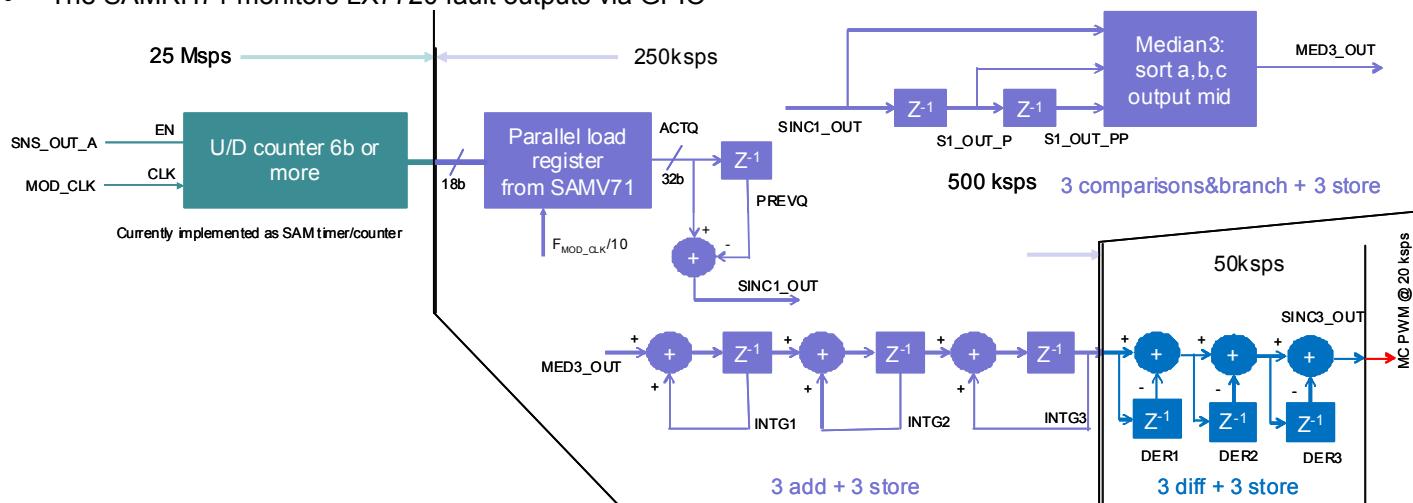


Figure 3. Firmware Block Diagram

1.3 Connector Kit

The kit comprises a small PCB with switches, and a flexible circuit which connects a SAMRH71F20-EK to an LX7720DB.

- The flexible circuit connects signals from SAMRH71F20-EK 0.1" headers J24 and J30 to LX7720DB's header J20
- A small PCB with switches connects to GPIOs on SAMRH71F20-EK 0.1" headers J25 via a 20 way ribbon cable
- The motor is Hurst DMA0204024B101, available as [Microchip AC300022](#). Table 3 on page 4 provides connections.

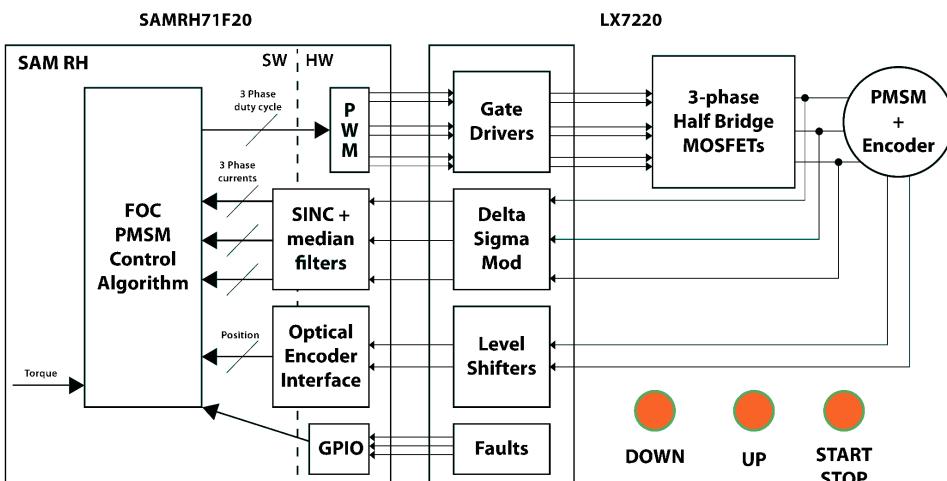


Figure 4. LX7720DB to SAMRH71EVB Detail Block Diagram

1.4 SAMRH71EVB Resource Allocation

Timer TC0 also generates a 4 μ s interrupt to trigger timer TC3. Note that although the motor phase C current $\Delta\Sigma$ serial stream SNS_OUT_C is available, the firmware infers this phase current from SNS_OUT_A and SNS_OUT_B.

Table 1. Resource Allocations and Functionality

LX7720DB Signal	LX7720DB Function	SAMRH71 Function	Pin	Timer
Motor Phase Waveform Generation				
LD_IN_A	Motor phase A lower FET PWM	PWMCO_PWML0	PA4	TC0
UD_IN_A	Motor phase A upper FET PWM	PWMCO_PWMH0	PA0	TC0
LD_IN_B	Motor phase B lower FET PWM	PWMCO_PWML1	PA5	TC0
UD_IN_B	Motor phase B upper FET PWM	PWMCO_PWMH1	PA1	TC0
LD_IN_C	Motor phase C lower FET PWM	PWMCO_PWML2	PA6	TC0
UD_IN_C	Motor phase C upper FET PWM	PWMCO_PWMH2	PA2	TC0
Motor Phase Current Acquisition				
SNS_OUT_A	Motor phase A current $\Delta\Sigma$ serial stream	TCLK9	PC21	TC3
SNS_OUT_B	Motor phase B current $\Delta\Sigma$ serial stream	TCLK10	PC28	TC3
SNS_OUT_C	Motor phase C current $\Delta\Sigma$ serial stream	TCLK11	PC25	TC3
Motor Quadrature Encoder Acquisition				
BLO1	Bi-level (comparator) output 1. Quadrature encoder output A is connected to BLI1	TIOA3	PB9	TC1
BLO2	Bi-level (comparator) output 2. Quadrature encoder output B is connected to BLI2	TIOB3	PB10	TC1
LX7720 Clock Generation				
CP_CLK	150kHz charge pump clock	Programmable clock PCK2	PA10	-
MOD_CLK	25MHz $\Delta\Sigma$ modulator clock	Programmable clock PCK0	PA11	-
LX7720 Status Monitoring, Switch Inputs, LED Drive, and unassigned LX7720 BLI/BLO comparators				
PR_FAULT	Power rail fault logic output	GPIO input	PA8	-
OC_FAULT	Over current fault logic output	GPIO input	PA9	-
OTW_FAULT	Over temperature fault logic output	GPIO input	PC9	-
RESET	Reset push switch, active low	GPIO input	PA20	-
DIRECTION	Direction push switch, active low	GPIO input	PA21	-
START/STOP	Start/Stop push switch, active low	GPIO input	PA22	-
INCREASE SPEED	Increase Speed push switch, active low	GPIO input	PA23	-
DECREASE SPEED	Decrease Speed push switch, active low	GPIO input	PA24	-
BLO3	Bi-level (comparator) output 3	Unassigned use; GPIO input	PB12	-
BLO4	Bi-level (comparator) output 4	Unassigned use; GPIO input	PB13	-
BLO5	Bi-level (comparator) output 5	Unassigned use; GPIO input	PB8	-
BLO6	Bi-level (comparator) output 6	Unassigned use; GPIO input	PB11	-
-	-	GPIO output - LED drive 1. See Table 2	PB15	-
-	-	GPIO output - LED drive 2. See Table 2	PB16	-

Table 2. LED Behavior

PB15	PB16	Green LED	Red LED	Motor Status
0	0	-	-	Stopped
0	1	-	Lit	Reverse motion
1	0	Lit	-	Forward motion
1	1	-	-	Stopped

1.5 LX7720DB Link Configuration

- Safe Mode Enable must be set (SM_EN=high) on the LX7720DB by leaving jumper J39 unlinked
- Simultaneous Conduction Protection must be set (SCP=high) on the LX7720DB by linking jumper J38 pins 1 to 2
- RESET signal must be routed to J20 on the LX7720DB by linking jumper J40 pins 2 to 3

1.6 Firmware Repository

https://github.com/Microchip-MPLAB-Harmony/motor_control/tree/master/apps/pmsm_foc_encoder_lx7720_sam_rh71_ek

1.7 Firmware Notes

The notes in this section below are taken from the `readme.md` documentation on [github](#).

Algorithm and current measurement

The control algorithm is the same as in the PMSM using an Encoder based Field Oriented Control (FOC) in the SAME70 microcontroller example

An additional algorithm is used to get the currents on phase A and B from the LX7720. A decimation filter is used to convert the sigma delta modulators output from LX7720.

Current conversion with decimation filter

The second order sigma delta modulator output of the LX7720 is a noise shaped signal where low frequency noise is pushed toward the high frequencies.

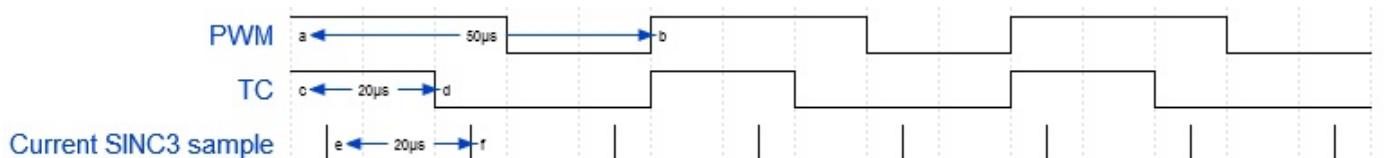
The SAMRH71 provide a 25MHz clock to the LX7720 modulator which in turn generates modulated signals that can be sampled by the SAMRH71.

The sampling is done with one timer counter per motor phase (A and B). The timer counters use two channels clocked at 50MHz. For each channel we use the "Burst signal" selection to have respectively XC0 (TCLK3) or (TCLK4) XC1 ANDed with the counting clock. The channel 0 of the same timer is used as reference to trigger a periodic interrupt for sampling, here every 4μs. This first sampling act as first SINC1 filter with OSR1=50.

A digital third order CIC filter (also known as SINC3) is used to do anti-aliasing filtering and decimate to the desired data-rate. This filter is applied on every SINC1 samples (OSR2=5). With this configuration we get SINC3 samples every 20μs which corresponds to 2.5 samples per PWM periods.

The final calculation for phases A and B currents is performed in the FOC control interrupt routine. The currents are calculated with a weighted average on the last 4 samples.

The FOC control loop is executed in an interrupt routine generated by a timer counter. This counter starts when the PWM event signal is raised. Then the interrupt is triggered after 20μs using the timer compare mode. This ensures that we have at least one current SINC3 sample calculated before the weight average calculation.



1.8 Hurst DMA0204024B101 Motor Connections

Table 3. Connections for Hurst Motor/Encoder to LX7720DB

Hurst Motor Connection	Wire Color	LX7720DB Connector	LX7720DB Signal
Motor winding phase A	white	J9 pin 1	Phase A
Motor winding phase B	black	J9 pin 2	Phase B
Motor winding phase C	red	J9 pin 3	Phase C
Encoder VDD	red	J15 pin 1	VCC (+3.3V)
Encoder GND	black	J15 pin 2	GND
Encoder Output A	white	J15 pin 3	BLI1
Encoder Output A	blue	J15 pin 4	BLI2

2 Schematic, PCB, and Ribbon Cable

The schematic is shown in Figure 8 on page 7. The PCB is built using a 2-sided flexible substrate to allow relative height differences between the LX7720DB and the SAMRH71F20-EK. The switch board is included in the layout, and is cut out. A drill hole in the two corners simplifies separation at the corners.

Figure 5 shows the PCB top and bottom foil patterns, looking through the board. Figure 6 on page 6 provides the bottom view with component identification.

The Gerber files and schematic/PCB source files for Altium or Protel are included as an attachment in this PDF. Save the attachment as SAMRH71 to LX7720 Flexi v2A.txt. Rename the file from .txt to .zip, and extract the files.

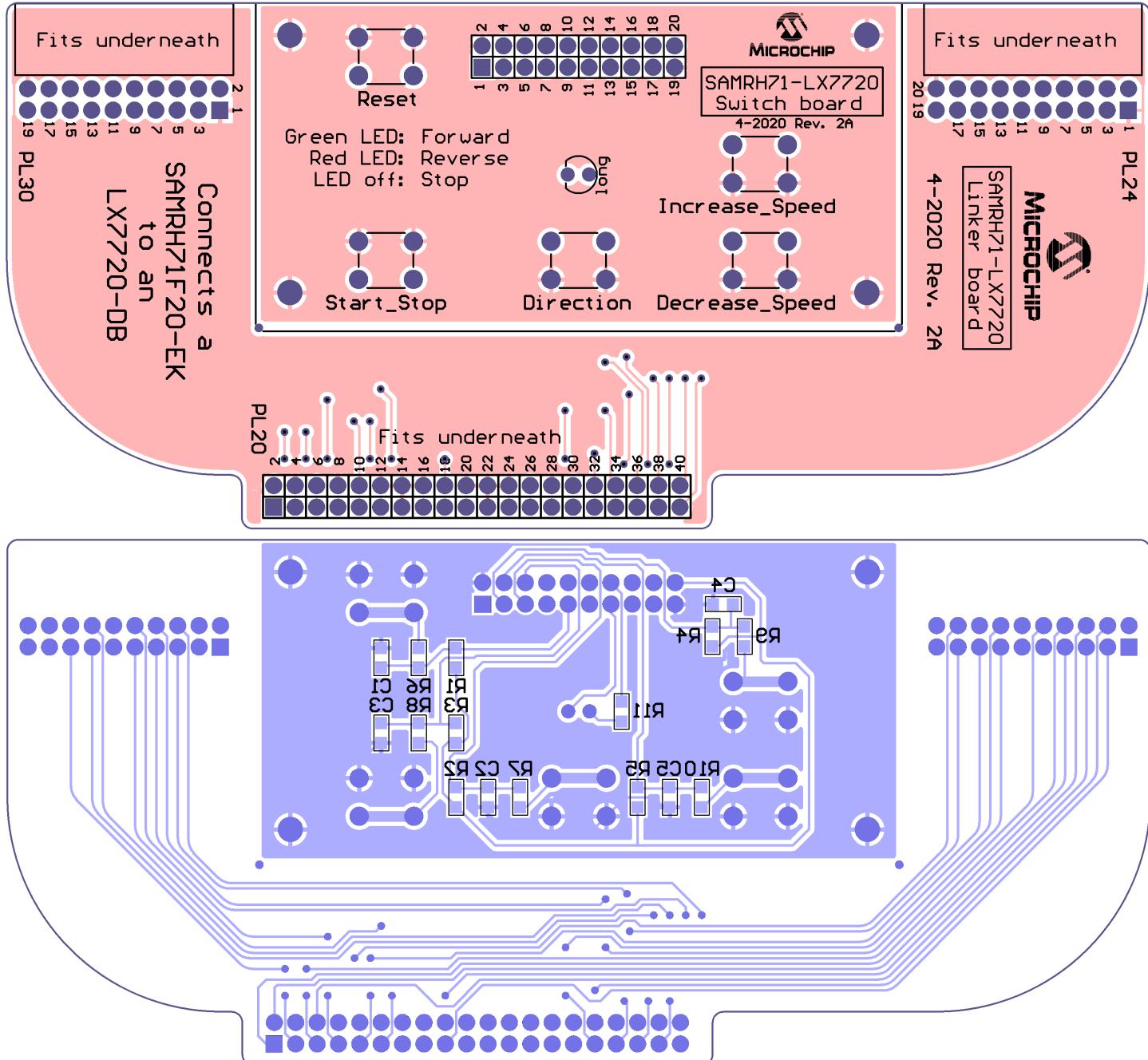


Figure 5. Combination Flexible PCB Layout Top Views

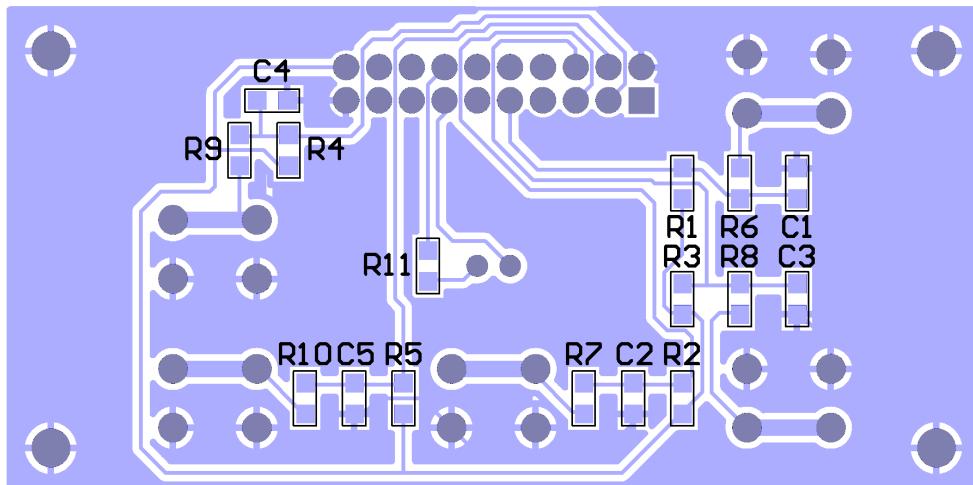


Figure 6. Switch PCB Bottom View

2.1 Ribbon Cable

A 20 way ribbon cable joins the 2x10way 0.1" shrouded pin header PL25 on the switch board to the 2x10way 0.1" open pin header J25 on the SAMRH71EVB board. The construction of the ribbon cable and IDC socket fitment at each end is shown in Figure 7 below. The ribbon length is unconstrained.

The IDC sockets (such as Assmann AWP 20-7240-T) have polarizing bumps, to locate in a slot in a mating housing. The switch board PL25 socket housing contains such a locating slot, so the cable fits only one way. SAMRH71EVB J25 is not polarized. Plug the cable into J25 with the IDC connector key facing down. The ribbon cable direction will be away from the top of the boards, as shown in Figure 1 on page 1.

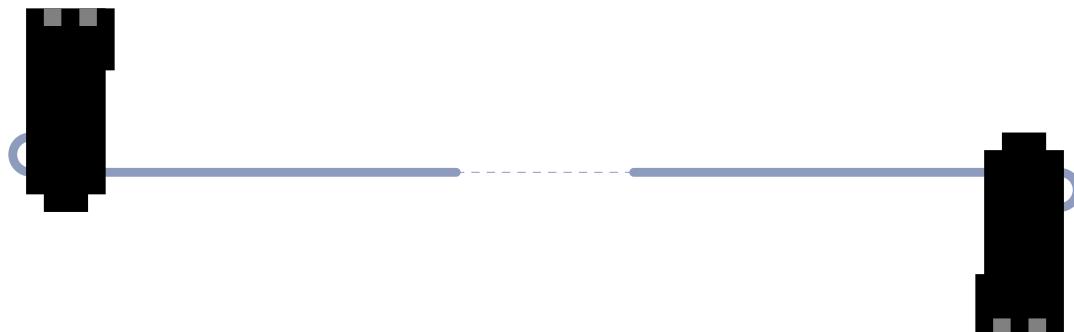


Figure 7. Ribbon Cable Construction

2.2 Parts List

The parts list for the PCB components is shown below in Table 4.

Table 4. Bill of Materials

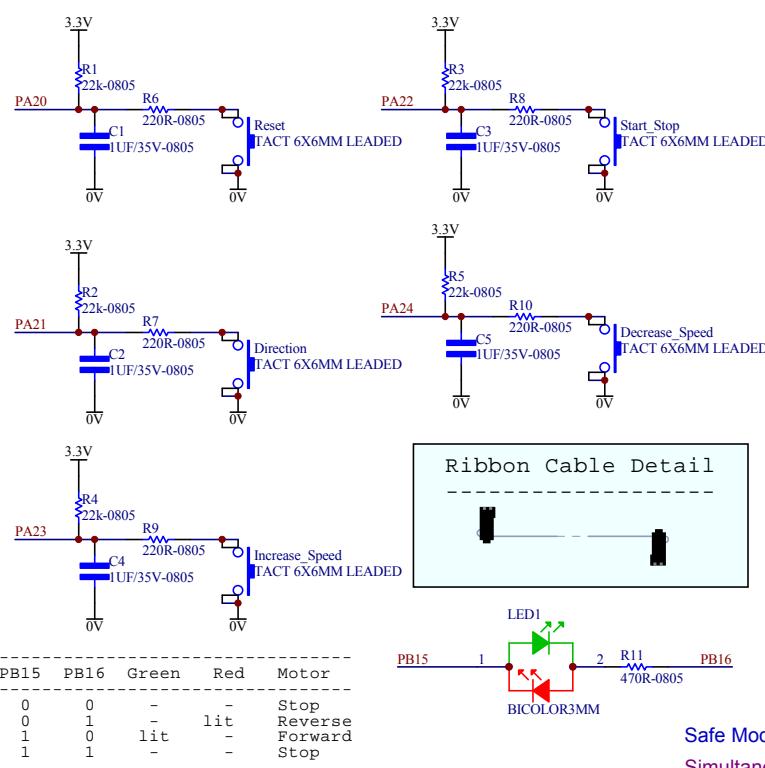
Designator	Quantity	Part Type
C1, C2, C3, C4, C5	5	1μF/10V X7R 0805 ±10%
LED1	1	LED 3mm Kingbright WP937EGW green-red
PL20	1	Connector 2 row 20 column socket header 0.1", Sullins SFH11-PBPC-D20-ST-BK
PL25	1	Connector 2 row 10 column right angle pin header 0.1", Assmann AWHW 20A-0202-T
PL24, PL30	2	Connector 2 row 10 column right angle socket header 0.1", Sullins PPPC102LJBN-RC
R1, R2, R3, R4, R5	5	Resistor 22kΩ 0805 1% 125mW
R6, R7, R8, R9, R10	5	Resistor 220Ω 0805 1% 125mW
R11	1	Resistor 470Ω 0805 1% 125mW
Start_Stop, Decrease_Speed, Increase_Speed, Direction, Reset	5	Switch tactile 6mm x 6mm body leaded, E-Switch TL1105BF250Q

Fault Handling and Reset

PR_FAULT, OC_FAULT, OTW_FAULT outputs are routed to SAMRH GPI PA8, PA9, PC9 on this board for monitoring.

SAMRH monitors the Reset switch on the switch board which connects to GPI PA20 on J25/PL25.

If the Reset switch is pressed momentarily, and there is a fault to clear, then SAMRH pulses RESET high with GPO PC10 to clear the LX7720 fault latch.



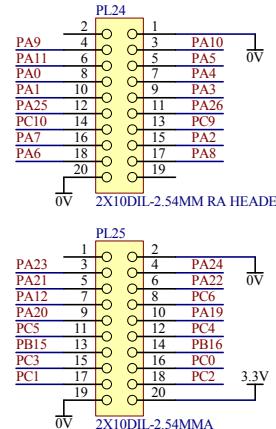
Ribbon cable joins switch board PL25 to SMARH71EVB J25

Switch board PL25 socket is polarized, so cable fits only one way

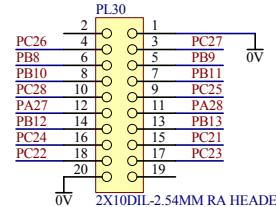
SMARH71EVB J25 is not polarized. Fit cable with IDC connector key facing down

NB: Green cathode terminal 2 is longer lead, sometimes also a flat on body

NB: PL24, PL25, PL30 connections are mirrored (odd pins <=> even pins)
because these right angle connectors are actually mounted underneath



J29 not used



Safe Mode Enable must be set (SM_EN=high) on LX7720 DB by leaving jumper J39 unlinked

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RESET signal must be routed to J20 on LX7720 DB by linking jumper J40 pins 2 to 3



LX7720DB to SAMRH71EVB

Size Letter	Number	Revision
Date:	20-Apr-2020	2
File:	C:\LX7720 to SAMRH71 v2.ddb	Sheet 1 of 1 Drawn By:

Figure 8. Schematic

3 Change Log

Date	Issue	Part Type
2020-04-21	1	First release
2020-04-29	1A	Added firmware repository link. Updated switch PCB with bigger SMC pads for easier assembly
2020-06-12	2	Updated firmware repository link and readme.md text



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