MICROCHIP


# Getting Started With the PolarFire™ SoC FPGA

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# First Thursday's

**May 2 - Webinar 1: Discover Renode for PolarFire™ SoC Design and Debug**

**June 6 - Webinar 2: How to Get Started with Renode for PolarFire SoC**

**July 4 - Webinar 3: Learn to Debug a Bare-Metal PolarFire SoC Application with Renode**

**Aug. 1 - Webinar 4: Tips and Tricks for Even Easier PolarFire SoC Debug with Renode**

**Sept. 5 - Webinar 5: Add and Debug PolarFire SoC Peripherals with Renode**

**Oct. 3 - Webinar 6: Intro to PolarFire SoC MSS Configuration and Software Flow**


# PolarFire SoC Introduction

## Session 1: Discover Renode for Design and Debug

# Enabling Purpose-Built, Real-Time Low Power Systems

Safety Critical Systems

Imaging and Machine Learning

Collaborative Robots

Industrial IoT

Secure Communications and Portable Embedded Systems

Smart Weapons, Drones and UAVs

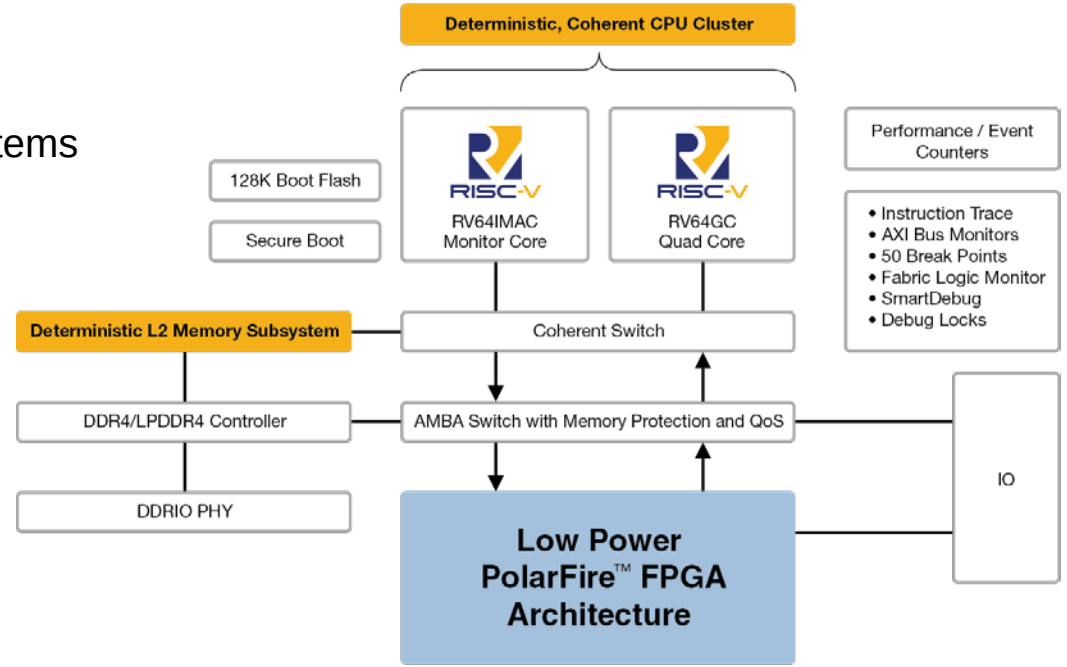
# PolarFire SoC Summary

- **Award Winning PolarFire FPGA Features**
  - 30 – 50 percent lower power
  - Defense grade security
  - Exceptional reliability
  - Smallest form factors – 11x11, 16x16, 19x19


- **Hardened RISC-V Microprocessor Subsystem**
  - Linux® and real time in a deterministic, coherent CPU cluster
  - 30 – 50 percent lower power
  - Defense grade secure boot
  - Spectre and Meltdown immune
  - SECDED on all memories

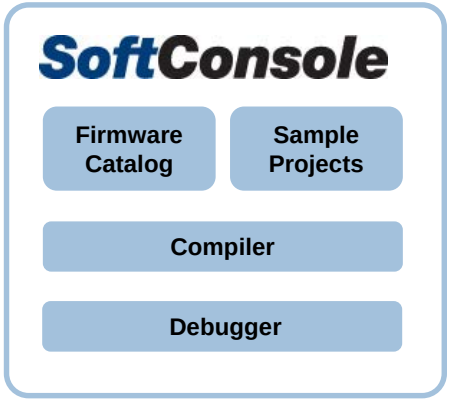
# RISC-V Enabled Innovation Platform

- **Freedom to Innovate in:**
  - Linux and real-time
  - Thermal and power constrained systems
  - Securely connected IoT systems
  - High-rel safety critical systems



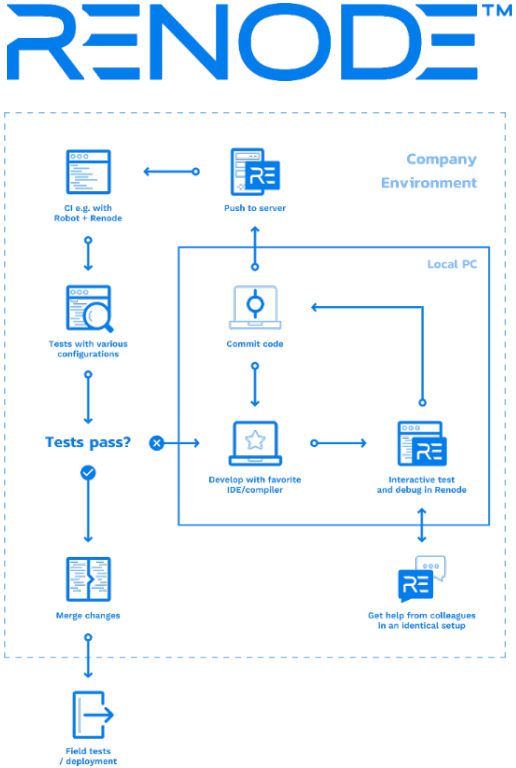

PolarFire SoC Architecture

# Freedom to Start Software Development




GDB

Eclipse IDE Design Flow



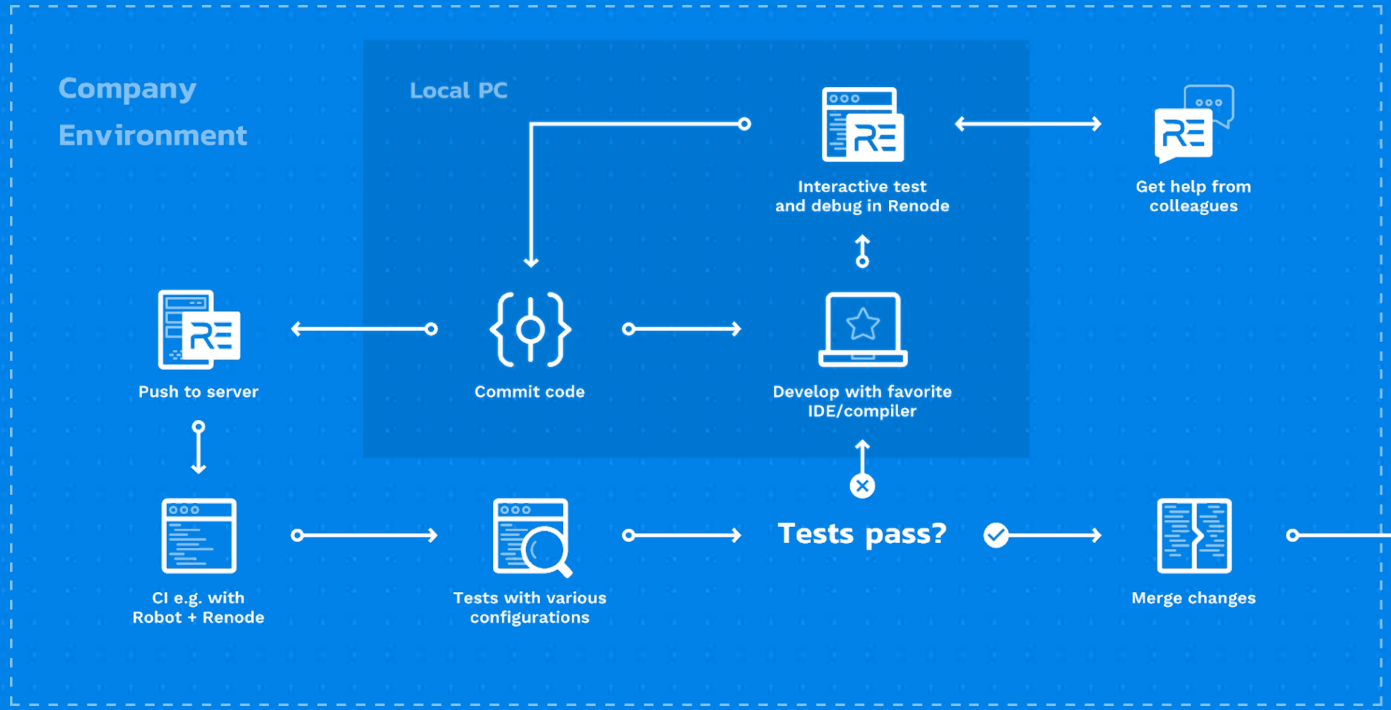

- Free rapid software development and debug capabilities without hardware
- Complete PolarFire SoC processor subsystem model
- Available now

antmicro

# Introduction to Antmicro

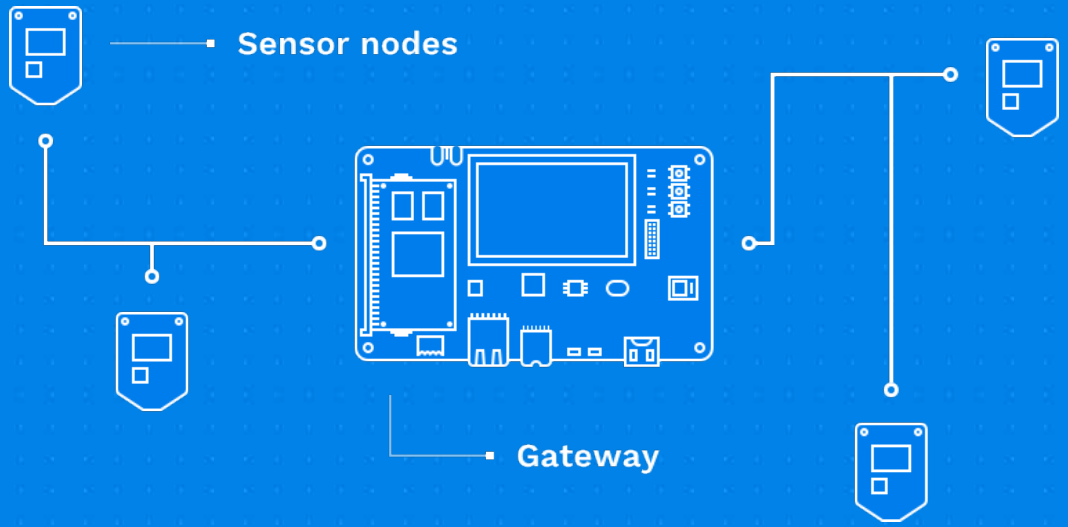
- **Mi-V Ecosystem Partner**
  - Embedded systems design and creation
  - Open source software, tools and hardware


# Continuous Integration Based Development

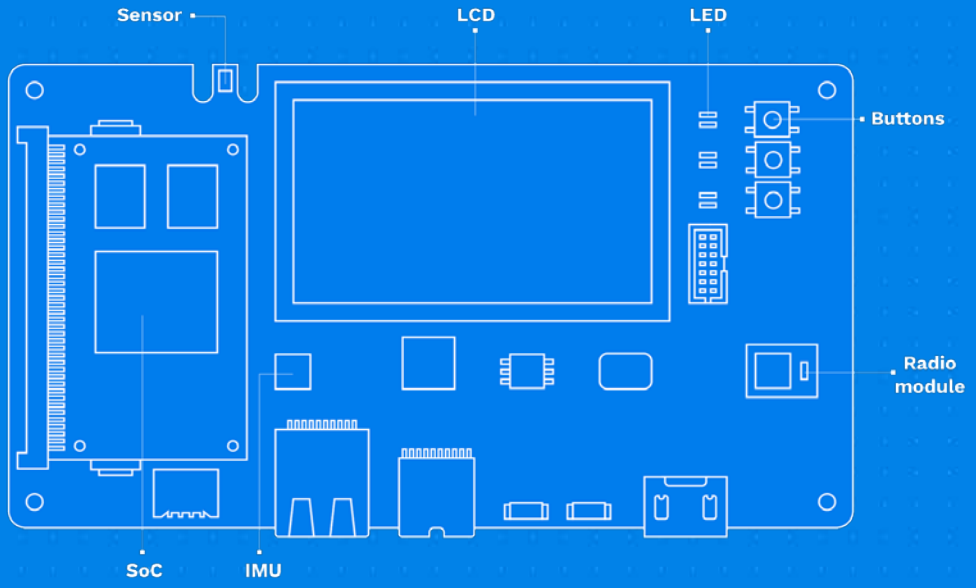



RENODE™ &
RISC-V®

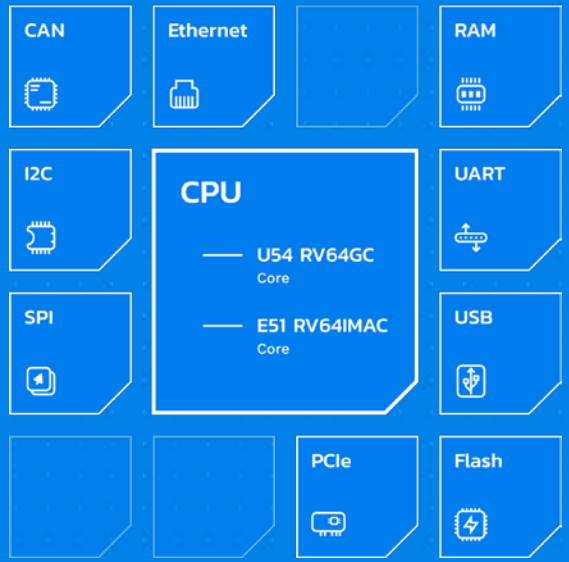
# Layer #3 : Complex System



# Layer #2 : The Device



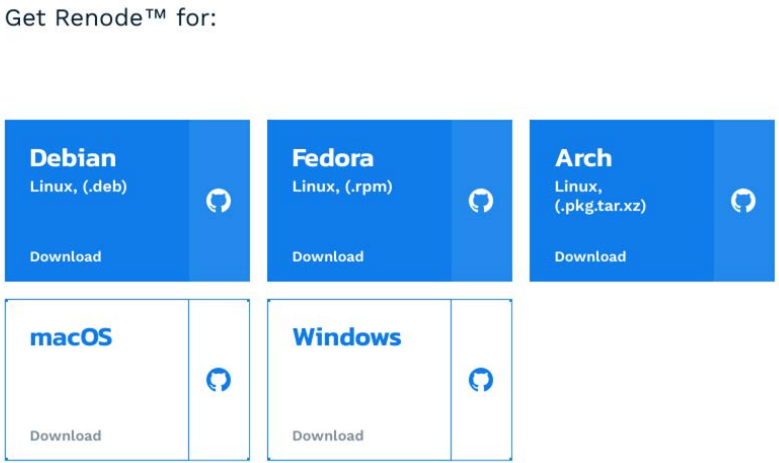
# Layer #1 : System-on-Chip

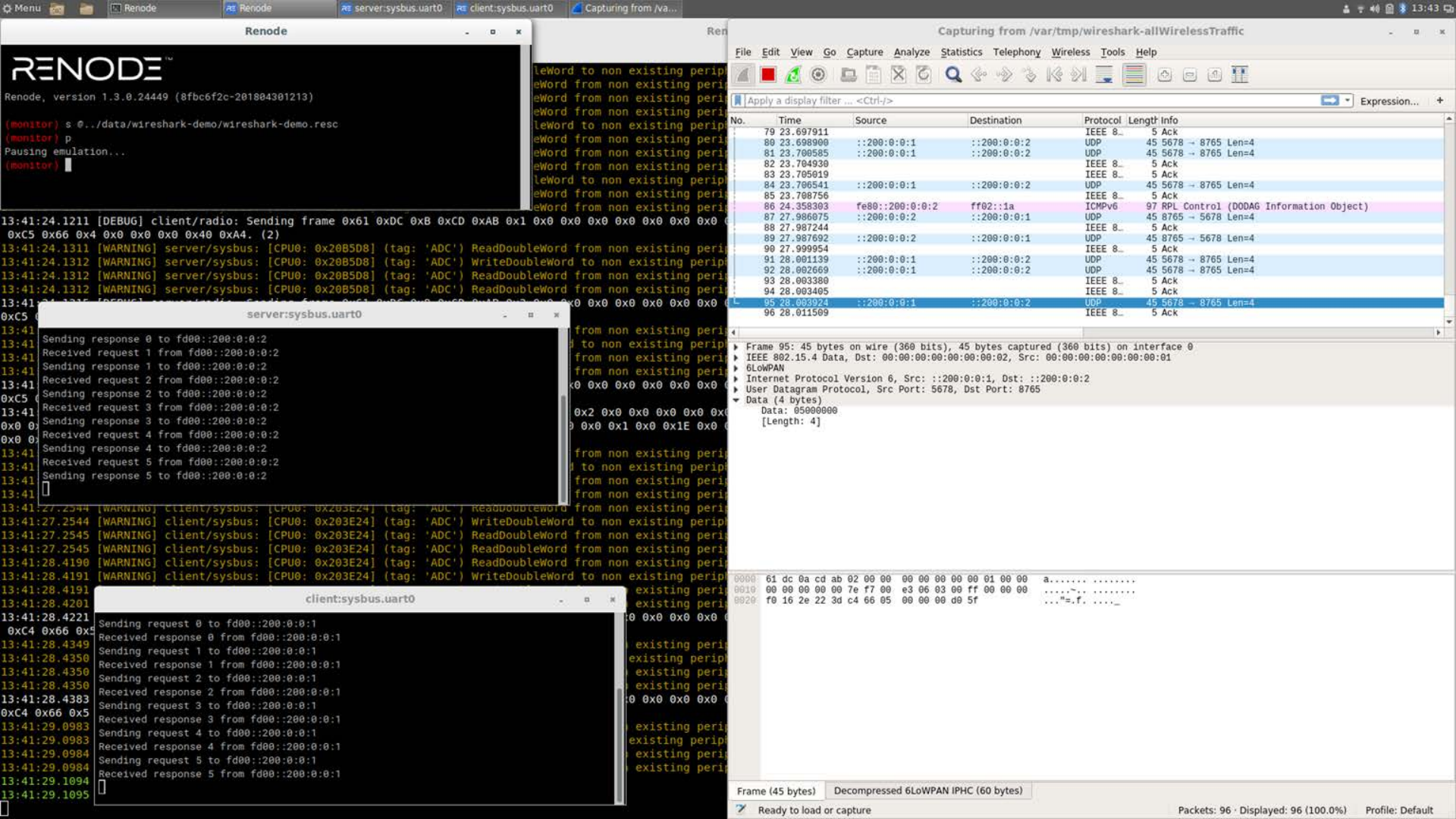


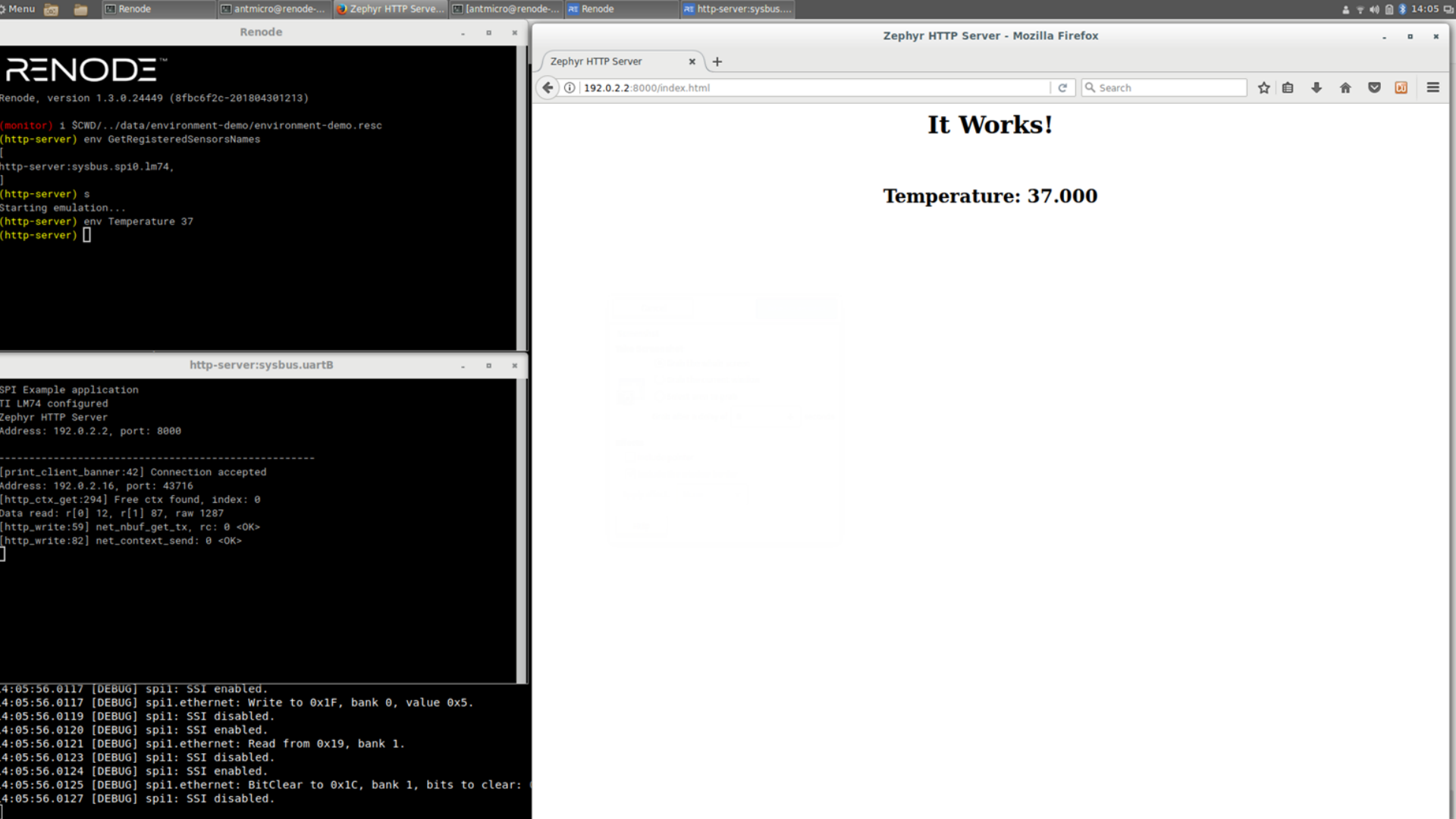
# PolarFire SoC FPGA Architecture
# “Enabling the Freedom to Innovate”

# Previously - a USD 3000 development platform

# Now - Renode, a free and open source framework that's in your PC (or server)




Menu
Renode
Renode
server:sysbus.uart0
client:sysbus.uart0
Capturing from /va...
13:43
Renode
RENODE
Renode, version 1.3.0.24449 (8fbc6f2c-201804301213)
(monitor) s @../data/wireshark-demo/wireshark-demo.resc
(monitor) p
Pausing emulation...
(monitor)
server:sysbus.uart0
Sending response 0 to fd00::200:0:0:2
Received request 1 from fd00::200:0:0:2
Sending response 1 to fd00::200:0:0:2
Received request 2 from fd00::200:0:0:2
Sending response 2 to fd00::200:0:0:2
Received request 3 from fd00::200:0:0:2
Sending response 3 to fd00::200:0:0:2
Received request 4 from fd00::200:0:0:2
Sending response 4 to fd00::200:0:0:2
Received request 5 from fd00::200:0:0:2
Sending response 5 to fd00::200:0:0:2
client:sysbus.uart0
Sending request 0 to fd00::200:0:0:1
Received response 0 from fd00::200:0:0:1
Sending request 1 to fd00::200:0:0:1
Received response 1 from fd00::200:0:0:1
Sending request 2 to fd00::200:0:0:1
Received response 2 from fd00::200:0:0:1
Sending request 3 to fd00::200:0:0:1
Received response 3 from fd00::200:0:0:1
Sending request 4 to fd00::200:0:0:1
Received response 4 from fd00::200:0:0:1
Sending request 5 to fd00::200:0:0:1
Received response 5 from fd00::200:0:0:1
Capturing from /var/tmp/wireshark-allWirelessTraffic
File Edit View Go Capture Analyze Statistics Telephony Wireless Tools Help
Apply a display filter ... <Ctrl-/>
Expression...
No. Time Source Destination Protocol Length Info
79 23.697911 IEEE 8... 5 Ack
80 23.698900 ::200:0:0:1 ::200:0:0:2 UDP 45 5678 → 8765 Len=4
81 23.700585 ::200:0:0:1 ::200:0:0:2 UDP 45 5678 → 8765 Len=4
82 23.704930 IEEE 8... 5 Ack
83 23.705019 IEEE 8... 5 Ack
84 23.706541 ::200:0:0:1 ::200:0:0:2 UDP 45 5678 → 8765 Len=4
85 23.708756 IEEE 8... 5 Ack
86 24.358303 fe80::200:0:0:2 ff02::1a ICMPv6 97 RPL Control (DODAG Information Object)
87 27.986075 ::200:0:0:2 ::200:0:0:1 UDP 45 8765 → 5678 Len=4
88 27.987244 IEEE 8... 5 Ack
89 27.987692 ::200:0:0:2 ::200:0:0:1 UDP 45 8765 → 5678 Len=4
90 27.999954 IEEE 8... 5 Ack
91 28.001139 ::200:0:0:1 ::200:0:0:2 UDP 45 5678 → 8765 Len=4
92 28.002669 ::200:0:0:1 ::200:0:0:2 UDP 45 5678 → 8765 Len=4
93 28.003380 IEEE 8... 5 Ack
94 28.003405 IEEE 8... 5 Ack
95 28.003924 ::200:0:0:1 ::200:0:0:2 UDP 45 5678 → 8765 Len=4
96 28.011509 IEEE 8... 5 Ack
Frame 95: 45 bytes on wire (360 bits), 45 bytes captured (360 bits) on interface 0
IEEE 802.15.4 Data, Dst: 00:00:00:00:00:00:00:02, Src: 00:00:00:00:00:00:00:01
6LoWPAN
Internet Protocol Version 6, Src: ::200:0:0:1, Dst: ::200:0:0:2
User Datagram Protocol, Src Port: 5678, Dst Port: 8765
Data (4 bytes)
Data: 05000000
[Length: 4]
0000 61 dc 0a cd ab 02 00 00 00 00 00 00 00 01 00 00 a.......
0010 00 00 00 00 00 7e f7 00 e3 06 03 00 ff 00 00 00 .....~..
0020 f0 16 2e 22 3d c4 66 05 00 00 00 d0 5f ...".=.f. ....
Frame (45 bytes)
Decompressed 6LoWPAN IPHC (60 bytes)
Ready to load or capture
Packets: 96 · Displayed: 96 (100.0%)
Profile: Default

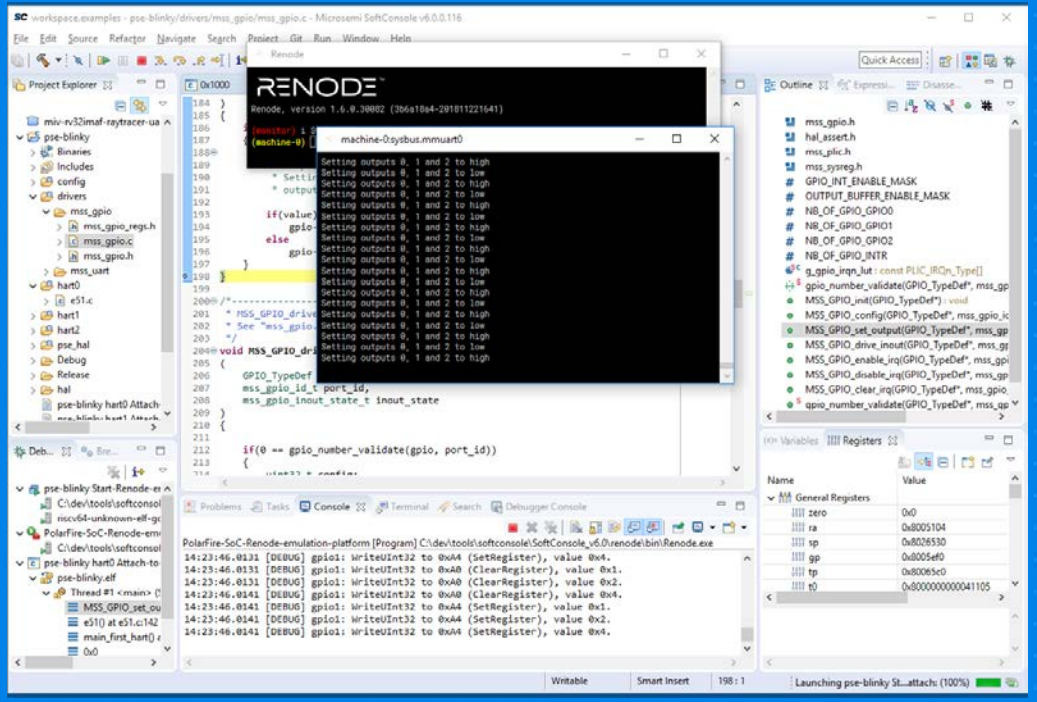

Menu
Renode
antmicro@renode-...
Zephyr HTTP Serve...
[antmicro@renode-...
Renode
http-server:sysbus....
14:05
Renode
RENODE
Renode, version 1.3.0.24449 (8fbc6f2c-201804301213)
(monitor) i $CWD/../data/environment-demo/environment-demo.resc
(http-server) env GetRegisteredSensorsNames
[
http-server:sysbus.spi0.lm74,
]
(http-server) s
Starting emulation...
(http-server) env Temperature 37
(http-server)
http-server:sysbus.uartB
SPI Example application
TI LM74 configured
Zephyr HTTP Server
Address: 192.0.2.2, port: 8000
[print_client_banner:42] Connection accepted
Address: 192.0.2.16, port: 43716
[http_ctx_get:294] Free ctx found, index: 0
Data read: r[0] 12, r[1] 87, raw 1287
[http_write:59] net_nbuf_get_tx, rc: 0 <OK>
[http_write:82] net_context_send: 0 <OK>
4:05:56.0117 [DEBUG] spi1: SSI enabled.
4:05:56.0117 [DEBUG] spi1.ethernet: Write to 0x1F, bank 0, value 0x5.
4:05:56.0119 [DEBUG] spi1: SSI disabled.
4:05:56.0120 [DEBUG] spi1: SSI enabled.
4:05:56.0121 [DEBUG] spi1.ethernet: Read from 0x19, bank 1.
4:05:56.0123 [DEBUG] spi1: SSI disabled.
4:05:56.0124 [DEBUG] spi1: SSI enabled.
4:05:56.0125 [DEBUG] spi1.ethernet: BitClear to 0x1C, bank 1, bits to clear:
4:05:56.0127 [DEBUG] spi1: SSI disabled.
Zephyr HTTP Server - Mozilla Firefox
Zephyr HTTP Server
192.0.2.2:8000/index.html
Search
It Works!
Temperature: 37.000

# PFSoC Support Highlights

- Interfaces for connection with multiple external elements
- Helps explore the flexibility of Renode

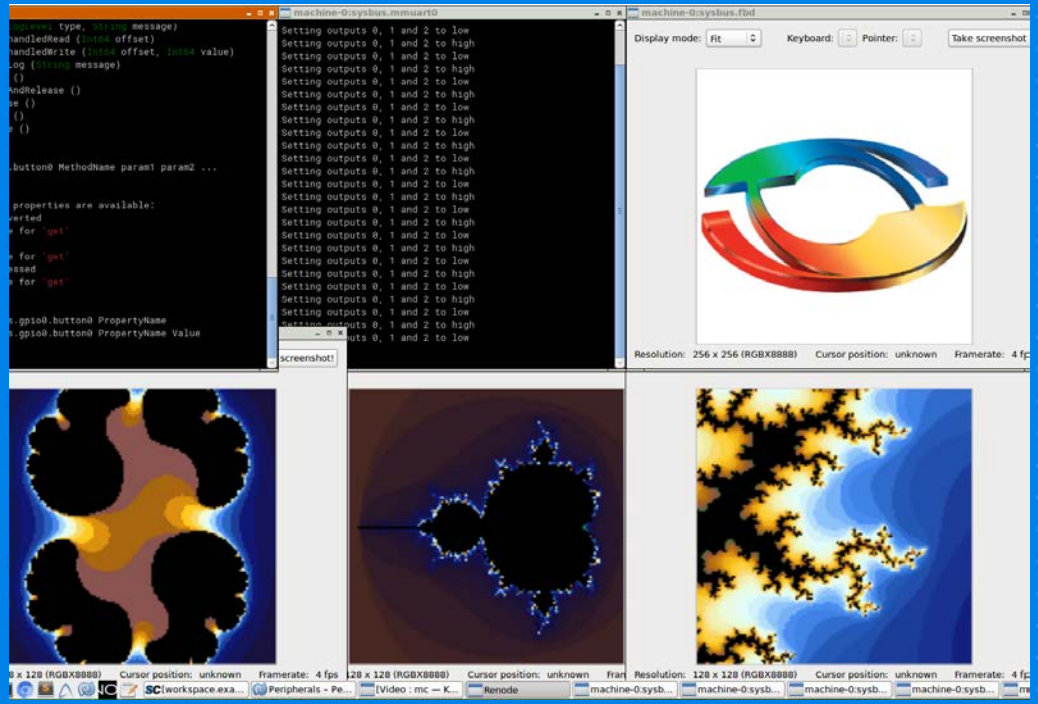
# SoftConsole Integration

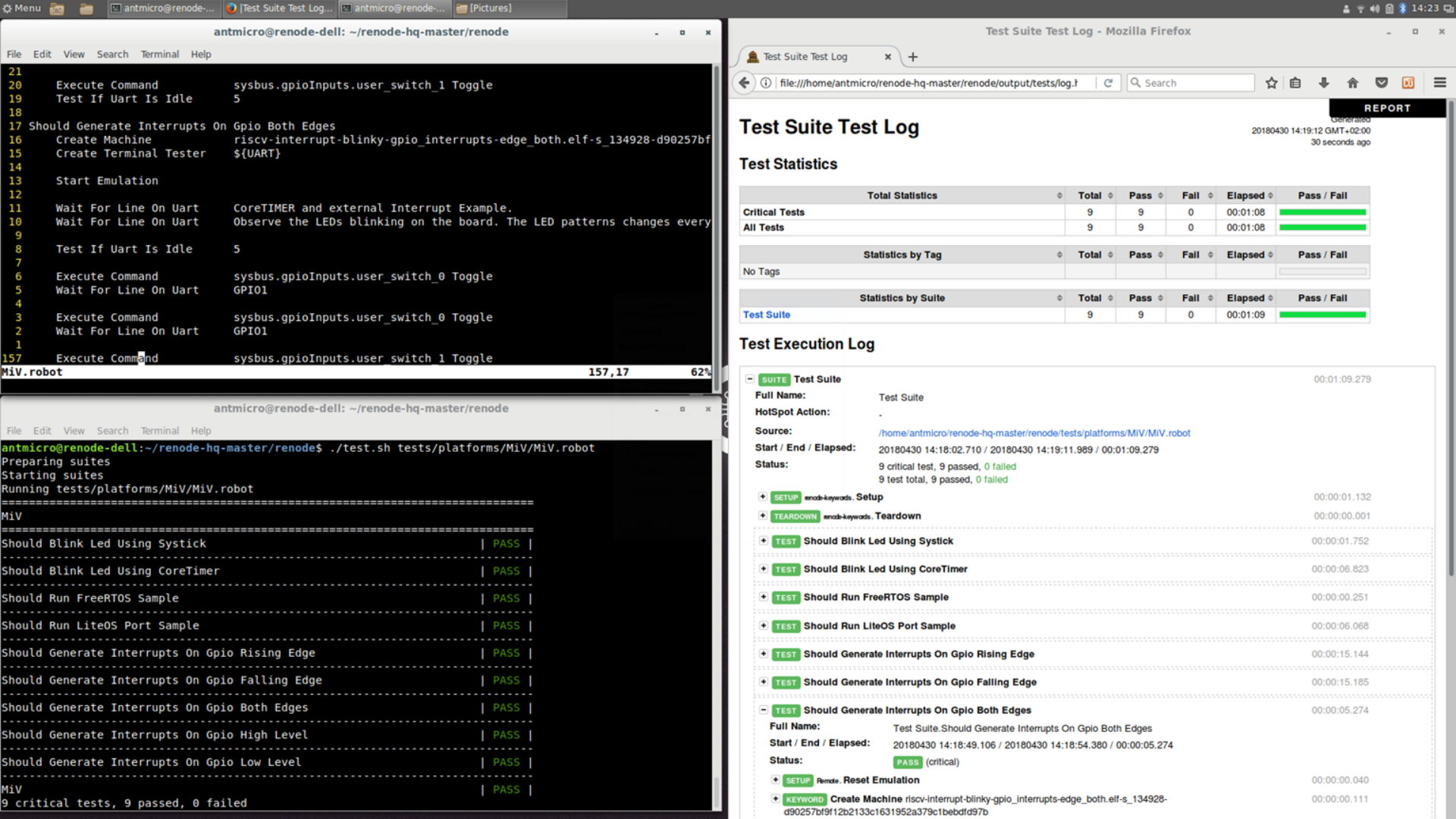
- Standard IDE, comes bundled
- Linux and Windows®
- Examine the entire system as you're developing code
- New and exciting abilities



# SoftConsole Integration

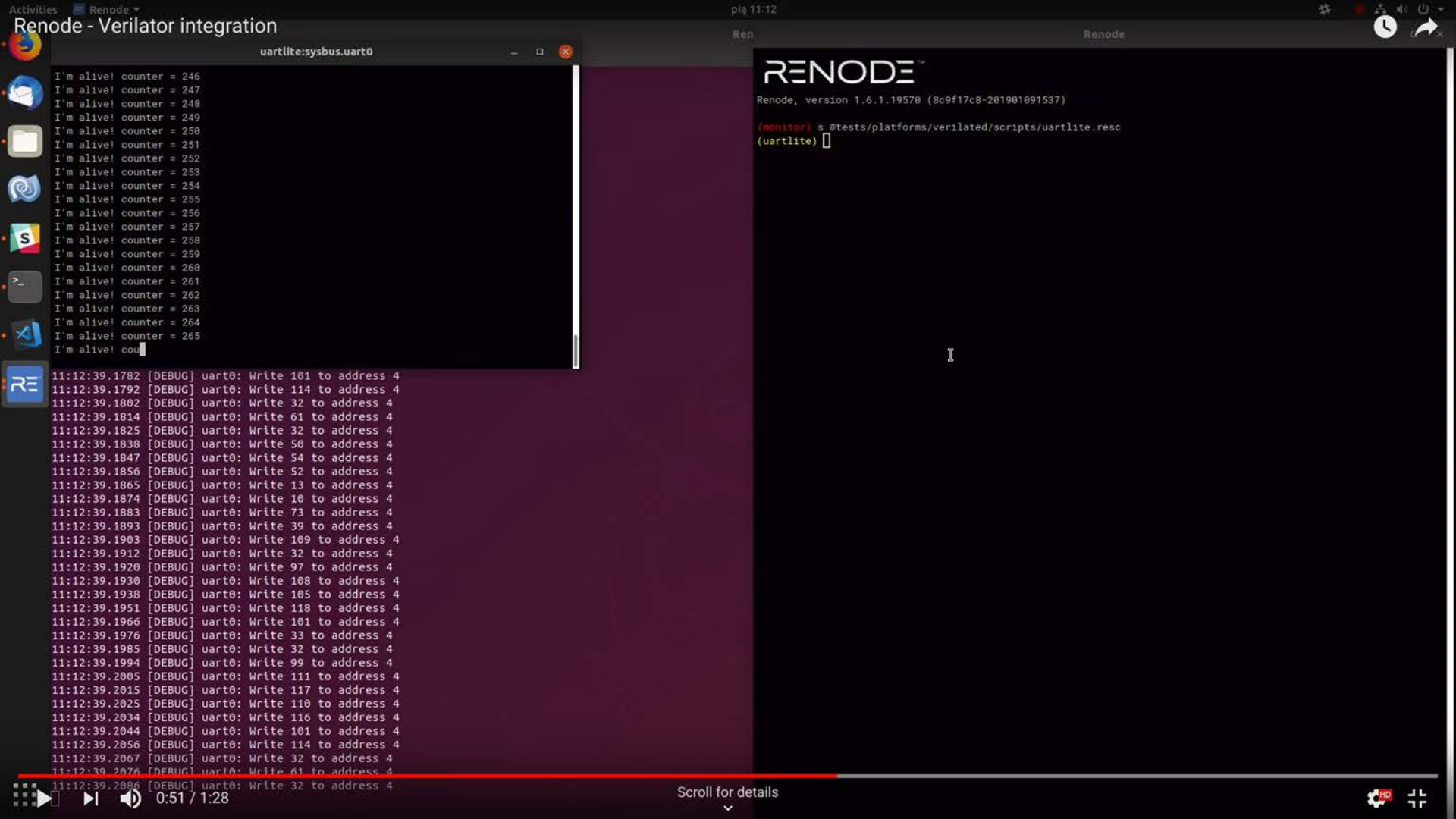
- Renode is extremely extendible
- Debug, tracing, visualization - we have all the data




antmicro@renode-dell: ~/renode-hq-master/renode
File Edit View Search Terminal Help
21
20 Execute Command sysbus.gpioInputs.user_switch_1 Toggle
19 Test If Uart Is Idle 5
18
17 Should Generate Interrupts On Gpio Both Edges
16 Create Machine riscv-interrupt-blinky-gpio_interrupts-edge_both.elf-s_134928-d90257bf
15 Create Terminal Tester ${UART}
14
13 Start Emulation
12
11 Wait For Line On Uart CoreTIMER and external Interrupt Example.
10 Wait For Line On Uart Observe the LEDs blinking on the board. The LED patterns changes every
9
8 Test If Uart Is Idle 5
7
6 Execute Command sysbus.gpioInputs.user_switch_0 Toggle
5 Wait For Line On Uart GPIO1
4
3 Execute Command sysbus.gpioInputs.user_switch_0 Toggle
2 Wait For Line On Uart GPIO1
1
157 Execute Command sysbus.gpioInputs.user_switch_1 Toggle
MiV.robot 157,17 62%
antmicro@renode-dell: ~/renode-hq-master/renode
File Edit View Search Terminal Help
antmicro@renode-dell:~/renode-hq-master/renode$ ./test.sh tests/platforms/MiV/MiV.robot
Preparing suites
Starting suites
Running tests/platforms/MiV/MiV.robot
MiV
Should Blink Led Using Systick | PASS |
Should Blink Led Using CoreTimer | PASS |
Should Run FreeRTOS Sample | PASS |
Should Run LiteOS Port Sample | PASS |
Should Generate Interrupts On Gpio Rising Edge | PASS |
Should Generate Interrupts On Gpio Falling Edge | PASS |
Should Generate Interrupts On Gpio Both Edges | PASS |
Should Generate Interrupts On Gpio High Level | PASS |
Should Generate Interrupts On Gpio Low Level | PASS |
MiV | PASS |
9 critical tests, 9 passed, 0 failed
Test Suite Test Log - Mozilla Firefox
Test Suite Test Log
file:///home/antmicro/renode-hq-master/renode/output/tests/log.h
Search
REPORT
Test Suite Test Log
Generated
20180430 14:19:12 GMT+02:00
30 seconds ago
Test Statistics
Total Statistics Total Pass Fail Elapsed Pass / Fail
Critical Tests 9 9 0 00:01:08
All Tests 9 9 0 00:01:08
Statistics by Tag Total Pass Fail Elapsed Pass / Fail
No Tags
Statistics by Suite Total Pass Fail Elapsed Pass / Fail
Test Suite 9 9 0 00:01:09
Test Execution Log
SUITE Test Suite 00:01:09.279
Full Name: Test Suite
HotSpot Action: -
Source: /home/antmicro/renode-hq-master/renode/tests/platforms/MiV/MiV.robot
Start / End / Elapsed: 20180430 14:18:02.710 / 20180430 14:19:11.989 / 00:01:09.279
Status: 9 critical test, 9 passed, 0 failed
9 test total, 9 passed, 0 failed
SETUP renode-keywords . Setup 00:00:01.132
TEARDOWN renode-keywords . Teardown 00:00:00.001
TEST Should Blink Led Using Systick 00:00:01.752
TEST Should Blink Led Using CoreTimer 00:00:06.823
TEST Should Run FreeRTOS Sample 00:00:00.251
TEST Should Run LiteOS Port Sample 00:00:06.068
TEST Should Generate Interrupts On Gpio Rising Edge 00:00:15.144
TEST Should Generate Interrupts On Gpio Falling Edge 00:00:15.185
TEST Should Generate Interrupts On Gpio Both Edges 00:00:05.274
Full Name: Test Suite.Should Generate Interrupts On Gpio Both Edges
Start / End / Elapsed: 20180430 14:18:49.106 / 20180430 14:18:54.380 / 00:00:05.274
Status: PASS (critical)
SETUP Remote . Reset Emulation 00:00:00.040
KEYWORD Create Machine riscv-interrupt-blinky-gpio_interrupts-edge_both.elf-s_134928-d90257bf9f12b2133c1631952a379c1bebdfd97b 00:00:00.111

```
cpu: CPU.RiscV32 @ sysbus
    cpuType: "rv32g"
    privilegeArchitecture: PrivilegeArchitecture.Priv1_09
    clint: clint

plic: IRQControllers.PlatformLevelInterruptController @ sysbus 0x40000000
    [0-3] -> cpu@[8-11]
    numberOfSources: 31
    prioritiesEnabled : false

// Power/Reset/Clock/Interrupt
clint: IRQControllers.CoreLevelInterruptor  @ sysbus 0x44000000
    frequency: 66000000
    [0, 1] -> cpu@[3, 7]

ram: Memory.MappedMemory @ sysbus 0x60000000
    size: 0x06400000

uart0: Verilated.Uart @ sysbus <0x70000000, +0x100>
    filePath: "../../renode-verilator-integration/samples/uartlite/uartlite"
    frequency: 100000000
    limit: 10000
```

# Renode - Verilator integration




0:51 / 1:28

Scroll for details

# Summary

- PolarFire SoC for purpose-built, real-time, low power systems
- Get started today by downloading SoftConsole v6.0
- Use the Renode rapid development framework to build software including real, end-user applications
- Visit www.microsemi.com/mi-v for complete Renode webinar series details, and recordings
- See you June 6th on WebEx, June 12-14 @ RISC-V Workshop Zurich


# Thank You