Hello FPGA Libero Design User Guide

Introduction (Ask a Question)

Hello FPGA is a low cost, compact-sized, and a feature-rich FPGA kit based on the non-volatile, Flash-based, and low-power SmartFusion® 2 SoC FPGA (M2S010). SmartFusion 2 SoC FPGAs offer more resources in low density with a complete Microcontroller Subsystem (MSS) that includes a 166 MHz Arm® Cortex®-M3 processor with an Embedded Trace Macrocell (ETM) and Instruction Cache, embedded Flash, and extensive peripherals including CAN, TSE, and USB.

An ultra low-power Flash*Freeze feature of SmartFusion 2 SoC FPGAs allows the retention of design while maintaining the I/O state for low-power applications. A single pin interrupt puts the device in the Flash*Freeze mode and brings up these FPGAs to operational modes (within ~13 microseconds).

These FPGAs are ideal for general purpose functions such as Gigabit Ethernet or dual PCI Express control planes, bridging functions, input/output (I/O) expansion and conversion, video/image processing, system management and secure connectivity. These FPGAs are used by in Communications, Industrial, Medical, Defense, and Aviation markets.

The Hello FPGA kit is designed for FPGA beginners and enthusiasts. The Hello FPGA kit is ideal for developing control logic and data acquisition, image processing, signal processing, and artificial intelligence applications.

The kit supports the measurement of the live FPGA core power consumption while running the designs. The kit also allows you to freeze the design. The Hello FPGA kit includes a Microchip PIC32 MCU that is used to program the SmartFusion 2 SoC FPGA, monitor power, and general-purpose functions.

The Hello FPGA Kit demonstrates the following features of the SmartFusion 2 SoC FPGA:

- DSP functions: FIR Filter
- Parallel Processing and Complex functions: Artificial Intelligence (real time hand-written digit recognition)
- Low-Power: Shows power consumption in operational and Flash*Freeze modes
- Instant ON: Highlighting fast wake-up from the Flash*Freeze mode to Fully Functional mode

This user guide describes the following designs, which can be run on the kit:

1. Video Demo Design
2. Digit Recognition (AI) Demo Design
3. DSP FIR Filter Demo Design
4. Program and Debug

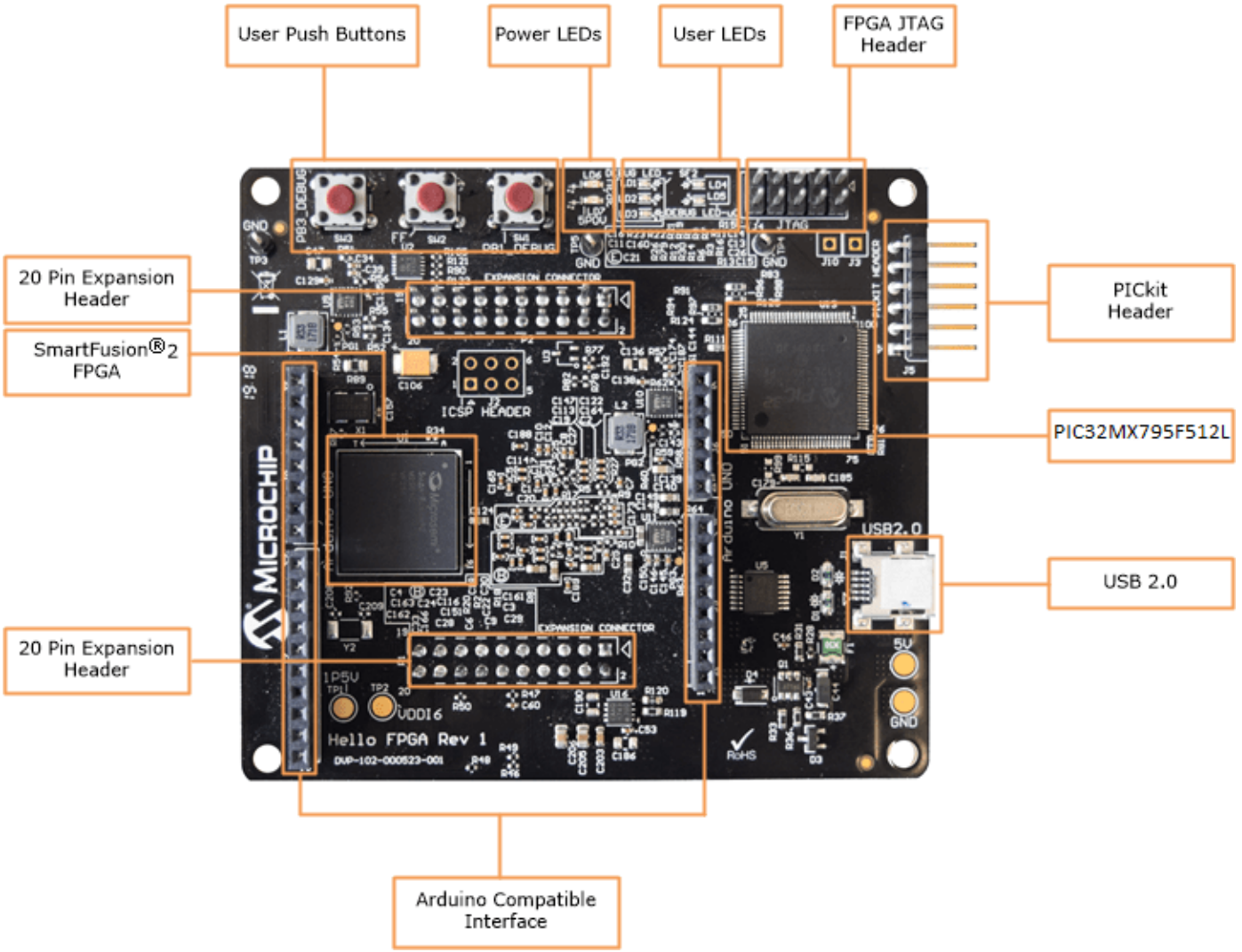
These designs are created using Microchip's Libero SoC Design Software. The software includes all of the necessary IPs required to build such application prototypes.

Important: These designs also include a user-friendly GUI application to test specific features functions. These demo designs include the Flash*Freeze feature for demonstration. You can monitor the power consumption when FPGA is in Operational and Flash*Freeze modes to evaluate the advantage of low-power.

The kit includes Arduino and Mikrobus connectors for flexibility for prototyping and expansion kits. This can be very useful as your knowledge of FPGA and the associated tools experience increases. The kit can work as a standalone unit or as an extension to existing Microchip kits.

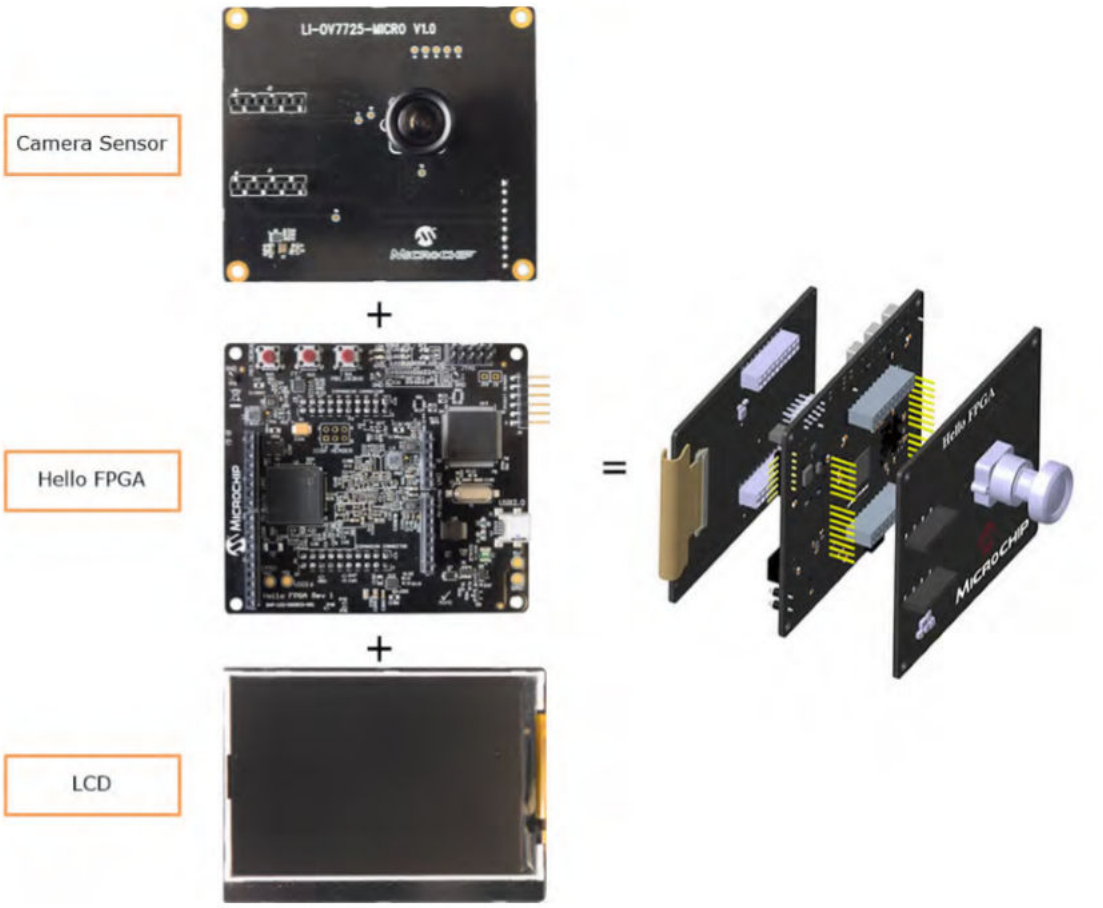
The following figure shows the Hello FPGA kit, that has the SmartFusion 2 FPGA and MCU (PIC32MX795F512L).

Figure 1. Hello FPGA Kit



The Hello FPGA kit includes the LCD board and the camera sensor. These boards can be connected to the Hello FPGA kit as shown in the following figure.

Figure 2. LCD and Camera Sensor Boards



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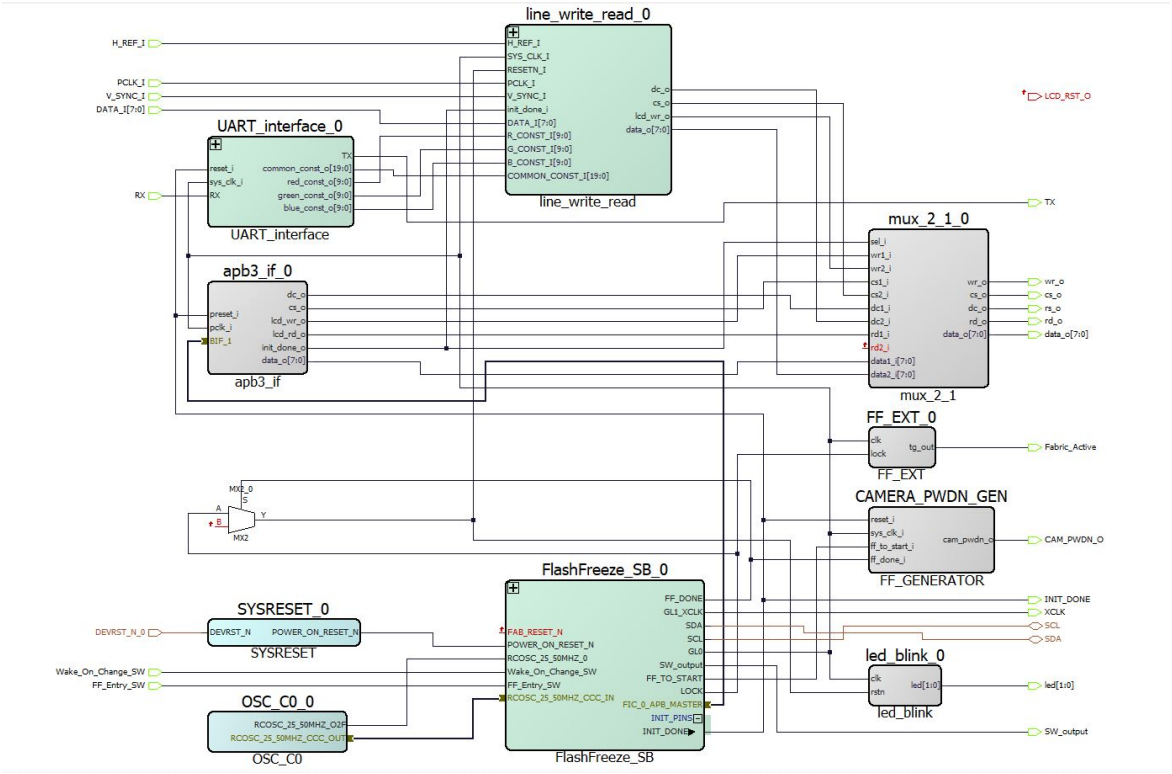
1. Video Demo Design (Ask a Question)

The following figure shows the top-level video demo design in Libero® SoC software.

Figure 1-1. Top-Level Hardware Implementation (Video Demo)



The video demo design interfaces the Camera Sensor OV7725 and LCD with the SmartFusion 2 SoC FPGA. The design also includes the Flash*Freeze feature.

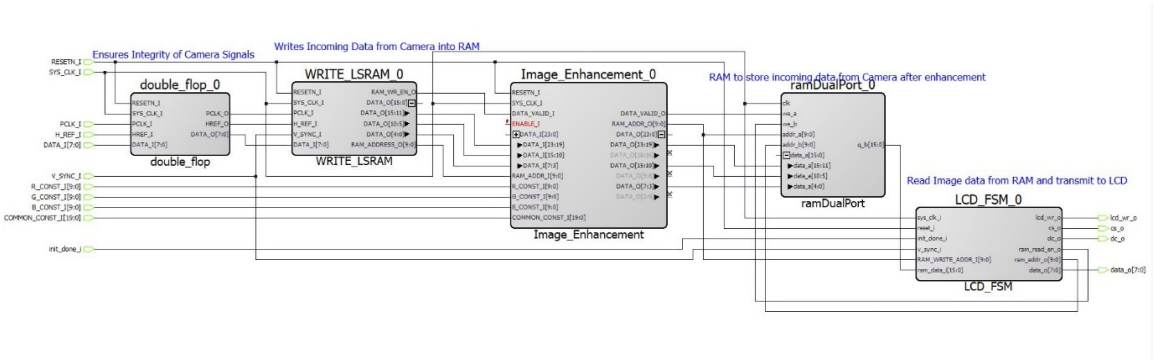
The top module contains the following modules:

1.1 Line_write_read Module (Ask a Question)

The Line_write_read module acquires the data from the OV7725 Camera sensor, performs image scaling as well as image enhancement, and sends the data to the LCD screen. The OV7725 camera has an array size of 640 x 480 and is configured to operate in RGB 565 format. The LCD ILI9488 has a display resolution of 480 x 320. The WRITE_LSRAM module down samples the 640 x 480 camera data to 480 x 320 LCD resolution. After down sampling the image, data goes through image enhancement that can be configured through UART. The Image Enhancement block writes the data into the

dual-port RAM. LCD_FSM reads the data from the dual-port RAM and sends it to the LCD display as per the LCD interface protocol. The following figure shows the components of the Line_read_write module.

Figure 1-2. Line_write_read Module in SmartDesign



The Line_write_read module contains the following components:

1.1.1 WRITE_LSRAM_0 (Ask a Question)

Signals from the Camera PLK_I, H_REF, and DATA_I(8) are transferred through the double flip-flop synchronizer circuit to ensure the integrity of these signals. Input data signal from the camera DATA_I is considered valid when the H_REF signal is high. Data from the camera is in the form of RGB 5:6:5 format and is split across two clock cycles. Down sampling from 640 pixels per horizontal line to 480 pixels per horizontal line is achieved by skipping a pixel for every four pixels. Down sampling from 480 lines to 320 lines is achieved by skipping one horizontal line for every three lines.

1.1.2 Image Enhancement (Ask a Question)

This module performs modification on the pixel output data from WRITE_LSRAM based on the user-controlled data provided by the UART block. User-controlled data includes contrast, brightness, and RGB color adjustment values.

1.1.3 LCD_FSM (Ask a Question)

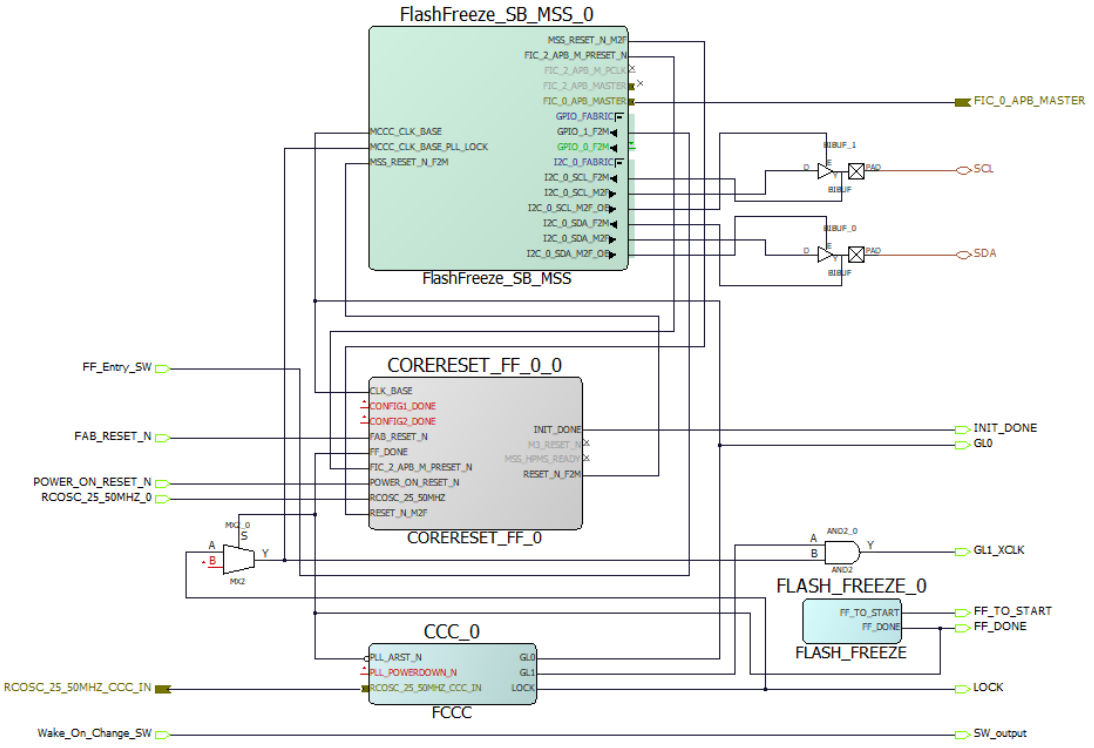
The LCD_FSM module reads data from the dual-port RAM and sends it to the LCD display. The module starts reading the dual-port RAM when the write address in WRITE_LSRAM reaches 160. The LCD_FSM module also resets the registers of the LCD based on the V_Sync signal of the camera, which indicates the start of new frame data. LCD_FSM provides data to the LCD based on the interface protocol.

1.2 FlashFreeze_SB Module (Ask a Question)

The FlashFreeze_SB_MSS module configures the MSS. The I^2C peripheral in MSS is used to configure camera registers. MSS is the APB initiator which is connected to the APB target (apb3_if) module to initialize LCD registers during start-up. The FlashFreeze_SB_MSS module provides the feature of low power flip-flop (FF) mode to the FPGA. The FF_Entry_SW signal provides the hardware interrupt for FF to MSS. When interrupt comes, MSS executes the instruction related to FF firmware through which FPGA goes into the Flash*Freeze mode. MSS is in an infinite loop when the FPGA fabric is

in the Flash*Freeze mode. The following figure shows the components of the FlashFreeze_SB_MSS module.

Figure 1-3. FlashFreeze_SB_MSS_0 Module

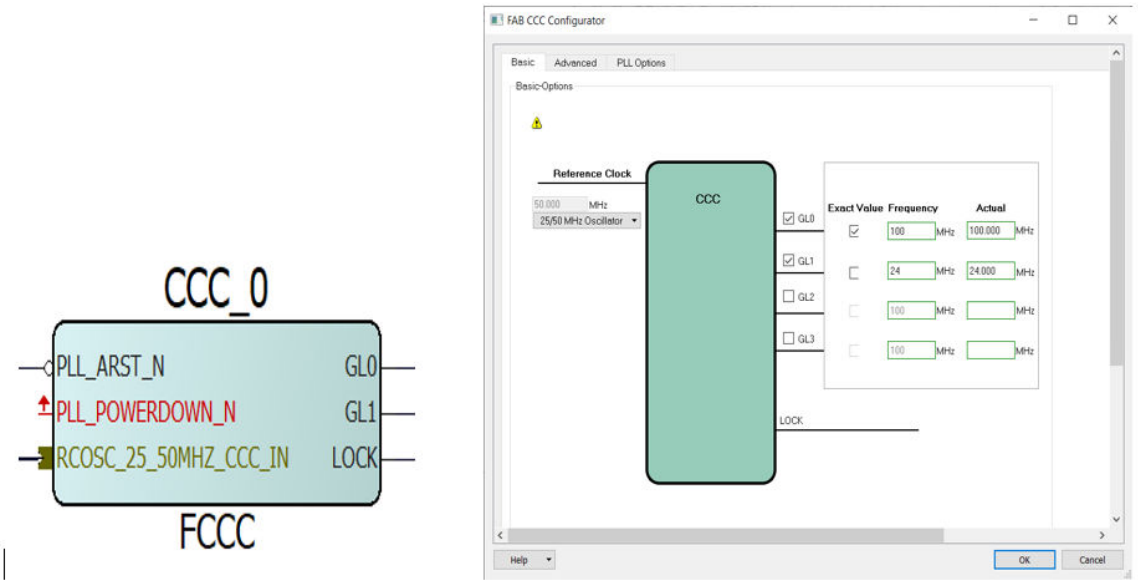


1.2.1 CCC IP (Ask a Question)

The CCC IP is available from the **Clock and Management** group in the Libero SoC IP catalog. The CCC IP acquires the 25/50 MHz clock from the on-chip oscillator IP and generates the GL0 clock of 100 MHz and GL1 of 24 MHz clock. All the modules inside FPGA work on GL0 clock.

The following figure shows the configuration of the CCC IP.

Figure 1-4. CCC IP Configuration

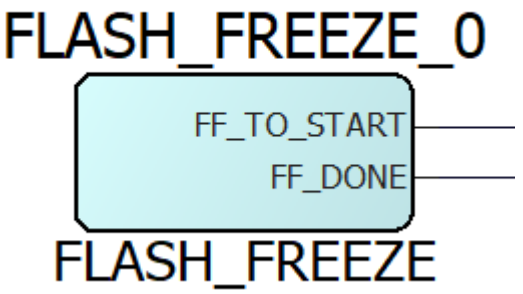


1.2.2 FLASH_FREEZE IP (Ask a Question)

The FLASH_FREEZE IP is available in Libero SoC > Catalog. The SmartFusion 2 SoC FPGA devices provide an ultra-low static power solution through Flash*Freeze technology. The Flash*Freeze mode entry retains all the Static Random Access Memory (SRAM) and registers information. The Flash*Freeze mode exit achieves rapid recovery to Active mode (approximately 13 µs).

The following figure shows the FLASH_FREEZE IP.

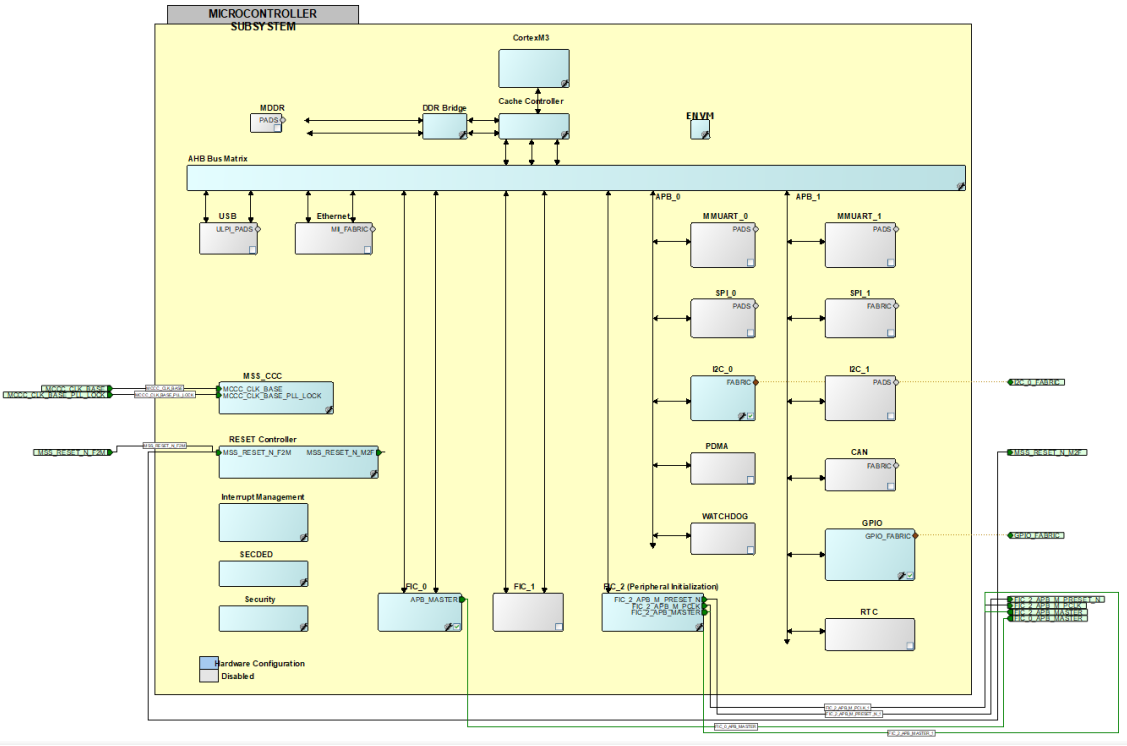
Figure 1-5. FLASH_FREEZE IP



1.2.3 MSS IP (Ask a Question)

The SmartFusion 2 Microcontroller Subsystem (MSS) IP is available under **Libero SoC** > **Catalog** > **Processors**. The MSS Component Configurator represents a graphical block diagram of the SmartFusion 2 Microcontroller Subsystem. Each of MSS sub-blocks can be enabled or disabled as per the application requirements. This design uses FIC_0 for APB interface and I2C_0 to enable camera configuration interface and GPIO to acquire an external signal.

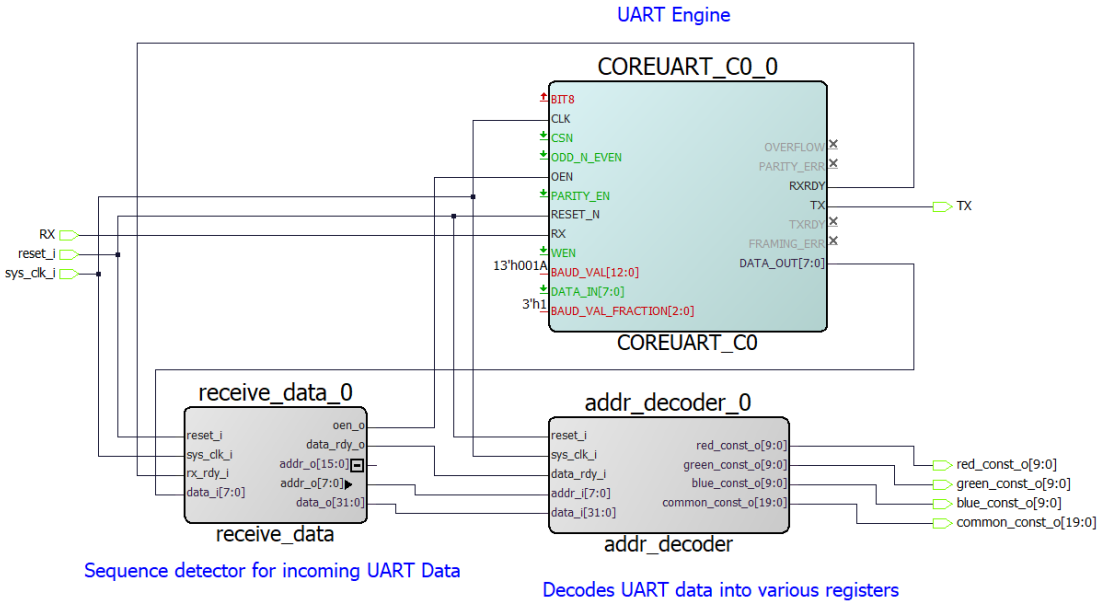
Figure 1-6. MSS Component Configuration



1.3 UART_interface (Ask a Question)

The following figure shows the UART_interface in SmartDesign.

Figure 1-7. UART_interface

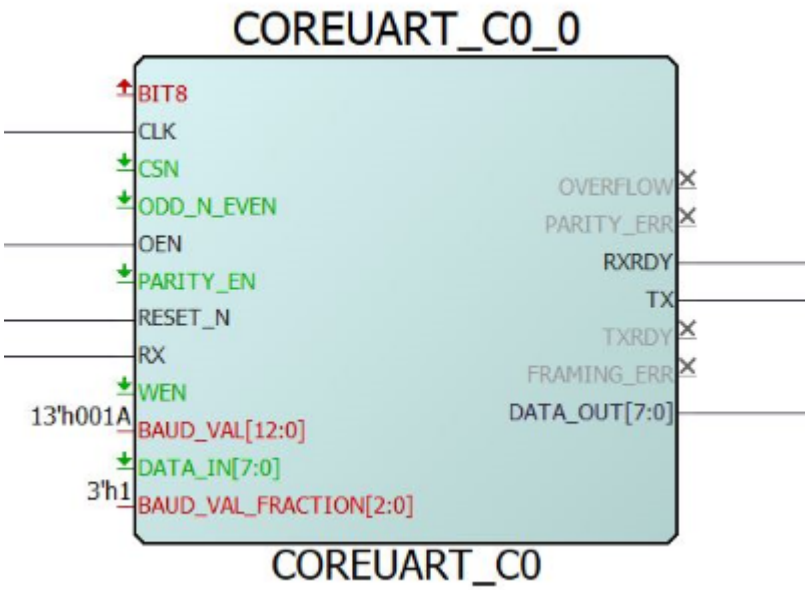


The UART_interface SmartDesign performs the task of communication between the SmartFusion 2 FPGA and the PC with PIC microcontroller as a bridge. Based on the data from Hello_FPGA GUI, receive_data module generates the address and data. The Addr_decoder module generates the values of brightness, contrast, and color and provides it to the Image_enchancement module.

1.3.1 COREUART_C0 (Ask a Question)

The COREUART IP is available in the Libero SoC peripheral IP catalog. The BAUD rate of UART is 230400, based on the operating clock frequency, BAUD_VAL, and BAUD_VAL_FRACTION values. The following figure shows the CoreUART configuration.

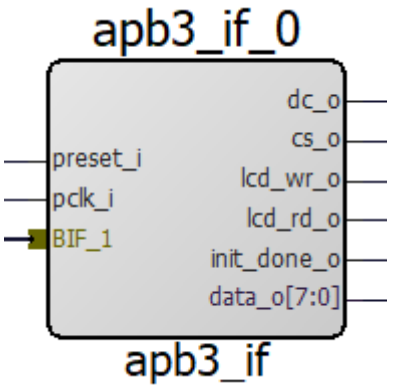
Figure 1-8. COREUART_C0_0 Configuration



1.4 APB3_if (APB Target) (Ask a Question)

The following figure shows the APB3 interface module.

Figure 1-9. Apb3_if

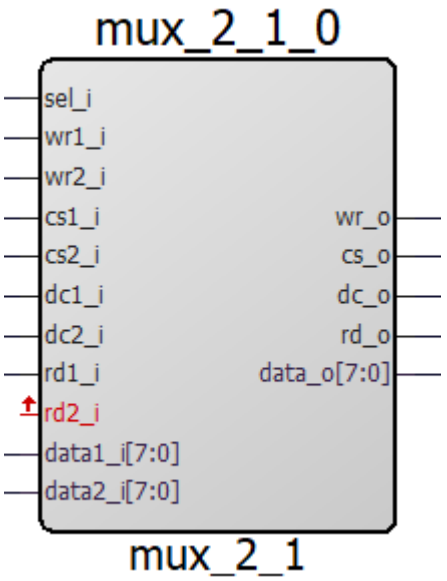


The Apb3_if module implements the APB target interface to communicate with APB3 initiator (MSS). LCD initialization is done through this module based on the control and data provided by MSS. After LCD initialization, MSS gives the command to the APB target to generate init_done signal.

1.5 Mux_2_1 (Ask a Question)

The following figure shows the Mux_2_1 configuration.

Figure 1-10. mux_2_1_0



MSS provides the select signal (Init_done) to the MUX, MSS first initializes LCD and after initialization, MSS gives the LCD control to the FPGA fabric.

1.6 FF_EXT (Ask a Question)

The following figure shows the FF_EXT configuration.

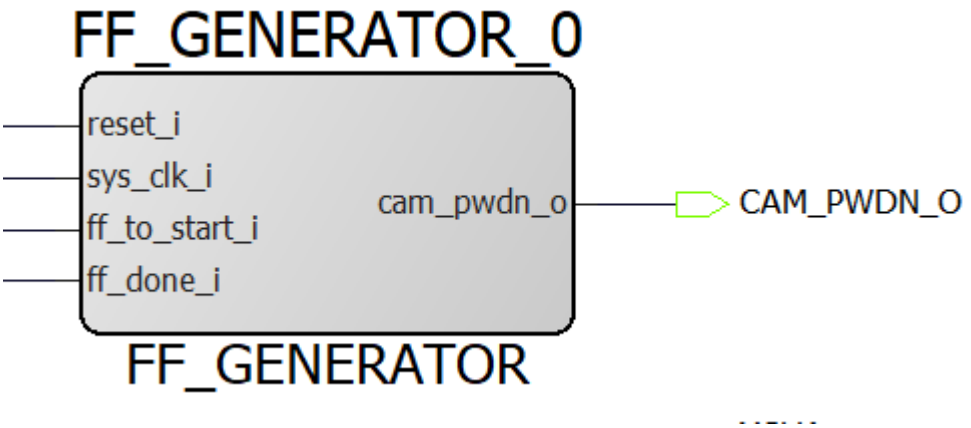
Figure 1-11. FF_EXT_0 Module

The FF_EXT module generates the pulse based on the PPL lock signal. The output pulse is given to the PIC controller, which signifies that the FPGA fabric is out of Flash*Freeze mode.

1.7 FF_GENERATOR (Ask a Question)

The following figure shows the FF_GENERATOR configuration.

Figure 1-12. FF_GENERATOR_0 Module



The FF_Generator module implements a power-down signal for the camera module based on the Flash*Freeze signal FF_to_start_i, which indicates that the fabric is in Flash*Freeze or Active mode.

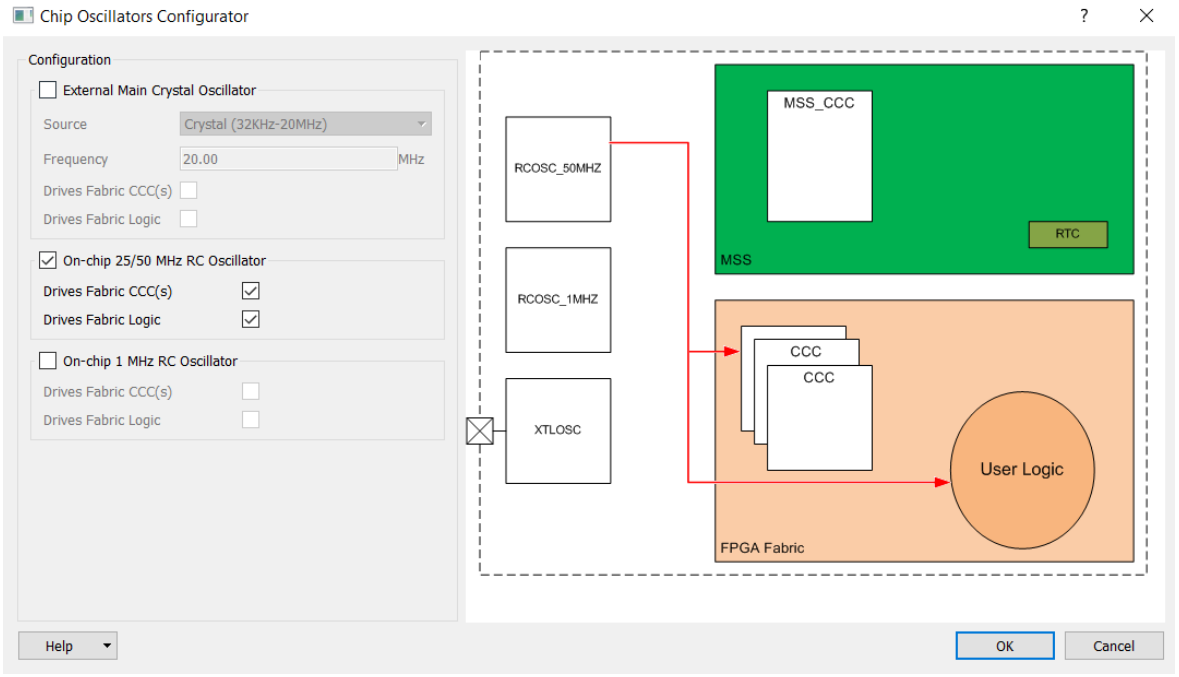
1.8 OSC_C0 IP (Ask a Question)

The OSC_C0 IP is available in the Libero SoC clock and management IP catalog. There are three oscillator blocks in the SmartFusion 2 device that can be used in different use models:

- On-chip 25/50 MHz RC Oscillator: This oscillator generates a 50 MHz waveform when the core supply voltage is 1.2V and 25 MHz when the supply voltage is 1.0V. The device core voltage can be selected from the Libero SoC Device Settings dialog box.
- On-chip 1 MHz RC Oscillator
- Main Crystal Oscillator

The following figure shows the configuration of the OSC_C0 IP core.

Figure 1-13. OSC_C0 IP Core Configuration



1.9 Resource Utilization (Ask a Question)

The following table lists the resource utilization of the Video demo design.

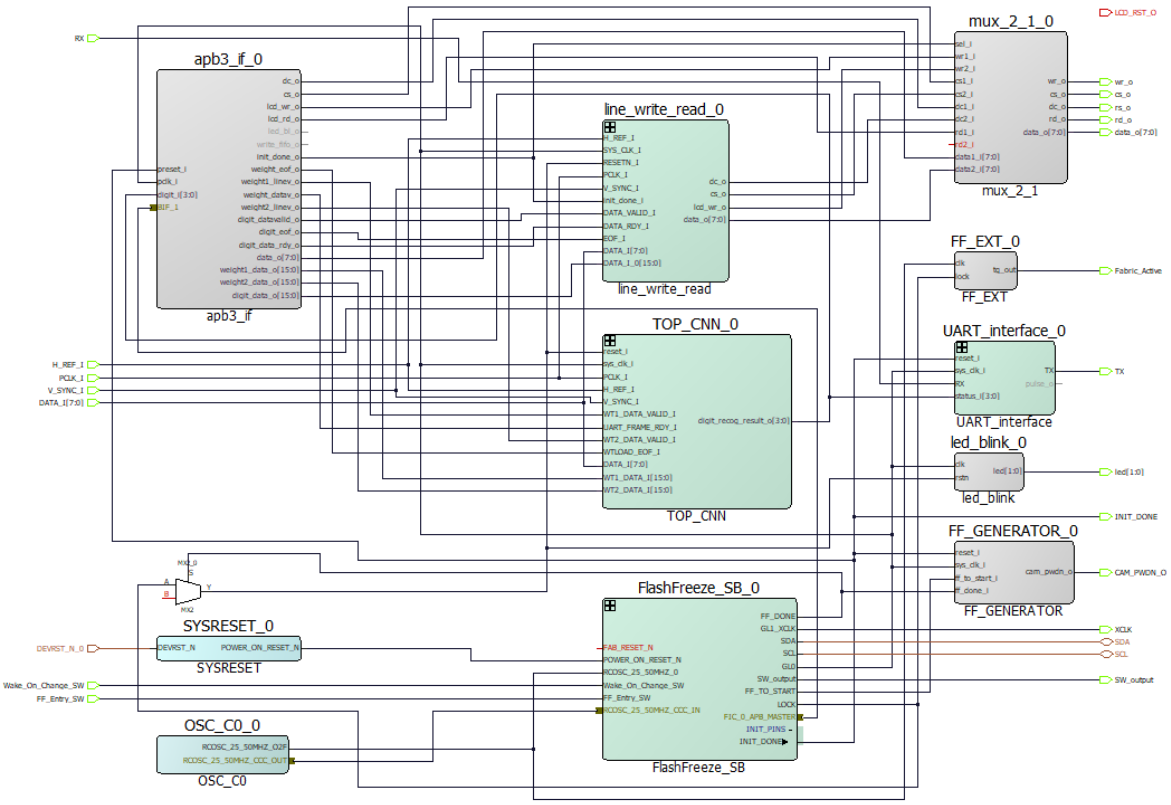
Table 1-1. Resource Utilization

Type	Used	Total	Percentage
4LUT	558	12084	4.62
DFF	584	12084	4.83
User I/O (single-ended)	37	138	26.81
RAM1K18	1	21	4.76
MACC	3	22	13.64

2. Digit Recognition (AI) Demo Design (Ask a Question)

The following figure shows the top-level AI digit recognition demo design in Libero SoC software.

Figure 2-1. Top-Level Hardware Implementation (AI Digit Recognition)

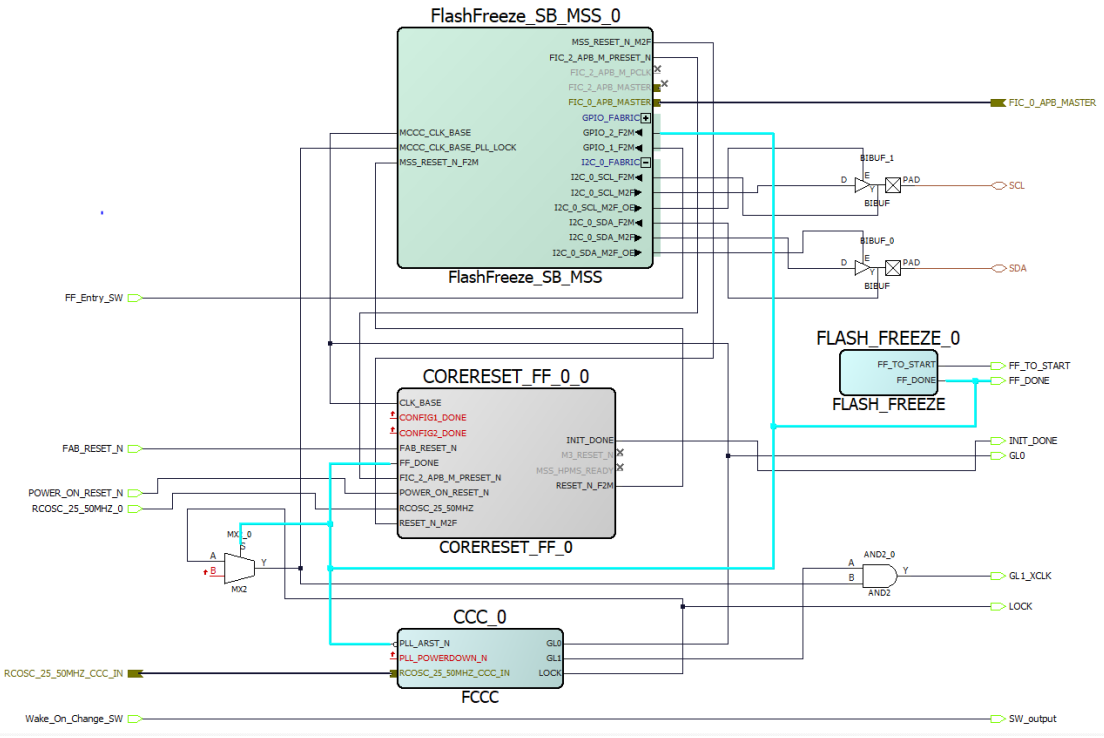


AI Digit Recognition Libero project aims to show Artificial Intelligence (AI) application. The Libero design for AI digit recognition is similar to the Video Demo Libero project with the following additional modules.

2.1 FlashFreeze SmartDesign (Ask a Question)

The following figure shows the FlashFreeze_SB configuration.

Figure 2-2. FlashFreeze_SB_MSS_0



The FlashFreeze_SB_MSS configures MSS. The I2C peripheral in MSS is used to configure camera registers. MSS is the APB initiator which is connected to the APB target (apb3_if) module to initialize LCD registers during startup.

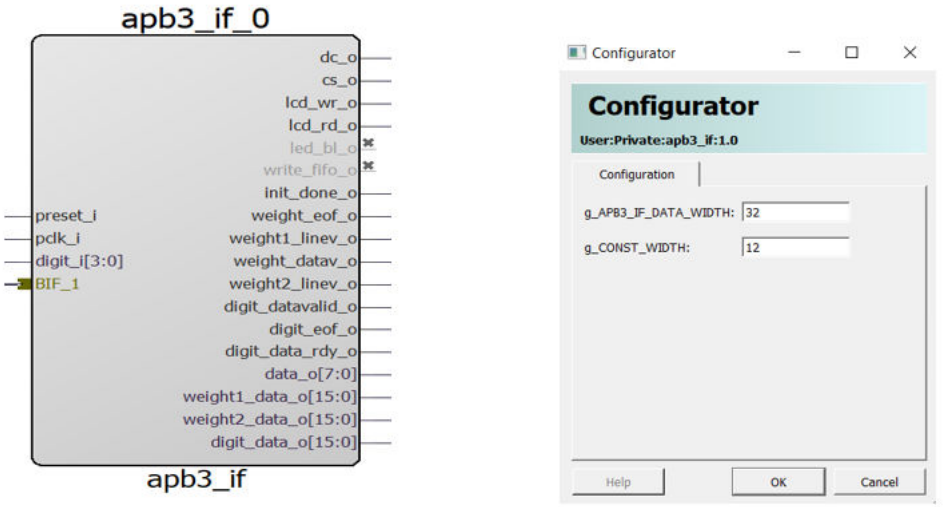
The Flash_FREEZE module provides the feature of low power Flash*Freeze mode to the FPGA. The FF_Entry_SW signal provides the hardware interrupt for Flash*Freeze to MSS. When there is an interrupt, MSS executes the instruction related to Flash*Freeze firmware through which FPGA goes into the Flash*Freeze mode. While FPGA is in Flash*Freeze mode, MSS will wait for the FPGA to come out of Flash*Freeze. MSS identifies that the FPGA is out of Flash*Freeze mode based on the FF_done signal interrupt. After receiving the FF_done signal interrupt, the MSS can communicate with FPGA through APB.

2.2 Apb3_if (APB Target) (Ask a Question)

The Apb3_if IP is an APB target module that communicates with the MSS. MSS first loads the weights into the Convolution Neural Network (CNN) SD through APB target. After loading weights, MSS initializes the LCD display and transfers the LCD control to the FPGA fabric through init_done signal. APB target acquires the digit recognized result from the CNN SD. MSS loads the graphics related to the recognized digit in to the LSRAM for On Screen Display (OSD) of the recognized digit.

The following figure shows the APB target module configuration.

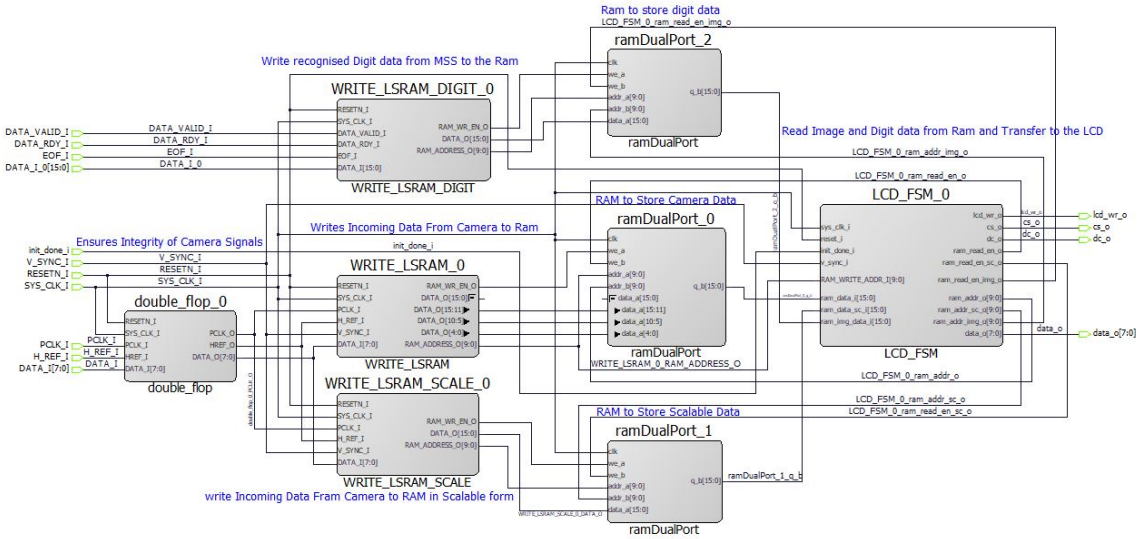
Figure 2-3. apb3_if_0 Target Module Configuration



2.3 Line_write_read SmartDesign (Ask a Question)

The following figure shows the Line_write_read module.

Figure 2-4. Line_write_read SmartDesign



Line_write_read SmartDesign displays the following images on LCD:

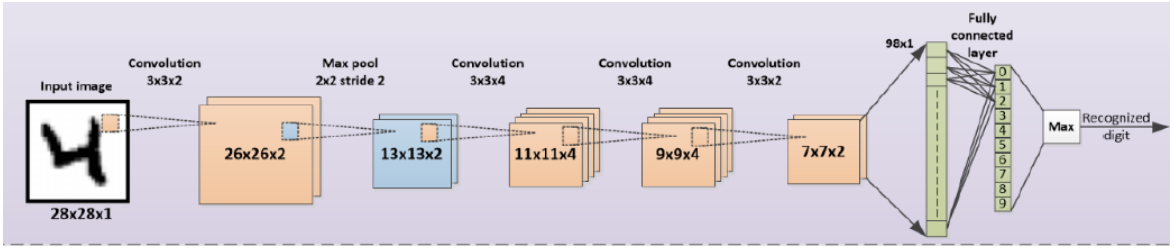
- Image from camera
- Image from camera in the scalable of size 28 x 28 at top left corner of LCD
- Recognized digit of size 80 x 80 at bottom left corner

FPGA receives video from the camera with a resolution of 640 x 480 at 30 fps. WRITE_LSRAM performs scaling of the input video to the 480 x 320 video format of LCD and writes scalable data on the ramDualPort_0. Similarly, WRITE_LSRAM_SCALE performs scaling of video from the camera to the 28 x 28, which is the resolution required by CNN. The actual scaled image passed on to CNN is displayed through the 28 x 28 scaled image. Recognized digit OSD data is provided by the MSS through the APB target of size 80x80; the WRITE_LSRAM_DIGIT module saves digit OSD data into the ramDualPort_2. The Init_done signal from MSS indicates that the LCD is initialized and MSS gives control of LCD to the LCD_FSM module. The LCD_FSM module reads data from all these RAMs and displays it on the LCD according to the interface protocol.

2.4 TOP CNN (Ask a Question)

The following figure shows the block diagram of the implemented SmartDesign.

Figure 2-5. Implemented SmartDesign Block Diagram



The network implemented in the demo contains four convolution layers, a max pool layer, and a fully connected layer. The network is trained from the standard MNIST handwritten digit database, which contains the digits in 28 x 28 resolution images. CNN can detect a single digit in the 28 x 28 image when the aspect ratio of the digit is approximately equal to the aspect ratio of the trained image data set. The network is built for only 10 classes for digits from 0 to 9 and does not use a class that shows no digit. Even though the camera is not pointing to a digit, the network still outputs a digit that has the maximum value from the fully connected layer.

2.5 Resource Utilization (Ask a Question)

The following table lists the resource utilization of the digit recognition demo design.

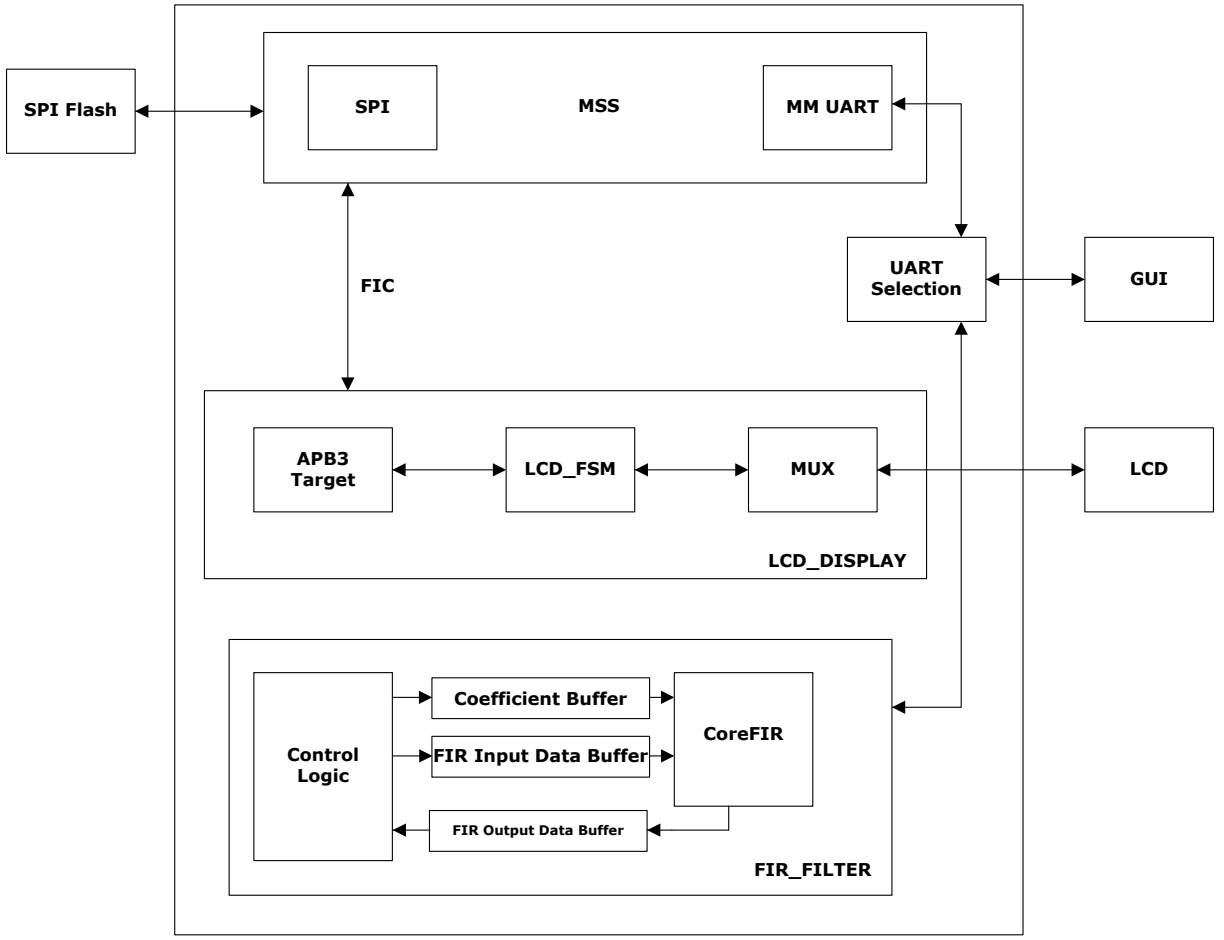
Table 2-1. Resource Utilization

Type	Used	Total	Percentage
4LUT	7203	12084	59.61
DFF	7168	12084	59.32
User I/O (single-ended)	37	138	26.81
RAM1K18	20	21	95.24
MACC	20	22	90.91
Chip Globals	8	8	100

3. DSP FIR Filter Demo Design (Ask a Question)

In this DSP FIR filter demo design, the FIR filter is implemented in the fabric for Low pass, High pass, Band pass, and Band reject filtering operations. The host interface is implemented in the fabric to communicate with the host PC. A user friendly Graphical User Interface (GUI) generates the filter coefficients, input signals (Pass-band frequency + Stop-band frequency) and also plots the input/ output waveforms and the required spectrum. Microchip's CoreFIR filter IP is used to suppress the unwanted frequency components and generates the output signals to verify the filtering operation.

Figure 3-1. DSP FIR Filter Block Diagram

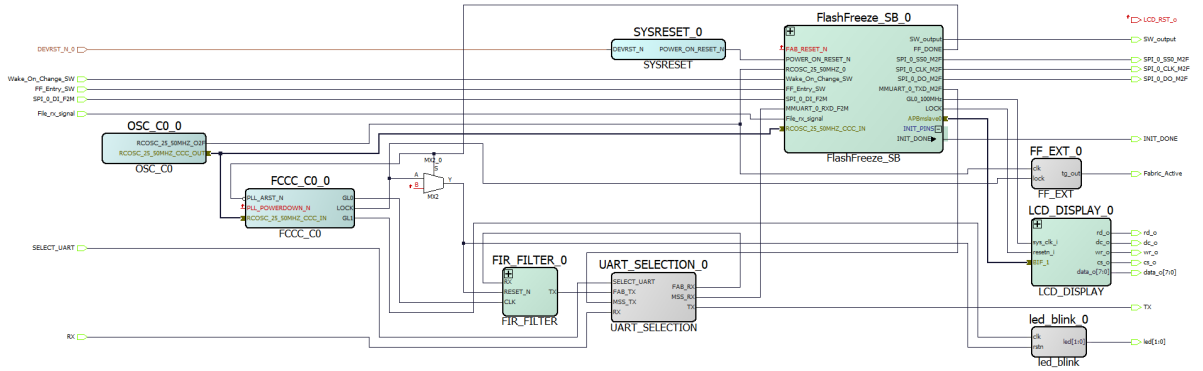


The demo design also implements an LCD display application, which displays images stored in SPI Flash on an ILI9488 LCD display. MSS UART is used to read and write the image data into the SPI Flash. For this demo, the SPI Flash is preloaded with Microchip's logo and a Hello FPGA board image.

Both the applications use UART communication to interface with PIC32 microcontroller which is interfaced with host PC for GUI, due to which a UART_SELECTION module is used to switch between fabric UART and MSS UART. The Fabric UART is used for DSP FIR application and MSS UART is used for LCD display application.

The following figure shows the top-level DSP FIR_LCD_FF demo design in Libero SoC software.

Figure 3-2. Top-Level DSP Design



The top module contains the following modules:

3.1 FlashFreeze_SB_0 Module (Ask a Question)

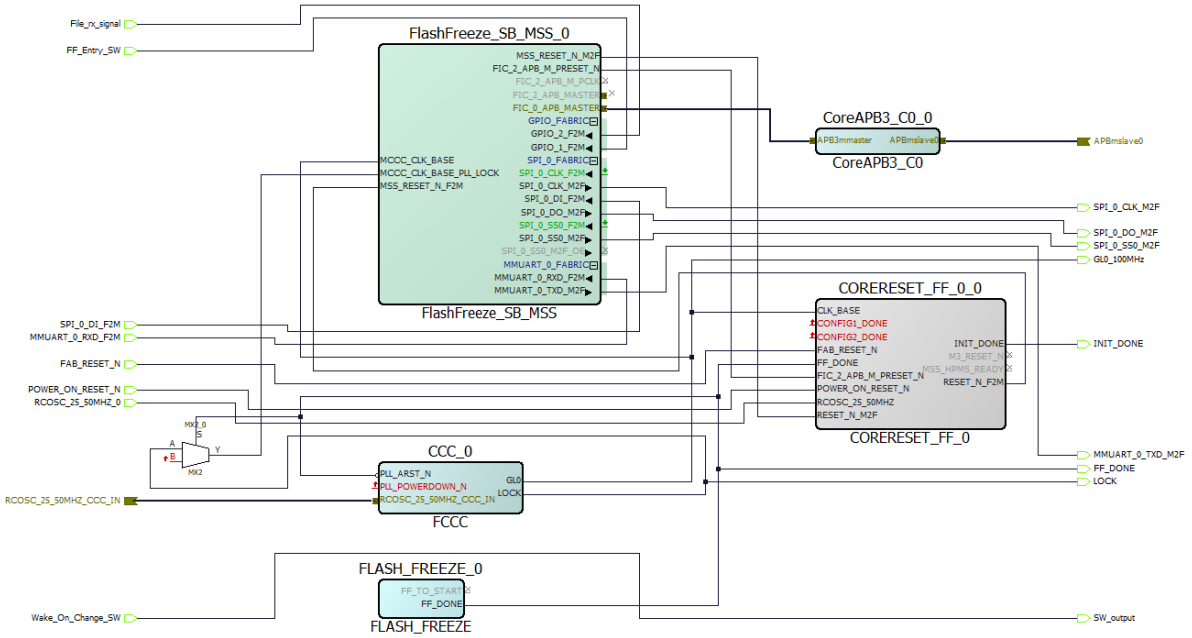
The FlashFreeze_SB_0 module configures the MSS for the following tasks.

- The SPI peripheral in MSS is used to store the images in SPI Flash and to read the images from SPI Flash.
- The UART peripheral in MSS is used to communicate with a GUI on host PC through PIC32 microcontroller.
- MSS is the APB initiator which is connected to the APB target (apb3_if) module to initialize LCD registers during start-up.
- The Flash_FREEZE module provides the feature of low-power Flash*Freeze mode to the FPGA. The FF_Entry_SW signal provides the hardware interrupt for Flash*Freeze to MSS.

When a Flash*Freeze user interrupt is received by MSS, the instruction related to Flash*Freeze is executed and the FPGA goes into the Flash*Freeze mode. MSS is in an infinite loop when the FPGA fabric is in the Flash*Freeze mode.

The following figure shows the blocks in the FlashFreeze_SB_0 module.

Figure 3-3. FlashFreeze_SB_0 Module



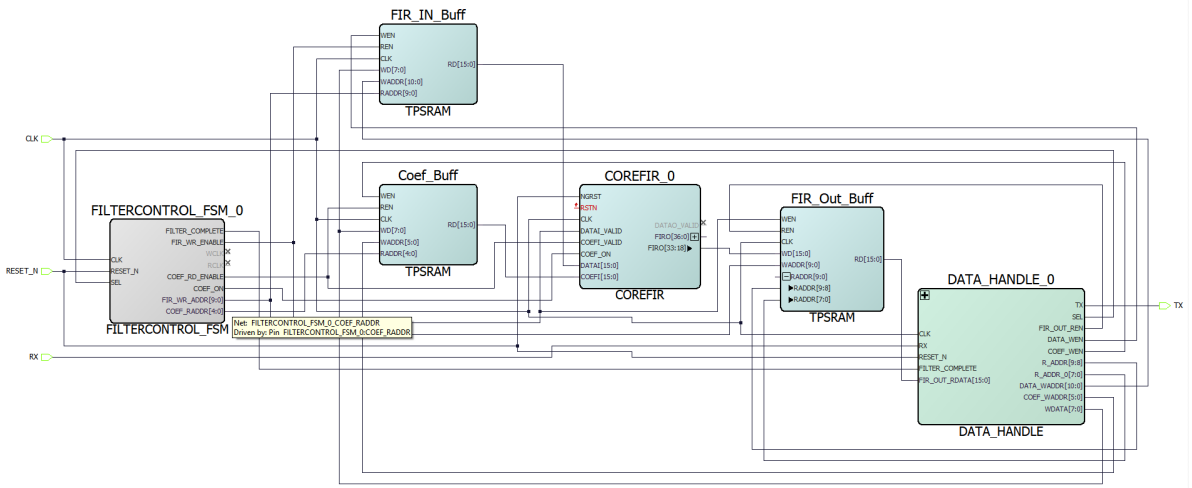
3.2 FIR_FILTER_0 Module (Ask a Question)

The FIR_FILTER_0 module implements the user logic in the fabric. This module implements the following finite-state machines.

- Data Handling: Implements and controls operations such as loading the filter input data to the corresponding input data buffer and loading filter coefficients to the corresponding coefficient memory buffers.
- Filter Control: Controls the FIR filter operation. Loads the filtered data into the corresponding output buffer.
- CoreFIR IP: The Core FIR IP is used in Re-loadable Coefficient mode to support Low pass, High pass, Band pass, and Band reject filters.
- TPSRAM IP: The TPSRAM IP is used to implement Filter coefficient buffer, Input signal data buffer, and Output signal buffer.

The following figure shows the blocks in the FIR_FILTER_0 module.

Figure 3-4. FIR_FILTER Module



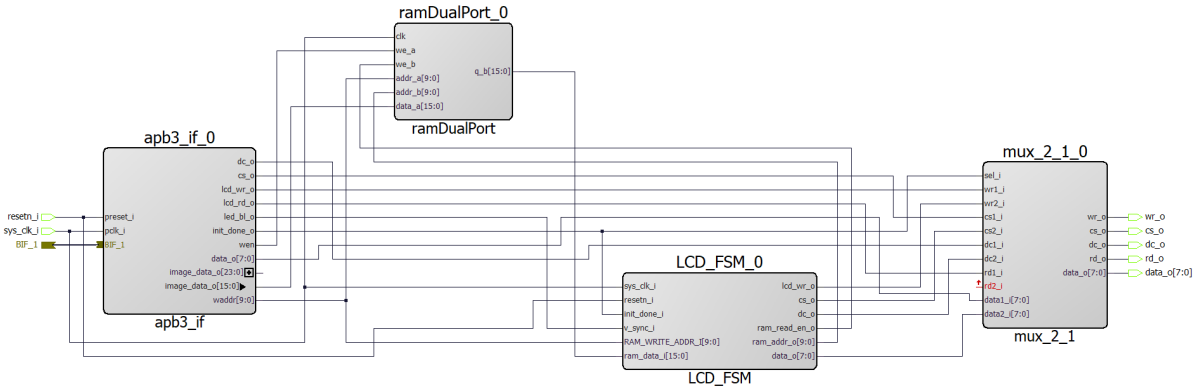
3.3 LCD_DISPLAY_0 Module (Ask a Question)

The LCD_DISPLAY_0 module implements the following functionalities:

- apb3_if: Apb3_if module implements the APB target Interface to communicate with APB3 initiator (MSS). LCD initialization is done through this module based on the control and data words provided by MSS. After LCD initialization, MSS gives the command to the APB target to generate init_done signal. After the init_done signal, MSS reads the images from SPI Flash and stores the data into the dual-port RAM through abp3_if module.
- LCD_FSM: The LCD_FSM module reads data from the dual-port RAM and sends it to the LCD display. The module starts reading the dual port RAM when the write address in WRITE_LSRAM reaches 160. The LCD_FSM also resets the registers of the LCD based on the V_Sync signal of the camera, which indicates the start of new frame data. LCD_FSM provides data to the LCD based on the interface protocol.
- mux_2_1: MSS provides the select signal (Init_done) to the MUX; MSS first initializes the LCD and after initialization; MSS gives LCD control to the FPGA fabric.

The following figure shows the blocks in the LCD_DISPLAY_0 module.

Figure 3-5. LCD_DISPLAY_0 module



3.4 Resource Utilization (Ask a Question)

The following table lists the resource utilization of the DSP demo design.

Table 3-1. Resource Utilization

Type	Used	Total	Percentage
4LUT	1430	12084	11.83
DFF	2335	12084	19.32
Logic Element	2540	12084	21.02

4. Program and Debug (Ask a Question)

The PIC Microcontroller **PIC32MX795F512L** of hello FPGA kit is pre-programmed with firmware. This microcontroller is used to program the SmartFusion 2 device with bit stream and measure the FPGA core power.

This PIC microcontroller executes the In-System programming application using DirectC to program the SmartFusion 2 device with the provided bit stream file (`.dat`). The microcontroller gets the bit stream file from host PC over UART with a baud rate of 460800 and programs FPGA. The microcontroller executes the DirectC JTAG program and enables five GPIO pins, which are interfaced with the JTAG pins of the FPGA for programming. The PIC microcontroller transfers the data to the SmartFusion 2 device over an UART interface. The UART module of SmartFusion 2 device is configured to operate at baud rate of 230400.

The PIC microcontroller communicates with the current sensor IC (PAC1710) over I2C and gets the data to calculate the FPGA core power and displays it in the GUI. It also sends signals to FPGA for Flash*Freeze entry and exit operations. It also measures the time taken from Flash*Freeze exit to FPGA functional. The microcontroller receives data from GUI using UART1 and transfers the data to FPGA using UART2. The microcontroller receives the data from FPGA using UART2 and transfers the data to GUI using UART1.

This PIC microcontroller can be programmed using the PICkit™3 - 6-pin connector, which is connected to header J5 of the Hello FPGA Kit. Using MPLAB X IDE, MPLAB XC32 Compiler, and MPLAB Harmony, you can develop and debug the microcontroller application. For more information, see https://www.microchip.com/en-us/tools-resources/develop/mplab-x-ide#Downloads%20and%20Documentation.

The Libero SoC GUI provides an option to program FPGA using the demo design programming files. If you want to perform program and debug operations on FPGA, the external hardware FlashPro4 (https://www.microchip.com/en-us/development-tool/FLASHPRO4) is required. Flashpro4 can be connected using the FPGA JTAG header on the kit to the host PC.

Important: Libero SoC software must be installed on a host PC to develop any FPGA designs and program the SmartFusion 2 device.

The SmartFusion 2 device includes Cortex-M3 microcontroller, which runs the user applications. These applications can be developed and debugged using the SoftConsole software and FlashPro4 hardware.

For more information about Libero SoC and SoftConsole tools, see https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools.

The demo design files can be customized and reprogrammed to Hello FPGA Kit. You can download the demo design file from: www.microchip.com/en-us/development-tool/M2S-HELLO-FPGA-KIT#resources.

5. Revision History (Ask a Question)

The revision history table describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 5-1. Revision History

Revision	Date	Description
A	06/2023	The following is a summary of changes made in this revision. • The document was migrated to the Microchip template. • The document number was updated to DS50003539A from UG0891. • Added Program and Debug section.
1.0	—	This is the first publication of the document.

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