Application Note
AN-250
Designing an IEEE802.3af/at/bt PoE System Based on PD692x0/PD69208

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Microsemi
a Microchip company

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1

Revision 1 is the initial issue of this document. This document is based on the previously published AN211 (Designing an IEEE 802.3af/at/bt- Compliant Based PD69200/PD69208 48-Port PoE System) and AN240 (Designing an IEEE 802.3af/at/bt- Compliant Based PD69210/PD69208 48-Port PoE System), with additional detail about protection and 4 pair support.

2 Overview

This application note provides detailed information and circuitry design guidelines for the implementation of a Power over Ethernet (PoE) Power Supplying Equipment (PSE) system, based on Microsemi's PD68208T4, PD69204T4 or PD69208M PoE Managers and PD69210 or PD69200 PoE Controllers. This document enables designers to integrate PoE capabilities (as specified in IEEE 802.3af, IEEE 802.3at, IEEE 802.3bt, and PoH standards) into an Ethernet switch.

The PD69210 and PD69200 Controllers are functionally identical. The PD69210 is based on the Microchip SAM D21 family that is embedded with the 32-bit Cortex-M0+ MCU core. This is the preferred Controller for all new designs. The PD69200 is based on the NXP Kinetis L family, MKL15Z128VFM4. This IC supports legacy designs and is not recommended for new designs.

The PoE manager can have 8 ports or 4 ports. PD69208M and PD69208T4 have 8 ports, while the PD69204T4 has 4 ports. The PD69208M, supports up to type-3 PSE, 60W, while the PD69204T4 or PD69208T4, supports up to type-4, 90W power. Any combination of PD69208M, PD69208T4, and PD69204T4 and any combination of 2-pair and 4-pair in the same system is possible and supported. Up to 12 ICs, which enables a 48 logical port system supported by a single PD692x0 Controller is supported.

The chip set implements real-time functions as specified in the standards (including detection, classification, and port-status monitoring) and system-level activities such as power management and management information base (MIB) support for system management. The PoE manager is designed to detect and disable disconnected powered devices (PDs) using DC disconnection methods, as specified in the standards. The chip set also provides real-time PD protection through the following mechanisms: overload, underload, over voltage, and short-circuit. The PD69208/4 share the same design, package, and features.

Contact your Microchip account representative for an Evaluation Board Recommendation. A layout guideline for a PoE system based on PD69208/4 is also included in this document.

2.1 Features

- A single PD692x0 Controller supports up to 48 2-pair or 4-pair logical ports.
- IEEE 802.3af-2003 standard compliant (Type 1)
- IEEE 802.3at-2009 standard compliant (Type 2)
- IEEE 802.3bt-2018 standard compliant (Type 3/4)
- Power over HD BaseT standard compliant (60 W/95 W)
- Configurable standard/reduced capacitor detection mode
- Supports pre-standard PD detection
- Supports Cisco devices detection
- Single DC voltage input (44 V_{DC}–57 V_{DC})
- Up to five event classification
- Voltage monitoring/protection
- Low power dissipation
- Internal sense resistor (0.1 Ω)
- Internal MOSFET with low RDS_ON (approximately 0.24 Ω)
- Internal power on reset
- Only one external front-end component per port
- Includes reset input from hosting system
- Four direct address configuration pins
- Continuous port monitoring and system data
- Configurable load current setting
- On-chip thermal protection
- Built-in 3.3 V_{DC} and 5 V_{DC} regulators
- Emergency power management supporting sixteen configurable power banks
- Can be cascaded to up to 12 PoE devices (48 logical ports in four pairs configuration)
- Supports 2 pair or 4 pair connection
- Wide temperature range: –40 °C to 85 °C
- PD69210 MSL1
- PD69208 and PD69200 MSL3
- RoHS compliant
- Supports I^2C and UART communication and software update

2.2 Integration

Using a single PD692x0 Controller up to a 48-logical port switch can be implemented, either by 4-pair or 2-pair, using up to 12 PD69208 Managers. Any combination of PD69208M, PD69208T4, and PD69204T4 can be implemented. The same design can be applied to 1–12 PoE Managers, controlling for example, eight 2-pair ports each (from 8 ports to 96 physical ports in multiples of 8) or with PD69204 in multiples of 4 ports. Similar design modularity may be achieved with 4-pair ports.

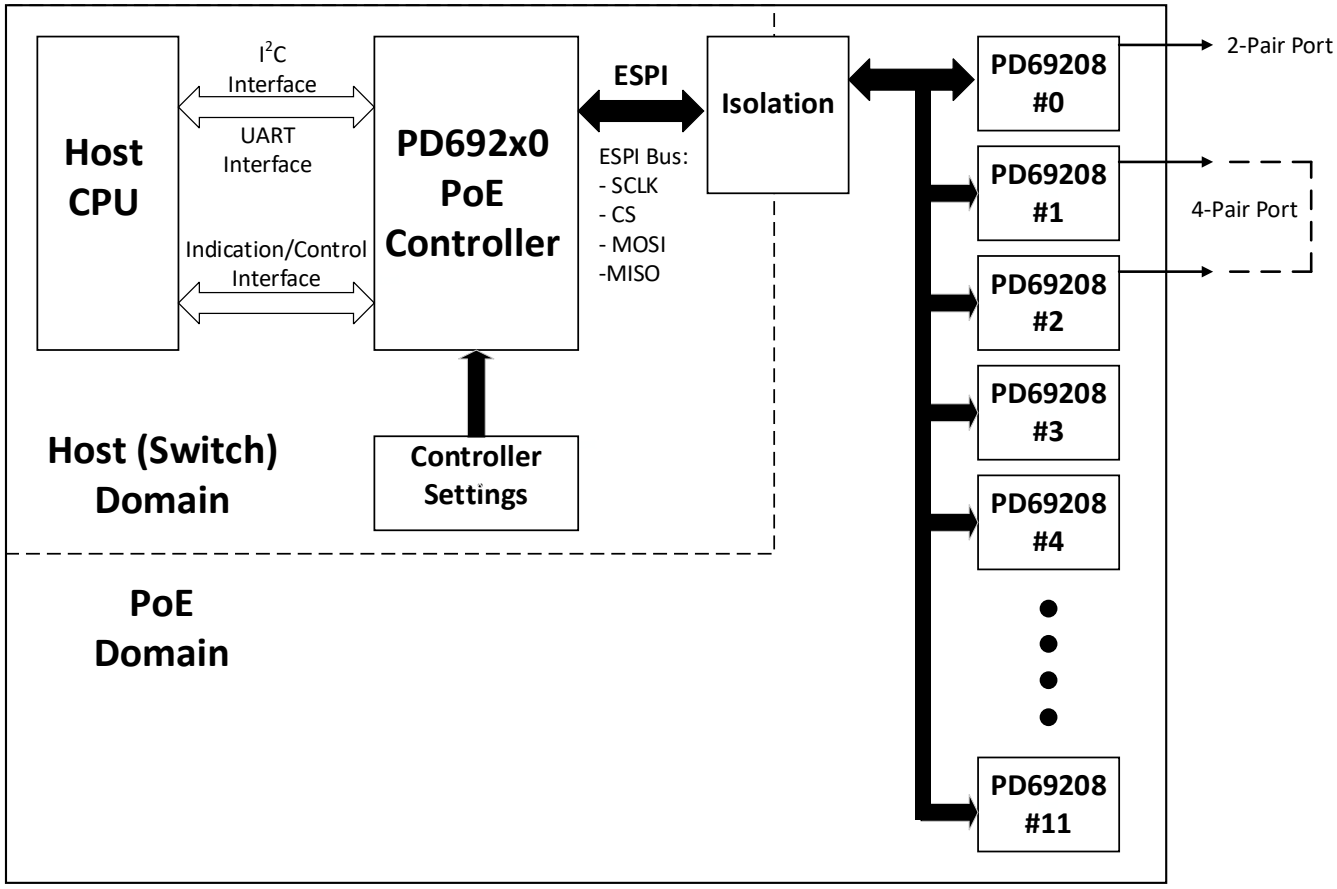
3 Functional Descriptions

A typical application includes the following blocks:

- PoE circuit for 48 Logical Ports, either 4-Pair or 2-Pair, based on up to twelve PD69208 Managers per single PD692x0 Controller.
- Controller circuit, used to initialize, control, and monitor each of the PD69208 through an internal enhanced serial peripheral interface (ESPI) isolated bus. The PoE controller communicates with the host CPU through a non-isolated UART or an I^2C interface.
- Isolation circuit for ESPI bus.

This is shown in Figure 1.

Figure 1 • 48 Logical Port Configuration Block Diagram



3.1 General Circuit Description

The 48 logical port configuration for a PoE system shown in the preceding figure comprises of twelve PoE manager circuits (PD69208) controlled by a PoE controller (PD692x0). The PoE controller uses the ESPI bus to control the PoE managers. The PoE operations are automatically performed by PoE manager circuits, while the PoE controller performs power management and other tasks.

3.1.1 Communication Interfaces

Communication between the host CPU and the local PoE controller is performed through a UART or an I^2C interface. For more information, see the **PD692x0 Serial Communication Protocol User Guide or PoE Host software communication API IEEE802.3af-at/bt User Guide.**

3.1.2 Communication Flow

The host CPU issues commands, utilizing a dedicated serial communication protocol to the PoE controller.

The PoE controller converts the serial communication protocol to ESPI communication and sends it through isolated ESPI lines to the appropriate PD69208. This isolation is a basic requirement of IEEE PoE standards.

3.1.3 ESPI Bus

The ESPI bus, used for internal communication, includes the following lines:

- Master out/slave in (MOSI) provides communication from the PoE controller to the PD69208.
- Master in/slave out (MISO) provides communication from the PD69208 to the PoE controller.
- SCK is the serial clock generated by the controller.
- Chip select (CS) is utilized by the PoE controller to transmit data simultaneously to all PD69208 ICs, while only the chosen PoE manager responds.

3.1.4 Control

An xReset_IN control signal driven by the host CPU is used to reset the PoE system. An xDisable_ports control signal driven by the host CPU is used to disable all PoE ports at once.

3.1.5 Indications

An xSystem_ok signal is generated by the PoE controller, indicating that the main input voltage is within range. This pin is determined by a 15-byte serial communication protocol. An xInt_out interrupt signal is designed to indicate PoE events such as port on, port off, port fault, PoE manager fault, voltage out of range, and so on. An xI2C_Message_Ready indicates that a message is ready to be read by the host. For the complete list of interrupt events, see the **PD692x0 Serial Communication Protocol User Guide**.

3.1.6 Main Supply

The PoE system operates within a range of 44 V_{DC} to 57 V_{DC} (IEEE 802.3at/bt Vmain range is 50 V_{DC} to 57 V_{DC}). To comply with UL SELV regulations, the maximum output voltage should not exceed 60 V_{DC}.

3.1.7 Hot-swap Circuit

The hot-swap circuit is crucial for applications where DC hot plug is present because the absence of such a circuit will cause the DC voltage to oscillate (ring), which leads to application malfunctions. The selected MOSFET is rated for 80 A and the R_{DS} is 10 mΩ. For more information, see Hot-Swap Circuit.

For more information on timing and power loss in the MOSFET, see the **hot-swap test report (PD-000308569)**.

3.1.8 Grounds

Several grounds are utilized in the system: PoE domain analog, PoE domain digital, chassis, and host domain floating.

Digital and analog grounds are the same ground, electrically. However, to reduce noise coupling, grounds are physically separated and connected only at a single point.

The chassis ground is connected to the switch's chassis ground. This ground plane should be 1500 V_{rms} isolated from PoE circuitry.

The PoE controller relates to the host domain floating ground, which is isolated from the PoE domain grounds.

3.1.9 5 V DC and 3.3 V DC Regulators

Each PD69208 has a 5 V_{DC} and a 3.3 V_{DC} regulator for internal IC circuitry and can provide up to 6 mA to be utilized for powering components in the PoE domain. The 5 V has been powered from V_{MAIN} by an internal regulator and the 3.3 V has been powered from the 5 V with another internal regulator. In order to minimize time between the 5 V and 3.3 V rise during the first system power up, a 4.7 µF capacitor should be placed between those pins (pin 20 and pin 22).

An external boost transistor can be added to the 5 V DC regulator's output (instead of R1007) to increase the current, as shown in Boost Transistor to the 5 V DC Regulator. The transistor can provide a total of 30 mA to the PoE controller and to the isolation circuits. This total current is the sum of 5 V and 3.3 V currents. All external components in this circuitry should also be isolated from the switch circuitry by 1500 V_{RMS}.

Using a boost transistor reduces the internal heat generated by the PD69208.

3.2 Detailed Circuit Description

The following sections provide a detailed description of the circuit.

3.2.1 Communication Interfaces/Isolation

There are two communication interfaces in this circuitry.

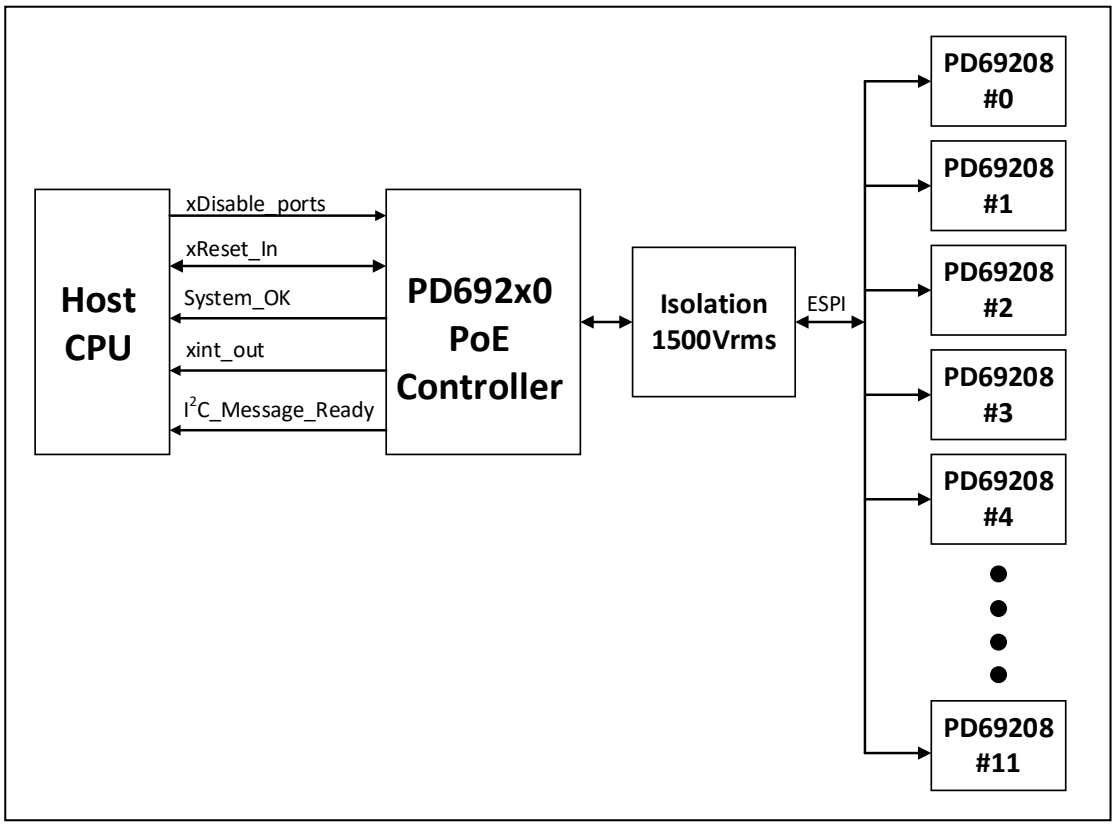
- An interface between the Ethernet switch and the PoE controller. This interface is an I^2C or an UART interface and does not require isolation.
- An interface between the PoE controller and PoE managers with 1500 V_{RMS} isolation. This interface is a standard SPI.

The isolation circuit is comprised of a Digital Isolator. Each side of the isolator circuitry is fed by a separate power supply.

3.2.2 Control and Indication Signals

Control/indication signals are single hardware lines that runs between the host CPU and the PoE controller as shown in Figure 2.

Figure 2 • Control and Indication Signals



3.2.2.1 Control Signals

There are two control lines driven by the host CPU to the PoE controller.

- xDisable_ports: Disables all PoE ports. When the PoE controller detects low level voltage at PD69200's pin number 31 or PD69210's pin number 4, it sends a disable command through ESPI to all PoE manager ports.
- xReset_In: Resets the PoE controller and all PoE managers. When the PoE controller detects low level voltage at PD96200's pin number 19 or PD69210's pin number 26, it enters reset mode and all of its output pins switch to tri-state mode. When `xReset_In` line returns to high, the PoE controller initializes and sends a RESET command to the PoE managers through the ESPI bus. xReset_In is also used by the PoE controller watchdog to reset itself, and so the host should drive a reset using an open-drain output and a pull-up.

In case the host drives the reset pin from a push-pull output, a 1 KΩ resistor should be located between the host's output and the PD692x0 xReset_In.

3.2.3 PoE Controller Circuitry

The following section describes the PD69200 and PD69210 PoE controllers circuitry, which are shown in PD69200 PoE Controller Circuitry and PD69210 PoE Controller Circuitry.

3.2.3.1 Interface to PoE Manager

The PoE controllers PD692x0 features 1 Mbps ESPI for each of the PoE managers, and a communication interface with host CPU through UART or I^2C protocol.

3.2.3.2 Interface to Host

UART (set to 19200 bps) or I^2C (up to 400 KHz) communication between the host CPU and PoE controllers are managed by setting the PD69200's address, pin number 22 (I2C_ADDR) or PD69210's address, pin number 13(I2C_ADDR). For the UART and I^2C communication address table, see **Serial Communication Configuration.**

3.2.3.3 Clock

The PoE controllers run at 47.972 MHz, facilitated by an internal clock.

3.2.3.4 Supply

The PoE controllers requires stable, filtered power for its operation coming from the host (3_3V_iso), so a number of decoupling capacitors are included in the design (C56, C71, C92 for PD69200 and C13, C15, C16, C17 for PD69210). The expected current consumption of the PoE controller circuitry should be below 20 mA.

3.2.3.5 Self Reset

As required by the application, the PoE controllers can reset themselves. This reset can also be performed by an external source utilizing the xReset_In signal (usually by the host controller). If the host utilizes xReset_In, it should drive a reset using an open-drain output and a pull up.

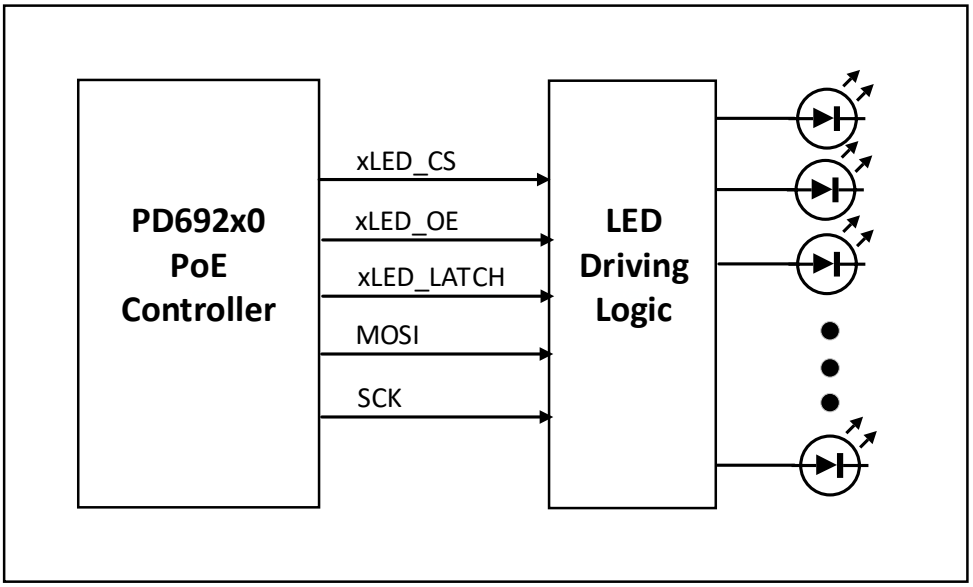
It is not recommended to connect the xReset_In signal to the common reset signal of the whole system, to prevent whole system reset when the PD692x0 resets itself.

3.2.3.6 LED Support

LED support for port status indication is accomplished by utilizing the ESPI bus (SCK and MOSI), xLED_CS, xLED_OE, and xLED_Latchsignals. Bus behavior is 1 MHz synchronous serial communication (clock and data) in one direction (write only) that transmits the status up to 48 logical ports.

Figure 3 shows the SPI bus and LED support.

Figure 3 • SPI Bus and LED Support



3.2.3.7 Emergency Power Management

PoE circuits can be powered by up to four separate power supplies. It is recommended that each power supply be capable of generating a logic signal, indicating its operate/fail status. For more information, see Power Good.

The following table lists the pins used for emergency power management.

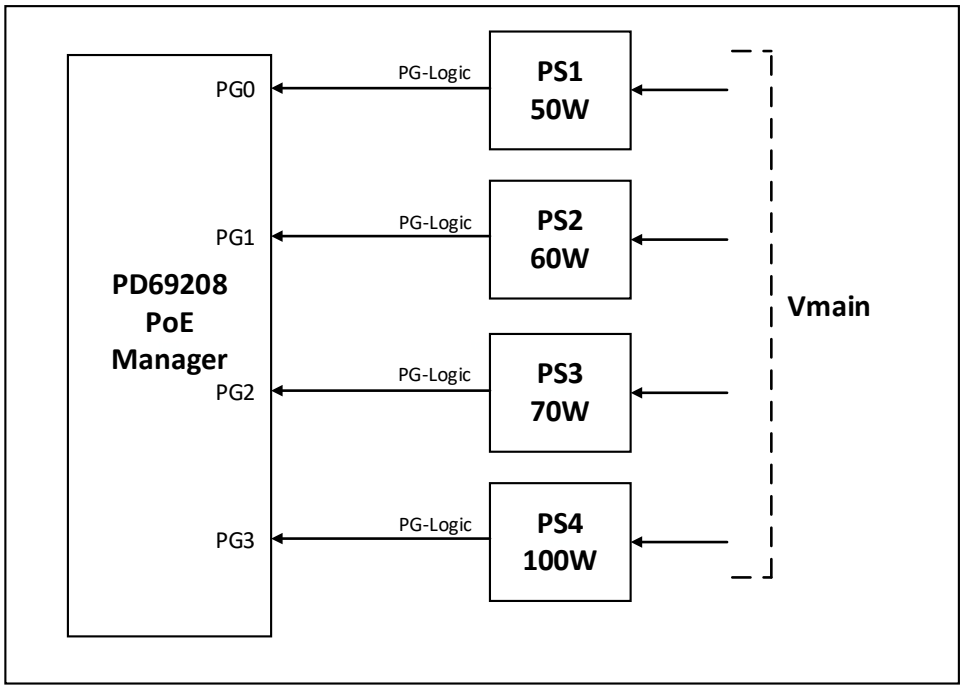
Table 1 • Emergency Power Management Pins

PD69208 Pin Number	Signal	Description
56	PG0	Power Good 0
41	PG1	Power Good 1
46	PG2	Power Good 2
47	PG3	Power Good 3

The PoE circuit allocates power to the system in 16 power levels (power banks) programmed by users. Power bank values are based on each supplies' available power and on the state of the logic signals PG[0..3] coming from power supplies. If PG pin is not used, the pin must be connected to GND or V_{DD}.

Figure 4 shows the connections between the logic signals of the power supplies and the PoE manager.

Figure 4 • Power Good



Note: The system V_{MAIN} capacitor should hold the voltage from dropping for 5 µs until the emergency power management reacts.

3.2.4 PoE Manager Circuitry

The PD69208 performs a variety of internal operations and PoE functions, requiring a minimal number of external components.

The PoE manager number with its related components for an 8-port 2-pair configuration is shown in PD69208 Circuitry for PoE Manager number. For 48 2-pair ports, this is circuitry is duplicated six times.

3.2.4.1 Reference Current Source

The reference for internal voltages within the PD69208 is set by a precision resistor (R60), 28.7 kΩ 1%.

In a PoH and IEEE 802.3bt 99W system, the precision resistor should be 0.1%.

3.2.4.2 Sense Resistors

The PD69208 provides an internal sense resistor of 100 mΩ. This resistor is utilized to measure port current.

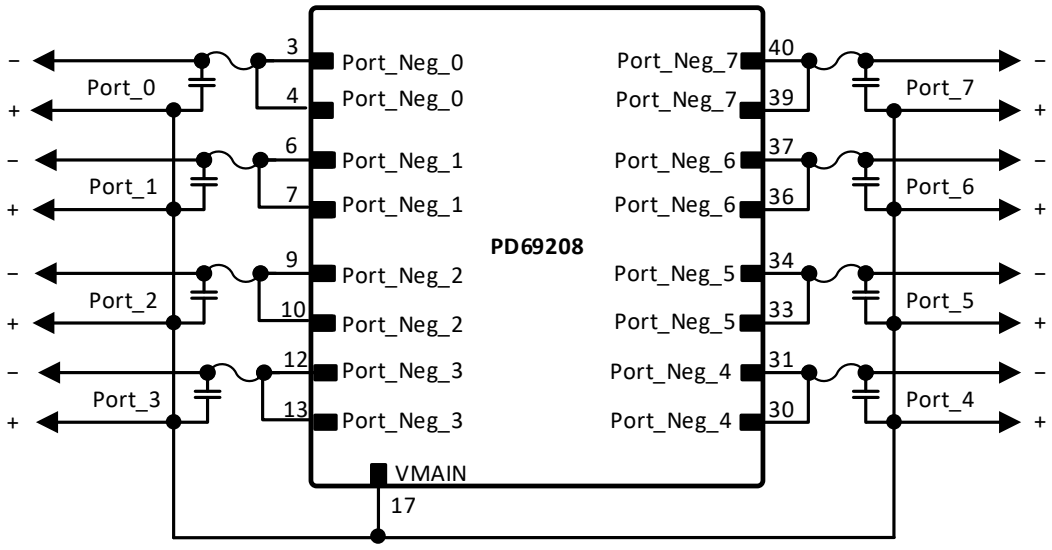
3.2.4.3 Front-End Components

A single capacitor per port is the only external front-end component used. The capacitor value can be between 22nF and 220nF. Using 220nF is recommended to improve the PSE immunity to 50 Hz/60 Hz noise. All other components such as reverse diode, port protection, sense resistor, and switching MOSFET are internal.

Fuses per port are not required for use in circuits with a total power level of up to 3 kW, as the PD69208 is designed to fulfill limited power source (LPS) requirements per the latest editions of IEC60950-1 and EN60950-1. However, IEC62368-1 ED3 which was released in October 2018 and becomes effective December 2020 requires per port fuses for a system power supply greater than 250 W.

Figure 5 shows the front-end components of the PD69208 Manager.

Figure 5 • 8-Port Front End Components



3.2.4.4 Line Transformer

A line transformer that is dedicated to PoE (with the desired PoE current for the specific applications in mind) should be used.

3.2.5 Serial Communication Host-Controller

The PoE controllers can communicate with the hosting system using UART or I²C communication. The PoE controller may be one of few controlled devices on the I²C communication bus reporting to the host, requiring the user to configure a dedicated address for the PoE controller. This is done by selecting a value for R93 for PD69200 (see PD69200 PoE Controller Circuitry for more information) or R33 for PD69210 (see PD69210 PoE Controller Circuitry for more information). Those resistors set the analog level into pin number 22 for PD69200 or into pin number 13 for PD69210 (I2C_ADDR_Meas), as specified in the following tables.

Table 2 • Serial Communication Configuration for PD69200

I²C Address	Address (Hex)	R93 (Ω)
#0	UART	N.C
#1	0x4	97600
#2	0x8	53600
#3	0xC	35700
#4	0x10	25500
#5	0x14	19100
#6	0x18	14700
#7	0x1C	11300
#8	0x20	8870
#9	0x24	6810
#10	0x28	5230
#11	0x2C	3920
#12	0x30	2800
#13	0x34	1870
#14	0x38	1020
#15	0x3C	324

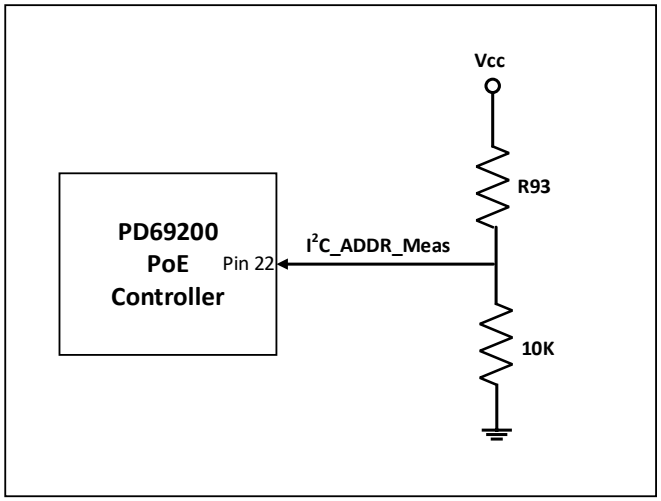
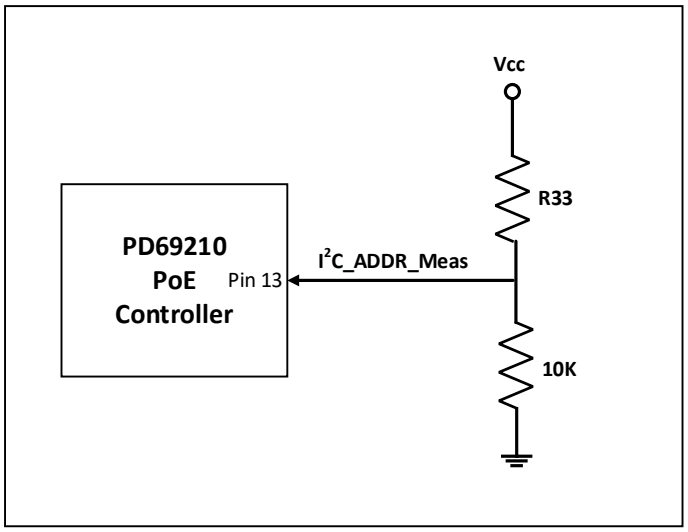


Table 3 • Serial Communication Configuration for PD69210

I²C Address	Address (Hex)	R33 (KΩ)
#0	UART	N.C
#1	0x4	147
#2	0x8	86.6
#3	0xC	57.6
#4	0x10	43.2
#5	0x14	34
#6	0x18	26.7
#7	0x1C	22.1
#8	0x20	18.2
#9	0x24	15.4
#10	0x28	13
#11	0x2C	11
#12	0x30	9.31
#13	0x34	7.87
#14	0x38	6.49
#15	0x3C	5.49



3.2.5.1 UART

The Rx signal should be connected to pin number 11 and the Tx signal should be connected to pin number 12 of the PoE controller PD69200.

The Rx signal should be connected to pin number 16 of the PoE controller and the Tx signal should be connected to pin number 15 of the PoE controller PD69210.

A pull-up resistor is required on the UART communication line (for more information, see PD69200 PoE Controller Circuitry and PD69210 PoE Controller Circuitry.

3.2.5.2 I2C

An SDA signal should be connected to pin number 21 of the PoE controller PD69200. An SCL signal should be connected to pin number 20 of the PoE controller PD69200.

A pull-up resistor is required on the I^2C communication lines (pin 21 and pin 20).

An SDA signal should be connected to pin number 21 of the PoE controller PD69210. An SCL signal should be connected to pin number 22 of the PoE controller PD69210.

A pull-up resistor is required on the I^2C communication lines (pin 21 and pin 22).
The PD692x0 requires the host to support I^2C clock stretch.

3.2.6 Ground Interface Connection (AGND)

The power supplies' ground connector enables the current a path back to the power supply. The ground connection should be capable of carrying all current back to power supplies.

3.2.7 Four-Pair Connectivity

Designing a PoE port delivering power to over RJ45 four pairs of wires is quite easy by utilizing any of the PD69208M, PD69204T4, and PD69208T4 PSE managers. Just connect any two ports of the PD69208T4 to a single RJ45 connector and configure the PoE Controller PD692x0 accordingly. The two ports utilized for the four-pair output terminal can be taken from the same PD69208T4 or from any two PD69208T4 ICs in the system. The PD69208M, PD69204T4 and PD69208T4 PSE managers can deliver AT power (enabling delivery of 30W over 2 pairs). The PD69208M supports IEEE802.3bt Type3 power (delivering 60W over 4 pairs) and the PD69204T4/PD69208T4 support IEEE802.3bt Type4 / PoH power (delivering >90W power over four pairs).

For more information on PD692x0 configuration process, see the **PD692x0 Serial Communication Protocol User Guide.**

4 4-Pair Ports for IEEE802.3bt

4.1 Scope

This section describes the basic steps to configure PSE Systems to support IEEE802.3bt 4-Pair applications based on the PD692x0 PoE Manager and PD69208M-PD69208T4 PoE Controller.

4.2 Background

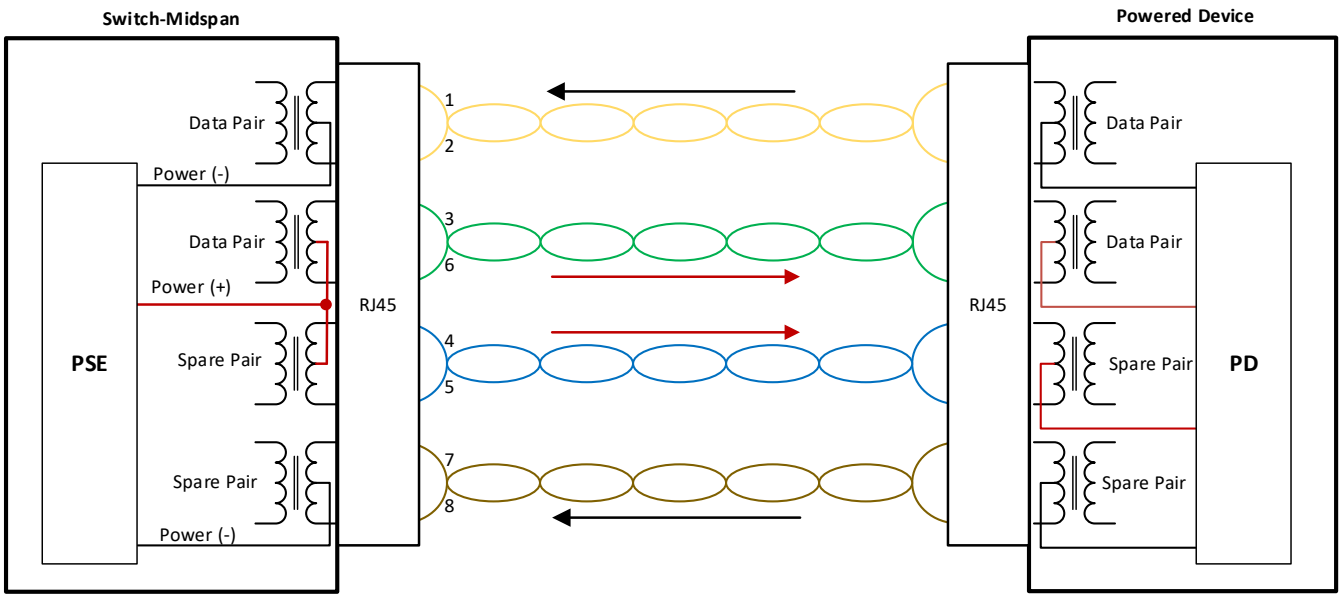
The IEEE 802.3af standard described Power Source Equipment (PSE) power of 15W over 2-pair and the IEEE 802.3at standard described PSE power of 30W over 2-pair. In order to increase the maximum PoE power supplied by the PSE to the Powered Device (PD) 4-Pairs ports utilizing all four pairs of the structured RJ45 wiring are used.

The IEEE 802.3bt-2018 standard, introduced the “Type 3” and "Type 4" PSE/PD capable of supporting 60W/90W output power using two PSE ports on all wires of the RJ45 cable.

The PD69208M supports up to 30W per 2-pair or 60W per 4-pair (Type 3). The PD69208T4 supports up to 45W per 2-pair or 90W per 4-pair (Type 3 or Type 4).

The “Data Pair” is defined as “Alternative A” at the PSE side and “Mode A” at the PD side. The “Spare Pair” is defined as “Alternative B” at the PSE side and “Mode B” at the PD side. This is illustrated in Figure 6.

Figure 6 PoE 4-Pair Architecture



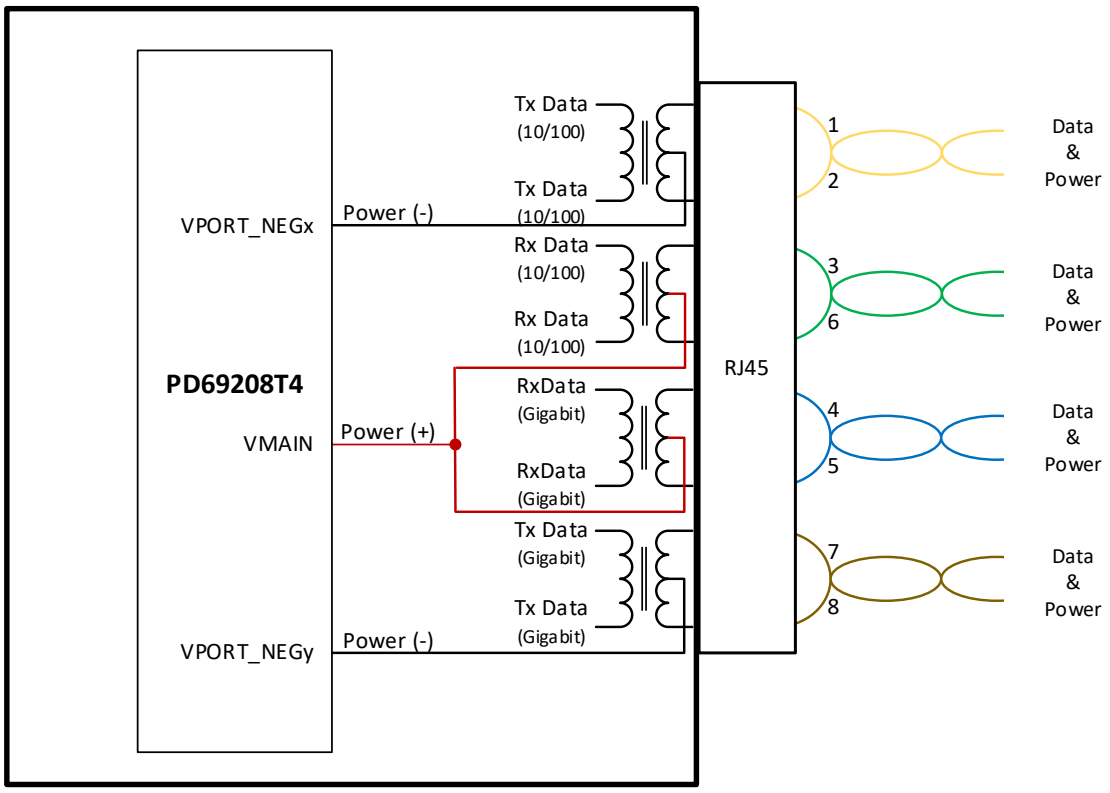
4.3 Implementation

4.3.1 Hardware Set Up

4.3.1.1 PSE

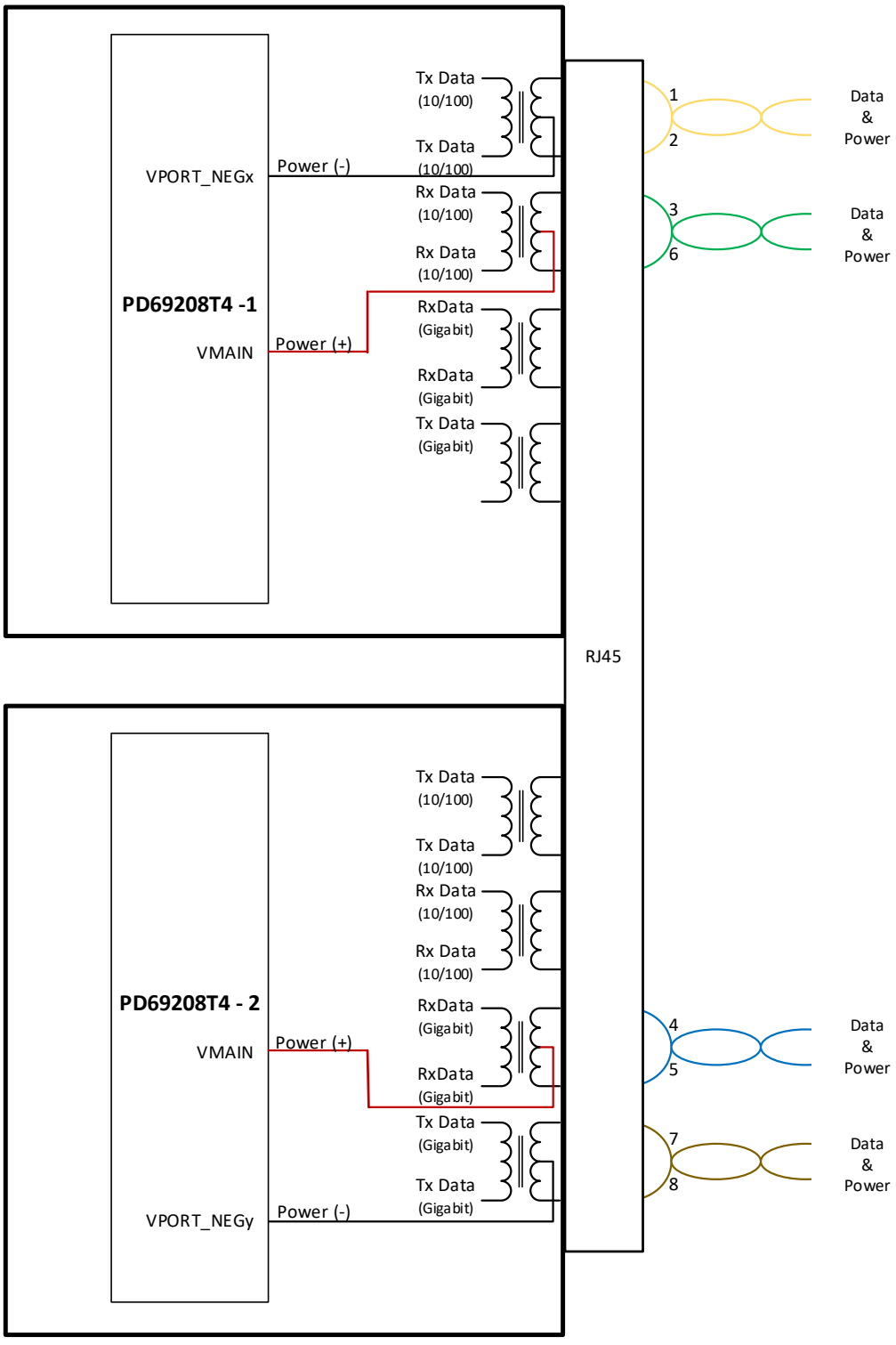
There are different ways to physically implement 4-Pair Powering. The System Designer should consider Heating effect, PCB lay-out etc before making the decision. In one configuration all of the 4-Pair come from a single PB69208 IC. This will tend to make the PCB layout simpler. This is shown in Figure 7.

Figure 7 Single Manager 4-Pair Implementation



An alternative configuration is to take 2-Pair from one PD69208 IC and the second 2-pair from a second PD69208 IC. MCHP recommends using different ICs and it will minimize heating of the ICs. There are many ways to implement 4-pair powering via 2 PD-69208ICs. Microchip suggest taking 2-Pair from Alternative A of IC1 and the second 2-pair from Alternative B of IC2. (and Visa versa). This is illustrated in Figure 8.

Figure 8 Dual Manager 4-Pair Implementation



4.3.1.2 Polarity

Type 4 is limited to a “fixed polarity”, that is the IEEE802.3bt strictly defines the connection of the positive VMAIN voltage and return (PORT_NEG) paths to the physical pairs. For Type 3 applications the standard is flexible allowing a variety of connection options. This is shown in Table xxx.

Table 4. Allowed Polarity

Pairset	Color	Alternative	Type 3	Type 3	Type 3	Type 3 Type 4
1-2	Orange	Data (Alt A)	PORT_NEGx	VMAIN	VMAIN	PORT_NEGx
3-6	Green	Data (Alt A)	VMAIN	PORT_NEGx	PORT_NEGx	VMAIN
4-5	Blue	Spare (Alt B)	PORT_NEGy	PORT_NEGy	VMAIN	VMAIN
7-8	Brown	Spare (Alt B)	VMAIN	VMAIN	PORT_NEGy	PORT_NEGy

4.3.1.3 PD Side

The schematic in Figure 9 describes how to physically connect 4-pair ports to a Signal Signature and Figure 10 describes how to physically connect to a Dual Signature Pd.

Figure 9. PD 4 pair SSPD Implementation

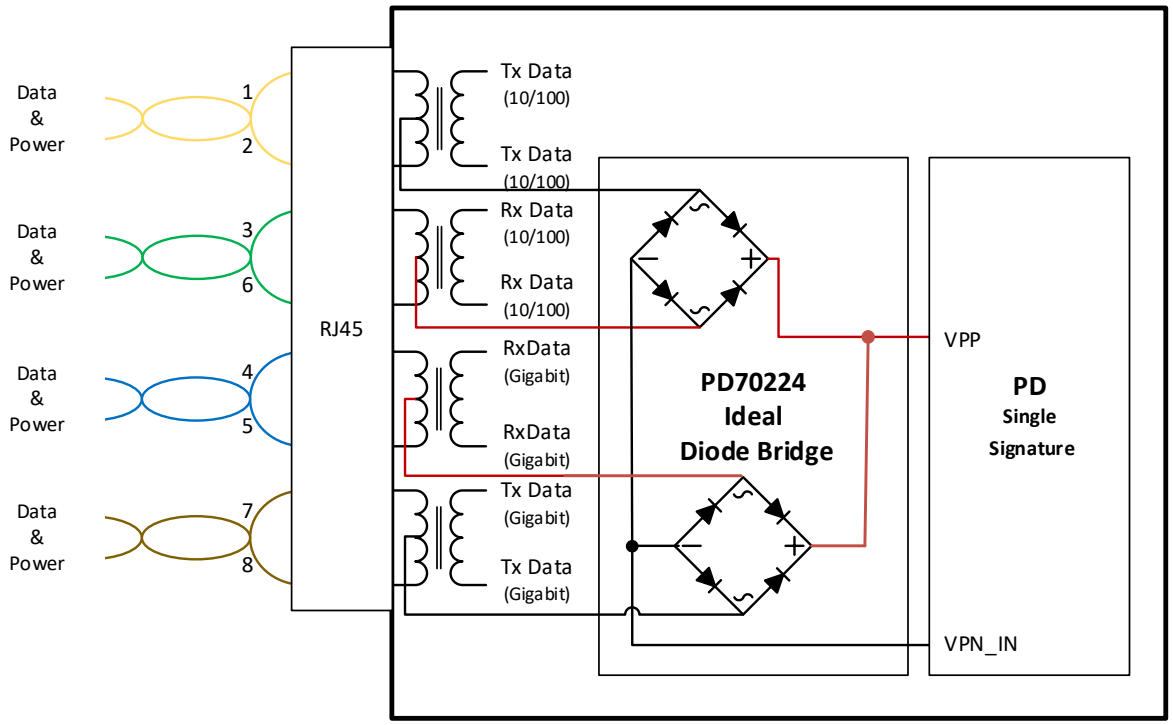
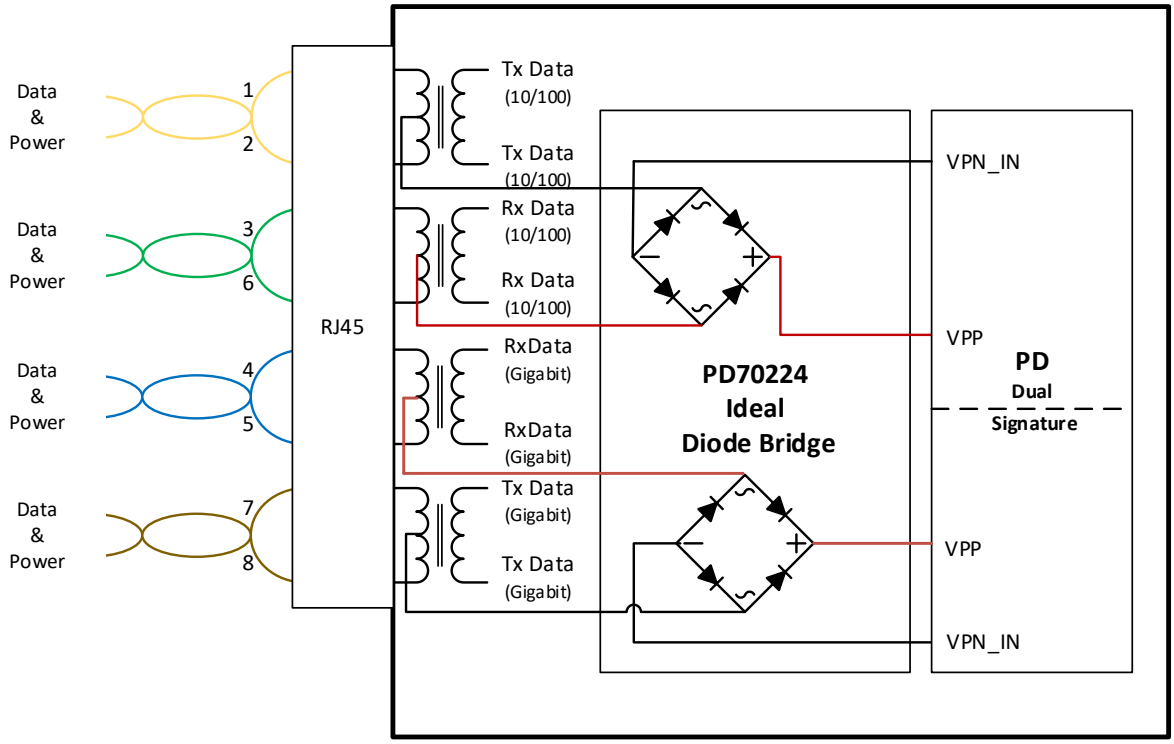


Figure 10. PD 4 pair DSPD Implementation



4.3.2 Controller Set Up

One logical port is implemented by utilizing 2 physical ports of the PD69208M/T4 PoE Manager as described above. Each physical 2-pair port delivers a maximum of 30W/45Wof power, enabling delivery of 60W/90W over 4 pairs. The 4 pairs which is two physical ports is considered as one logical port by the PoE firmware. The two physical ports each drive separate 2 pairs which connect together inside the PD after the serial diodes as shown in Figure xx or can be separated to implement a dual signature PD architecture.

The ports will be managed by PD692x0 with certain rules. The PD692x0 can support up to 48 logical 4-pairs ports (96 physical ports).

The Host should set command values in the port conversion matrix according to PCB layout. Programming this matrix sets the internal port numbering arrangement with respect to the Host system port numbering. This matrix feature gives the designer flexibility in laying out PCB traces. The command supports a mix of 4-Pair / 2-Pair configurations, as well as any combination of AF, AT and BT power levels. The command supports up to 48 logical ports (0 to 47) and up to 96 physical ports (0 to 95). Port count starts from 0 in system and in device. Device numbering is based on SPI address settings. (The lowest address that responds to MCU messaging is treated as the 1st device). The automatic device search is performed after any MCU Reset. Physical port numbering should be calculated based on the number of valid PoE device addressing and the number of supported ports on each device.

The following instructions describe how to define a 4-pair port using Microchip's GUI or communication protocol commands via direct UART or I^2C commands to the PD692x0 according to the communication protocol.

4.3.2.1 Set Temporary Matrix

To use the GUI, run "PoE Manager Enhanced Mode GUI" which is available on Microchip's Software Library at https://www.microchip.com/doclisting/SoftwareLib.aspx

Set the ports matrix in the "Matrix" tab on the GUI. Set ports matrix to program the physical ports with respect to the logical numbering. Make sure that no physical port is set to two separate logical ports. In the example below on the example below ports 0,1,2 & 3 are set as 2-pair ports utilizing physical ports 0,1,2 & 3, and ports 4-8 are set as 4-pair ports utilizing physical ports 4+5,6+7,8+9,10+11. See Figure 11.

To set the "matrix" via direct I^2C or UART commands "Set temporary Matrix" command. A detailed description how to set the matrix can be found in the "PD69200_BT-PoE_Communication_protocol" document. See Figure 12

Figure 11. Set Temporary Matrix via GUI

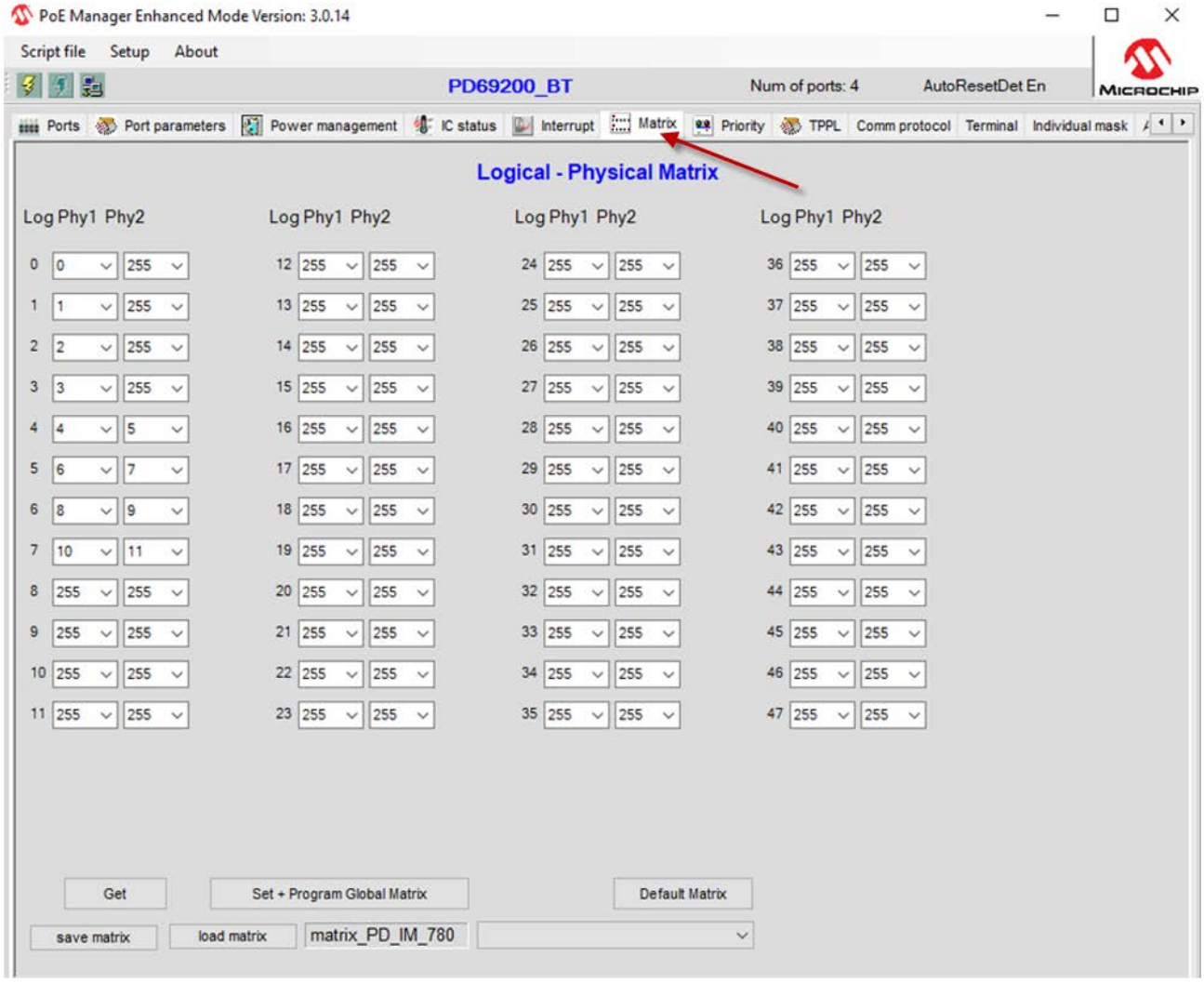


Figure 12. Set Temporary Matrix via I²C or UART

4.3.1 Set Temporary Matrix

[0] KEY	[1] ECHO	[2] SUB	[3] SUB1	[4] SUB2	[5] DATA	[6] DATA	[7] DATA	[8] DATA	[9] DATA	[10] DATA	[11] DATA	[12] DATA
0x00	##	0x05	0x43	Val	Val	Val	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E
Command		Channel	TmpMatrix	CH Num	Physical Number A	Physical Number B	N	N	N	N	N	N

4.3.2.2 Program Temporary Matrix as Active Matrix

The matrix is not yet loaded as the working matrix until it is set as the active matrix. To program the temporary matrix as the active matrix press the "Set+Program Global Matrix" button in the "Matrix" tab (Figure xxx) on the GUI or use command "Program Global Matrix" (Figure xxx)

Figure 13. Load Temporary Matrix via GUI

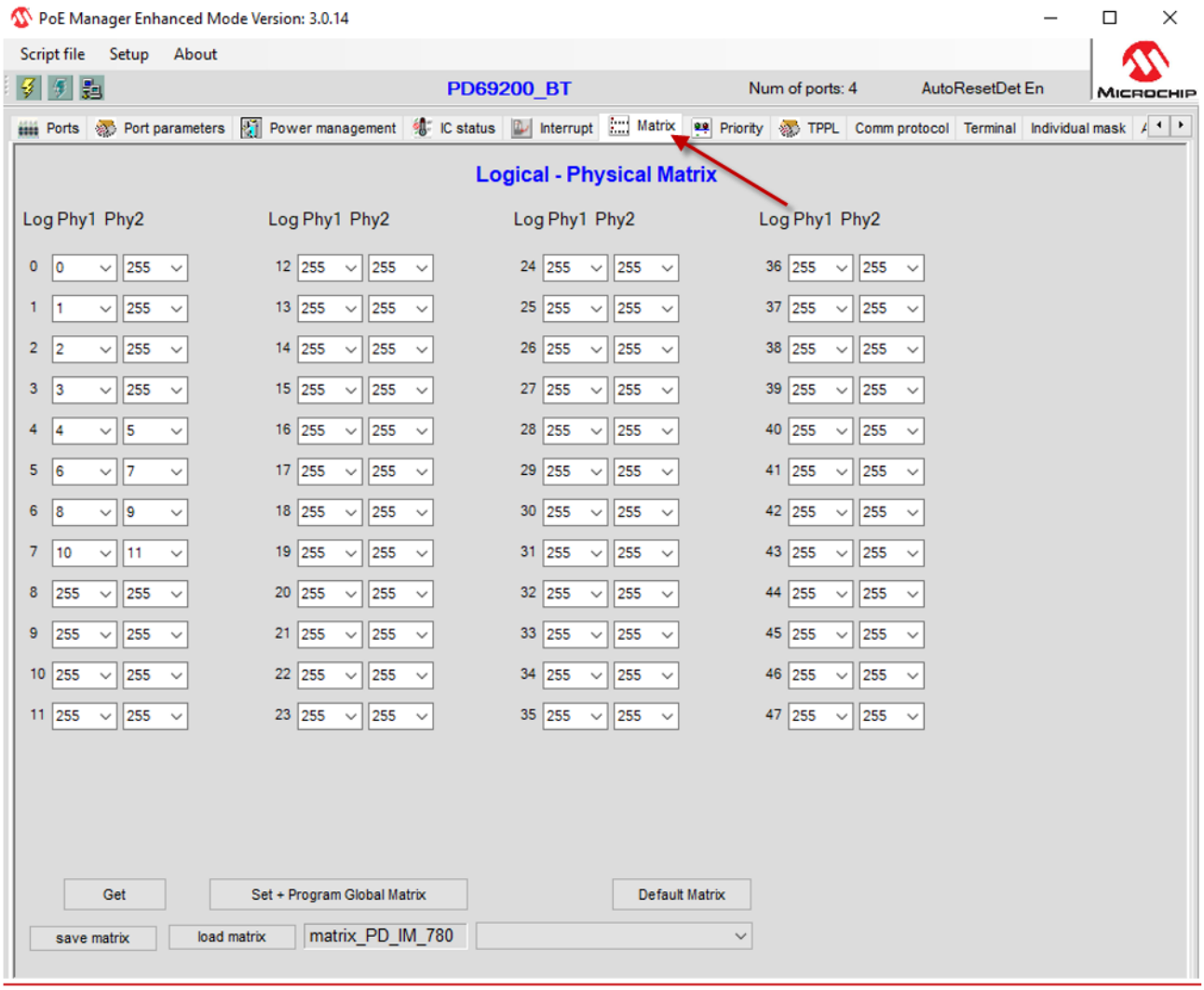


Figure 14. Load Temporary Matrix via I²C or UART

4.3.3 Program Global Matrix

[0] KEY	[1] ECHO	[2] SUB	[3] SUB1	[4] SUB2	[5] DATA	[6] DATA	[7] DATA	[8] DATA	[9] DATA	[10] DATA	[11] DATA	[12] DATA
0x00	##	0x07	0x43	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E
Command		Global	TmpMatrix	N	N	N	N	N	N	N	N	N

This command causes temporary matrix values to be copied into the active working matrix. Upon completion of this command, and successful matrix validation, the active matrix is updated, PD69200 software is restarted and the status of PoE ports is refreshed according to the new matrix. During this flow ports will be disconnected.

4.3.2.3 Set Port Power Level

To set ports power level, use the Port Parameter Tab on the GUI (Figure xxx) or use Command "Set BT port Parameters" (Figure xxx). For details about each field refer to the "PD69200_BT-PoE_Communication_protocol" document

Figure 15. Set Power Levels via GUI

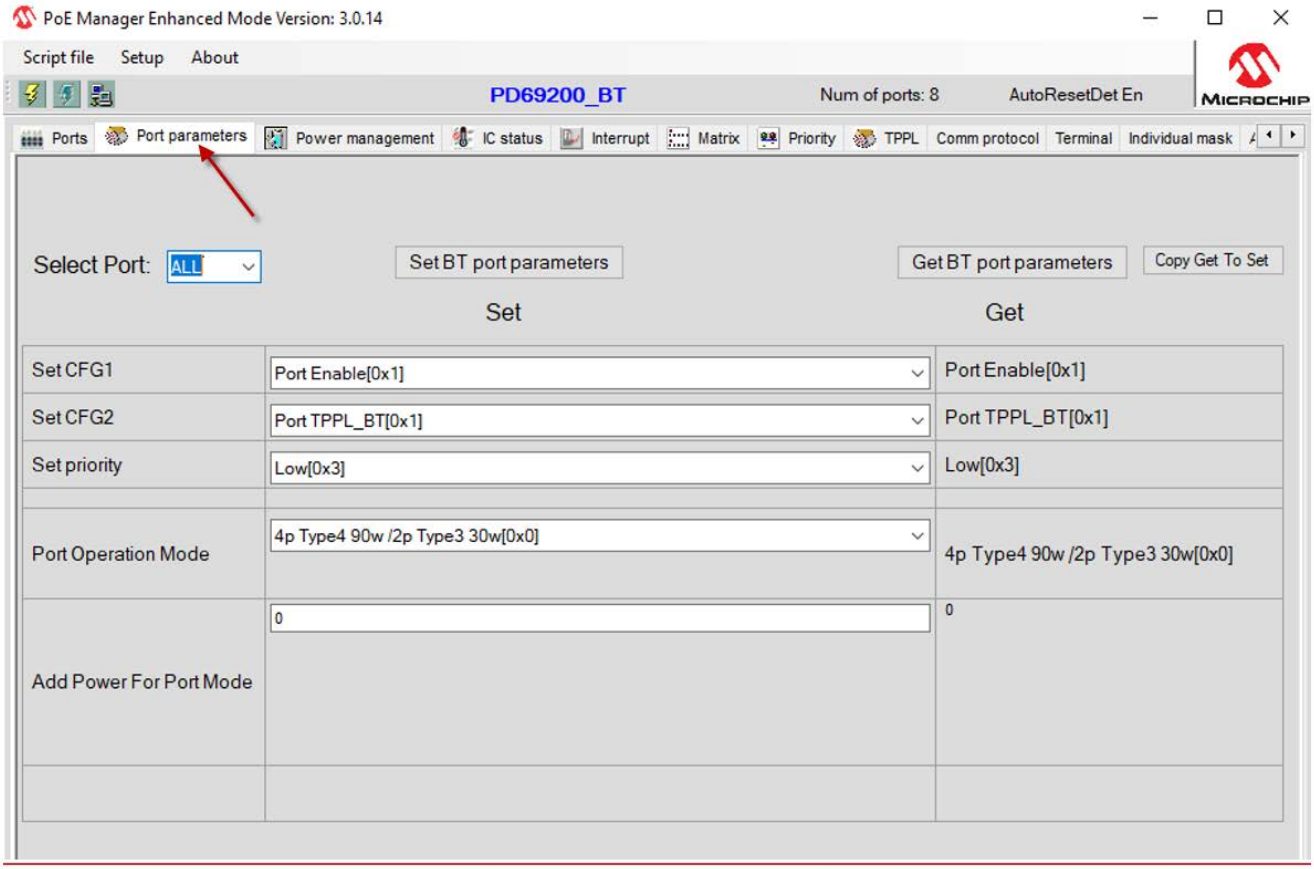


Figure 16 Set Power Levels via I²C or UART

4.3.6 Set BT Port Parameters

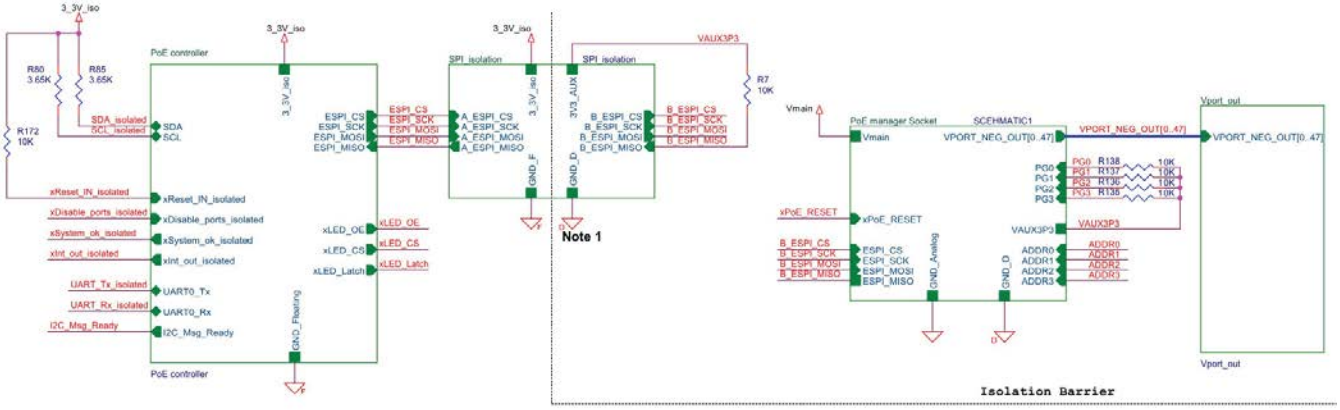
[0] KEY	[1] ECHO	[2] SUB	[3] SUB1	[4] SUB2	[5] DATA	[6] DATA	[7] DATA	[8] DATA	[9] DATA	[10] DATA	[11] DATA	[12] DATA
0x00	##	0x05	0xC0	Val	Val	Val	Val	Val	0x4E	0x4E	0x4E	0x4E
Command		Channel	BT Port Config1	Port Num	Port Mode CFG1	Port Mode CFG2	Port Operation Mode	Add Power for Port Mode	Priority	N	N	N

This command can set various configuration parameters of a single port or apply the configuration to all system ports.
The command can enable/disable port operation, enable/disable legacy capacitor support, set the power limit,set the priority and set the PM mode of the BT port.

5 Schematics

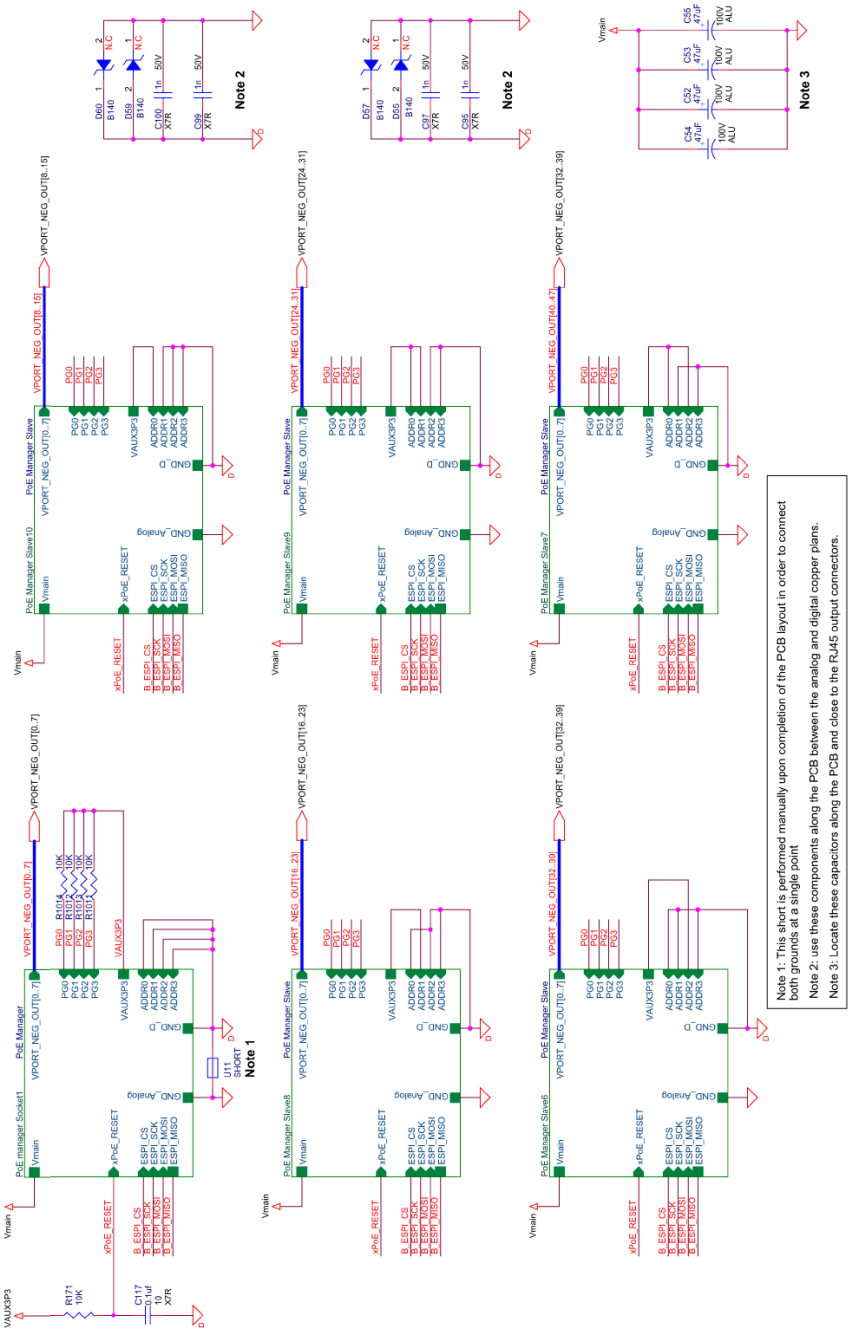
The following section shows the detailed device level schematic and BOM of a 48-physical port system based on six PD69208 Managers and a single PD69200 or PD69210 Controller. These 48 physical ports may be configured as described in Section 4 as 48 2-pair ports or 24 4-Pair ports. This schematic will meet Surge as defined in EN 61000-4-5:2006. For higher level of surge protection, such as ITU-Tk.21 - 2018 please see AN-205 (Document Number PD-000392048).

Figure 17 • 48-port System Main Blocks



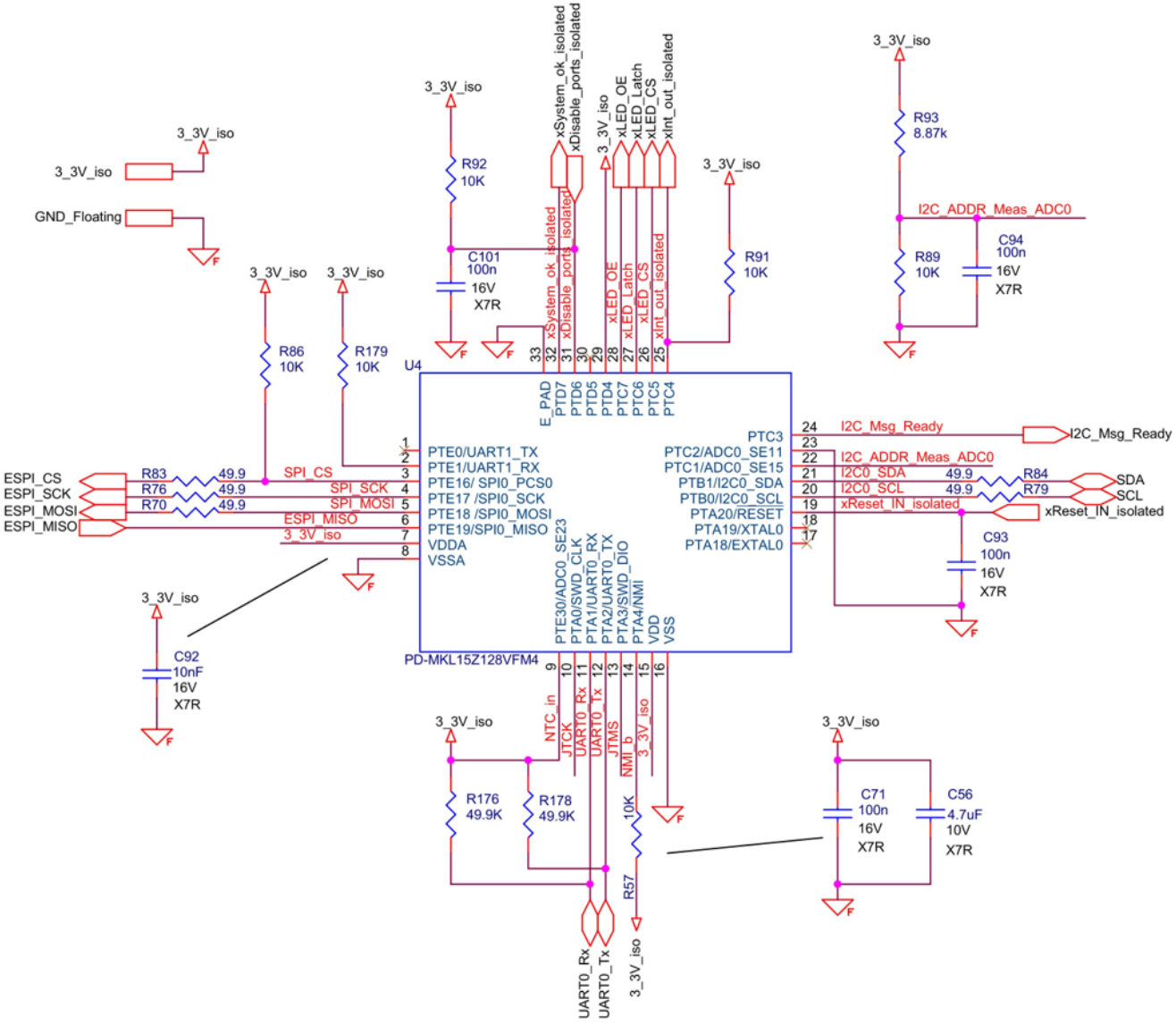
The following figure shows the six PD69208 PoE manager circuitry. For descriptions and more information, see Vmain Capacitors.

Figure 18 • 48-port PoE Manager Blocks



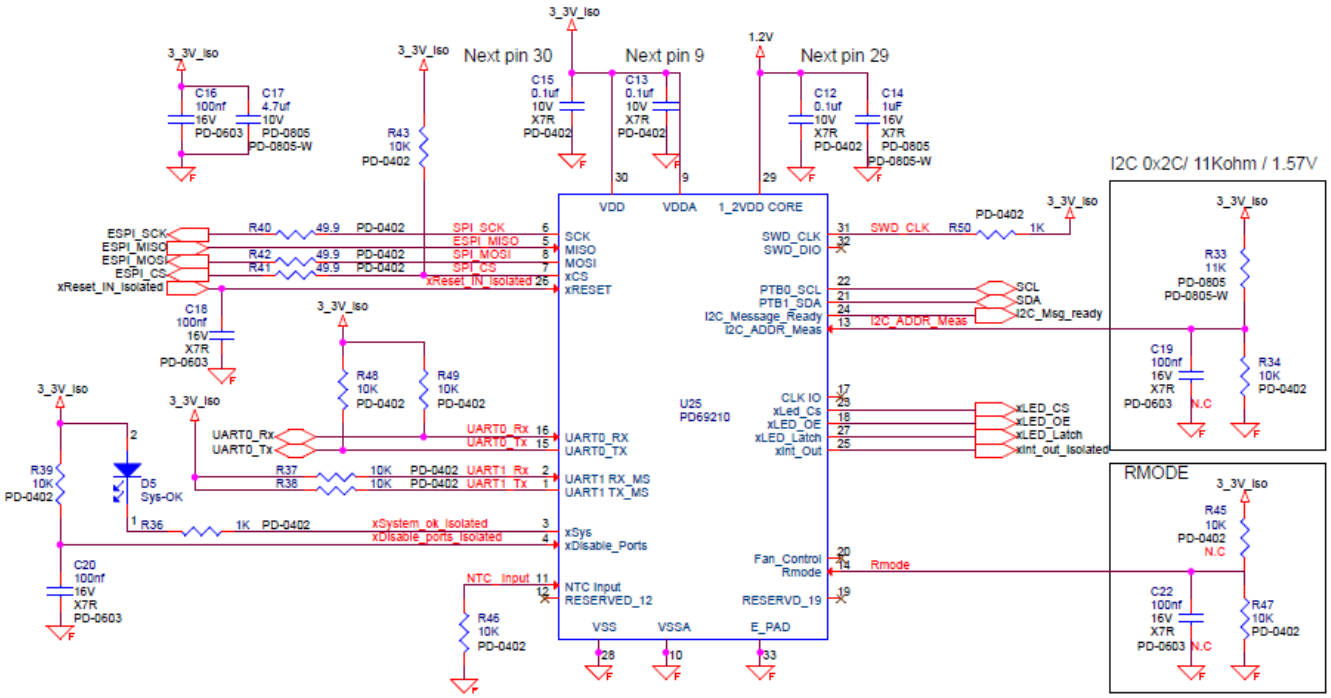
The following figure shows the PD69200 PoE controller circuitry. For descriptions and more information, see PD69200 PoE Controller Circuitry. In an actual circuit design either the PD69200 (Figure 9) or the PD69210 (Figure 10) Controller is used. The PD69210 is recommended for all new designs, the PD69200 should only be used for Legacy designs.

Figure 19 • PD69200 PoE Controller Circuitry



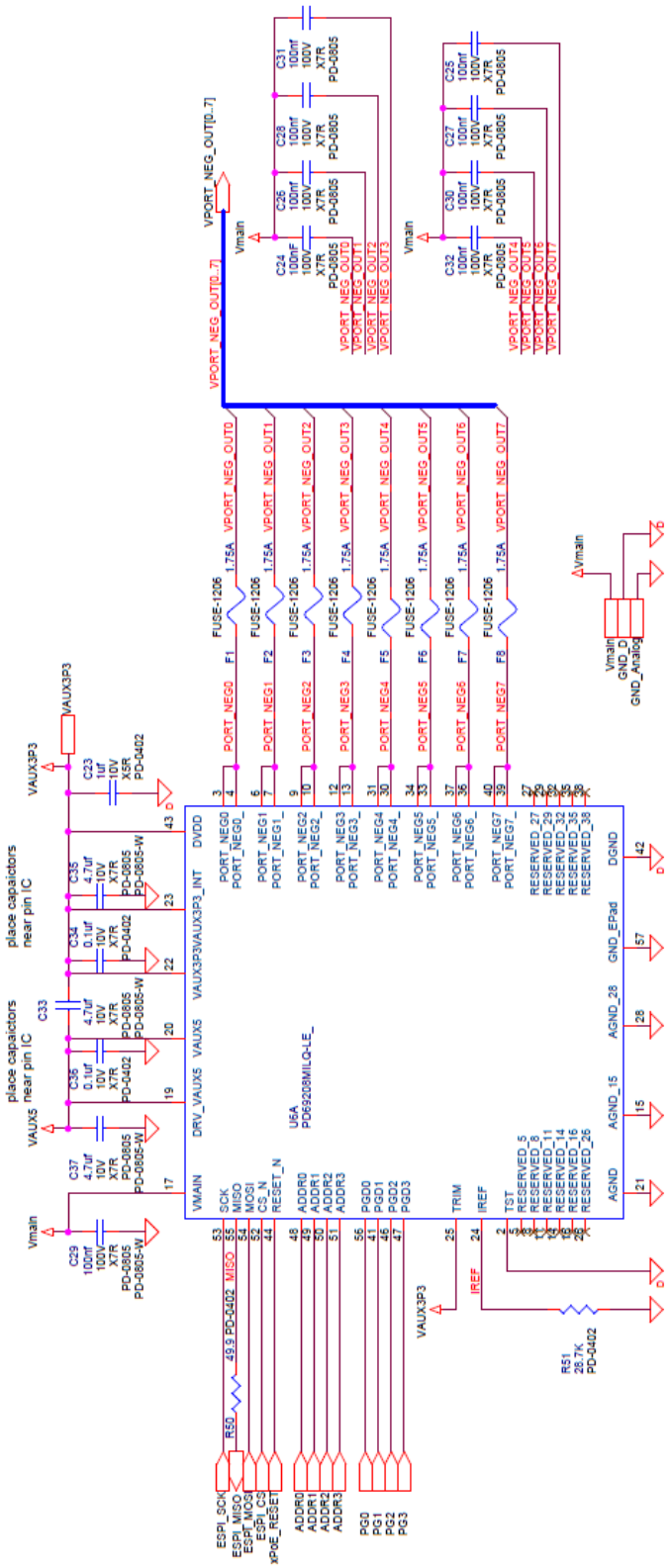
The following figure shows the PD69210 PoE controller circuitry. For more information, see PD69210 PoE Controller Circuitry. In an actual circuit design either the PD69200 (Figure 9) or the PD69210 (Figure 10) Controller is used. The PD69210 is recommended for all new designs, the PD69200 should only be used for Legacy designs.

Figure 20 • PD69210 PoE Controller Circuitry



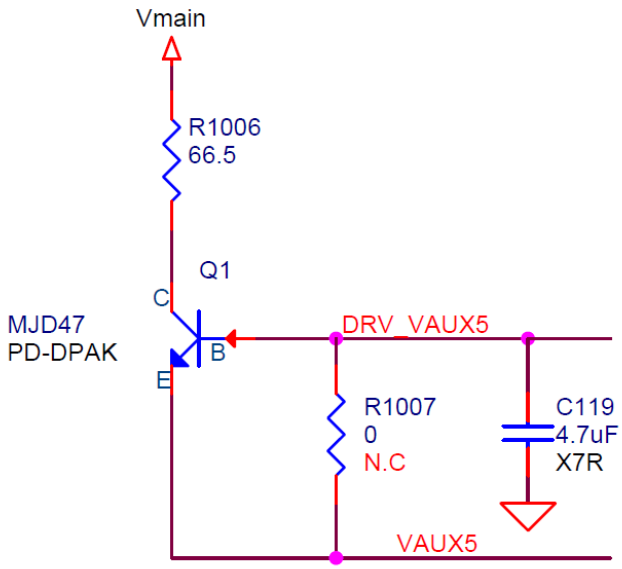
The following figure shows the PD69208 circuitry for PoE manager number 0. For descriptions and more information, see PoE Manager Circuitry.

Figure 21 • PD69208 PoE Manager Circuitry



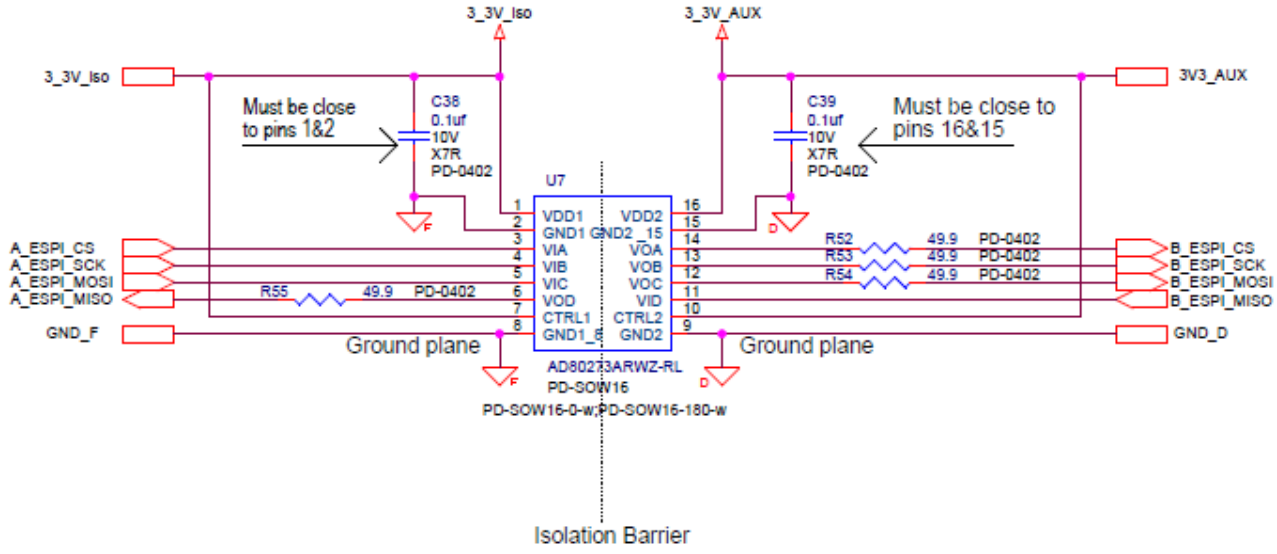
The following figure shows the optional boost transistor to the 5 V_{DC} regulator. For descriptions and more information, see 5 VDC and 3.3 VDC Regulators.

Figure 23 • (Optional) Boost Transistor to the 5 VDC Regulator



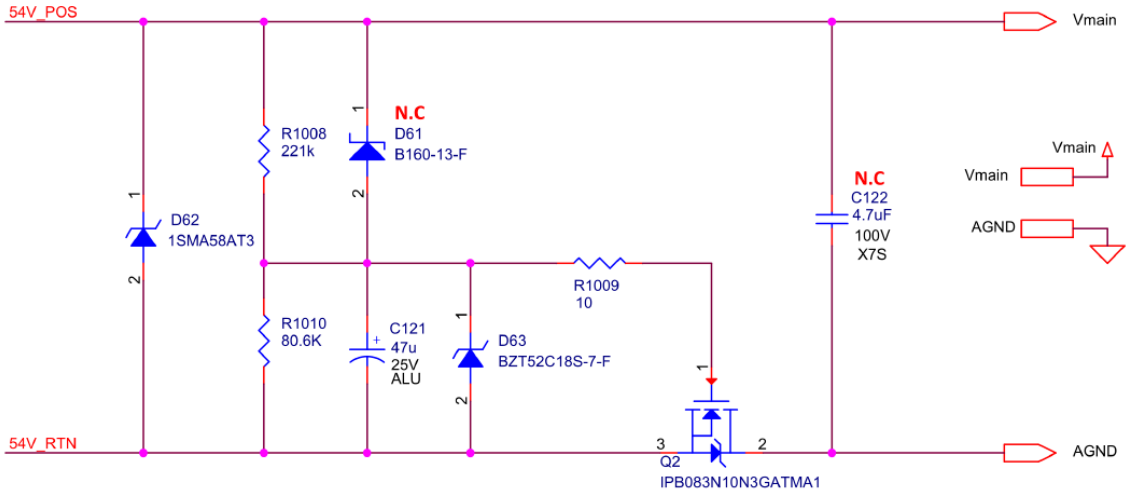
The following figure shows the digital isolator. For descriptions and more information, see Communication Interfaces/Isolation.

Figure 22 • Digital Isolator



The following figure shows the hot-swap circuit. For descriptions and more information, see Hot-swap Circuit.

Figure 23 • Hot-Swap Circuit



6 Bill of Materials for a 48 Port PoE System

The following tables list the bill of materials for a PoE system.

Table 5 • 48-port System Main Blocks Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
2	R80 R85	3.65 KΩ	3.65K 62.5 mW 1% 0402	Yageo	RC0402FR-073K65L
6	R7 R135 R136 R137 R138 R172	10 KΩ	10K 1% 62.5 mW 0402	Vishay	CRCW040210K0FKED

Table 6 • 48-port PoE Manager Blocks Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
4	C52 C53 C54 C55	47 µF	Capacitor ALU 47 µF 100 V 20% 8 x 11.5 105 °C	Rubycon	100PX47M T7 8X11.5
4	C95 C97 C99 C100	1 nF	Capacitor X7R, 1 nF 50 V 10% 0402	Murata	GRM155R71H102KA01D
4	D55, D57, D59 D60	B140	Schottky diode 40 V 1 A SMAT	Diodes Inc.	B140
4	R1111 R1112 R1113 R1114	10 KΩ	10K 1% 62.5 mW 0402	Vishay	CRCW040210K0FKED

Table 7 • PD69200 PoE Controller Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
4	C71, C93, C94, C101	100 nF	Capacitor 100 nF 16 V 10% X7R 0603	Samsung	CL10B104KO8NNNC
1	C56	4.7 µF	Capacitor 4.7 µF 10 V 10% X5R 0805	Taiyo Yuden	LMK212BJ475KD-T
1	C92	10 nF	Capacitor X7R 10 nF 16 V 10% 0402	Samsung	CL05B103KO5NCNC
6	R57, R86, R89, R91, R92, R179	10 KΩ	10K 100 mW 1% 0603	Samsung	RC1608F1002CS
2	R176, R178	49.9 KΩ	49.9K 125 mW 1% 0805	Samsung	RC2012F4992CS
5	R70, R76, R83, R79, R84	49.9 Ω	49.9R 1% 62.5 mW 0402	Yageo	RC0402FR-0749R9L
1	R93	8.87 KΩ	8.87K 125 mW 1% 0805	Yageo	RC0805FR-078K87-L
1	U4	PD69200	PoE PSE controller	Microsemi	PD69200X-GGGG

Table 8 • PD69210 PoE Controller Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
1	U25	PD69210	POE PSE controller	Microchip	PD69210-gggg[1]
10	R34 R37, R38, R39 R43, R45, R46 R47, R48, R49	10 KΩ	10K 1% 62.5 mW 0402	Bourns	CR0402-FX-1002GLF
2	R36[2], R50	1 KΩ	1K 1% 62.5 mW 0402	Bourns	CR0402-FX-1001GLF
3	R40, R41, R42	49.9 KΩ	49.9R 1% 62.5 mW 0402	Bourns	CR0402-FX-49R9GLF
1	R33	11 KΩ	11K 125mW 1% 0805	Samsung	RC2012F1102CS
3	C12, C13, C15,	0.1 µF	CAP CER 0.1 µF 10 V X7R 10% 0402 SMT	Nic	NMC0402X7R104K10TRP
1	C14	1 µF/16 V	CAP CRM 1 µF 16 V 10% 0805 X7R SMT	Murata	GRM21BR71C105KA01
1	C17	4.7 µF/10 V	CAP CRM 4.7 µF 10 V 10% X5R 0805 SMT	Taiyo Yuden	LMK212BJ475KD-T
5	C16, C18, C19 C20, C22	0.1 µF	CAP CRM 100nF 16V 10% X7R 0603 SMT	Taiyo Yuden	EMK107B7104KA-T
1	D5[2]	Sys-OK	LED SuperYelGrn 100-130o 20-40mcd h=1 0603 SMD	Everlight	19-21-SYGCS530E3TR8

1 - gggg refers to the firmware version.

2 – Optional Component

Table 9 • PD69208 PoE Manager Circuitry Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
8	C24–C32	100 nF	Capacitor 100 nF 100 V 10% X7R 0805	Samsung	CL21B104KCFSFNE
3	C33, C35, C37	4.7 µF	Capacitor 4.7 µF 10 V 10% X5R 0805	Murata	GRM219R61A475KE19D
2	C34, C36	0.1 µF	Capacitor 0.1 µF 10 V X7R 10% 0402	Murata	GRM155R71A104KA01J
1	C23	1.0 µF	Capacitor 1.0 µF 10 V X5R 10% 0402	Panasonic	ECJ-0EB1A105M
1	R51	28.7 KΩ	28.7K 125 mW 1% 0805 (For PoH and IEEE 802.3bt, 99 W should be 0.1%)	Vishay	CRCW080528K7FKEA
1	R50	49.9 Ω	49.9R 1% 62.5 mW 0402	Bourns	CR0402-FX-49R9-ELF
1	U6A	PD69208	8 Port PSE PoE Manager SMT	Microsemi	PD69208T4/M/PD69204T4
8	F1–F8	1.75 A		Bourns	SF-1206SP175L-2-A9[1]

1 - Special part number for Microsemi PoE applications; preferential pricing for Microsemi customers.

Note: Fuses per port are not required for use in circuits with a total power level of up to 3 kW. This is because PD69208 is a UL 2367 (category QVRQ2)-recognized component and fulfills limited power source (LPS) requirements of the latest editions of IEC60950-1 and EN60950-1. However, IEC62368-1 ED3 which was released in October 2018 and becomes effective December 2020 requires per port fuses for a system power supply greater than 250 W.

Table 10 • (Optional) Boost Transistor to the 5 VDC Regulator

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
1	Q1	1A 250V V_{CEO}	DPAK – High Voltage Power Transistor	ON Semi	MJD47
1	C119	4.7 µF	Capacitor 4.7 µF 10 V 10% X5R 0805	Taiyo Yuden	LMK212B7475KG-T
1	R1006	66.5Ω	5% 125mW 0805	Yageo	GRM155R71A104KA01J
1	R1007	0Ω	0402	Yageo	RC0402JR-070RL

Table 11 • Digital Isolator Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
2	C38, C39	0.1 µF	Capacitor 0.1 µF 10 V X7R 10% 0402	Murata	GRM155R71A104KA01J
4	R52, R53, R54, R55	49.9 Ω	49.9R 1% 62.5 mW 0402	Yageo	RC0402FR-0749R9L
1	U7	AD80273ARWZ	IC digital isolator SO16	Analog Devices	AD80273ARWZ-RL[1]

1 - Special part number for Microsemi PoE applications; preferential pricing for Microsemi customers.

Table 12 • Hot-swap circuit Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
1	Q2	IPB083N10N3	MOSFET N-CH 100 V 80 A 8.3 mΩ TO263-3	Infineon	IPB083N10N3GATMA1
1	C121	47 µF	Capacitor ALU 47 µF 25 V 20% SMT	SUNCON	25CE47FS
1	R1008	221 KΩ	221K 1% 1/10 W 0603	Yageo	RC0603FR-07221KL
1	R1010	80.6 KΩ	80.6K 125 mW 1% 0603	ASJ	CR16-8062FL
1	R1009	10 Ω	10.0R 1% 62.5 mW 0402	Yageo	RC0402FR-0710R0L
1	D63	BZT52C18S-7-F	Diode Zener, 18 V 200mW SOD323	Diodes Inc.	BZT52C18S-7-F
1	D62	1SMA58AT3	DIO TVS 58 V 40 A SRG400WPK SMA SMT	ON Semiconductor	1SMA58AT3

7 Layout Guidelines

This section provides detailed information and PCB design guidelines for the implementation of a 48-port PoE system, based on Microsemi's PD69208 8-channel PoE manager.

7.1 Isolation and Termination

According to PoE standards, certain isolation requirements need to be met in all the PoE equipment. In addition, EMI limitations should be considered, as specified in the FCC and European EN regulations. These requirements are considered by the PoE switch vendors while designing the switch circuitry. However, when a PoE manager is integrated into a switch, special design considerations must be met because of the unique combination of data and power circuitries.

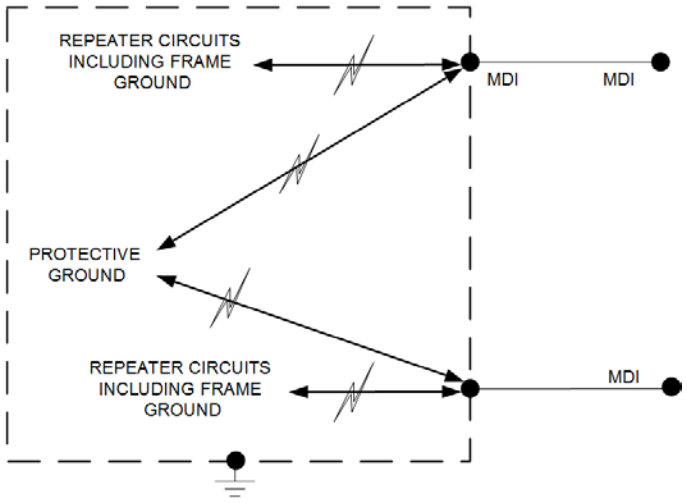
The following sections define the requirements and provide recommendations for their implementation in an effort to assist designers in meeting those requirements, while also integrating Microsemi's PoE chipset and its daughter boards.

7.1.1 Isolation

As specified in the IEEE PoE standards, 1500 V_{RMS} isolation is required between the switch's main board circuitry (including protective and frame ground) and the media dependent interface (MDI).

The following figure shows the overall isolation requirements.

Figure 24 • Isolation Requirements



Reference to environment A
1. IEEE 802.3 Repeater 500 Vrms min. (27.5.3.1 ;9.7.1)
2. IEEE 802.3 Repeater, PMA to MDI 1500 Vrms min. (23.5.1.1)
3. UL1950: 1500 Vrms

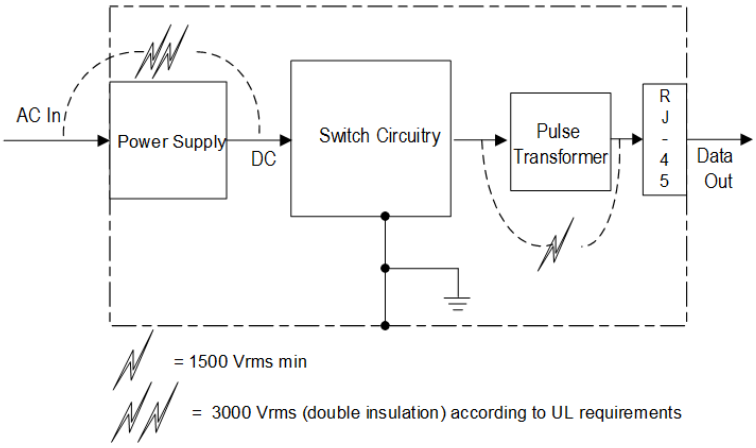
1500 =Vrms min.

PMA :Physical Medium Attachment
MDI :Media Dependent Interface

7.1.2 High Voltage Isolation

For a switch with no PoE circuitry, isolation requirements between the physical inputs and the data connectors are met by using an isolated AC/DC power supply and isolated pulse transformers, as shown in the following figure.

Figure 25 • Standard Switch Circuitry

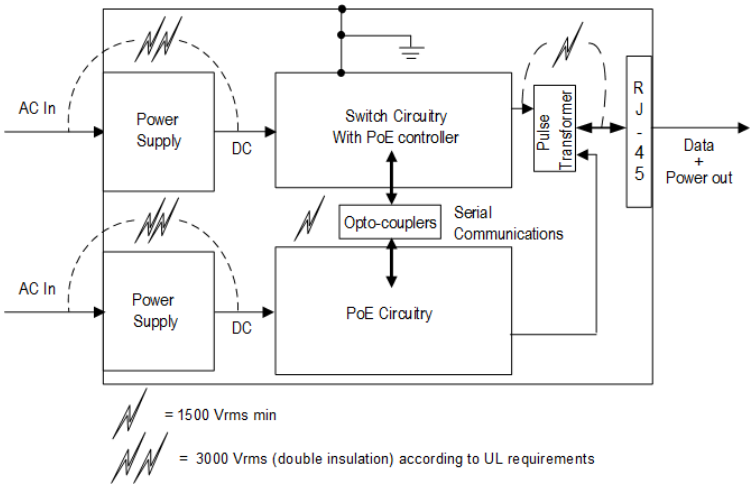


When integrating PoE circuitry into a switch, the output power can be supplied through the central tap of the pulse transformer's secondary side (unless the power is provided over the spare pairs). This connectivity can bypass the pulse transformer's isolation if the PoE ground or DC input is connected to the switch's circuitry/ground.

To comply with these isolation requirements, the PoE managers must be isolated in regards to all other switch circuitries. Use one of the following methods.

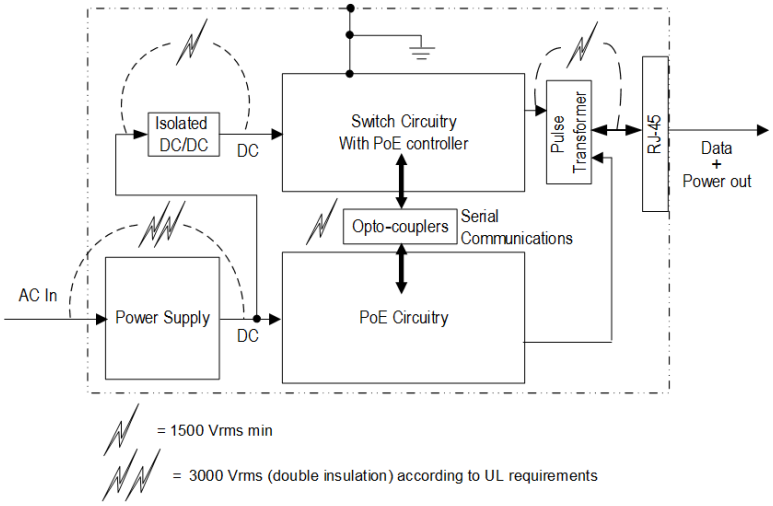
- A separate DC input for the switch and the PoE circuitry and isolated serial communication between the PoE circuitry and the switch circuitry, as shown in the following figure.

Figure 26 • Switch Circuitry with Two DC Source



- A single DC input (separate power supplies) for both the switch and PoE circuit as well as additional or integrated isolated DC/DC circuitry for the switch input and isolated serial communication port between the PoE circuitry and the switch's circuitry, as shown in the following figure.

Figure 27 • Switch Circuitry with a Single DC Source

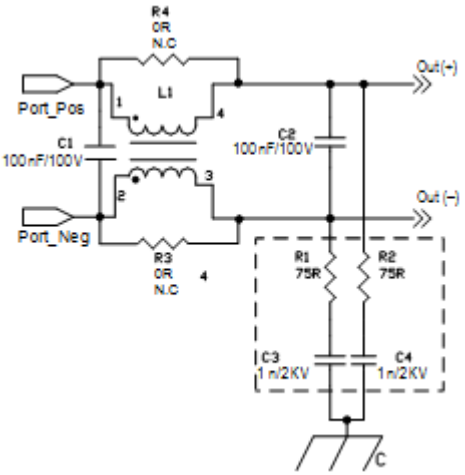


To maintain 1500 V_{RMS} isolation between two adjacent layers of a NEMA FR-4 multi-layer PCB, a minimum of 15 mils isolation thickness is recommended to provide a safe margin for hi-pot requirements.

7.1.3 PoE Output Ports Filtering and Terminations

A switch normally creates a noisy environment. To meet EMI requirements, high filtering and line terminations may be needed when connecting the PoE circuit outputs to the switch circuitry, as shown in the following figure.

Figure 28 • Recommended EMI Filter



Note: In most PoE systems, it is recommended to use 0 Ω resistors for R1 and R2. However, certain systems may benefit from 75 Ω resistors. Filtering provisions should be made. In quiet PoE systems, the EMI filter can be replaced (bypassed) using R3 and R4.

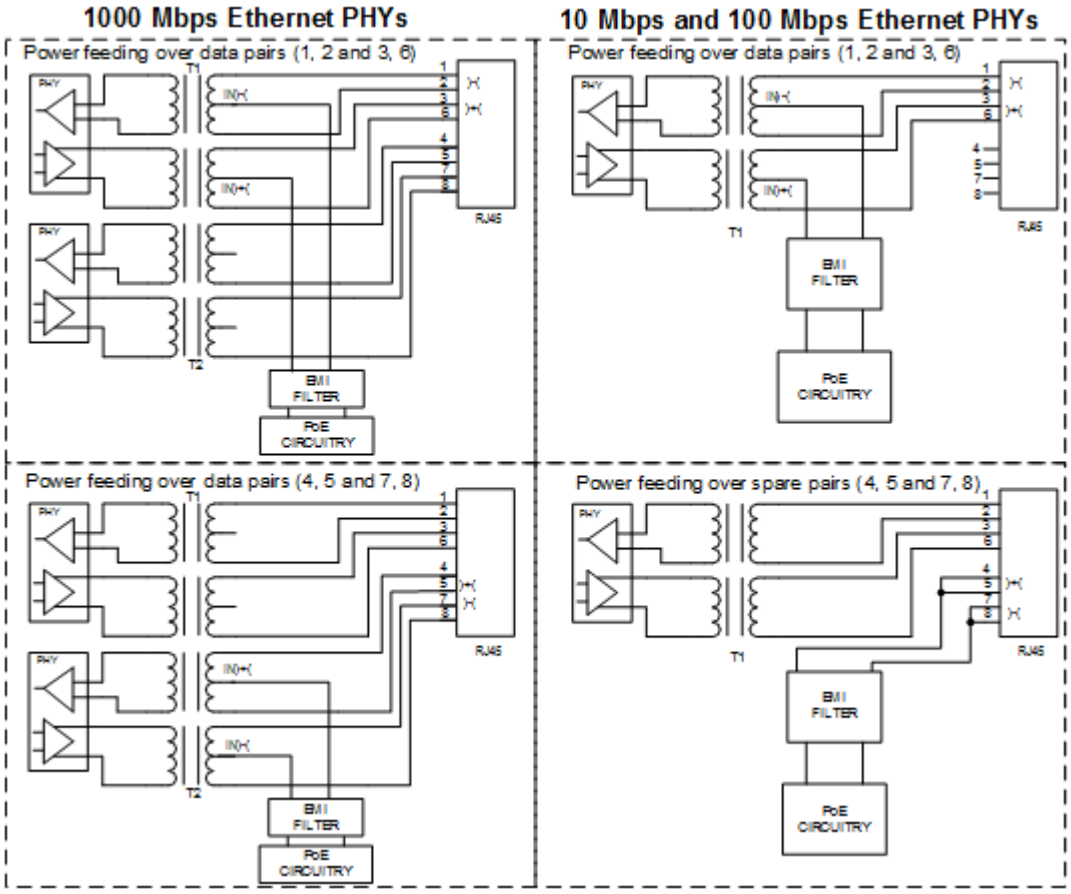
A circuitry for the recommended filter includes the following.

- A common mode choke for conducted EMI performances (such as ICE CS01 series)
- Output differential cap filter for radiated EMI performances
- Y-capacitive/resistive network to chassis as each system is a unique EMI case, this circuit is a good starting point for EMI suppression.

Note: For best EMI performance and to avoid additional noise accumulated on the lines between the filter and the port connectors, it is recommended to implement this circuitry on the switch's main board, located as close as possible to the port connectors.

As specified in the IEEE PoE standards, PoE output power can be supplied over the data pairs or the spare pairs. Both the methods are shown in the following figure where an MDI-X (or Auto MDI-X) connection is associated with the switch.

Figure 29 • Output Ports Design Details



7.1.4 Isolating the Stacked Modular Jack Assembly

The IEEE PoE standards require 1500 V_{RMS} isolation between PoE voltages and frame ground (EGND). The RJ45 jack assemblies have a metal cover of 80 mils that almost reaches to the PCB surface. Maintain an 80 mils traces clearance between EGND traces for the RJ45 modular jack assembly metal covering and adjacent circuit paths and components. To prevent 1500 V_{RMS} isolation violation, it is necessary to provide layout clearances of PoE traces on the top layer, in the vicinity of the RJ45 connector assemblies.

PoE technology involves voltages as high as 57 V_{DC}. Therefore, plan adjacent traces for 100 V_{DC} operational creepage. Operational creepage should be maintained to prevent breakdown between traces carrying these potentials.

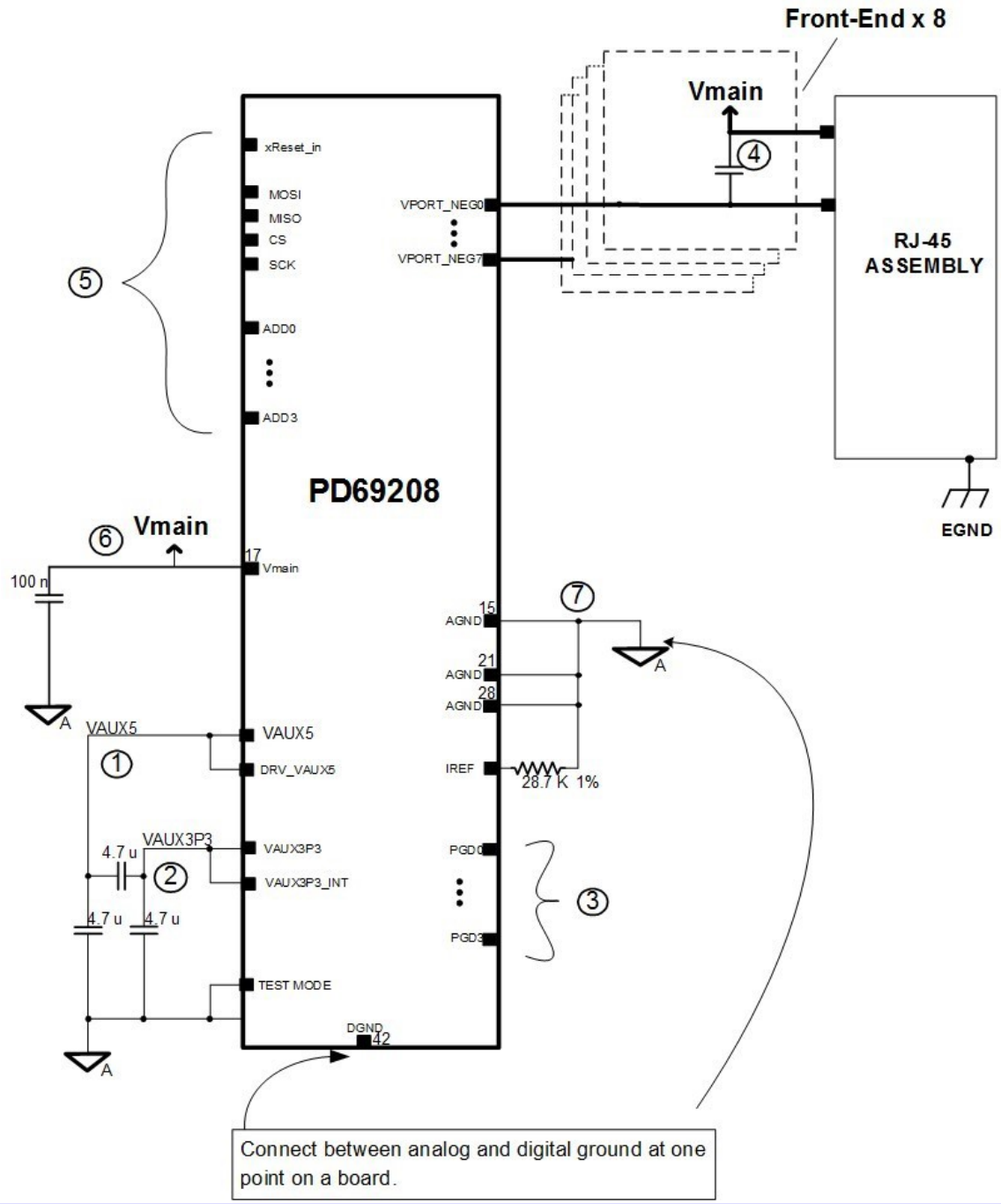
7.2 Guidelines

Microsemi's PD69208 PoE manager is designed to simplify the integration of PoE circuitry into switches based on the IEEE PoE standards. The pinout arrangement has been configured for optimal PCB routing.

The following figure shows the various circuits and elements surrounding the PD69208 PoE manager. This block diagram includes the following peripheral elements, identified by numbers.

- 5 V voltage source (VAUX5) (1)
- 3.3 V voltage source (VAUX3P3) (2) Power good inputs (3)
- Output capacitor used for filtering (4) ESPI bus, ESPI address lines (5)
- Vmain input (6)
- Analog ground/AGND (7)

Figure 30 • Component Identification for PD69208 Circuitry

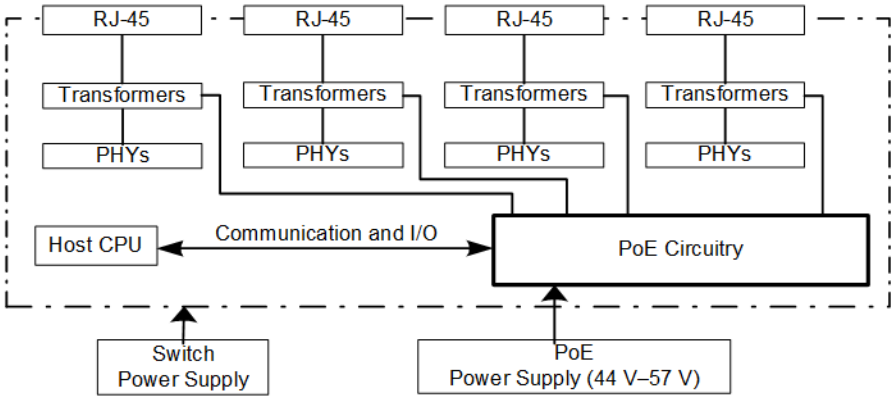


Note: The VAUX5 supply may include an external transistor connected to pin 20, to increase current drive for external circuitry. To prevent heat from being transferred to the PD69208, place this transistor away from the PoE managers.

7.2.1 Locating PoE Circuitry in a Switch

To minimize the length of high current traces as well as RFI pick-up, place the PoE circuitry as close as possible to the switch's pulse transformers. The circuit can be fully integrated into the switch's PCB, or can be easily placed on top of the switch's using a daughter board. Typical integration of PoE modules inside a switch is shown in the following figures.

Figure 31 • PoE Circuitry Inside the Switch



7.2.2 Ground and Power Planes

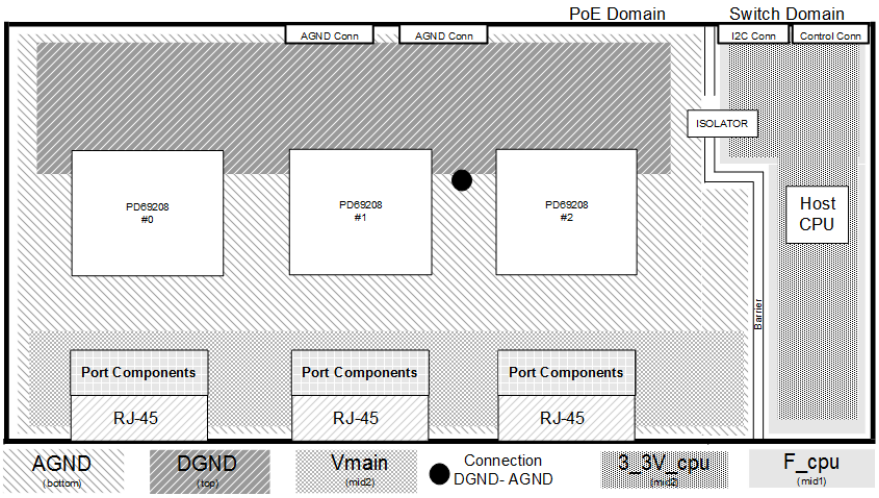
As the PoE solution is a mixed-signal (analog and digital) circuitry, care must be taken when routing the ground and power signals lines.

The reference design assumes a four-layer board such as, top, mid1, mid2, and bottom. The main planes are Vmain/AGND and DGND.

Ground planes are crucial for proper operation and should be designed in accordance with the following guidelines.

- Separate analog and digital grounds, with a gap of at least 40 mils.
- Analog ground plane (AGND) is utilized to transfer the heat generated by the PD69208. The AGND should be located on external layer.
- Earth ground is used to tie in the metal frame of the RJ45 connectors. This ground is to be routed separately and connected to the switch's metal chassis/enclosure.
- To prevent ground loop currents, use only a single connection point between the digital and analog grounds, as shown in the following figure.

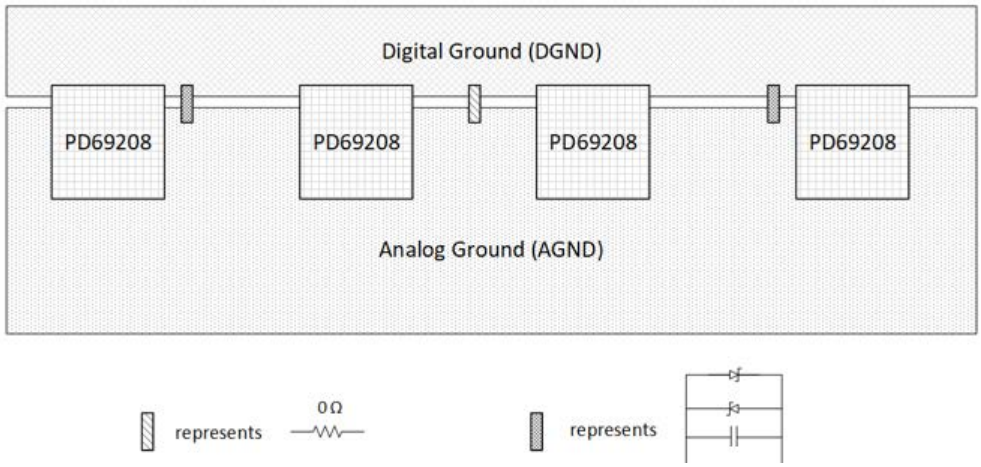
Figure 32• Ground and Power Planes



- To connect various digital ground (DGND) points and to enable stable impedance to the ESPI bus traces, extend the DGND surface under pins 41–56 of the PD69208 managers.

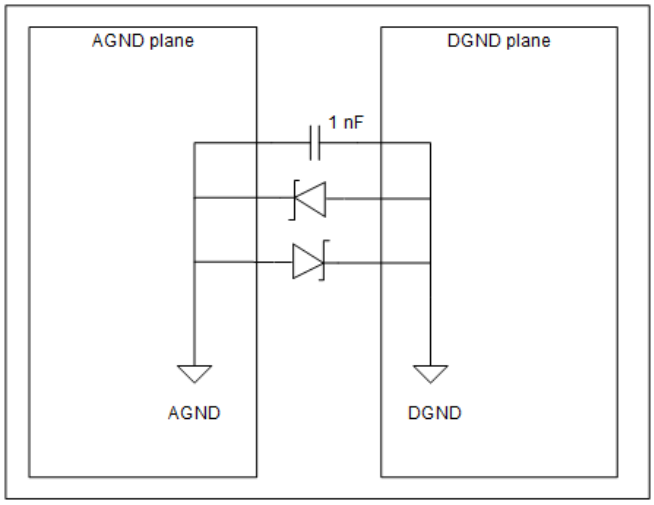
- A focal interconnection point for the digital and analog grounds should be located at about the middle of the overlapping section, as shown in the following figure.

Figure 33 • Single-Point Connection Between DGND and AGND



- Leave spacing for a ceramic 1 nF bypass capacitor and two parallel and inversed Schottky diodes near each PoE manager between the analog and digital layers, as shown in the following figure. The capacitors form low impedance paths for digital driving signals.

Figure 34 • Grounding Scheme

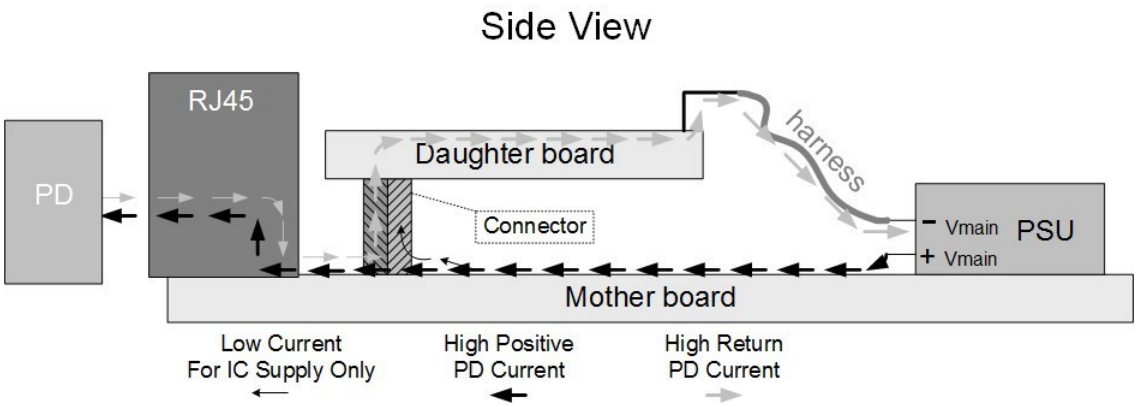


- The power and return (ground) planes for the 48 V supply must be designed to carry the system maximum continuous current, based on the design capacity. Minimize DC power losses on these planes by using wide copper lands. When implementing the PoE circuitry on a daughter board, the high current does not have to be routed through the daughter board but only the return path, as seen in Side View Component Identification for PD69208 Circuitry.

7.2.3 Current Flow through the PoE Application

The current flow through the PoE application is shown in the following figure.

Figure 35 • Component Identification for PD69208 Circuitry (Side View)



The port's DC current flows in an application utilizing a PoE daughter board (DB) as follows.

1. Coming from the switch's power supply positive to the center taps of the line transformer through a mother board wide trace (not through the DB)
2. From the center tap of the line transformer through the switch's RJ45 to the PD side
3. The return current from the PD flows through the RJ45 and the line transformer to the DB PoE circuitry
4. From the DB analog ground (AGND), the current flows back to the switch's power supply negative through harness.
   Note: The positive port's heavy current flows directly to the PD side without going through the PoE managers on the DB.

7.3 Specific Component Placement

The following section provides placement details for specific components.

7.3.1 Peripheral Components

To minimize heat transfer among various components, a gap between them should be maintained. The following are suggested gaps, but any gap can be used as long as the designer monitors the thermal performance during the design and follows the maximum temperatures allowed at the various components.

- Minimum gap between the PD69208 ICs should be 50 mm.
- Minimum gap between the PD69208 and the PoE controller should be 30 mm.
- Minimum gap between the PD69208 and the NPN transistor regulator (if used) should be 50 mm.

7.3.2 PoE Controllers and Peripherals

For PD69210, see Microchip Semiconductor **SAM D21 Family** datasheet for recommendations related to the PoE controller layout guidelines.

For PD69200, see the Freescale Semiconductor **MKL15Z128VFM4** datasheet for recommendations

related to the PoE controller layout guidelines.

The following guidelines are for the integration of the PoE controller into a PoE circuit.

- Locate the filtering capacitors for VDD and for VDDA close to power and ground pins.
- Termination resistors for the outgoing ESPI digital lines should be located close to the respective driving pins.

7.3.3 PD69208T4, PD69208M, or PD69204T4 PoE Manager and Peripherals

- The side of the PoE manager that includes pins 41–56 should face the DGND plane. These pins function as communication and control pins for the manager; connect between the PoE manager and the PoE controller through isolation circuitry.
- Locate the bypass capacitors for the PoE manager supply input close to the relevant pin. In cases where two bypass capacitors are placed on the same line, locate the lower valued capacitor closer to the pin on the same layer and place the higher valued capacitor at a more distant location.
- Locate the VAUX5 and VAUX3P3 0.1 µF and 4.7 µF filtering capacitors as close as possible to the PoE manager's pins 20 and 22, respectively.

7.3.4 Vmain Capacitors

It is a good design practice to have three 47 µF capacitors over V_{MAIN} to prevent noise and spikes events to penetrate into the V_{MAIN} rail.

7.4 Conductor Routing

The following sections describe the conductor routing guidelines.

7.4.1 General Guidelines

The conductor (or printed lands) routing is performed as practiced in the general layout guidelines, specifically listed as follows.

- Conductors that deliver a digital signal are routed between the analog and the digital ground planes.
- Avoid routing analog signals above the digital ground.

7.4.2 Specific Requirements for Clock and Sensitive Signals

Issues that require special design considerations:

- The I_{REF} resistor (connects to pin 24), used for current reference, must be directly connected to AGND and pin 24 using the shortest path.
- Route the ESPI communication clock (SCK) line coming from the PoE controller carefully so that it does not disturb the other lines. Two ground lines (connected to DGND) could be routed alongside the clock line to isolate it from the rest of the lines.

7.4.3 Port Outputs

For robust design, the port output traces are 45-mil wide to handle maximum current and port power. However, to obtain a 10 °C (maximum) copper rise under 1 A per port, set the minimum width for traces in accordance with the layer location and copper thickness, listed as follows.

- For two ounce copper, external layer: 15 mils
- For two ounce copper, internal layer: 20 mils
- For one ounce copper, external layer: 25 mils
- For one ounce copper, internal layer: 40 mils
- For 1/2 ounce copper, external layer: 30 mils
- For 1/2 ounce copper, internal layer: 55 mils (20 °C copper rise)

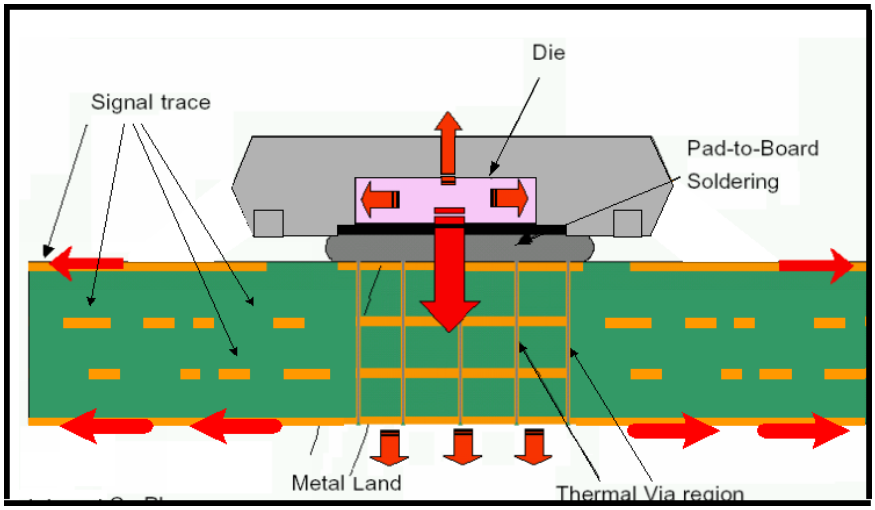
Additionally, the following port output guidelines should be considered.

- The port output traces must be short and parallel to each other to reduce RFI pickup and keep the series resistance low.
- The PoE port outputs must be connected to the switch's pulse transformers as shown in Output Ports Design Details). The common mode choke and Bob Smith termination (resistor- capacitor) to chassis ground are optional and used to reduce RFI noise. The circuit is located as close as possible to the pulse transformer.

8 Thermal Pad Design

The PD69208 exposed pad is a metal substrate on the bottom of the package. The attachment process for the exposed pad package is equivalent to standard surface mount packages.

Figure 36 • Heat Dissipation in PCB



For proper heat dissipation, the following footprint/layout guidelines must be followed.

- All thermal vias are connected to the AGND area under the PD69208.
- Via diameter should be approximately 0.3 mm with one-ounce copper barrel plating. Solder flow into the vias from the component side can result in voids during the solder process and this must be avoided.
- If copper plating does not plug the vias, apply stencil print solder paste onto the printed circuit side. This provides sufficient solder paste, filling those vias to avoid the mentioned voids. Top solder mask layer, lower layer, and internal layers copper plane show the associated solder printing masks (CS and PS). The solder mask openings are lined up with respect to the 7×7 thermal via array as large solder printing mask openings may result in poor release, the opening should be subdivided as shown in the preceding figure.
- Per IPC7093 standard standoff should be minimum of 2mil (0.050mm), with a MCHP recommended target of 2.5mil (0.0635mm). For this reason a solder mask stencil thickness of 5 mils should be considered.

See the **device datasheet** for package footprint guidelines.

9 References

The following documents can be obtained from Microsemi website.

- PD69208T4 and PD69210 Datasheet 8-Port PSE PoE Manager and PSE PoE Controller PD000357193
- PD69204T4 and PD69210 Datasheet 4-Port PSE PoE Manager and PSE PoE Controller PD000359832
- PD69208M and PD69210 Datasheet 8-Port PSE PoE Manager and PSE PoE Controller PD000359833
- Serial Communication Protocol user guide.

In addition, the following non-Microsemi documents can be consulted.

- IEEE 802.3af-2003 Standard, DTE Power via MDI
- IEEE 802.3at-2009 Standard, DTE Power via MDI
- IEEE 802.3bt-2018 Standard

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