Radiation-Tolerant PolarFire® FPGA Product Overview

Overview

Radiation-Tolerant (RT) PolarFire® FPGAs are derived from PolarFire, the fifth-generation family of non-volatile FPGA devices from Microchip, built on 28nm process technology. RT PolarFire FPGAs deliver the lowest power at high density, and integrate the industry's lowest power FPGA fabric. RT PolarFire also provides the lowest power transceiver lanes at 12.7 Gbps, built-in low power dual PCI Express Gen2 (EP/RP), and an integrated low-power crypto coprocessor. RT PolarFire FPGAs can operate at 1.0V and 1.05V core voltage, offering the end user the ability to trade off power and performance to match the application requirements.

The RTPF500T device uses the same silicon design as commercial PolarFire FPGAs, with modifications to the flip-chip bump spacing to facilitate integration into hermetically-sealed ceramic packages. The RTPF500ZT device has enhanced radiation performance over RTPF500T.

This document describes the features of the RT PolarFire FPGAs. The AN4903 application note has detailed differences between RTPF500T and RTPF500ZT FPGAs. For current silicon status and electrical characteristics, refer to the datasheet.

Table of Contents

1. Summary of Features

- 481K logic elements consisting of a 4-input Look-Up Table (LUT) with a fractureable D-type flip-flop
- 20 Kbit dual- or two-port Large Static Random Access Memory (LSRAM) block with built-in Single Error Correct Double Error Detect (SECDED)
- 64 × 12 two-port µRAM block implemented as an array of latches
- 18 × 18 math block with a pre-adder, a 48-bit accumulator, and an optional 16 deep x 18 coefficient ROM
- Built-in µPROM, modifiable at program time, readable at run time for user data storage
- High-speed serial connectivity with built-in, multi-gigabit, multi-protocol transceivers from 250 Mbps to 12.7 Gbps
- Integrated dual PCIe for up to ×4 Gen2 End Point (EP) and Root Port (RP) designs
- High-Speed I/O (HSIO) supporting up to 1333 Mbps DDR4, 1067 Mbps DDR3L, and 1067 Mbps LPDDR3/DDR3 memories with integrated I/O digital
- General Purpose I/O (GPIO) supporting 3.3V (RTPF500ZT only and for LET ≤ 37 MeV.cm^2/mg), 2.5V, built-in CDR for serial gigabit Ethernet, 800 Mbps DDR3, and 1250 Mbps LVDS I/O speed with integrated I/O digital logic
- Low-power Phase-Locked Loops (PLLs) and Delay-Locked Loops (DLLs) for high precision and low jitter
- 1.0V and 1.05V operating modes
- Hermetically-sealed flip-chip ceramic column grid array and ceramic land grid array packages
- Path to Mil Std 883 class B, QML class Q, and QML class V qualification

1.1 Radiation Features

- Maintains datasheet parameters at 100 krad total ionizing dose
- Total ionizing dose test reports available for each wafer lot
- Immune to radiation-induced configuration upsets to 75 MeV.cm^2/mg
- Single-event latch-up threshold varies depending on GPIO voltage level. Refer to the AN4903 application note for details.
- Single-event upset protection in fabric flip-flops (TMR) can be instantiated by synthesis tools
- Built-in SECDED and memory interleaving on LSRAMs
- System controller suspend mode protects against radiation single-event upsets

1.2 Low-Power Features

- Low device static power
- Low inrush current
- Low power transceivers

1.3 Security Features

- Cryptography Research Incorporated (CRI)-patented Differential Power Analysis (DPA) bitstream protection
- Integrated Physically Unclonable Function (PUF)
- Up to 56 Kbytes of secure Non-Volatile Memory (sNVM)
- Built-in tamper detectors and countermeasures

- Digest integrity check for FPGA, µPROM, and sNVM
- Data security features in S devices—true random number generator, integrated Athena's TeraFire® EXP5200B Crypto Coprocessor, suite B capable, and CRI DPA countermeasure pass-through license

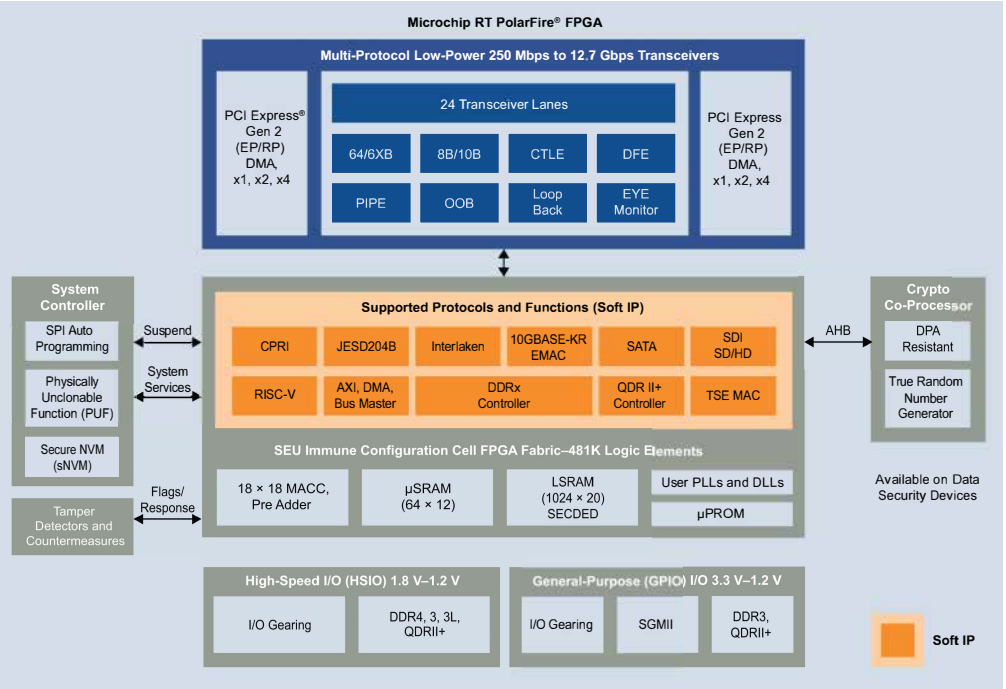
1.4 Libero® SoC FPGA Toolset

- Complete FPGA and embedded software development environment
- Includes Synplify Pro synthesis and Siemens EDA ModelSim ME simulation

2. Block Diagram

The following illustration shows the functional blocks of the RT PolarFire FPGA.

Figure 2-1. RT PolarFire FPGA Block Diagram



3. Product Family Table

The following table lists the product overview and packaging overview of the RT PolarFire FPGA product family.

Table 3-1. RT PolarFire FPGA Product Family

Features	Features	RTPF500T, RTPF500TL, RTPF500TS, RTPF500TLS	RTPF500ZT, RTPF500ZTL, RTPF500ZTS, RTPF500ZTLS
FPGA fabric	K Logic elements (4 LUT + DFF)	481	481
	Math blocks (18 × 18 MACC)	1480	1480
	LSRAM blocks (20 Kbits)	1520	1520
	µSRAM blocks (64 × 12)	4440	4440
	Total RAM (Mbits)	33	33
	µPROM (Kbits 9-bit bus)	513	513
	sNVM (Kbytes)	56	48
	User DLLs/PLLs	8	8
High-speed I/O	250 Mbps to 12.7 Gbps transceiver lanes	24	24
	PCIe Gen2 endpoints/root ports	2	2
Total I/Os	Total user I/Os	632	632
	HSIO	324	324
	GPIO	308	308
Packaging	CG1509, LG1509 1.0 mm 40 mm × 40 mm	632	632

Notes: TS and TLS FPGAs contain an Athena™ TeraFire F5200B crypto coprocessor.

4. Product Screening Flows

Table 4-1. RT PolarFire EV Flow and V Flow (QML Class V, MIL-PRF-38535)

Step	Screen	Test Method	Requirement
1	Internal Visual	2010, Condition A	100%
2	Serialization	In accordance with applicable Microchip device specification	100%
3	Temperature Cycling	1010, Condition C, 10 cycles minimum	100%
4	Constant Acceleration	Not required for RT PolarFire flip-chip technology	N/A
5	Particle Impact Noise Detection (PIND)	Not required for RT PolarFire flip-chip technology	N/A
6	Fine and Gross Leak	1014	100%
7	Radiographic (X-Ray)	Not required for RT PolarFire package with seam seal welding	N/A
8	Pre-Burn-In Electrical Parameters	In accordance with applicable Microchip device specification, with data Read and Record	100%
9	Dynamic Burn-In	1015, Condition D, 240 hours at 125 °C or 120 hours at 150 °C minimum	100%
10	Post-Dynamic-Burn-In Electrical Parameters	In accordance with applicable Microchip device specification, with data Read and Record	100%
11	Static Burn-In	1015, Condition C, 144 hours at 125 °C or 72 hours at 150 °C minimum	100%
12	Post-Static-Burn-In Electrical Parameters	In accordance with applicable Microchip device specification, with data Read and Record	100%
13	Percent Defective Allowable (PDA) Calculation	5004, 5% Overall, 3% Functional Parameters at 25 °C	All Lots, 100%
14	Final Electrical Test	In accordance with applicable Microchip device specification, with data Read and Record. Microchip device specification includes a, b, and c:	100%
	a. Static Tests		100%
	(1) 25 °C (2) –55 °C and +125 °C	5005, Table 1, Subgroup 1 5005, Table 1, Subgroup 2, 3	
	b. Functional Tests		
	(1) 25 °C (2) –55 °C and +125 °C	5005, Table 1, Subgroup 7 5005, Table 1, Subgroup 8a, 8b	
	c. Switching Tests at 25 °C	5005, Table 1, Subgroup 9	
15	Fine and Gross Leak	1014	100%
16	External Visual	2009	100%
17	Wafer Lot Specific Life Test (Group C)	MIL-PRF-38535, Appendix B, sec. B.4.2.c	All Lots
18	Assembly Lot Specific Destructive Physical Analysis (DPA)	MIL-STD-1580	All Lots

Notes:

1. EV flow and V flow are only available for RTPF500ZT, RTPF500ZTS, RTPF500ZTL, and RTPF500ZTLS.
2. For CCGA devices, all Assembly, Screening, and TCI testing are performed at LGA level. Only QA electrical and mechanical visual are performed after solder column attachment.
3. RT PolarFire low-power and standard-power device types have the same silicon and are distinguished by screening the IDC current (measured on the VDD core supply voltage) limits at 125 °C final electrical test.

4. EV flow (equivalent V flow) is offered as an interim product prior to the qualification and certification to QML class V. When the QML class V qualification is completed, the EV flow part numbers will be obsoleted and customers will be able to purchase FPGAs fully qualified to QML class V.

Table 4-2. RT PolarFire E Flow (Microchip Extended Flow)

Step	Screen	Test Method	Requirement
1	Internal Visual	2010, Condition A	100%
2	Serialization	In accordance with applicable Microchip device specification	100%
3	Temperature Cycling	1010, Condition C, 10 cycles minimum	100%
4	Constant Acceleration	Not required for RT PolarFire flip-chip technology	N/A
5	Particle Impact Noise Detection (PIND)	Not required for RT PolarFire flip-chip technology	N/A
6	Fine and Gross Leak	1014	100%
7	Radiographic (X-Ray)	Not required for RT PolarFire package with seam seal welding	N/A
8	Pre-Burn-In Electrical Parameters	In accordance with applicable Microchip device specification, with data Read and Record	100%
9	Dynamic Burn-In	1015, Condition D, 240 hours at 125 °C or 120 hours at 150 °C minimum	100%
10	Post-Dynamic-Burn-In Electrical Parameters	In accordance with applicable Microchip device specification, with data Read and Record	100%
11	Static Burn-In	1015, Condition C, 144 hours at 125 °C or 72 hours at 150 °C minimum	100%
12	Post-Static-Burn-In Electrical Parameters	In accordance with applicable Microchip device specification, with data Read and Record	100%
13	Percent Defective Allowable (PDA) Calculation	5004, 5% Overall, 3% Functional Parameters at 25 °C	All Lots, 100%
14	Final Electrical Test	In accordance with applicable Microchip device specification, with data Read and Record. Microchip device specification includes a, b, and c:	100%
	a. Static Tests		100%
	(1) 25 °C (2) –55 °C and +125 °C	5005, Table 1, Subgroup 1 5005, Table 1, Subgroup 2, 3	
	b. Functional Tests		
	(1) 25 °C (2) –55 °C and +125 °C	5005, Table 1, Subgroup 7 5005, Table 1, Subgroup 8a, 8b	
	c. Switching Tests at 25 °C	5005, Table 1, Subgroup 9	
15	Fine and Gross Leak	1014	100%
16	External Visual	2009	100%

Notes:

1. For CCGA devices, all Assembly, Screening, and TCI testing are performed at LGA level. Only QA electrical and mechanical visual are performed after solder column attachment.
2. RT PolarFire low-power and standard-power device types have the same silicon and are distinguished by screening the IDC current (measured on the VDD core supply voltage) limits at 125 °C final electrical test.
3. Microchip offers E Flow for users requiring additional screening beyond MIL-STD-833 Class B requirement. E Flow incorporates the majority of the screening procedures as outlined in Method 5004 of MIL-STD-883, Class S.

4. The Quality Conformance Inspection (QCI) for E Flow devices still comply with MIL-STD-833 Class B requirement.

Table 4-3. RT PolarFire B Flow (MIL-STD-883 Class B)

Step	Screen	Test Method	Requirement
1	Internal Visual	2010, Condition B	100%
2	Serialization	In accordance with applicable Microchip device specification	100%
3	Temperature Cycling	1010, Condition C, 10 cycles minimum	100%
4	Constant Acceleration	Not required for RT PolarFire flip-chip technology	N/A
5	Particle Impact Noise Detection (PIND)	Not required for RT PolarFire flip-chip technology	N/A
6	Fine and Gross Leak	1014	100%
7	Pre-Burn-In Electrical Parameters	In accordance with applicable Microchip device specification	100%
8	Dynamic Burn-In	1015, Condition D, 160 hours at 125 °C or 80 hours at 150 °C minimum	100%
9	Percent Defective Allowable (PDA) Calculation	5004, 5%	All Lots, 100%
10	Final Electrical Test	In accordance with applicable Microchip device specification, which includes a, b, and c:	100%
	a. Static Tests		100%
	(1) 25 °C (2) –55 °C and +125 °C	5005, Table 1, Subgroup 1 5005, Table 1, Subgroup 2, 3	
	b. Functional Tests		
	(1) 25 °C (2) –55 °C and +125 °C	5005, Table 1, Subgroup 7 5005, Table 1, Subgroup 8a, 8b	
	c. Switching Tests at 25 °C	5005, Table 1, Subgroup 9	
11	External Visual	2009	100%

Notes:

1. For CCGA devices, all Assembly, Screening, and TCI testing are performed at LGA level. Only QA electrical and mechanical visual are performed after solder column attachment.
2. RT PolarFire low-power and standard-power device types have the same silicon and are distinguished by screening the IDC current (measured on the VDD core supply voltage) limits at 125 °C final electrical test.

Table 4-4. RT PolarFire PROTO Flow (Microchip RT-PROTO Flow)

Step	Screen	Test Method	Requirement
1	Final Electrical Test	In accordance with applicable Microchip device specification, which includes a, b, and c:	100%
	a. Static Tests		100%
	(1) 25 °C (2) –55 °C and +125 °C	5005, Table 1, Subgroup 1 5005, Table 1, Subgroup 2, 3	
	b. Functional Tests		
	(1) 25 °C (2) –55 °C and +125 °C	5005, Table 1, Subgroup 7 5005, Table 1, Subgroup 8a, 8b	
	c. Switching Tests at 25 °C	5005, Table 1, Subgroup 9	
2	Dimple Process	In accordance with applicable Microchip device specification	100%
3	External Visual	2009	QA Sample

Notes:

1. For column and ball grid array packages, all Assembly and Screening are performed at LGA level. Only QA electrical and mechanical visual are performed after solder column and ball attachment.
2. RT PolarFire low-power and standard-power device types have the same silicon and are distinguished by screening the IDC current (measured on the VDD core supply voltage) limits at 125 °C final electrical test.
3. RT PolarFire PROTO follows Microchip RT-PROTO Guidelines.

5. Non-Volatile FPGA Fabric

The non-volatile FPGA fabric is built on a 28nm low-power, non-volatile process technology. The RT PolarFire FPGA fabric is composed of the following building blocks:

- Logic element
- On-chip memory (LSRAM, µSRAM, sNVM, and µPROM)
- Math block

The FPGA fabric configuration cells are SEU immune and are used to configure I/Os and other aspects of the device. Non-volatile FPGAs do not require the configuration process inherent in SRAM FPGAs. Non-volatile FPGAs power-up quickly like an ASIC with minimal inrush current, and are ideal for root-of-trust, first-up functionality in any system.

5.1 Logic Element

The 4-input LUT can be configured either to implement any 4-input combinatorial function or to implement an arithmetic function where the LUT output is XORed with a carry input to generate the sum output.

The logic element has the following features:

- A fully permutable 4-input LUT optimized for lowest power
- A dedicated carry chain based on a carry look-ahead technique
- A separate flip-flop that can be used independently from the LUT

5.2 On-Chip Memory

RT PolarFire FPGAs integrate four different types of memories that allow the designer to optimize for power, functionality, and area. Two memory types are volatile and two memory types are non-volatile.

Volatile memories include:

- LSRAM
- µSRAM

The LSRAMs are 20 Kbit SRAMs with a built-in SECDED and interleaving to prevent Multi-Bit-Upsets (MBUs). The µSRAMs are small distributed 64 × 12 RAMs, well suited for efficient implementation of small buffers, thereby reserving LSRAM usage for the wider and deeper memories.

Non-volatile memories (NVMs) include:

- µPROM
- sNVM

The µPROM, constructed of SEU-immune FPGA configuration non-volatile cells, is readable at runtime and writable during device programming. It provides users with SEU-immune parameters, constants, IDs, and parametric or initialization data. The sNVM is accessible through system service calls. Data written to the sNVM can be protected by the PUF. The sNVM is readable and writable by the designer's application during runtime, before entering system controller suspend mode (RTPF500T) or after temporarily exiting system controller suspend mode (RTPF500ZT). It is an ideal storage location for soft processor boot code, or user security keys.

5.3 LSRAM

Each LSRAM block consists of 20,480 bits of RAM and includes functionality to support dual-port and two-port modes. There are numerous configurations and features for each block. The Libero SoC toolset has an LSRAM configurator that provides automated combining and cascading of several LSRAM blocks into larger memories.

LSRAM features include:

- Up to 385 MHz operation
- True dual-port memory
- Two-port memory (one dedicated write port and one dedicated read port)
- Data widths of ×1, ×2, ×5, ×10, ×20, ×40, and ×33 with SECDED enabled
- Multi-bit-upset mitigation
- Synchronous operation
- Independent port clocks
- Byte enables
- Registered inputs
- Output registers with separate enables and synchronous resets
- Read enables to conserve power while retaining output data
- Power switch to minimize static power when the LSRAM is not used
- Fast zeroization mode

5.3.1 Dual-Port Mode

In dual-port mode, the width of both ports is less than 33 and the ports are independent of each other. The write and read operations can occur independently of each other, at any location. On write collisions, while the write operations occur correctly, the read operations can return ambiguous results while the write completes. After completing the write operation, the read data reads the newly written write data correctly.

5.3.2 Two-Port Mode

In two-port mode, at least one port has a width of 32 or 40 (or 33 with SECDED). Port A is dedicated for reads and port B for writes.

The following illustration shows port widths in various modes.

Figure 5-1. LSRAM Dual- and Two-Port Configurations

Port B Width \ Port A Width	x1/x1	x1/x2	x1/x4	x1/x8	x1/x16	W1/R32	N/A
	x2/x1	x2/x2	x2/x4	x2/x8	x2/x16	W2/R32	N/A
	x4/x1	x4/x2	x5/x5	x5/x10	x5/x20	W5/R40	N/A
	x8/x1	x8/x2	x10/x5	x10/x5	x10/x20	W10/R40	N/A
	x16/x1	x16/x2	x20/x5	x20/x10	x20/x20	W20/R40	N/A
	W32/R1	W32/R2	W40/R5	W40/R10	W40/R20	W40/R40	N/A
	N/A	N/A	N/A	N/A	N/A	N/A	Wx33/R33

Dual Port
Two Port
Two Port SECDED

5.4 µSRAM

The µSRAM is a two-port memory embedded in the FPGA fabric, which is provided for an efficient low-power implementation for small buffers. On write collisions, the write operations occur correctly, while the read operations can return ambiguous results while the write completes. After completing the write operation, the read data reads the newly written write data.

The following are key features of the µSRAM block:

- Up to 430 MHz operation
- Two-port memory with 64 words of 12 bits
- The write port operates synchronously
- The write port has a fixed width
- The read port operates asynchronously and supports synchronous and pipeline operations with the FPGA fabric flip-flops
- The Libero SoC toolset provides automated combining and cascading for larger memories
- Multiple memory blocks can be combined to extend the depth or width
- Provides a state-keeping, low-power suspend mode
- Implemented as an array of latches

5.5 µPROM

The µPROM is a single monolithic non-volatile memory that provides a PROM-like storage for a variety of purposes, including but not limited to: initialization data for other memories, user calibration data, and so on. The memory cells are constructed from the FPGA configuration cells and are updated when the device is programmed.

The following are key features of the µPROM:

- 10 ns read access time
- Programmed with the FPGA bitstream
- Asynchronous or synchronous read access mode from the FPGA fabric

5.6 sNVM

Each RTPF500T FPGA has 56 Kbytes of sNVM. The sNVM is organized into 221 pages of 236 or 252 bytes, depending on whether the data is stored as plain text or encrypted/authenticated data. Each RTPF500ZT FPGA has 48 Kbytes of sNVM that is organized into 221 pages, each of which holds 220 bytes of non-authenticated plain text or 204 bytes of authenticated plain text/cipher text. It is accessible to users through system services calls to the RT PolarFire FPGA system controller. Pages within the sNVM can be marked as ROM during bitstream programming. The sNVM content can be used to initialize LSRAM and µSRAMs with secure data. The sNVM is only accessible through system service calls. Data written to the sNVM can be protected by the PUF.

5.7 Math Block

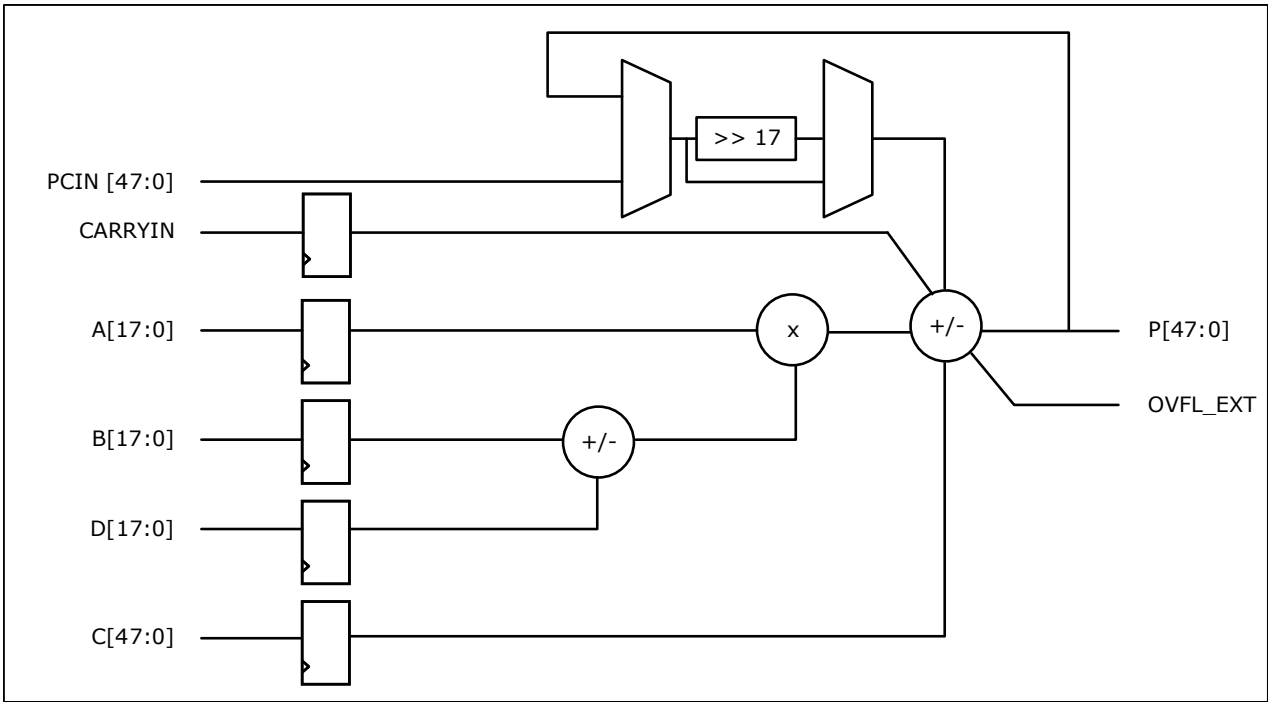
The fundamental building block in any digital signal processing algorithm is the Multiply-Accumulate (MACC) operation. RT PolarFire FPGAs implement a custom 18 × 18 MACC block for an efficient low-power implementation of complex DSP algorithms such as Finite Impulse Response (FIR) filters, Infinite Impulse Response (IIR) filters, and Fast Fourier Transform (FFT) for filtering and image processing applications. An optional 16-word coefficient ROM can be constructed from logic elements located near the math block.

The following are key features of the math block functionality:

- Up to 450 MHz operation
- 18 × 18 two's complement multiplier accumulator with an output width of 48 bits
- Power-saving pre-adder to optimize linear phase FIR filter applications and reduce the math block usage
- Optional pipelining and dedicated buses for cascading
- Dot-Product mode for complex multiplies

The following illustration shows the functional blocks of the math block.

Figure 5-2. Math Block



6. Clock Management

In each RT PolarFire FPGA, there are eight DLLs and eight PLLs to provide flexible clock generation and management capabilities. In addition to these DLLs and PLLs, up to 15 transceiver lane transmit PLLs are also available.

The following are key highlights of the clock management architecture:

- High-speed buffers and routing for low-skew clock distribution
- Frequency synthesis and phase shifting
- Low-jitter clock generation and jitter filtering

6.1 DLL

The DLL provides a calculated PVT compensated delay to the I/O's digital delay lines as well as delay or phase-shifted clocks to the FPGA fabric.

The following are the major modes to which the DLL can be configured.

- Time Reference mode—the DLL takes a single clock as an input and determines how many delay line buffer taps are required for a signal to pass through them to rotate a signal. The main use of Time Reference mode is to know how many delay taps are needed to delay the clock by 90 degrees. The value is then provided to the Data Strobe Signal (DQS)/DQSn input signals for Double Data Rate (DDR) memory controllers to delay all DQS/DQSn signals by the required 90-degree phase shift to capture the data from the memory devices. Multiple memory interfaces of the same clock rate can reuse the same DLL with lane level controls for PVT updates.
- Clock Injection Delay mode—the DLL can be used to compensate for the clock injection delay associated with the source synchronous receive interfaces. The DLL can match delays for the global, regional, and high-speed bank clocks. There are two outputs from the DLL in this mode: a x1 output fixed in time and another output that can be divided by x1, x2, or x4 and can be phase shifted.

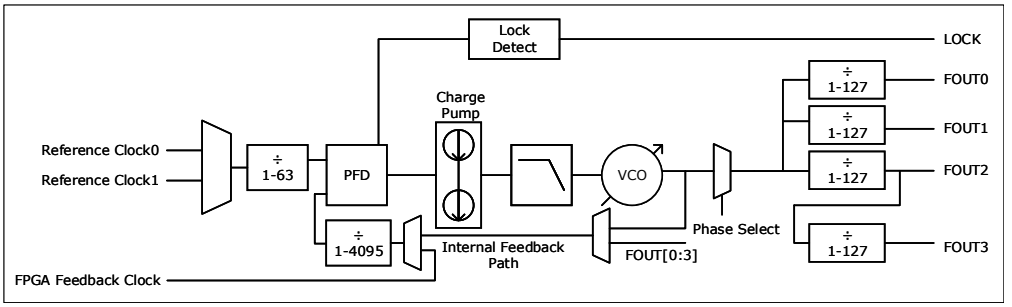
6.2 PLL

The programmable Delta-Sigma low-jitter fractional PLLs are multi-function and general purpose frequency synthesizers, as shown in PLL Block Diagram. Wide input and output ranges along with the best-in-class jitter performance allow these PLLs to be used for almost any clocking application. With excellent supply noise immunity, the PLL is ideal for use in noisy FPGA environments.

- The PLL output clock is available in eight phases with 45-degree phase differences. All eight phases are selectable to drive four separate outputs from the PLL, where each output can select any of the eight phases independent of other output selections and that each output can also be driven to a zero output when not used.
- Each of the four outputs from the PLL can then be divided independently for any value from 1 to 127. Each of the PLL outputs can have the output divider released by up to seven VCO/4 cycles. The delayed outputs can be set independently for each output clock.
- Fractional-N (24-bit accuracy) capability is added to the feedback divider to have the VCO frequency be a non-integer divide of the reference clock input frequency. The base frequency is applied to all PLL outputs.
- The PLL supports glitch-free start and stop on any one of the four outputs independently by either a register map or a fabric control. This capability also allows the output divider values and the VCO/4 phase selection to be modified glitch-free during the time that the clock is stopped.
- For fine granularity phase control of the PLLs, they can be cascaded with DLLs located near the PLLs, whereby the DLL delay lines can be used in a Process, Voltage, and Temperature (PVT) compensated or non-PVT compensated mode to provide the phase control needed.

The following illustration shows the flow of the PLL functionality.

Figure 6-1. PLL Block Diagram



6.3 Clock Network

The clock network is designed to route clocks and asynchronous Reset signals to large sections of the fabric with limited skew. On occasion, the network can also be used for other high fanout signals that can tolerate long delays, such as non-timing-critical synchronous enables or Resets. There are two main clock networks for the FPGA fabric, global and regional clocks.

6.3.1 Global Clocks

There are 24 clocks on the device with global low skew scope to all synchronous elements. The global can be divided into left and right sides of the device. Thus, the number of globals can increase to 48 total clocks with 24 in the left and 24 in the right.

6.3.2 Regional Clocks

There are up to 38 regional clock domains that interface to the edges of the device. The regional clocks provide a fixed number of logic elements based on the size of the device. Up to 14 clocks are available for the FPGA I/Os and up to 24 clocks for the transceiver lanes, one for each lane direction. These are the fast insertion clock networks used to move data in and out of the fabric.

7. I/Os

RT PolarFire device user I/Os support multiple I/O standards while providing the high bandwidth needed to maximize the internal logic capabilities of the device and achieve the required system-level performance.

7.1 Low-Power High-Speed Transceiver Lane

All RT PolarFire FPGAs contain state-of-the-art low-power transceiver lane capabilities from speeds as low as 250 Mbps up to 12.7 Gbps. The PMA is designed to support multiple protocols (as listed in the following table) with state-of-the-art control and debug features. PCI Express Gen1 or Gen2 support is provided by a hard macro. All other protocols are implemented with a soft IP. Serial Gigabit Ethernet is also supported with GPIO 2.5V LVDS differential pairs. A single transmit PLL can provide a high-speed clock up to four transceiver lanes.

Table 7-1. Transceiver Lane Protocol Support

Protocol	Data Rate (Gbps)	Channels Bonded
PCIe	2.5, 5	1, 2, 4
Interlaken	6.375	1–16
10GBASE-R/KR[2]	10.3125	1
SGMII/QSGMII	1.25–5	1
XAUI	3.125	4
RXAUI	6.25	2, 3, 4, 6
HiGig/HiGig+/HiGiGII	3.75–4.065	4
CPRI	0.6144–12.165	1
Fiber channel	0.6144–12.165	1
SRIO	1.25–10.3125	1, 2, 4, 8
SATA	1.5–6	1
JESD204B	0.5–12.5	1–4
Display port	2, 5, 8	4
SDI	0.277–11.88	1

Note:

1. Not all channel bonding is supported at all data rates.
2. KR is supported in -1 speed only.

7.1.1 Low-Power Transceiver Lane Features

The following are low-power transceiver lane features:

- Advanced low-power modes
- Programmable transmit amplitude and emphasis control
- Low-speed CDR operation with support for 270 Mbps SMPTE serial line rates
- Continuous Time Linear Equalization (CTLE) and Decision Feedback Equalization (DFE) for long-reach or backplane applications
- Auto-adaption at receiver equalization and integrated eye monitor feature for easy serial link tuning
- Eye monitor and/or equalization can be powered down to reduce power if not needed

- Out-of-band, electrical idle signaling capability for SAS, SATA, and PCIe
- Multiple loopback modes for test and debug
- Transmit jitter attenuation for loop timing applications (SyncE compatible)
- Hot-socketing capable
- IEEE® 1149.6 AC JTAG
- Adjacent channel loopback modes allow transceiver lane data streams to remain active during FPGA fabric programming

7.1.2 Transmitter

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 8, 10, 16, 20, 32, 40, 64, or 80 bits. It allows the designer to trade-off data path width for timing margin in high-performance designs. These transmitter outputs drive the PC board with a differential output signal. TX_CLK is the appropriately divided serial data clock available to the fabric, and can be used directly to register the parallel data coming from the internal logic. The transmit parallel data has additional hardware support for the 8b/10b, 64b/66b, or 64b/67b encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. The output signal pair supports a wide variety of serial protocols and has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to lower power consumption. Each transmit lane can be sourced by one of two transmit PLLs. Each transmit PLL can drive up to four transceiver lanes. Transmitter PLLs are state-of-the-art fractional frequency synthesizers with integrated jitter attenuation.

7.1.3 Receiver

The receiver is fundamentally a serial-to-parallel converter with clock recovery changing the incoming bit-serial differential signal into a parallel stream of words of 8, 10, 16, 20, 32, 40, 64, or 80 bits. This allows the FPGA designer to trade off the internal data path width versus logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable linear and decision feedback equalizers (to compensate for PC board and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. The data pattern uses Non-Return-to-Zero (NRZ) encoding and optionally guarantees sufficient data transitions by using the selected encoding scheme. The outgoing parallel data has additional hardware support for the 8b/10b, 64b/66b, or 64b/67b encoding schemes to provide a sufficient number of transitions. Parallel data is transferred into the FPGA logic using the recovered clock (RX_CLK).

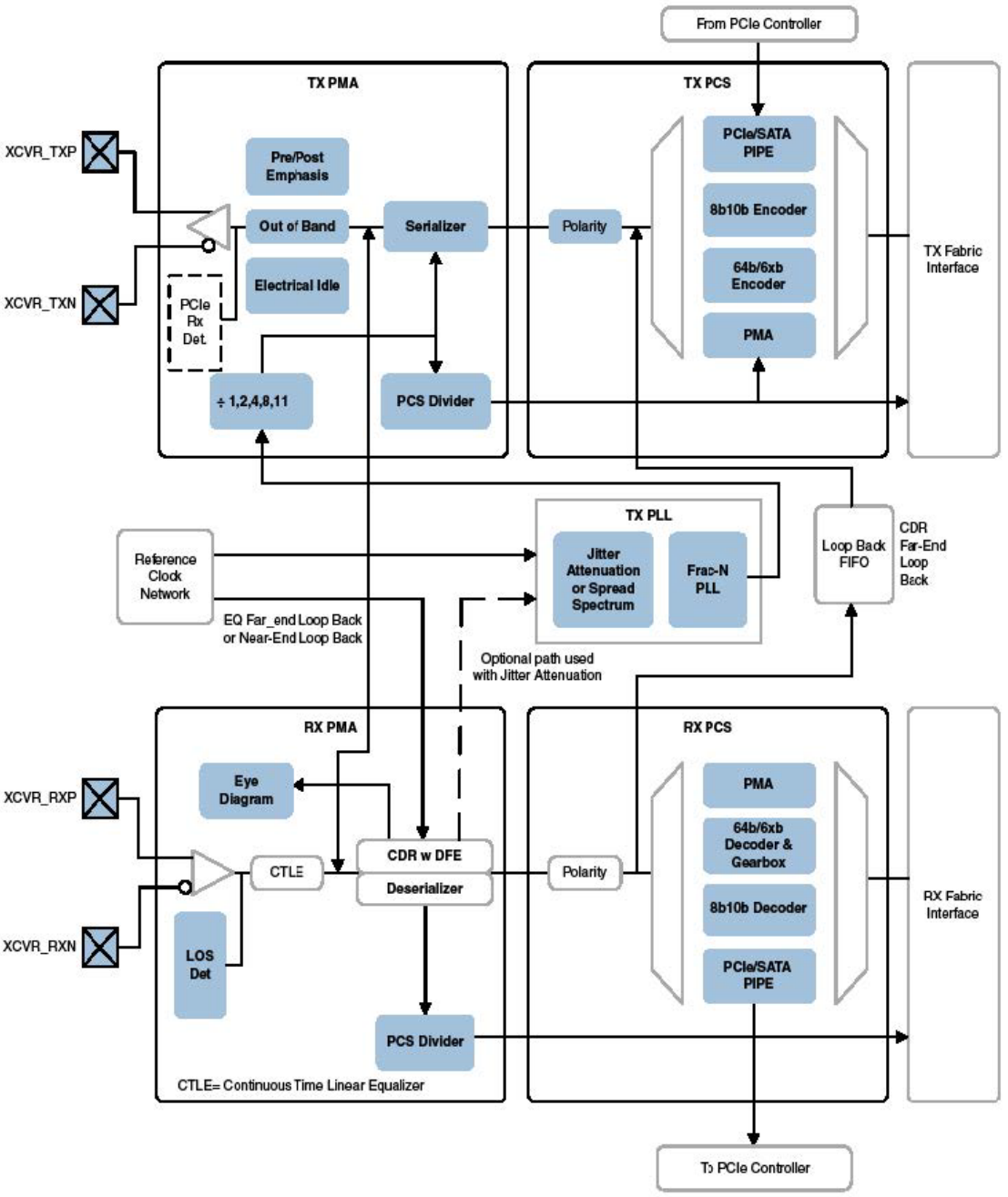
7.1.4 Transceiver Lane Modes

The transceiver lane supports five different modes of operations:

- PMA—direct access to the PMA without any encoding
- 8b/10b—8b/10b encoding/decoding is provided
- 64b/6xb—64b/66b or 64/67b encoding/decoding with gearbox logic is provided
- PIPE—a PIPE interface supporting both PCIe Gen2 and SATA 3.0
- PCIe—direct connection to the embedded PCIe Gen2 controller

The following illustration shows the collaboration of five modes that transceiver lanes support.

Figure 7-1. Transceiver Lane Modes

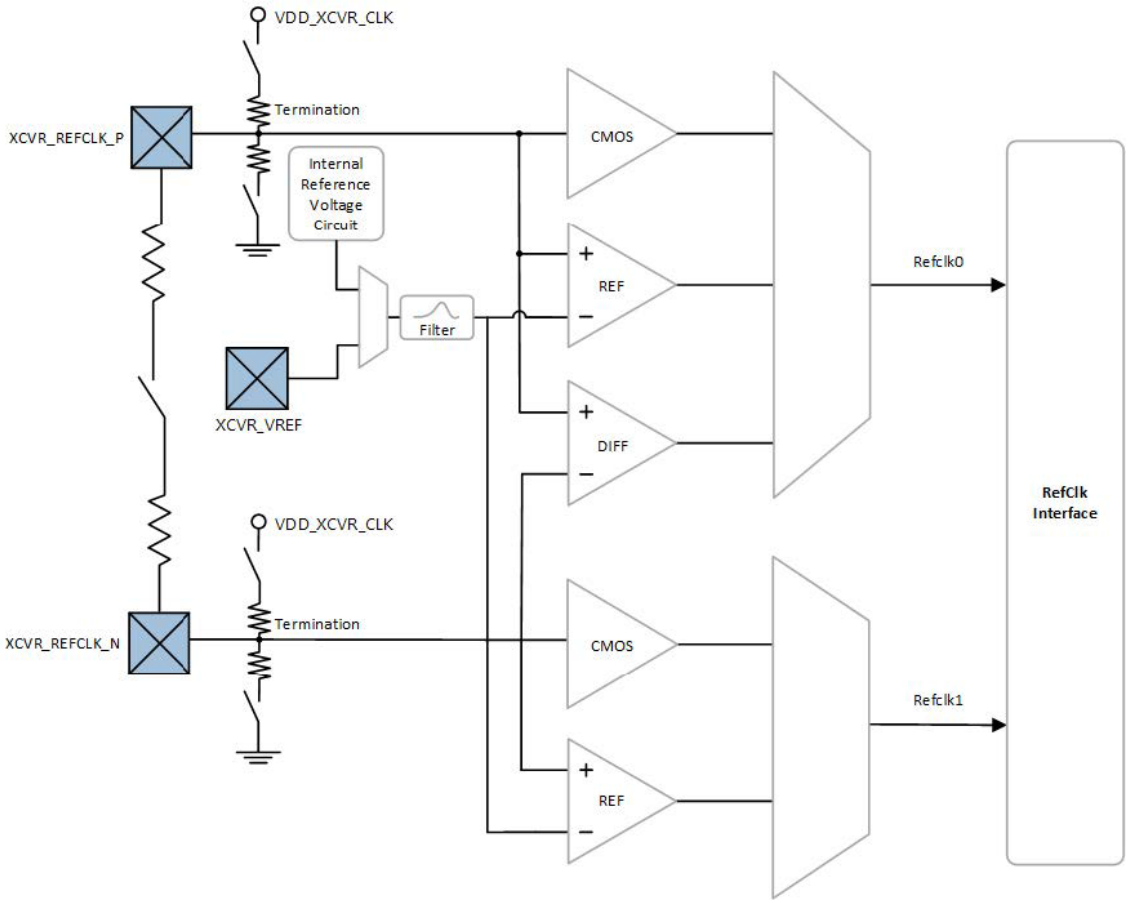


7.1.5 Reference Clock

The reference clock pins allow connections directly with the transceiver lane quads. The reference clock inputs provide flexibility to interface with both single-ended and differential clocks, and can drive up to two independent clocks per transceiver lane quad. These reference clocks can also be sources for the global and regional clock networks in the FPGA fabric of the device.

The following illustration shows the connectivity between the reference clock and transceiver lane quads.

Figure 7-2. Reference Clock



7.1.6 Quad Lane Overlay Assignments

The transceiver lane either connects the parallel side of the interface to the PCIe Gen2 controller or to the fabric. The PCIe connections are fixed in the hardware and have a dedicated number of combinations between the two controllers. The fabric interface is used to support the PMA, 8b/10b, 64b/6xb, and PIPE modes and has complete flexibility into the fabric connections.

The following table lists the combinations between the PCIe and fabric controllers.

Table 7-2. Quad0 Lane Assignments

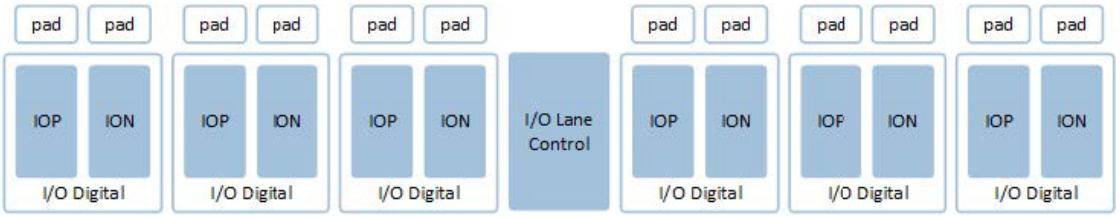
PCIe_0 Controller	Quad0 Lane 0	Quad0 Lane 1	Quad0 Lane 2	Quad0 Lane 3	PCIe_1 Controller
x1	PCIe_0	Not available	Not available	PCIe_1	x1
x1	PCIe_0	Unused	PCIe_1	PCIe_1	x2
x2	PCIe_0	PCIe_0	Not available	PCIe_1	x1
x2	PCIe_0	PCIe_0	PCIe_1	PCIe_1	x2
x4	PCIe_0	PCIe_0	PCIe_0	PCIe_0	Unused
x1	PCIe_0	Not available	Fabric	Fabric	Unused
x2	PCIe_0	PCIe_0	Fabric	Fabric	Unused
Unused	Fabric	Fabric	Not available	PCIe_1	x1
Unused	Fabric	Fabric	PCIe_1	PCIe_1	x2
Unused	Fabric	Fabric	Fabric	Fabric	Unused

Note: Fabric includes PMA, 8b/10b, 64b/66b, 64b/67b, and PIPE modes.

7.2 Inputs/Outputs

RT PolarFire FPGA I/Os are grouped into pairs to meet the differential I/O standards. Additionally, they are grouped in lanes of 12 buffers with a lane controller for memory interfaces, as shown in the following illustration.

Figure 7-3. I/O Topology



The number of I/O pins varies depending on the device and package size. The persistent I/O feature preserves a state on an I/O without user intervention during Programming mode. The RT PolarFire FPGA I/O buffers are constructed from the following main sub modules.

- Transmit buffer (PVT compensated)
- Receive buffer
- Termination (Thevenin, Differential, Up, and Down)
- Weak pull mode logic (Up, Down, and Bus-Hold)

Each I/O is configurable and can comply with a large number of I/O standards. There are two types of user I/Os in RT PolarFire FPGAs:

- High-Speed I/O (HSIO) optimized for DDR4 memories at speeds up to 1333 Mbps and a maximum voltage of 1.8V nominal
- GPIO capable of supporting multiple standards up to 2.5V in RTPF500T and 3.3V in RTPF500ZT (for LET ≤ 37 MeV.cm^2/mg) with an integrated CDR to support SGMII Ethernet applications

7.3 I/O Digital

The RT PolarFire FPGA I/O digital logic is used to interface between the FPGA fabric and the I/O buffers. It interfaces between the high-speed I/O buffers and lower-speed FPGA fabric. The I/O digital block consists of the following:

- A delay chain, for input or output delay
- Registers and control logic for input modes and output modes

The I/O digital registers can be configured for both input and output DDR and shift register modes and combined DDR-shift register modes. It allows gearing up the output data rate and gearing down the input data rate. The RT PolarFire FPGA I/O digital logic works in conjunction with fast and low-skew clock distributions that are optimized for DDR applications, special clock dividers, and other support circuits to guarantee clock domain crossings.

7.3.1 I/O Digital Features

The following are the I/O digital features:

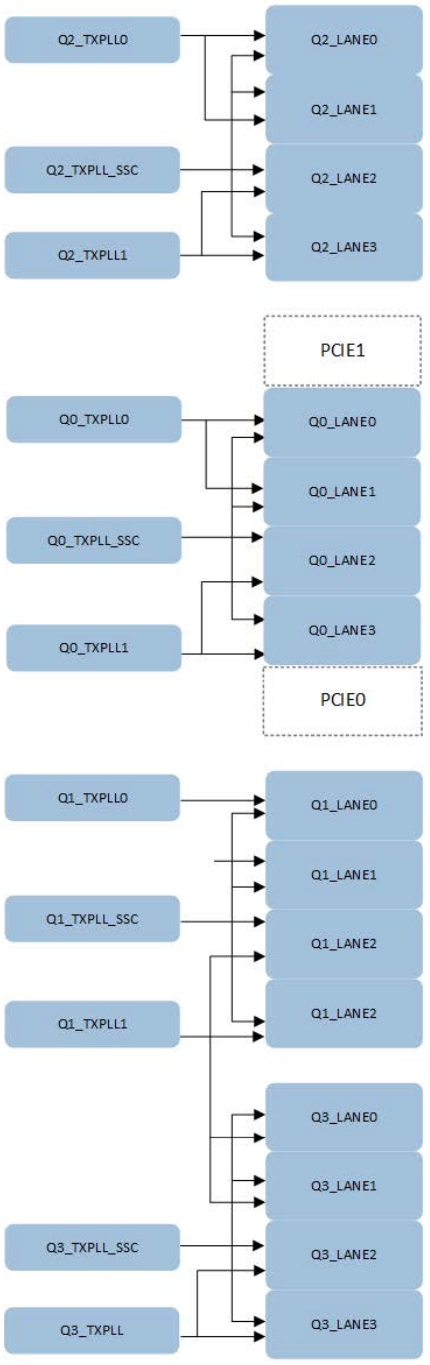
- Programmable input and/or output delay chain
- Data eye monitor for detecting margin to clock edges
- Data eye position optimizer

- Up to 10:1 input deserialization
- Up to 10:1 output serialization
- Support for DDR and SDR interfaces
- Receive slip control to facilitate word alignment
- Fast and low-skew lane clocks per 12 I/Os
- Clock recovery for SGMII and similar interfaces (one per 12 I/Os)

8. PCI Express

Each RT PolarFire FPGA integrates two low-power built-in PCIe Gen2 controllers, allowing seamless and easy connectivity to one or more host processors. The two PCIe controllers are shared across two quads, as shown in the following illustration. All PLLs are jitter attenuation-capable, while the SSC label indicates Spread Spectrum Clock (SSC) capability.

Figure 8-1. PCI Express Hard Macro Lane Sharing



8.1 PCI Express Features

The following are PCIe features:

- ×1, ×2, and ×4 lane support
- Suitable for root port, native endpoint
- PCI Express base specification revision 2.0 and 1.1 compliant
- AXI4 initiator and target interfaces to the FPGA fabric
- Single function capability
- Advanced Error Reporting (AER) support
- Integrated Clock Domain Crossing (CDC) to support user-selected AXI4 frequency
- Lane reversal support
- Legacy PCI power management support
- Native Active state power management L0s and L1 state support
- Power Management Event (PME message)
- MSI and legacy INT message support
- Latency Tolerance Reporting (LTR)
- L1 PM sub-states with CLKREQ
- Address translation tables between the PCIe and AXI4 domains

8.2 PCI Express DMA Engines

Each PCIe controller supports the following built-in DMA modes, enabling low-power and efficient data transfer into the FPGA fabric.

- Two DMA channels
- Eight outstanding read and write requests
- Completion reordering support
- Flexible scatter-gather DMA modes, including dynamic DMA control per descriptor
- Optional DMA engine reporting to the descriptor to ease software management
- Fetching of up to three descriptors to optimize throughput

9. System Controller

The RT PolarFire FPGA system controller is based on the industry-standard ARM Cortex-M3 and is only used for FPGA power-up, secure DPA safe FPGA programming, and executing and responding to system services. All internal memories are SECDED protected with background scrubbing capabilities to remove single bit errors.

9.1 System Services

System services provide the user with information about the state of the FPGA and allow the user to request the system controller to perform predefined functions using a standard Application Programming Interface (API).

Design services

- Bitstream authentication
- IAP image authentication

Data services

- sNVM read/write
- PUF emulation service
- Nonce service

Device services

- Serial number
- JTAG user code
- Design version number
- Device certificate

FPGA fabric services

- In-application programming
- Digest check

10. Debug Probe System

Two specified user I/Os can be configured (at design capture stage) as either two single-ended live probes or one differential live probe. These live probes can provide read access to any register in the FPGA fabric, to the output pipeline registers in the LSRAMs, and to all the registers in the math block in real-time without having to re-instrument the code. A snapshot of all internal probe points can be created and read out asynchronously. The live-probe feature can be considered like a two-channel oscilloscope, whose two channels can be routed out to I/Os for external observation, and to internal ports to allow fabric design observation. Selecting different probe points within the RT PolarFire FPGA occurs dynamically through commands over the JTAG port using SmartDebug. Reprogramming of the FPGA is not required.

The debug probe system includes the following:

- Active probe allows dynamic asynchronous read and write to a flip-flop or a probe point. This enables quick internal observation of the logic output or experimentation on how the logic will be affected by writing to a probe point.
- Memory debug allows dynamic asynchronous read and write to a µSRAM or a large SRAM block to quickly verify if the content of the memory is changing as expected.
- Probe insertion allows routing of nodes or debug points in the FPGA design externally through unused I/Os. An oscilloscope/logic analyzer can be attached to monitor them as live signals.

11. Programming

RT PolarFire FPGAs have multiple programming modes designed to enable various use models. All bitstreams are always encrypted and DPA safe. Each RT PolarFire FPGA can be programmed using a dedicated SPI peripheral and JTAG port. All RT PolarFire FPGAs are typically reprogrammed in less than 60 seconds. For device-specific programming timings, see the RT PolarFire Datasheet.

The following programming modes are supported:

- JTAG
- SPI-Target—an external SPI initiator programs the FPGA
- SPI-Initiator (also known as SPI-Controller)—In-Application Programming (IAP)
  - Auto update feature—the system controller on power-up checks for a new bitstream in an external SPI Flash and programs the FPGA.
  - Auto programming feature—on a blank device, the system controller on power-up checks for a bitstream in an external SPI Flash and programs the FPGA.
  - Programming recovery feature—if remote programming fails due to a power interruption, the system controller reprograms the FPGA on the next power-up cycle from a golden bitstream (located in an external SPI Flash).

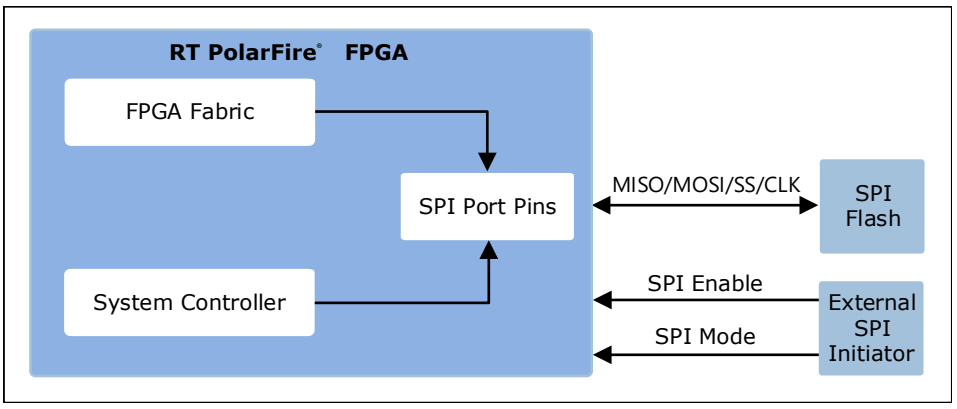
For differences in programming support between RTPF500T and RTPF500ZT FPGAs, refer to the AN4903 application note.

11.1 Dedicated SPI Programming Port

To facilitate the use of various programming modes, RT PolarFire FPGAs share dedicated SPI port pins between the system controller and user logic embedded in the FPGA. User logic must instantiate the PF_SPI macro to gain access to the pins from their design. The SPI port pins can be used as an initiator or a target programming port based on the signal level on the dedicated SPI mode pin. The dedicated SPI Enable pin also allows an external SPI initiator to program the on-board SPI Flash without an external MUX by tri-stating the SPI MOSI/MISO/SS/CLK pins on the RT PolarFire FPGA.

The following illustration shows the SPI port facilitating the use of various programming modes.

Figure 11-1. SPI Programming Port



12. Low Power

RT PolarFire FPGAs offer a variety of techniques and capabilities to lower the total application power. Users can take advantage of these features to lower both capital and operational expenditures with smaller or no heat sinks, smaller or fewer fans, lower cooling costs, and so on. Additionally, the lower total power advantage can also allow the user to pack more compute operations into an existing thermal budget.

12.1 Non-Volatile Technology

Using a non-volatile Complementary Metal–Oxide Semiconductor (CMOS) technology for the FPGA configuration cells offers several power advantages over SRAM FPGA technology.

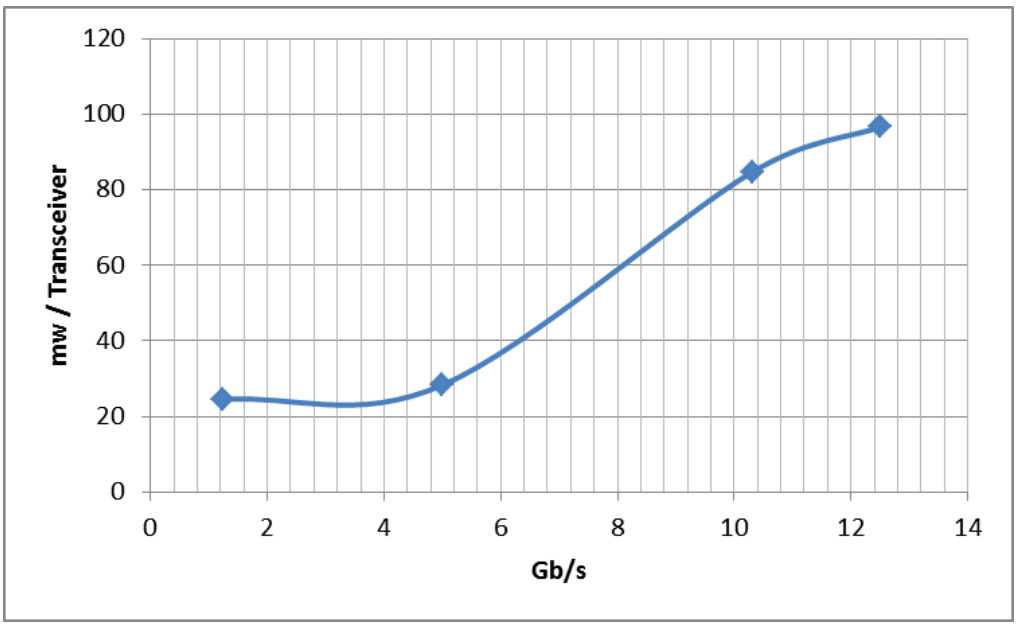
- A non-volatile switch has lower power than a SRAM switch, leading to lower static power consumption
- No SRAM configuration inrush currents
- An external configuration component is not necessary

12.2 Low-Power Transceiver Lane

RT PolarFire FPGAs' low-power capability is also extended to the industry's most power efficient transceiver lane, enabling 10GBASE-KR applications at less than 100 mW of power per lane. The transceiver lane has comprehensive power-down controls to optimize power consumption, including programmable amplitude and edge rate control.

The following illustration shows the connection between transceiver power and data rate.

Figure 12-1. Transceiver Power versus Data Rate



12.3 Low-Power (L) Devices

Low-power (L) devices provide up to 30% lower static power with identical electrical specifications to the STD speed grade device. L devices can be ordered as described in the section Ordering Information.

13. Reliability

Microchip continues to offer the industry's most reliable FPGAs for mission and safety critical applications.

13.1 FPGA Fabric

RT PolarFire FPGA configuration cells are inherently immune to SEUs caused by heavy ions, protons, and neutrons, without requiring scrubbing of the configuration cells. The configuration of the RT PolarFire FPGA fabric provides worry-free operation against random loss of configuration caused by SEUs.

13.2 LSRAM

LSRAMs have built-in SECDED capability on a 32-bit word boundary. Seven additional bits are used for error correction. Two flags are provided to the user to indicate SECDED. Mitigation against multi-bit upsets is provided by keeping all cells in a word separated by a minimum distance. Applications that require scrubbing need to be accomplished with user logic. The error correction logic can be turned ON and OFF by the user to enable easy validation of the error correction operation.

13.3 µSRAM

The 64 × 12 µSRAMs are constructed from latches and are not as sensitive to SEUs as SRAMs are.

13.4 Digests

Digests verify the integrity of the programmed non-volatile data. Digests are a cryptographic hash of various data areas. Any digest that reports back an error raises the digest tamper flag.

The following are digestible non-volatile areas:

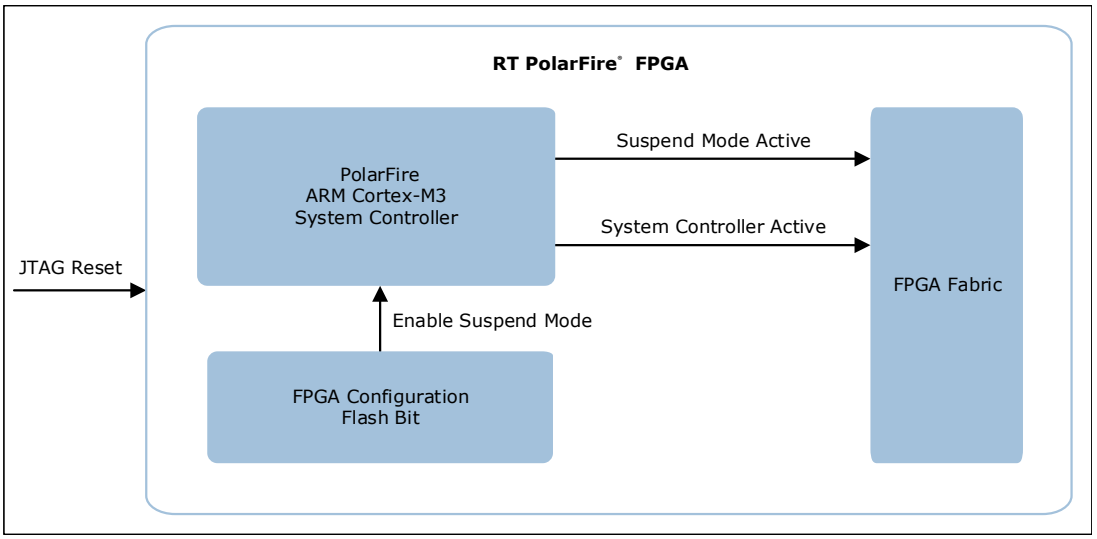
- The FPGA fabric and consequently the µPROM
- sNVM marked as ROM
- User key 1
- User key 2
- Factory parametric and key storage

13.5 System Controller Suspend Mode

For safety critical applications, RT PolarFire FPGAs allow the user to place the Cortex-M3-based system controller in a Reset state after the FPGA has powered up. By programming a SEU-immune non-volatile configuration bit, the Cortex-M3 is placed in reset by a triple-module redundant reset latch after FPGA power-up. User logic can monitor if the Suspend mode command is active. The system controller cannot fetch instructions while in the Reset state. The FPGA can be re-programmed after exiting the Suspend mode by asserting the appropriate JTAG signals. The JTAG TRSTB signal must be asserted low for the system controller to remain in Suspend mode.

The following illustration shows how to activate and deactivate Suspend mode.

Figure 13-1. System Controller Suspend Mode



14. Security

Microchip's RT PolarFire FPGAs implement layered security and represent the industry's most advanced and secure programmable FPGAs; Users may choose devices based on the level of security needed in their applications.

14.1 Hardware Security

Security considerations for an electronic system start from wafer manufacturing and continue all the way through to deployed end products. The following features provide state-of-the-art supply chain assurance in all RT PolarFire FPGAs:

- Secure supply chain management using hardware security modules (HSMs) during wafer testing and packaging.
- Supply chain assurance using a 768-byte digitally signed x.509 FPGA certificate embedded in every FPGA.
- Microchip's Secure Production Programming Solution (SPPS) extends the secure supply chain to the customer's manufacturing flow.

14.2 Design Security

The following features are available in all RT PolarFire FPGAs.

- CRI patent-protected DPA countermeasures, AES-256 encrypted bitstream, and key management protocols
- Built-in tamper detection using voltage monitors, temperature monitors, clock glitch detectors, frequency monitors, JTAG active detectors, and protective meshes. Programmable tamper responses like disabling specific I/Os, security lockdown, reset, and zeroization.
- Zeroization capabilities for all on-chip memories and the FPGA fabric
- Random number generation with Physically unclonable function (PUF) as the source of entropy

The following features are available in select devices (referred to as "S" devices with "TS" / "TLS" in the part number).

- Root of trust implementation: digital signature service to sign user-supplied SHA-384 hash
- Read and write authenticated plain text and cipher text to secure non-volatile memory
- PUF emulation for device authentication or pseudo-random bit string generation
- Nonce service provides an alternate source of entropy using the SRAM-PUF

14.3 Data Security

Select RT PolarFire FPGAs ("S" devices with "TS" / "TLS" in the part number) include a TeraFire EXP-F5200B cryptographic co-processor that enables high-speed DPA-safe cryptographic protocols at wire-line speeds. These data security features include:

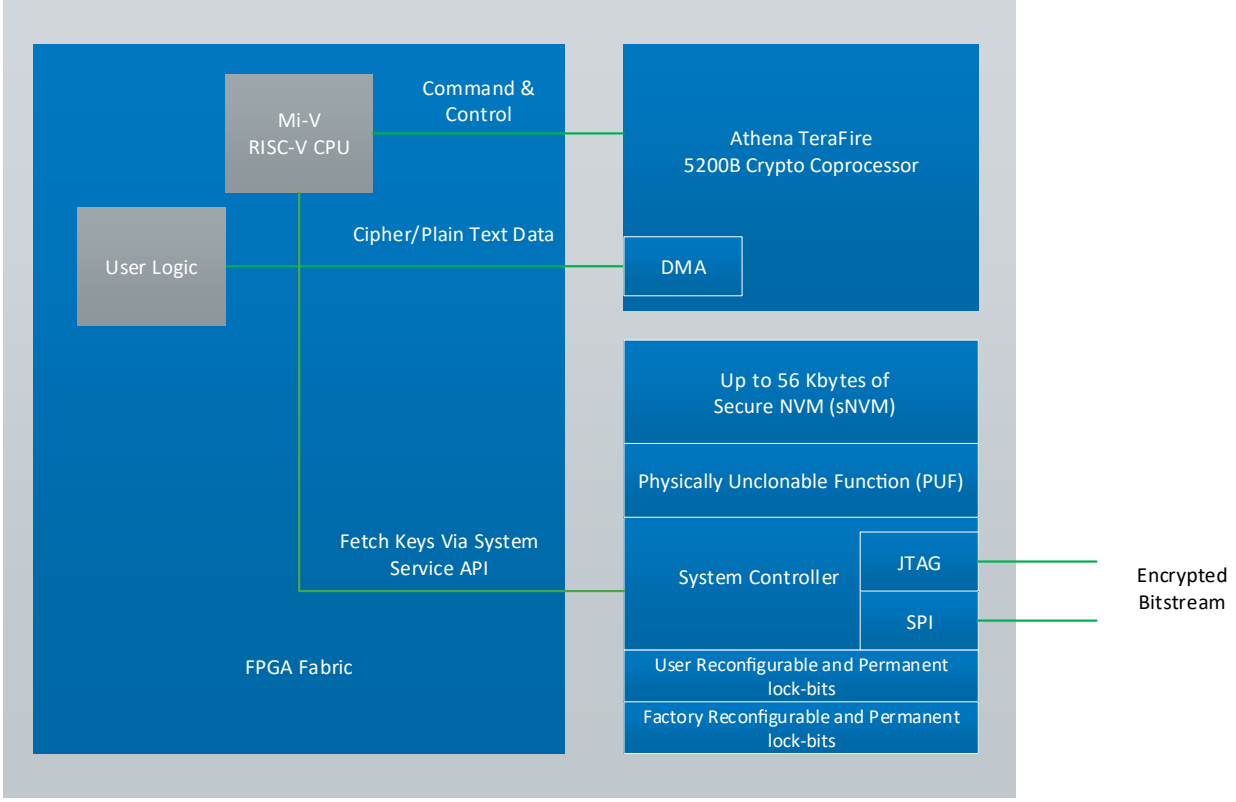
- Integrated true random number generator for modern cryptographic protocols at greater than 100 Mbps
- 189 MHz Athena TeraFire 5200B DPA safe Crypto Coprocessor capable of implementing Suite-B+ algorithms.
- CRI DPA pass-through licensing enables DPA-safe high-speed cryptographic designs in the FPGA fabric. A CRI license is included in the purchase price of the "S" device. There is no need to negotiate a separate license.
- NIST-certified protocols

The following are TeraFire EXP-F5200B supported protocols/features:

- TRNG (integrated): SP800-90A CTR_DRBG-256, and SP800-90B(draft) NRBG
- AES-128/192/256 E/D (ECB, CBC, CTR, OFB, CFB, CCM, GCM, KeyWrap)
- SHA-1/224/256/384/512
- HMAC-SHA-256/384/512; GMAC; CMAC
- SHA-256 Key Tree
- ECC-NIST P192/224/256/384/521 and Brainpool P256/384/512 curves with: KAS-ECC CDH; ECDSASigGen, SigVer, PKG, and PKV
- FFC: 1024/1536/2048/3072/4096-bits with: DSA SigGen and SigVer; and KAS-DH
- IFC: 1024/1536/2048/3072/4096/8192-bits with RSA E/D; SSA_PKCS1_V1_5 SigGen and SigVer; and ANSI X9.31 SigGen and SigVer

The following illustration shows a typical use model for using the Athena Crypto Coprocessor.

Figure 14-1. Using the Athena TeraFire 5200B Crypto Coprocessor



Users instantiate a RISC-V CPU for command and control, including fetching keys from the system controller through a system service API, initializing the Athena Core, and setting up DMA to perform the desired function. The TeraFire core comes with a complete firmware driver library for all supported protocols. These driver libraries are delivered to the designer's desktop through our Firmware Catalog within the Libero SoC toolset.

14.4 Security Features Summary

The tables below provide a summary of the security features and system services.

Feature		RT PolarFire FPGA	
		Non-S	S
Hardware Security	Supply chain assurance	Available	Available
	Anti-cloning protection	Available	Available
	Device integrity protection	Available	Available
	Hardware Access control with passcodes and security locks	Available	Available
Design Security	Key management	Available	Available
	Encrupted bitstream	Available	Available
	Bitstream versioning	Available	Available
	Digest for data integrity	Available	Available
	Tamper Monitoring on JTAG, Voltage, Temperature, clock glitch, clock frequency, Mesh	Available	Available
Data Security	User Cryptoprocessor and NRBG	—	Available
	DPA protection CRI pass-through license	—	Available
	Digital Signature Service	—	Available
	Secure NVM Write	Plaintext only	Plaintext Authenticated plaintext Authenticated ciphertext
	Secure NVM Read	Plaintext only	Plaintext Authenticated plaintext Authenticated ciphertext
	PUF Emulation	—	Available
	Nonce Service	Entropy from PUF	Entropy from PUF + Device unique key

System Services		RT PolarFire FPGA	
		Non-S	S
Device and Design Information Services	Serial Number Service	Available	Available
	Usercode Service	Available	Available
	Design Information service	Available	Available
	Device Certificate Service	Available	Available
	Read Digest SERvice	Available	Available
	Query Security Service	Available	Available
	Read Debug Information Service	Available	Available
Design Programming Services	Bitstream Authentication Service	Available	Available
	IAP Image Authentication Service	Available	Available

.....continued

System Services		RT PolarFire FPGA	
		Non-S	S
Fabric Services	Digest Check Service	Available	Available
	In-Application Programming Service	Available	Available
	Auto Update Service	Available	Available
SPI Flash Memory Read Service	SPI Copy Service	Available	Available

15. Device Offerings

RT PolarFire FPGAs offer low-power transceiver devices and various device offerings with transceivers, such as design security, data security, and low-power data security. All RT PolarFire FPGAs are integrated with multi-protocol industry-leading low-power transceivers. Low-power (L) devices provide up to 35 percent lower static power with identical electrical specifications to the STD speed grade device. Also, data security (S) devices integrate a DPA-resistant crypto accelerator.

The following table lists the RT PolarFire FPGA device options. Temperatures listed are junction temperatures.

Table 15-1. RT PolarFire FPGA Offerings

Device Options	Military Temperature –55 °C–125 °C	STD Speed Grade	–1 Speed Grade	Transceivers (T)	Lower Static Power (L)	Data Security (S)
RTPF500T, RTPF500ZT	Yes	Yes	Yes	Yes	—	—
RTPF500TL, RTPF500ZTL	Yes	Yes	—	Yes	Yes	—
RTPF500TS, RTPF500ZTS	Yes	Yes	Yes	Yes	—	Yes
RTPF500TLS, RTPF500ZTLS	Yes	Yes	—	Yes	Yes	Yes

The following table lists the temperature offerings for the RT PolarFire FPGA device.

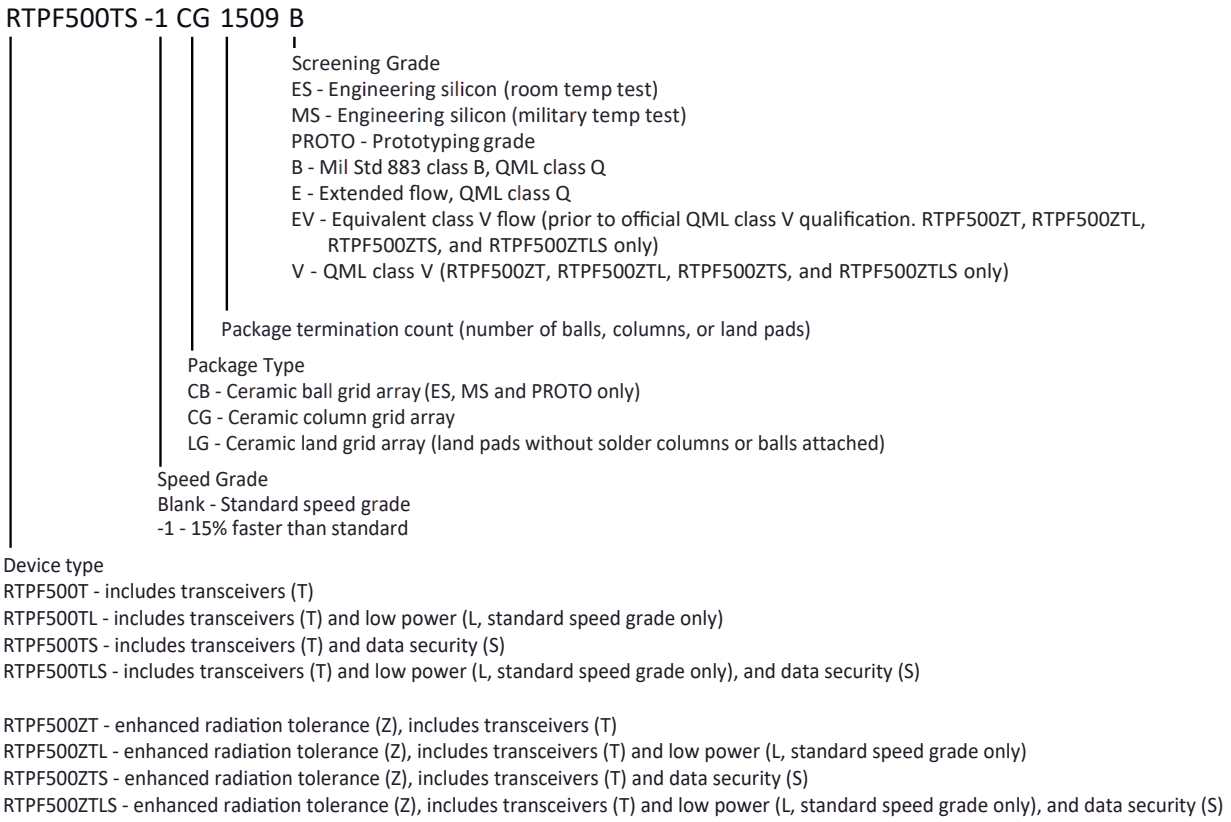
Table 15-2. RT PolarFire Temperature Rating

Screening Level	Junction Temperature Range
ES	0 °C to 100 °C (room temperature test only)
MS	–55 °C to 125 °C (tested at 125 °C)
PROTO	–55 °C to 125 °C
B	–55 °C to 125 °C
E	–55 °C to 125 °C
EV	–55 °C to 125 °C
V	–55 °C to 125 °C

16. Ordering Information

RT PolarFire FPGAs are offered with multiple speed grades, screening levels, and package combinations. All FPGAs are equipped with low-power transceivers.

Figure 16-1. Ordering Information



17. Export Classification

The following table lists the RT PolarFire FPGA export classification.

Table 17-1. RT PolarFire FPGA Export Classification

Device Options	ECCN
RTPF500T, RTPF500ZT	5A992.c
RTPF500TL, RTPF500ZTL	5A992.c
RTPF500TS, RTPF500ZTS	5A992.c
RTPF500TLS, RTPF500ZTLS	5A992.c

18. Revision History

Revision	Date	Description
A	08/2023	• Added a new column for RTPF500ZT, RTPF500ZTL, RTPF500ZTS, and RTPF500ZTLS in Table 3-1, Table 15-1, and Table 17-1. • Added RTPF500ZT FPGA organizational information in sNVM section. • Added RTPF500ZT, RTPF500ZTL, RTPF500ZTS, and RTPF500ZTLS to Figure 16-1. • Updated document to Microchip template. • Updated document number from 51700145 to DS00004232. • Updated transceiver performance to 12.7 Gbps maximum throughout document. • Added section Product Screening Flows. • Deleted placeholder I/O performance tables. For performance specifications, see the RT PolarFire FPGA Datasheet. • Deleted sections Input Buffer Speed, Output Buffer Speed, Maximum PHY Rate for Memory Interface IP, and I/O Digital Modes. • Added reference to the AN4903 application note in Overview and Programming sections. • Updated Single-Event Latch-Up Threshold values in Radiation Features section. • Replaced Figure 2-1 with new RT PolarFire FPGA Block Diagram.
1.0	10/2019	Initial Revision

Microchip Information

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable". Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure

that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet- Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, TrueTime, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, Clockstudio, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, GridTime, IdealBridge, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, IntelliMOS, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, KoD, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQI, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, Trusted Time, TSHARC, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

ISBN: 978-1-5224-9014-2

Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office	**Australia - Sydney**	**India - Bangalore**	**Austria - Wels**
2355 West Chandler Blvd.	Tel: 61-2-9868-6733	Tel: 91-80-3090-4444	Tel: 43-7242-2244-39
Chandler, AZ 85224-6199	**China - Beijing**	**India - New Delhi**	Fax: 43-7242-2244-393
Tel: 480-792-7200	Tel: 86-10-8569-7000	Tel: 91-11-4160-8631	**Denmark - Copenhagen**
Fax: 480-792-7277	**China - Chengdu**	**India - Pune**	Tel: 45-4485-5910
Technical Support:	Tel: 86-28-8665-5511	Tel: 91-20-4121-0141	Fax: 45-4485-2829
www.microchip.com/support	**China - Chongqing**	**Japan - Osaka**	**Finland - Espoo**
Web Address:	Tel: 86-23-8980-9588	Tel: 81-6-6152-7160	Tel: 358-9-4520-820
www.microchip.com	**China - Dongguan**	**Japan - Tokyo**	**France - Paris**
Atlanta	Tel: 86-769-8702-9880	Tel: 81-3-6880- 3770	Tel: 33-1-69-53-63-20
Duluth, GA	**China - Guangzhou**	**Korea - Daegu**	Fax: 33-1-69-30-90-79
Tel: 678-957-9614	Tel: 86-20-8755-8029	Tel: 82-53-744-4301	**Germany - Garching**
Fax: 678-957-1455	**China - Hangzhou**	**Korea - Seoul**	Tel: 49-8931-9700
Austin, TX	Tel: 86-571-8792-8115	Tel: 82-2-554-7200	**Germany - Haan**
Tel: 512-257-3370	**China - Hong Kong SAR**	**Malaysia - Kuala Lumpur**	Tel: 49-2129-3766400
Boston	Tel: 852-2943-5100	Tel: 60-3-7651-7906	**Germany - Heilbronn**
Westborough, MA	**China - Nanjing**	**Malaysia - Penang**	Tel: 49-7131-72400
Tel: 774-760-0087	Tel: 86-25-8473-2460	Tel: 60-4-227-8870	**Germany - Karlsruhe**
Fax: 774-760-0088	**China - Qingdao**	**Philippines - Manila**	Tel: 49-721-625370
Chicago	Tel: 86-532-8502-7355	Tel: 63-2-634-9065	**Germany - Munich**
Itasca, IL	**China - Shanghai**	**Singapore**	Tel: 49-89-627-144-0
Tel: 630-285-0071	Tel: 86-21-3326-8000	Tel: 65-6334-8870	Fax: 49-89-627-144-44
Fax: 630-285-0075	**China - Shenyang**	**Taiwan - Hsin Chu**	**Germany - Rosenheim**
Dallas	Tel: 86-24-2334-2829	Tel: 886-3-577-8366	Tel: 49-8031-354-560
Addison, TX	**China - Shenzhen**	**Taiwan - Kaohsiung**	**Israel - Ra'anana**
Tel: 972-818-7423	Tel: 86-755-8864-2200	Tel: 886-7-213-7830	Tel: 972-9-744-7705
Fax: 972-818-2924	**China - Suzhou**	**Taiwan - Taipei**	**Italy - Milan**
Detroit	Tel: 86-186-6233-1526	Tel: 886-2-2508-8600	Tel: 39-0331-742611
Novi, MI	**China - Wuhan**	**Thailand - Bangkok**	Fax: 39-0331-466781
Tel: 248-848-4000	Tel: 86-27-5980-5300	Tel: 66-2-694-1351	**Italy - Padova**
Houston, TX	**China - Xian**	**Vietnam - Ho Chi Minh**	Tel: 39-049-7625286
Tel: 281-894-5983	Tel: 86-29-8833-7252	Tel: 84-28-5448-2100	**Netherlands - Drunen**
Indianapolis	**China - Xiamen**		Tel: 31-416-690399
Noblesville, IN	Tel: 86-592-2388138		Fax: 31-416-690340
Tel: 317-773-8323	**China - Zhuhai**		**Norway - Trondheim**
Fax: 317-773-5453	Tel: 86-756-3210040		Tel: 47-72884388
Tel: 317-536-2380			**Poland - Warsaw**
Los Angeles			Tel: 48-22-3325737
Mission Viejo, CA			**Romania - Bucharest**
Tel: 949-462-9523			Tel: 40-21-407-87-50
Fax: 949-462-9608			**Spain - Madrid**
Tel: 951-273-7800			Tel: 34-91-708-08-90
Raleigh, NC			Fax: 34-91-708-08-91
Tel: 919-844-7510			**Sweden - Gothenberg**
New York, NY			Tel: 46-31-704-60-40
Tel: 631-435-6000			**Sweden - Stockholm**
San Jose, CA			Tel: 46-8-5090-4654
Tel: 408-735-9110			**UK - Wokingham**
Tel: 408-436-4270			Tel: 44-118-921-5800
Canada - Toronto			Fax: 44-118-921-5820
Tel: 905-695-1980			
Fax: 905-695-2078			