Terrestrial FPGA and SoC Product Families

Lowest Power, Proven Security and Exceptional Reliability

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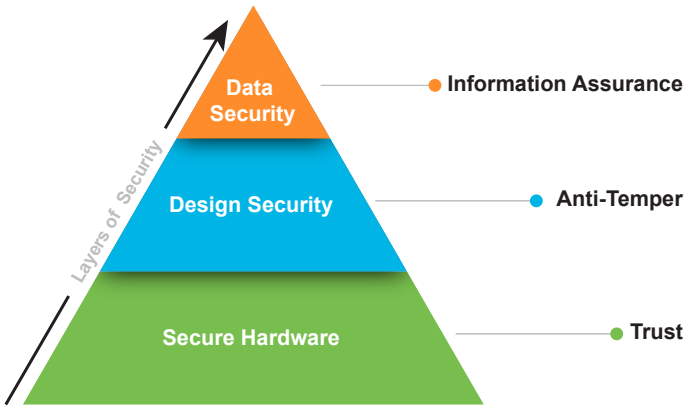
Value Proposition

Security

Securing the edge requires robust security. The PolarFire® family of FPGAs and SoC FPGAs is built upon the three fundamental security principles of confidentiality, integrity and authenticity.



- Cryptography Research Incorporated (CRI)-patented differential power analysis (DPA) bitstream protection
- Integrated physically unclonable function (PUF)
- 56 Kbytes of secure non-volatile memory (sNVM)
- Built-in tamper detectors and countermeasures
- Digest integrity check for FPGA, µPROM, and sNVM
- Data security features in S devices—true random number generator, integrated Athena's TeraFire® EXP5200B Crypto Coprocessor, suite B capable, and CRI DPA countermeasure pass-through license

To learn more please visit: https://www.microchip.com/en-us/products/security/secure-fpgas-and-soc-fpgas.

Reliability

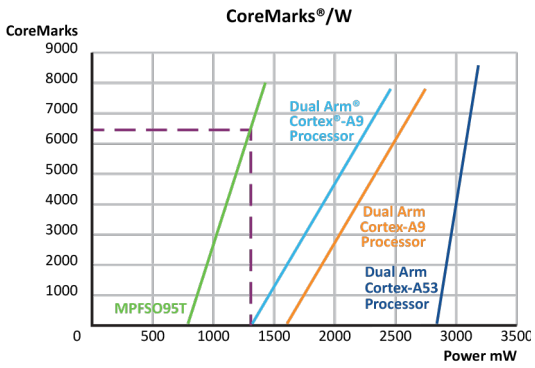
Our FPGAs address the high-reliability requirements of high-availability, safety-critical and mission-critical systems in industrial, aviation, military and communications applications. The growth in safety standards in a wide range of industries is driving these high-reliability requirements.

- FPGA configuration cells single event upset (SEU) immune
- Built-in SECDED and memory interleaving on LSRAMs
- System controller suspend mode for safety-critical designs

To learn more please visit: https://www.microchip.com/en-us/products/fpgas-and-plds/reliability.

Low Power

Microchip FPGAs and SoC FPGAs consume up to 50% lower total power than competitive FPGAs. Our nonvolatile process delivers FPGA families that are live at power-up with minimal in-rush current, and significantly lower leakage than SRAM-based alternatives. Take it one step further; run a power benchmark with our power estimator. Seeing is believing.



- Fanless enclosures with small/no heat sink
- Increased thermal headroom for more compute capability

To learn more please visit: https://www.microchip.com/en-us/products/fpgas-and-plds/low-power

Segments

Commercial Aviation

With our broad product portfolio and proven track record of innovation, quality and reliability on aerospace platforms over the past 20 years, we are excited to be a key partner on existing and future aerospace platforms. We continue to leverage our technology and extensive capabilities in this segment to support the ever-increasing electronic content in today's aircrafts. Our FPGAs have evolved to become a leading-edge systems solution for the most demanding aerospace applications.

To learn more please visit: https://www.microchip.com/en-us/solutions/aerospace-and-defense/aviation/fpga.

Defense

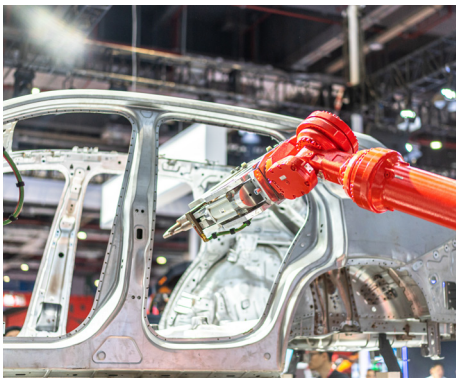
Power, security, reliability and military temperature range support are critical to defense applications such as radar and electronic warfare, guidance and control systems and secure communications used in autonomous weapons, missiles, smart munitions and other products. Our array of solutions reduces your integration risk, increases your productivity and speeds your time to mission.

To learn more please visit: https://www.microchip.com/en-us/solutions/aerospace-and-defense/defense.

Industrial

The fourth industrial revolution integrates connectivity and automation, supported by an increased focus on real-time analytics. It is also driving the shift in intelligent process loads from the cloud to the edge of the industrial networks to enable decentralized decision making. Our FPGAs offer increased design customizability, advanced data and design security features at small footprints and up to 50% lower power than the competition. Our FPGAs are an ideal fit for machine vision, robotics, thermal imaging and other industrial technologies that require power-efficient, accelerated processing.

To learn more please visit: https://www.microchip.com/en-us/solutions/industrial/fpga.



Automotive

We offer one of the widest automotive product portfolios for FPGAs and SoC FPGAs. Our customers use our low-power, instant-on and high-reliability AEC-Q100 FPGAs in many applications including inverter control and DC-DC conversion in electric/hybrid electric vehicles and Smart Embedded Vision (SEV) applications in various aspects of Advanced Driver-Assistance Systems (ADAS).

To learn more please visit: https://www.microchip.com/en-us/solutions/automotive-and-transportation/automotive-products/fpga.

Communication

Overcome power, system size, cost and security challenges across communication applications by selecting from our families of FPGAs. You'll find pre-built solutions for Digital Signal Processing (DSP), Serializer/Deserializer (SerDes), networking, microcontrollers (MCUs), microprocessors (MPUs) and even analog blocks to accelerate your design and simplify development. If your primary need is high speed, high security or high volume, we have an FPGA for your logic integration needs.

To learn more please visit: https://www.microchip.com/en-us/solutions/communications-infrastructure/fpga.

Medical

As the healthcare industry rapidly evolves, your ability to design smart, connected and secure IoT-enabled medical devices is critical. As an experienced medical supplier, we can help you meet these design requirements quickly. We've helped medical companies design and manufacture clinical, wearable, implantable and life-critical medical devices for many years. Not only do we have a comprehensive product portfolio, but we lower design barriers with our easy-to-use tools, software, and design files.

To learn more please visit: https://www.microchip.com/en-us/solutions/medical.

FPGAs and SoC FPGAs

Rethink FPGAs

Our unique, low-power, non-volatile technology sets Microchip's Field Programmable Gate Arrays (FPGAs) apart from traditional SRAM-based devices. With an extensive heritage of reliability, Microchip's FPGAs and SoCs meet demands for low power, and security in a variety of applications.

In wired and wireless communications, defense and aviation, and industrial embedded applications, Microchip FPGAs deliver ample resources at the lowest power, highest reliability and greatest security. Microchip FPGAs demonstrate value in applications such as hardware acceleration, artificial intelligence, image processing and edge computing with robust DSP and memory resources.

Broad Range FPGA Supplier

Features	SmartFusion® ProASIC3®, IGLOO®	SmartFusion® 2 IGLOO® 2	PolarFire® SoC PolarFire
Logic Elements	100–30K	5K–150K	25K–480K
Transceiver Rate	–	1–5 Gbps	250 Mbps–12.7 Gbps
I/O Speeds	400 Mbps LVDS	667 Mbps DDR3 750 Mbps LVDS	1600 Mbps DDR4 1.6 Gbps LVDS
DSP (18x18 Multipliers)	–	240	1480
Max RAM	144 Kb	5 Mb	33 Mb
Processor Option	Hard 100 MHz Arm® Cortex®-M3	Hard 166 MHz Arm Cortex-M3 Soft RISC-V	Soft RISC-V Quad Core RISC-V (PolarFire SoC only) Hard Crypto Processor
On-Board Flash	Up to 512 KB code store	Up To 512 KB code store	128 KB Code Storage 56 KB secure NVM
Family Type	CPLD Replacements Smallest Packages	Low Density FPGAs with more resources and lowest power	Mid-Range Density FPGAs Lowest Power, Cost Optimized

PolarFire SoC

Lowest-Power, Multi-Core RISC-V SoC FPGAs

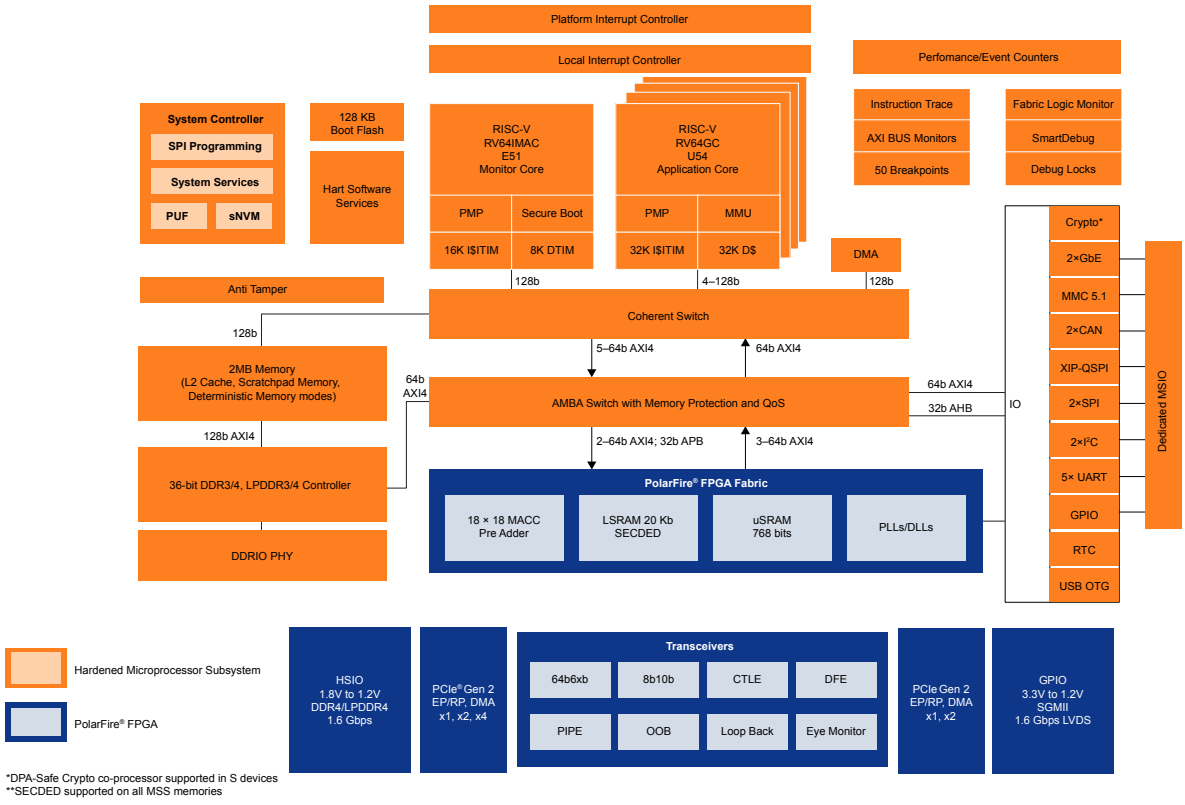
The PolarFire SoC FPGA family delivers a combination of low power consumption, thermal efficiency and defense-grade security for smart, connected systems. It is the first System-on-Chip (SoC) FPGA with a deterministic, coherent RISC-V CPU cluster and a deterministic L2 memory subsystem for creating Linux® and real-time applications. PolarFire SoC FPGAs span from 25K to 460K Logic Elements (LEs) and feature 12.7 Gbps transceivers.

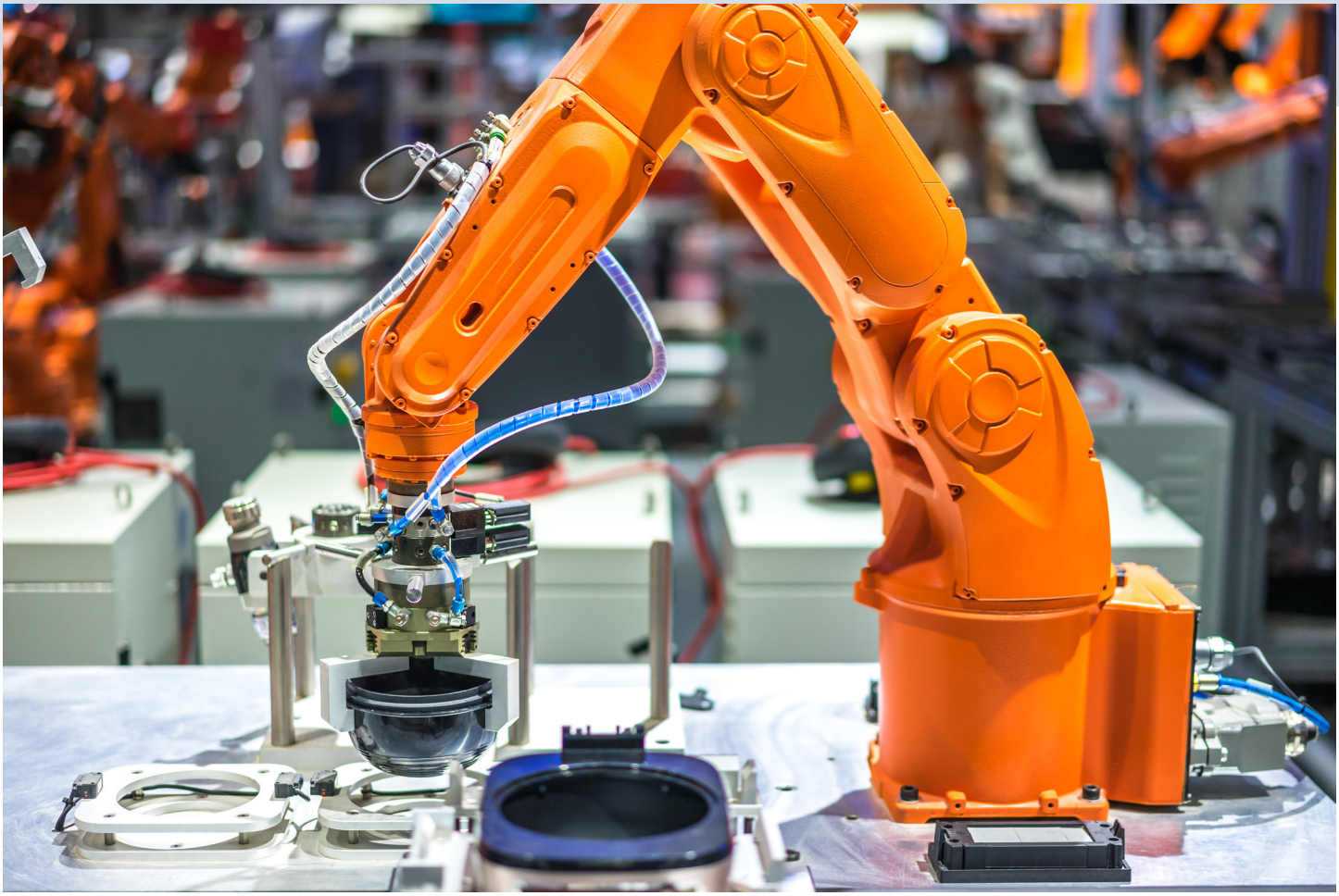
Lowest-Power SoC FPGAs

This graph of the EEMBC CoreMark-Pro benchmarks over power consumed illustrates the PolarFire SoC FPGA's low-power advantage.

Built on the award-winning, mid-range, low-power PolarFire FPGA architecture, PolarFire SoC delivers up to 50% lower power than comparable FPGAs.

At 1.3W, PolarFire SoC FPGAs deliver 6,500 CoreMarks while competing SoC FPGAs deliver 0 CoreMarks. PolarFire SoC FPGAs consume 55% lower power at 8,000 CoreMarks.





PolarFire® SoC Product Table						
	Features	**MPFS025T**	**MPFS095T**	**MPFS160T**	**MPFS250T**	**MPFS460T**
FPGA Fabric	K Logic Elements (4LUT + DFF)	23	93	161	254	461
	Math Blocks (18 × 18 MACC)	68	292	498	784	1420
	LSRAM Blocks (20 kbits)	84	308	520	812	1460
	uSRAM Blocks (64 × 12)	204	876	1494	2352	4260
	Total RAM Mbits	1.8	6.7	11.3	17.6	31.6
	uPROM Kbits	194	387	415	470	553
	User DLLs/PLLs	8 each	8 each	8 each	8 each	8 each
High Speed I/O	250 Mbps to 12.5 Gbps SerDes Lanes	4	4	8	16	20
	PCIe® Gen 2 End Points/Root Ports	2	2	2	2	2
Total FPGA I/O	HSIO+GPIO	108	276	312	372	468
Total MSS I/O	MSS I/O	136	136	136	136	136
MSS DDR DB	MSS DDR Data Bus	16 / 32 [1]	16 / 32 [1]	32	32	32

PolarFire® SoC Packaging					
Features	**MPFS025T**	**MPFS095T**	**MPFS160T**	**MPFS250T**	**MPFS460T**
Extended Commercial and Industrial	**Total User I/O: MSS-IO,HSIO,GPIO,XCVRs**				
FCSG325 (11 × 11, 11 × 14.5, 0.5 mm) [2]	102, 32, 48, 2	102, 32, 48, 2			
FCSG536 (16 × 16, 0.5 mm)		136, 60, 84, 4	136, 60, 108, 4	136, 60, 108, 4	
FCVG484 (19 × 19, 0.8 mm)	136, 60, 48, 4	136, 60, 84, 4	136, 60, 84, 4	136, 60, 84, 4	
FCVG784 (23 × 23, 0.8 mm)		136, 144, 132, 4	136, 144, 168, 8	136, 144, 180, 8	
FCG1152 (35 × 35, 1.0 mm)				136, 144, 228, 16	
Military 'S' devices only	**Total User I/O: MSS-IO,HSIO,GPIO,XCVRs**				
FCS325 (11 × 11, 0.5 mm)		102, 32, 48, 2			
FCS536 (16 × 16, 0.5 mm)				136, 60, 108, 4	
FCVG484 (19 × 19, 0.8 mm)				136, 60, 84, 4	
FCV784 (23 × 23, 0.8 mm)				136, 144, 180, 8	
FC1152 (35 × 35, 1.0 mm)				136, 144, 228, 16	
Automotive 'T2'	**Total User I/O: MSS-IO,HSIO,GPIO,XCVRs**				
FCSG536 (16 × 16, 0.5 mm)				136, 60, 108, 4	
FCVG484 (19 × 19, 0.8 mm)				136, 60, 84, 4	
FCVG784 (23 × 23, 0.8 mm)				136, 144, 180, 8	136, 180, 288, 20

Notes: 1. 16-bit DDR data bus width for the FCSG325 package 11 × 14.5 for MPFS095T

2. FCSG325 package is available in 11 × 11 for MPFS025T and

Quick Links for PolarFire SoC

PolarFire SoC FPGA Device: https://www.microchip.com/en-us/products/fpgas-and-plds/system-on-chip-fpgas/polarfire-soc-fpgas

PolarFire SoC Git Hub here: https://github.com/polarfire-soc

Mi-V RISC-V Ecosystem

Mi-V, pronounced "my five," is our continuously expanding, comprehensive suite of tools and design resources that we developed with numerous third parties to support RISC-V designs. The Mi-V ecosystem aims to increase adoption of the RISC-V Instruction Set Architecture (ISA) and our System on Chip (SoC) FPGA and RISC-V soft CPU portfolio.

To know more about Mi-V Ecosystem Visit: https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/mi-v

PolarFire Cost-Optimized to Deliver the Lowest Power at Mid-Range Densities

The PolarFire family extends Microchip's non-volatile FPGA leadership by offering up to 50% lower power than equivalent SRAM FPGAs. The devices are ideal for a wide range of implementations within wireline access networks and cellular infrastructure, defense and commercial aviation markets, as well as industrial automation and IoT markets. The devices offer unprecedented capabilities while maintaining all the advantages traditionally associated with non-volatile FPGAs such as the lowest static power, the best security and FPGA configuration cell Single Event Upset (SEU) immunity.

The PolarFire family is cost-optimized to give designers a mid-range portfolio of FPGAs with the SERDES and DSP resources needed for a range of high-speed and compute intensive applications constrained by low-power and small formfactor.

As a true broad-range FPGA supplier, Microchip offers FPGA product families spanning 1K to 500K Logic Elements (LEs).

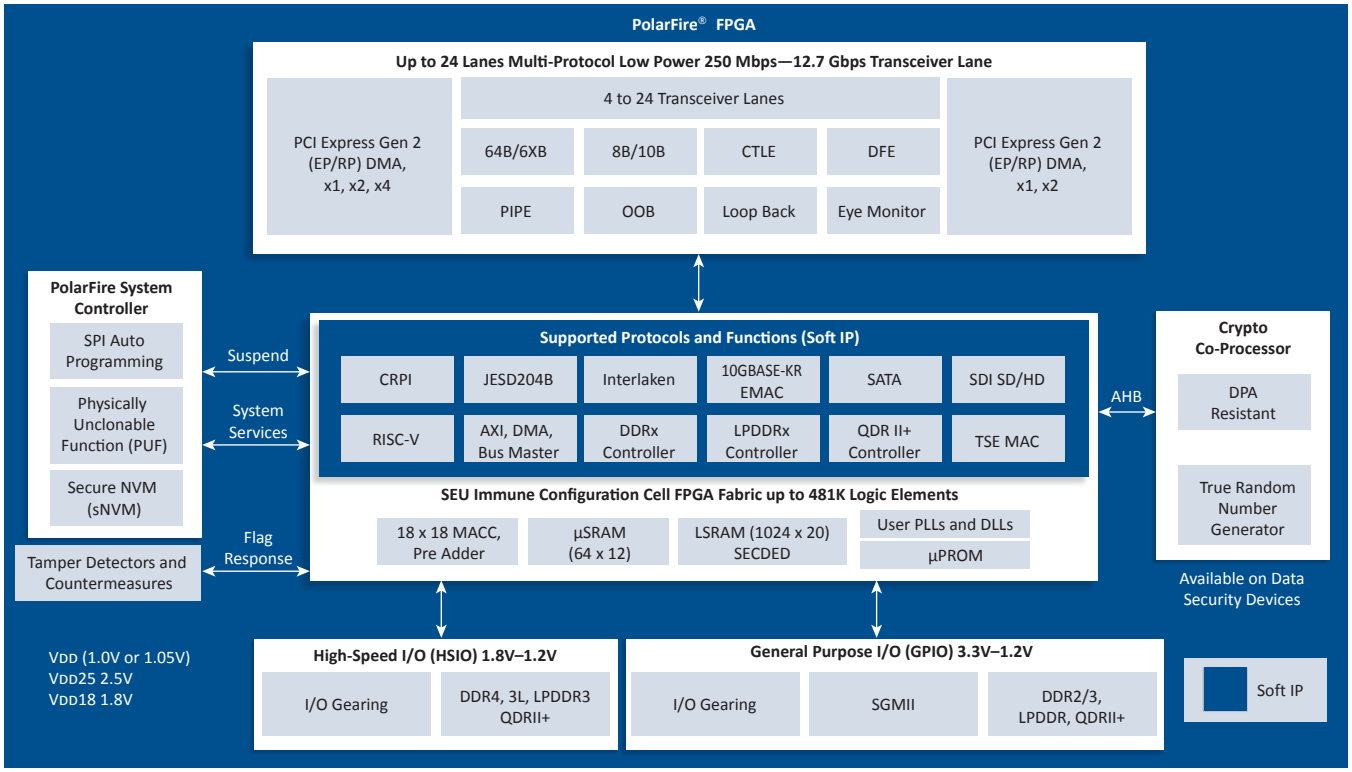
The devices offer unprecedented capabilities while maintaining all the advantages traditionally associated with non-volatile FPGAs such as the lowest static power, security and Single Event Upset (SEU) immunity.

Cost-Optimized Architecture

- Transceiver performance optimized for 12.7 Gbps, which yields smaller size
- Architecture and process optimizations for specific bandwidths (10 Gbps–40 Gbps) at specific densities
- 1.6 Gbps I/Os—best-in-class hardened I/O gearing logic with CDR (supports SGMII/GbE links on these GPIOs)
- High-performance, best-in-class hardened security IP in mid-range devices

Power Optimization

- The lowest static power—28 nm non-volatile process yields very-low static power
- Optimized for 12.7 Gbps, which yields the lowest power
- Integrated hard IP—DDR PHY, PCIe endpoint/root port, crypto processor
- Total power (static and dynamic)—up to 50% lower power


PolarFire® FPGA
Up to 24 Lanes Multi-Protocol Low Power 250 Mbps—12.7 Gbps Transceiver Lane
PCI Express Gen 2 (EP/RP) DMA, x1, x2, x4
4 to 24 Transceiver Lanes
64B/6XB
8B/10B
CTLE
DFE
PIPE
OOB
Loop Back
Eye Monitor
PCI Express Gen 2 (EP/RP) DMA, x1, x2
PolarFire System Controller
SPI Auto Programming
Physically Unclonable Function (PUF)
Secure NVM (sNVM)
Tamper Detectors and Countermeasures
Suspend
System Services
Flag Response
Supported Protocols and Functions (Soft IP)
CRPI
JESD204B
Interlaken
10GBASE-KR EMAC
SATA
SDI SD/HD
RISC-V
AXI, DMA, Bus Master
DDRx Controller
LPDDRx Controller
QDR II+ Controller
TSE MAC
SEU Immune Configuration Cell FPGA Fabric up to 481K Logic Elements
18 x 18 MACC, Pre Adder
µSRAM (64 x 12)
LSRAM (1024 x 20) SECDED
User PLLs and DLLs
µPROM
AHB
Crypto Co-Processor
DPA Resistant
True Random Number Generator
Available on Data Security Devices
VDD (1.0V or 1.05V)
VDD25 2.5V
VDD18 1.8V
High-Speed I/O (HSIO) 1.8V–1.2V
I/O Gearing
DDR4, 3L, LPDDR3 QDRII+
General Purpose I/O (GPIO) 3.3V–1.2V
I/O Gearing
SGMII
DDR2/3, LPDDR, QDRII+
Soft IP

PolarFire® Product Table						
Features		PolarFire FPGA				
		MPF050	MPF100	MPF200	MPF300	MPF500
FPGA Fabric	Logic Elements (4LUT + DFF)	48K	109K	192K	300K	481K
	Math Blocks (18 × 18 MACC)	150	336	588	924	1480
	LSRAM Blocks (20 Kb)	160	352	616)	952	1520
	uSRAM Blocks (64 × 12)	450	1008	1764	2772	4440
	Total RAM (Mb)	3.6	7.6	13.3	20.6	33
	uPROM (Kb)	216	297	297	459	513
	User DLLs/PLLs	8	8 each	8 each	8 each	8 each
High-Speed I/O	250 Mbps–12.7 Gbps Transceiver Lanes	4	8	16	16	24
	PCIe® Gen 2 Endpoints/Root Ports	2	2	2	2	2
Total I/O	Total User I/O	176	296	364	512	584

PolarFire® Packaging					
Features	**MPF050**	**MPF100**	**MPF200**	**MPF300**	**MPF500**
Extended Commercial and Industrial	**Total User I/O (HSIO/GPIO) GPIO CDRs/XCVRs**				
FCSG325 (11 × 11, 11 × 14.5 0.5 mm)	164 (84/80) 6/4	170 (84/86) 8/4	170 (84/86) 8/4		
FCSG536 (16 × 16, 0.5 mm)			300 (120/180) 15/4	300 (120/180) 15/4	
FCVG484 (19 × 19, 0.8 mm)	176 (96/92) 7/4	284 (120/164) 14/4	284 (120/164)14/4	284 (120/164) 14/4	
FCG484 (23 × 23, 1.0 mm)		244 (96/148) 13/8	244 (96/148) 13/8	244 (96/148) 13/8	
FCG784 (29 × 29, 1.0 mm)			364 (132/232) 20/16	388 (156/232) 20/16	388 (156/232) 20/16
FCG1152 (35 × 35, 1.0 mm)				512 (276/236) 24/16	584 (324/260) 24/24
Military 'S' devices only	**Total User I/O (HSIO/GPIO) GPIO CDRs/XCVRs**				
FCS325 (11 × 11, 11 × 14.5 0.5 mm)			170 (84/86) 8/4		
FCS536 (16 × 16, 0.5 mm)				300 (120/180) 15/4	
FCV484 (19 × 19, 0.8 mm)				284 (120/164) 14/4	
FC484 (23 × 23, 1.0 mm)				244 (96/148) 13/8	
FC784 (29 × 29, 1.0 mm)				388 (156/232) 20/16	388 (156/232) 20/16
FC1152 (35 × 35, 1.0 mm)				512 (276/236) 24/16	584 (324/260) 24/24
Automotive 'T2'	**Total User I/O (HSIO/GPIO) GPIO CDRs/XCVRs**				
FCSG325 (11 × 11, 11 × 14.5 0.5 mm)	164 (84/80) 6/4	170 (84/86) 8/4	170 (84/86) 8/4		
FCSG536 (16 × 16, 0.5 mm)			300 (120/180) 15/4	300 (120/180) 15/4	
FCVG484 (19 × 19, 0.8 mm)	176 (96/92) 7/4	284 (120/164) 14/4	284 (120/164)14/4	284 (120/164) 14/4	
FCG484 (23 × 23, 1.0 mm)		244 (96/148) 13/8	244 (96/148) 13/8	244 (96/148) 13/8	
FCG784 (29 × 29, 1.0 mm)				388 (156/232) 20/16	

To learn more please visit: https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/polarfire-fpgas/polarfire-mid-range-fpgas

Smart Fusion® 2 SoC FPGAs

More Resources in Low-Density Devices with Arm® Cortex®-M3 Processor

SmartFusion 2 SoC FPGAs deliver more resources in low-density devices with low-power requirements, proven security and exceptional reliability. These devices are ideal for general purpose functions such as Gigabit Ethernet or dual-PCI Express control planes, bridging functions, input/output (I/O) expansion and conversion, video/image processing, system management and secure connectivity. Our SoC FPGAs are used in communications, industrial, medical, defense and aviation markets.

- Embedded Arm Cortex-M3 Microcontroller Subsystem (MSS)
- PCIe Gen2 endpoints starting at 10K logic elements
- Embedded DDR3 memory controllers
- Small packages
- 1 mW in Flash*Freeze mode
- Single Event Upset (SEU) immune
- Secure boot for FPGA and processors
- Instant-on
- Zero FIT FPGA configuration cells
- SECDED memory protection
- NRBG, AES-256, SHA-256, ECC cryptographic engine
- User Physically Unclonable Function (PUF)
- CRI DPA pass-through license

SmartFusion® 2 Product Table								
	Features	**M2S005**	**M2S010**	**M2S025**	**M2S050**	**M2S060**	**M2S090**	**M2S150**
Logic/ DSP	Maximum Logic Elements (4LUT + DFF)[1]	6,060	12,084	27,696	56,340	56,520	86,316	146,124
	Math Blocks (18 × 18)	11	22	34	72	72	84	240
	Fabric Interface Controllers (FICs)	1	1	1	2	1	1	2
	Phase Locked Loops (PLLs) and Clocked Conditioning Circuitry (CCCs)	2	2	6	6	6	6	8
Security	AES256, SHA256, RNG	1 each	1 each	1 each	1 each	1 each	1 each	1 each
	ECC, PUF	-	-	-	-	1 each	1 each	1 each
MSS	Arm® Cortex®-M3 processor + instruction cache	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	eNVM (KB)	128	256	256	256	256	512	512
	eSRAM (KB)	64	64	64	64	64	64	64
	eSRAM (KB) Non SECDED	80	80	80	80	80	80	80
	CAN, 10/100/1000 Ethernet, HS USB	1 each	1 each	1 each	1 each	1 each	1 each	1 each
	Multi-Mode UART, SPI, I^2C, Timer	2 each	2 each	2 each	2 each	2 each	2 each	2 each
Fabric Memory	LSRAM 18K Blocks	10	21	31	69	69	109	236
	uSRAM 1K Blocks	11	22	34	72	72	112	240
	Total RAM (Kb)	191	400	592	1314	1314	2074	4488
High Speed	DDR Controllers (Count × Width)	1 × 18	1 × 18	1 × 18	2 × 36	1 × 18	1 × 18	2 × 36
	SerDes Lanes	0	4	4	8	4	4	16
	PCIe® End Points	0	1	1	1	2	2	4
User I/Os	MSIO (3.3V)	115	123	157	139	279	309	292
	MSIOD (2.5V)	28	40	40	62	40	40	106
	DDRIO (2.5V)	66	70	70	176	76	76	176
	Total User I/O	209	233	267	377	395	425	574

SmartFusion® 2 Packaging							
Features	**M2S005**	**M2S010**	**M2S025**	**M2S050**	**M2S060**	**M2S090**	**M2S150**
Commercial and Industrial	**I/O**						
TQG144 (20 x 20, 0.5 mm)	84	84					
FCSG158 (9 × 9, 0.5 mm)			82				
FCS(G)325 (11 × 11, 0.5 mm)			180	200	200	180	
VF(G)256 (14 × 14, 0.8 mm)	161	138	138				
FCS(G)536 (16 × 16, 0.5 mm)							293
VF(G)400 (17 × 17, 0.8 mm)	171	195	207	207	207		
FCV(G)484 (19 × 19, 0.8 mm)							248
FG(G)484 (23 × 23, 1 mm)	209	233	267	267	267	267	
FG(G)676 (27 × 27, 1 mm)					387	425	
VF(G)784 (23 × 23, 0.8 mm)					395		
FG(G)896 (31 × 31, 1 mm)				377			
FC(G)1152 (35 × 35, 1 mm)							574
Military	**I/O**						
FCV484 (19 × 19, 0.8 mm)							248
FG(G)484 (23 × 23, 1 mm)		233	267	267	267	267	
FC(G)1152 (35 × 35, 1 mm)							574
Automotive 'T2'	**I/O**						
TQG144 (20 x 20, 0.5 mm)	84	84					
VF(G)256 (14 × 14, 0.8 mm)	161	138					
VF(G)400 (17 × 17, 0.8 mm)	171	195	207		207		
FG(G)484 (23 × 23, 1 mm)	209	233	267		267	267	
FG(G)676 (27 × 27, 1 mm)					387	425	

Notes: 1. Total logic may vary based on utilization of DSP and memories in your design. Please see the SmartFusion 2 Fabric User Guide for details SmartFusion 2 Fabric User Guide

IGLOO®2 FPGAs

Low-Density Devices with High-Performance Memory Subsystem

IGLOO2 FPGAs deliver more resources in low-density devices with low-power requirements, proven security and exceptional reliability than any FPGAs in their class. These devices are ideal for general purpose functions such as Gigabit Ethernet or dual-PCI Express control planes, bridging functions, input/output (I/O) expansion and conversion, video/image processing, system management and secure connectivity. FPGAs are used in communications, industrial, medical, defense and aviation markets.

- High-performance memory subsystem
- PCIe Gen2 endpoints starting at 10K logic elements
- Embedded DDR3 memory controllers
- SECDED memory protection
- 1 mW in Flash*Freeze mode
- Instant-on
- Zero FIT FPGA configuration cells
- CRI DPA pass-through license
- Small packages
- NRBG, AES-256, SHA-256, ECC cryptographic engine
- User Physically Unclonable Function (PUF)

IGLOO® 2 Product Table								
	Features	**M2GL005**	**M2GL010**	**M2GL025**	**M2GL050**	**M2GL060**	**M2GL090**	**M2GL150**
Logic/ DSP	Maximum Logic Elements (4LUT + DFF)1	6,060	12,084	27,696	56,340	56520	86,316	146,124
	Math Blocks (18 × 18)	11	22	34	72	72	84	240
	Phase Locked Loops (PLLs) and Clocked Conditioning Circuitry (CCCs)	2	2	6	6	6	6	8
	SPI/HPDMA/ PDMA	1 each	1 each	1 each	1 each	1 each	1 each	1 each
	Fabric Interface Controllers (FICs)	1	1	1	2	1	1	2
	Security	AES256, SHA256, RNG	AES256, SHA256, RNG	AES256, SHA256, RNG	AES256, SHA256, RNG	AES256, SHA256, RNG, ECC, PUF	AES256, SHA256, RNG, ECC, PUF	AES256, SHA256, RNG, ECC, PUF
Memory	eNVM (KB)	128	256	256	256	256	512	512
	LSRAM 18K Blocks	10	21	31	69	69	109	236
	uSRAM 1K Blocks	11	22	34	72	72	112	240
	eSRAM (KB)	64 each	64 each	64 each	64 each	64 each	64 each	64 each
	Total RAM (Kb)	703	912	1104	1826	1826	2586	5000
High Speed	DDR Controllers	1 × 18	1 × 18	1 × 18	2 × 36	1 × 18	1 × 18	2 × 36
	SerDes Lanes	0	4	4	8	4	4	16
	PCIe® End Points	0	1	1	2	2	2	4
User I/Os	MSIO (3.3V)	115	123	157	139	279	309	292
	MSIOD (2.5V)	28	40	40	62	40	40	106
	DDRIO (2.5V)	66	70	70	176	76	76	176
	Total User I/O	209	233	267	377	395	425	574

IGLOO® 2 Packaging							
Features	**M2GL005**	**M2GL010**	**M2GL025**	**M2GL050**	**M2GL060**	**M2GL090**	**M2GL150**
Commercial and Industrial	**I/O**						
FCS(G)325 (11 × 11, 0.5 mm)			180	200	200	180	
VF(G)256 (14 × 14, 0.8 mm)	161	138	138				
FCS(G)536 (16 × 16, 0.5 mm)							293
VF(G)400 (17 × 17, 0.8 mm)	171	195	207	207	207		
FCV(G)484 (19 × 19, 0.8mm)							248
TQ(G)144 (20 × 20, 0.5 mm)	84	84					
FG(G)484 (23 × 23, 1 mm)	209	233	267	267	267	267	
FG(G)676 (27 × 27, 1 mm)					387	425	
VFG784 (23 × 23, 0.8 mm)					395		
FG(G)896 (31 × 31, 1 mm)				377			
FC(G)1152 (35 × 35, 1 mm)							574
Military	**I/O**						
FCV484 (19 × 19, 0.8 mm)							248
FG(G)484 (23 × 23, 1 mm)		233	267	267	267	267	
FC(G)1152 (35 × 35, 1 mm)							574
Automotive 'T1'	**I/O**						
FGG484 (23 × 23, 1 mm)	209	233	267	267	267	267	
Automotive 'T2'	**I/O**						
VFG256 (14 ×14, 0.8 mm)	161	138	138				
VFG400 (17 × 17, 0.8 mm)	171	195	207		207		
TQG144 (20 × 20, 0.5 mm)	84	84					
FGG484 (23 × 23, 1 mm)	209	233	267	267	267	267	
FGG676 (27 × 27, 1 mm)					387	425	

Notes: 1. Total logic may vary based on utilization of DSP and memories in your design. Please see the IGLOO2 and SmartFusion2 Fabric User Guide for details.
To learn more please visit: https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/igloo-2-fpgas

IGLOO FPGAs

The Ideal Low-Power, Programmable Solution for CPLD Replacement

The IGLOO family of reprogrammable and full-featured Flash FPGAs is designed to meet the low-power and area requirements of today's portable electronics. Based on nonvolatile Flash technology, the 1.2V to 1.5V operating voltage family offers the industry's lowest-power consumption—as low as 5 µW. The IGLOO family supports up to 35K logic elements with up to 504 kbits of true dual-port SRAM, up to six embedded PLLs, and up to 620 user I/Os. Low-power applications that require 32-bit processing can use the Arm Cortex-M1 processor without license fees or royalties in M1 IGLOO devices. Developed specifically for implementation in FPGAs, Cortex-M1 devices offer an optimal balance between performance and size to minimize power consumption.

- Low-power FPGAs
- Flash*Freeze technology for low-power consumption
- 1.2V core and I/O voltage
- Instant-on
- AES-protected In-System Programming (ISP)
- User nonvolatile FlashROM

IGLOO®/e Product Table								
IGLOO/e Devices	**AGL030**	**AGL060**	**AGL125**	**AGL250**	**AGL400**	**AGL600**	**AGL1000**	**AGLE3000**
Arm® Cortex®-M1-Based Devices				**M1AGL250**		**M1AGL600**	**M1AGL1000**	**M1AGLE3000**
Equivalent LEs	330	700	1.5K	3K	5K	7K	11K	35K
System Gates	30,000	60,000	125,000	250,000	400,000	600,000	1,000,000	3,000,000
Quiescent Current (typical) in Flash*Freeze Mode (µW)	5	10	16	24	32	36	53	137
RAM Kb (1,024 bits)		18	36	36	54	108	144	504
4,608-bit Blocks		4	8	8	12	24	32	112
FlashROM Bits	1,024	1,024	1,024	1,024	1,024	1,024	1,024	1024
Secure (AES) ISP[1]		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Integrated PLLs in CCCs		1	1	1	1	1	1	6
Maximum User I/Os	77	71	133	143	178	215	300	341

Notes: 1. AES is not available for Arm processor-enabled IGLOO devices

To learn more please visit: https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/igloo-fpgas

IGLOO®/e Packaging								
Commercial and Industrial	**Single-Ended I/Os/Differential I/O Pairs**							
IGLOO Devices	**AGL030**	**AGL060**	**AGL125**	**AGL250**	**AGL400**	**AGL600**	**AGL1000**	**AGLE3000**
Arm® Cortex®-M1-Based Devices				**M1AGL250**		**M1AGL600**	**M1AGL1000**	**M1AGLE3000**
QNG48 (6 × 6 mm, 0.4 mm)	34							
CSG81 (5 × 5 mm, 0.5 mm)	66							
VQ(G)100 (14 × 14 mm, 0.5 mm)	77	71	71	68/13				
CS(G)196 (8 × 8 mm, 0.5 mm)			133	143/35	143/35			
FG(G)144 (13 × 13 mm, 1.0 mm)			97	97/24		97/25	97/25	
FG(G)256 (17 × 17 mm, 1. 0mm)					178/38	177/43	177/44	
CS(G)281 (10 × 10 mm, 0.5 mm)						215/53	215/53	
FG(G)484 (23 × 23 mm, 1.0 mm)							300/74	341/168

IGLOO Family: IGLOO nano FPGAs

The Industry's Lowest-Power, Smallest-Size Solution

IGLOO nano products offer groundbreaking possibilities in power, size, lead-times, operating temperature ranges and cost. Available in logic densities from 100–3K logic elements, 1.2V to 1.5V IGLOO nano devices have been designed for high-volume applications where power and size are the key decision criteria. IGLOO nano devices are perfect ASIC or ASSP replacements, yet retain the historical FPGA advantages of flexibility and quick time-to-market in low-power and small footprint profiles.

- Ultra-low power in Flash*Freeze mode, as low as 2 µW
- Small footprint packages from 14 mm × 14 mm to 3 mm × 3 mm
- Enhanced commercial temperature
- 1.2V to 1.5V single voltage operation
- Enhanced I/O features
- Embedded SRAM and non-volatile memory (NVM)
- ISP and security
- Instant-on

IGLOO® nano Product Table					
IGLOO nano Devices	**AGLN010**	**AGLN020**	**AGLN060**	**AGLN125**	**AGLN250**
Equivalent LEs	100	200	700	1.5 K	3K
System Gates	10,000	20,000	60,000	125,000	250,000
Flash*Freeze Mode (typical, µW)	2	4	10	16	24
RAM Kb (1,024 bits)			18	36	36
4,608-bit Blocks			4	8	8
FlashROM Bits	1,024	1,024	1,024	1,024	1,024
Secure (AES) ISP			Yes	Yes	Yes
Integrated PLLs in CCCs			1	1	1
Maximum User I/Os	34	52	71	71	68

IGLOO® nano Packaging					
IGLOO nano Devices	**AGLN010**	**AGLN020**	**AGLN060**	**AGLN125**	**AGLN250**
Commercial and Industrial	**Single-Ended I/Os**				
UCG36 (3 × 3 mm, 0.4 mm)	23				
QNG48 (6 × 6 mm, 0.4 mm)	34				
QNG68 (8 × 8 mm, 0.4 mm)		49			
CSG81 (5 × 5 mm, 0.5 mm)		52	60	60	60
VQ(G)100 (14 × 14 mm, 0.5 mm)			71	71	68

To learn more please visit: https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/igloo-fpgas

IGLOO Family: IGLOO PLUS FPGAs

Low-Power FPGA with Enhanced I/O Capabilities

IGLOO PLUS products deliver low-power consumption and enhanced I/Os in a feature-rich programmable device, offering more I/Os per logic element than IGLOO devices and supporting independent Schmitt trigger inputs, hot-swapping, and Flash*Freeze bus hold. Ranging from 330–1.5K logic elements, 1.2V to 1.5V IGLOO PLUS devices have been optimized to meet the needs of I/O-intensive, power-conscious applications that require exceptional features.

- I/O-optimized FPGA
- Low power in Flash*Freeze mode, as low as 5 µW
- Small footprint and low-cost packages
- Reprogrammable Flash technology
- 1.2V to 1.5V single voltage operation
- Embedded SRAM NVM
- AES-protected ISP
- Instant-on

IGLOO® PLUS Product Table		
IGLOO® PLUS Devices	**AGLP030**	**AGLP060**
Equivalent LEs	330	700
System Gates	30,000	60,000
Quiescent Current (typical)	5	10
in Flash*Freeze Mode (µW)		
RAM Kb (1,024 bits)		18
4,608-bit Blocks		4
FlashROM Bits	1,024	1,024
Secure (AES) ISP		Yes
Integrated PLLs in CCCs		1
Maximum User I/Os	120	157

To learn more please visit: https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/igloo-fpgas

IGLOO® PLUS Packaging		
IGLOO® PLUS Devices	**AGLP030**	**AGLP060**
Commercial and Industrial	**I/Os**	
CSG201 (8 × 8 mm, 0.5mm)	120	157
CSG281 (10 × 10 mm, 0.5mm)		
VQG128 (14 × 14 mm, 0.4mm)	101	

ProASIC®3 Family: ProASIC3/E FPGAs

Low-Density FPGAs for Replacing CPLDs

The ProASIC3 series of Flash FPGAs offers a breakthrough in power, performance, density and features for today's most demanding high-volume applications. ProASIC3 devices support the Arm Cortex-M1 processor, offering the benefits of programmability and time-to-market at low cost. ProASIC3 devices are based on nonvolatile Flash technology and support 330–35K logic elements and up to 620 high-performance I/Os. For automotive applications, selected ProASIC3 devices are qualified to AEC-Q100 and are available with AEC T1 screening and PPAP documentation.

- 1.5V single voltage operation
- 350 MHz system performance
- Instant-on
- Configuration memory error immune
- Advanced I/O standards
- Secure ISP

ProASIC® 3/e Product Table										
ProASIC 3/3e Devices	**A3P030**	**A3P060**	**A3P125**	**A3P250**	**A3P400**	**A3P600**	**A3P1000**	**A3PE600**	**A3PE1500**	**A3PE3000**
Arm® Cortex®-M1 Based Devices				**M1A3P250**	**M1A3P400**	**M1A3P600**	**M1A3P1000**		**M1A3PE1500**	**M1A3PE3000**
Equivalent LEs	330	700	1.5K	3K	5K	7K	11K	7K	16K	35K
System Gates	30,000	60,000	125,000	250,000	400,000	600,000	1,000,000	600,000	1,500,000	3,000,000
RAM Kb (1,024 bits)		18	36	36	54	108	144	108	270	504
4,608-bit Blocks		4	8	8	12	24	32	24	60	112
FlashROM Bits	1,024	1,024	1,024	1,024	1,024	1,024	1,024	1,024	1,024	1,024
Secure (AES) ISP1		Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PLLs		1	1	1	1	1	1	6	6	6
Maximum User I/Os	77	96	133	157	178	235	300	270	444	620

To learn more please visit: https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/proasic-3-fpgas

ProASIC® 3/e Packaging										
ProASIC 3/3e Devices	**A3P030**	**A3P060**	**A3P125**	**A3P250**	**A3P400**	**A3P600**	**A3P1000**	**A3PE600**	**A3PE1500**	**A3PE3000**
Arm® Cortex®-M1 Based Devices				**M1A3P250**	**M1A3P400**	**M1A3P600**	**M1A3P1000**		**M1A3PE1500**	**M1A3PE3000**
Commercial and Industrial	**Single-Ended I/Os/Differential I/O Pairs**									
QNG48 (6 × 6 mm, 0.4 mm)	34									
QNG68 (8 × 8 mm, 0.4 mm)	49									
VQG100 (14 × 14 mm, 0.5 mm)	77	71	71	68/13						
TQG144 (20 × 20 mm, 0.5 mm)		91	100							
PQG208 (28 × 28 mm, 0.5 mm)			133	151/34	151/34	154/35	154/35		147/65	147/65
FG(G)144 (13 × 13 mm, 1.0 mm)		96	97	97/24	97/25	97/25	97/25			
FG(G)256 (17 × 17 mm, 1.0 mm)				157/382	178/38	177/43	177/44		165/79	
FG(G)484 (23 × 23 mm, 1.0 mm)						235/60	300/74	270/135	280/139	341/168
FG(G)324 (19 × 19 mm, 1.0 mm)										221/110
FG(G)676 (27 × 27 mm, 1.0 mm)									444/222	
FG(G)896 (31 × 31 mm, 1.0 mm)										620/310
Military	**Single-Ended I/Os/Differential I/O Pairs**									
VQ(G)100 (14 × 14 mm, 0.5 mm)				68/13						
PQG208 (28 × 28 mm, 0.5 mm)						154/35	154/35			
FG(G)144 (13 × 13 mm, 1.0 mm)				97/24			97/25			
FG(G)256 (17 × 17 mm, 1.0 mm)							177/44			
FG(G)484 (23 × 23 mm, 1.0 mm)							300/74			
Automotive 'T'	**Single-Ended I/Os/Differential I/O Pairs**									
VQG100 (14 × 14 mm, 0.5 mm)		71	71	68/13						
FG(G)144 (13 × 13 mm, 1.0 mm)		96	97	97/24			97/25			
FG(G)256 (17 × 17 mm, 1.0 mm)				157/382			177/44			
FG(G)484 (23 × 23 mm, 1.0 mm)							300/74			

ProASIC3 Family: ProASIC3 nano FPGAs

Low-Density CPLD Replacement with Small Package Footprint

Our innovative ProASIC3 nano devices bring a new level of value and flexibility to high-volume markets. When measured against the typical project metrics of performance, cost, flexibility and time-to-market, ProASIC3 nano devices provide an attractive alternative to ASICs and ASSPs in fast-moving or highly competitive markets. Customer-driven total-system cost reduction was a key design criteria for the ProASIC3 nano program. Single-chip implementation and a broad selection of small footprint packages contribute to lower total system costs.

- 1.5V core for low power
- 350 MHz system performance
- Configuration memory error immune
- Enhanced commercial temperature
- Enhanced I/O features
- ISP and security
- In-System Programming (ISP) and security
- Hot-swappable and cold-sparing I/Os

ProASIC®3 nano Product Table					
ProASIC 3 nano Devices	**A3PN010**	**A3PN020**	**A3PN060**	**A3PN125**	**A3PN250**
Equivalent LEs	100	200	700	1.5 K	3K
System Gates	10,000	20,000	60,000	125,000	250,000
RAM Kb (1,024 bits)			18	36	36
4,608-bit Blocks			4	8	8
FlashROM Bits	1,024	1,024	1,024	1,024	1,024
Secure (AES) ISP			Yes	Yes	Yes
Integrated PLLs in CCCs			1	1	1
Maximum User I/Os	34	49	71	71	68
ProASIC 3 nano Packaging					
Features	**A3PN010**	**A3PN020**	**A3PN060**	**A3PN125**	**A3PN250**
Commercial and Industrial	**Single-Ended I/O**				
QNG48 (6 × 6 mm, 0.4 mm)	34				
QNG68 (8 × 8 mm, 0.4 mm)		49			
VQ(G)100 (14 × 14 mm, 0.5 mm)			71	71	68

To learn more please visit: https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/proasic-3-fpgas

ProASIC3 Family: ProASIC3L FPGAs

Low-Density, Low-Power CPLD Replacement FPGA

ProASIC3L FPGAs feature lower dynamic and static power requirements than the previous generation of ProASIC3 FPGAs and requirements by orders of magnitude than SRAM competitors, combining dramatically reduced power consumption with up to 350 MHz operation. The ProASIC3L family also supports the free implementation of an FPGA-optimized 32-bit Arm Cortex-M1 processor, enabling you to select the Microchip Flash FPGA solution that best meets your speed and power requirements, regardless of application or volume. Optimized software tools using Power-Driven Layout (PDL) provide instant power-reduction capabilities.

- Low-power 1.2V to 1.5V core operation
- 700 Mbps DDR, LVDS capable I/Os
- Up to 350 MHz system performance
- Configuration memory error immune
- ISP and security
- Flash*Freeze technology for low power
- Available in military temperature grade

ProASIC®3L Product Table				
ProASIC 3L Devices	**A3P600L**	**A3P1000L**	**A3PE600L**	**A3PE3000L**
Arm® Cortex®-M1 Based Devices	M1A3P600L	M1A3P1000L		M1A3PE3000L
Equivalent LEs	7K	11K	7K	35K
System Gates	600,000	1,000,000	600,000	3,000,000
RAM Kb (1,024 bits)	108	144	108	504
4,608-bit Blocks	24	32	24	112
FlashROM Bits	1,024	1,024	1,024	1,024
Secure (AES) ISP1	Yes	Yes	Yes	Yes
Integrated PLLs in CCCs2	1	1	6	6
Maximum User I/Os	235	177	270	620
Typical Static/Flash*Freeze Power (mW) at VCC = 1.2V	0.66	1.06	TBA	3.3
ProASIC 3L Packaging				
Commercial and Industrial	**Single-Ended I/Os/Differential I/O Pairs**			
PQG208 (28 × 28 mm, 0.5 mm)				147/653
FG(G)144 (13 × 13 mm, 1.0 mm)	97/25	97/25		
FG(G)256 (17 × 17 mm, 1.0 mm)		177/44		
FG(G)324 (19 × 19 mm, 1.0 mm)				221/110
FG(G)484 (23 × 23 mm, 1.0mm)	235/60		270/135	341/168
FG(G)896 (31 × 31 mm, 1.0 mm)				620/310
Military	**Single-Ended I/Os/Differential I/O Pairs**			
FG(G)484 (23 × 23 mm, 1.0 mm)			270/135	341/168
FG(G)896 (31 × 31 mm, 1.0 mm)				620/310

To learn more please visit: https://www.microchip.com/en-us/products/fpgas-and-plds/fpgas/proasic-3-fpgas

SmartFusion SoC FPGAs

Low-Cost FPGA With Integrated Arm Cortex-M3 Processor

SmartFusion SoCs integrate an FPGA fabric, an Arm Cortex-M3 processor, and a programmable Analog Compute Engine (ACE), offering full customization, IP protection and ease-of-use. Based on Microchip's proprietary Flash process, SmartFusion SoCs are ideal for hardware and embedded designers who need a true system-on-chip that gives more flexibility than traditional fixed-function microcontrollers without the excessive cost of soft processor cores on traditional FPGAs.

- Available in commercial, industrial and military grades
- Hard 100 MHz 32-bit Arm Cortex-M3 CPU
- Multi-layer AHB communications matrix with up to 16 Gbps throughput
- 10/100 Ethernet MAC
- Two peripherals of each type: SPI, I^2C, UART and 32-bit timers
- Up to 512 KB Flash and 64 KB SRAM
- External Memory Controller (EMC)
- 8-channel DMA controller
- Integrated Analog-to-Digital converters (ADCs) and Digital-to-Analog converters (DACs) with 1% accuracy
- On-chip voltage, current and temperature monitors
- Up to ten 15 ns high-speed comparators
- Analog Compute Engine (ACE) offloads CPU from analog processing
- Up to 35 analog I/Os and 169 digital GPIOs

SmartFusion® Product Table								
FPGA Fabric	A2F200				A2F500			
	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
Equivalent LEs	2K				6K			
System Gates	200,000				500,000			
Tiles (D-Flip-Flops)	4,608				11,520			
RAM Blocks (4,608 bits)	8				24			
Flash (Kbytes)	256				512			
SRAM (Kbytes)	64				64			
Arm® Cortex®-M3 Processor with MPU	Yes				Yes			
10/100 Ethernet MAC	Yes				Yes			
External Memory Controller (EMC)	26- bit address/16- bit data				—	26- bit address/16- bit data		
DMA	8 Ch				8 Ch			
I²C	2				2			
SPI	1	2			1	2		
16550 UART	2				2			
32-Bit Timer	2				2			
PLL	1				1	2	1	2
32 KHz Low-Power Oscillator	1				1			
100 MHz On-Chip RC Oscillator	1				1			
Main Oscillator (32 kHz to 20 MHz)	1				1			
Programmable Analog	PQ208	CS288	FG256	FG484	PQ208	CS288	FG256	FG484
ADCs (8-/10-/12-bit SAR)	2				2			3
DACs (8-/16-/24-bit sigma-delta)	2				2			3
Signal Conditioning Blocks (SCBs)	4				4			5
Comparators	8				8			10
Current Monitors	4				4			5
Temperature Monitors	4				4			5
Bipolar High Voltage Monitors	8				8			10

SmartFusion® Packaging										
Features	**A2F200**					**A2F500**				
Commercial and Industrial	**Total Analog Inputs**	**Total Analog Outputs**	**MSS I/Os**	**FPGA I/Os**	**Total I/Os**	**Total Analog Inputs**	**Total Analog Outputs**	**MSS I/Os**	**FPGA I/Os**	**Total I/Os**
PQ208 (28 × 28 mm, 0.5 mm)	24	1	22	66	113	24	1	22	66	113
CS(G)288 (11 × 11 mm ,0.5 mm)	24	2	31	78	135	24	2	31	78	135
FG(G)256 (17 × 17 mm, 1.0 mm)	24	2	25	66	117	24	2	25	66	117
FG(G)484 (23 × 23 mm, 1.0 mm)	24	2	41	94	161	32	3	41	128	204
Military						**Total Analog Inputs**	**Total Analog Outputs**	**MSS I/Os**	**FPGA I/Os**	**Total I/Os**
FG(G)256 (17 × 17 mm, 1.0 mm)						24	2	25	66	117
FG(G)484 (23 × 23 mm, 1.0 mm)						32	3	41	128	204

To learn more please visit: https://www.microchip.com/en-us/products/fpgas-and-plds/system-on-chip-fpgas/smartfusion-fpgas

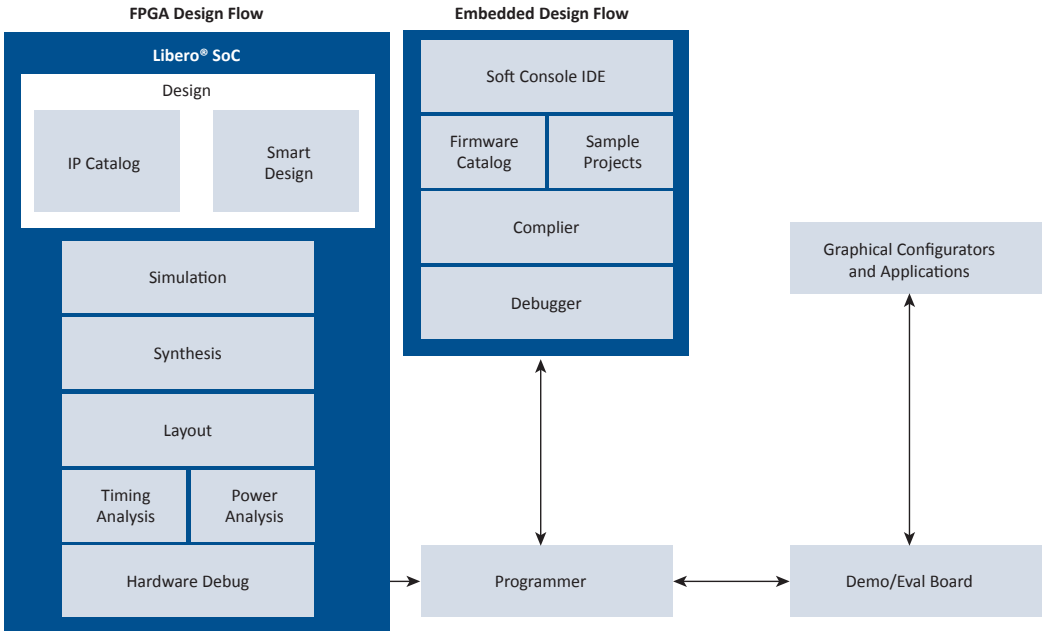
Ecosystem for FPGAs and SoC FPGAs

Libero® SoC Design Suite

Microchip's Libero SoC design suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools for designing on behalf of I30402.

Libero SoC Design Suite provides integrated hardware tool suite incorporating RTL entry through programming and debug, a rich IP library and complete reference designs. Benefit from:

1. Best-in-class power, performance and area optimizations
2. Easy block-based system design
3. Fast RTL debug and integrated logic analyzer
4. Rich library of IPs and integrated blocks
5. Integrated structural, behavioral and back-annotated design simulation
6. Secure Production Programming Solution (SPPS) to prevent overbuilding and cloning .



SmartDebug

The SmartDebug tool is used to debug the FPGAs fabric and SERDES without using an Integrated Logic Analyzer (ILA). SmartDebug utilizes the dedicated and specialized probe points built into the FPGA fabric, which significantly accelerates and simplifies the debug process. It also provides the ability to change probe points on the fly without recompiling and reprogramming the FPGA that saves significant debug time. additional overhead and saves significant recompile time. SmartDebug supports PolarFire SoC, PolarFire, IGLOO2, SmartFusion2, RTG4 FPGA families only.

License Types				
Features	**Silver**	**Gold**	**Platinum**	**Platinum Archival**
Validity Period	One Year	1/3 Years	1/3 Years	20 Years (No Upgrades)
Device Support	https://ww1.microchip.com/downloads/aemDocuments/documents/FPGA/core-docs/fp/Libero_License_Selector_Guide_v24.xls			
DirectCores	Refer to DirectCores IP Web Page			
Siemens ModelSim/QuestaSim ME	Mixed Language			
Synopsys Synplify Pro® ME	X	X	X	X
Programming	X	X	X	X
Synopsys Identify ME	X	X	X	X

SmartHLS Compiler Software

SmartHLS enables faster design and easier Verification of software accelerators. It raises the FPGA design abstraction from traditional hardware description languages to C/C++ software, enabling shorter design time, easier verification and faster time to market for designs using Microchip FPGAs.

Intellectual Property

Microchip enhances your design productivity by providing an extensive suite of proven and optimized IP Cores for use with FPGAs and SoC FPGA that covers key markets and applications. IPs are organized as either Microchip-developed DirectCoresTM or third party-developed CompanionCores™.

Libero SoC Design suite provides access to all the Microchip's in-house (DirectCores) IP Cores covering a broad range of functionality. Most of the DirectCores are available for free with any Libero license. Some of the high valued IP cores like 10GMAC, QSGMII, 10GBASEKR_PHY, XAUI, TSE, 429, 1553BRT, 1553BRM, etc needs to be purchased separately.

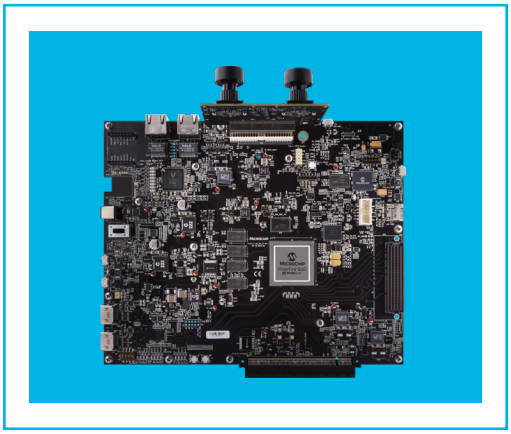
The CompanionCores are supplement to our extensive suite of DirectCore IP cores. Our CompanioCores are paid cores and our partners will provide the commercial and technical support for these cores.

IPs available with Libero

Visit FPGA IP Search page to identify required IP Cores using keyword, Product Family, Vendor Type and Application filters.

Development Kits

PolarFire SoC Video Kit

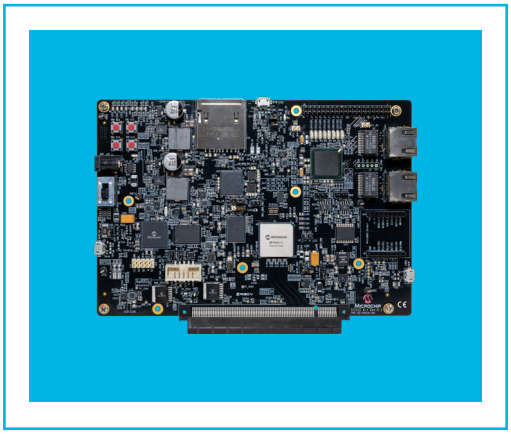


Part No: MPFS250-VIDEO-KIT

This kit is a full-featured embedded vision development platform targeting secure, reliable, and power-efficient vision applications at the edge.

- PolarFire SoC FPGA (MPFS250TS-1FCG1152I), SiFive E51 Monitor core (1 x RV64IMAC) , SiFive U54 Application cores (4 x RV64GC), and Secure boot
- Sony 4K Dual Camera Sensors (IMX334), Onboard JTAG & embedded FlashPro
- 4 GB DDR4 x64, 2GB LPDDR4 x32, 1Gb SPI Flash, 8 GB eMMC Flash and 16 GB SD card slot (multiplexed)
- HPC FMC, PCIe Gen 2 ×4, a Mikrobus socket
- UART (via USB Bridge), CAN-FD Header, GbE RJ-45 Connectors, microUSB High speed USB 2.0 OTG, I2C (via USB bridge)
- HDMI2.0 Video Input/Output, MIPI DSI Output, MIPI CSI-2 Input

PolarFire SoC Icicle Kit

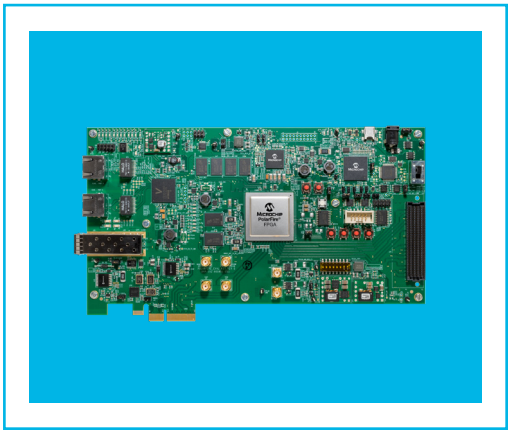


Part No: MPFS-ICICLE-KIT-ES

The PolarFire SoC Icicle kit is a low-cost development platform that enables evaluation of the five-core Linux capable RISC-V microprocessor subsystem and more.

- PolarFire SoC (MPFS250T-FCVG484EES) with 1× RV64IMAC core and 4× RV64GC cores by SiFive, 4× 12.7 Gbps SERDES ad Secure boot
- 2 GB LPDDR4 × 32, 1 Gb SPI Flash, 8 GB eMMC Flash or SD card slot, 2× Gigabit Ethernet
- mikroBUS socket, UART via micro USB, Onboard JTAG connector or embedded FlashPro6 (multiplexed)
- PCIe Gen 2, Micro USB 2.0 Hi-Speed OTG, 4× UART (via single micro USB)

PolarFire Evaluation Kit



Part No: MPF300-EVAL-KIT

This kit is ideal for high-speed transceiver evaluation, 10 Gb Ethernet, IEEE 1588, JESD2048, SyncE, CPRI and more.

- 300K LE PolarFire FPGA in an FCG1152 Package (MPF300TS-1FCG1152I)
- 4 GB 32-bit DDR4, 2GB 16-bit DDR3 and 1Gb SPI Flash Memory
- 2× RJ45 ports with PHY, 4× FMC connector

PolarFire Splash Kit

Part No: MPF300-SPLASH-KIT

The PolarFire Splash Kit provides general-purpose interfaces for evaluation and development. It comes with 300K LE PolarFire FPGA in a FCG484 Package (MPF300T-1FCG484E)

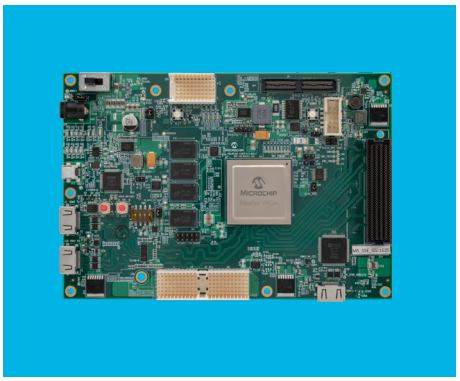
- ×32 bit DDR4 and 1 Gb SPI Flash Memory
- RJ45 port with PHY, FMC connector
- PCI express (×4) edge connector

PolarFire Video Kit

Part No: MPF300-VIDEO-KIT-NS

This Kit offers a high-performance evaluation of 4K image processing. It comes with 300K LE PolarFire FPGA in an FCG1152 Package

- Sony Dual Camera Sensor (IMX334) over Amphenol FCI connector
- 4GB DDR4 ×32, 1× 1Gb SPI Flash Memory
- HDMI 2.0 RX and TX , HDMI 1.4 TX
- DSI Connector, CSI-2 TX Connector, HPC FMC Connector

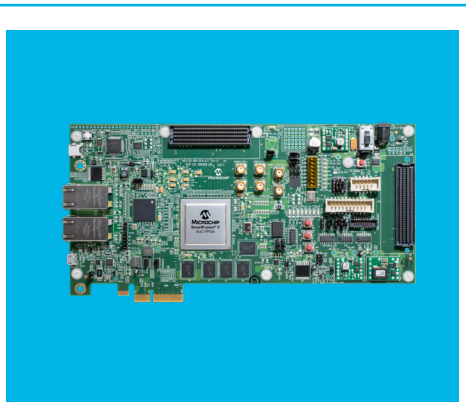


SmartFusion2 Advanced Development Kit

Part No.: M2S150-ADV-DEV-KIT

This Kit supports numerous standards and interfaces for motor control, industrial automation, high-speed I/O and security applications. It comes with 150K LE SmartFusion2 device

- DDR3 SDRAM, SPI Flash, FTDI programmer interface
- SMA connectors, two FMC connectors, PCIe x4 edge connector
- 2xRJ45 interface for 10/100/1000 Ethernet, USB micro-AB connector



SmartFusion2 Security Evaluation Kit

Part No.: M2S090TS-EVAL-KIT

This Kit evaluates the data security features of SmartFusion2 SoC 90K LE SmartFusion2 device

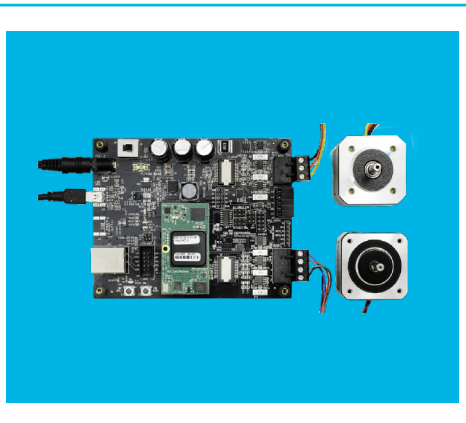
- 64 Mbit SPI Flash memory, 512 MB LPDDR
- PCI Express Gen2 ×1 ,RJ45 interface, JTAG/SPI programming interface
- Four SMA connector, Headers for I2C, SPI, GPIOs

IGLOO2 Evaluation Kit

Part No.: M2GL-EVAL-KIT

This kit comes preloaded with a PCIe control plane demo IGLOO2 FPGA in the FGG484 package (M2GL010T-1FGG484)

- JTAG/SPI programming interface, Gigabit Ethernet PHY and RJ45 connector
- USB 2.0 OTG interface connector, Gen2×1 PCIe edge connector
- 1 GB LPDDR, 64 MB SPI Flash, Headers for I^2C, UART, SPI, GPIOs



SmartFusion2 Dual-axis Motor Control Starter Kit

Part No.: SF2-MC-STARTER-KIT

This Multi-axis deterministic motor control on a single system-on-chip (SoC) FPGA is efficient, reliable, and safe drive with product longevity.

- Motor performance is tested for speeds exceeding 100,000 RPM for sensorless field oriented control (FOC).
- The low latency of 1s for FOC loop from ADC measurement to PWM generation allows switching frequencies up to 500 kHz.
- A compact solution which provides Design flexibility with modular IP suite

Say Hello to FPGAs

Part No.: M2S-HELLO-FPGA-KIT

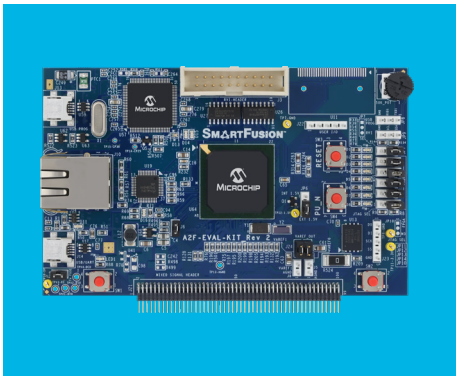
- Artificial Intelligence demo: Uses Parallel Processing to do real-time hand-written digit recognition
- Digital Signal Processing demo: Creating FIR/FFT filters
- Power monitor GUI: Shows how fast the instant-on wake-up time is while displaying the power consumption for both operational and Flash*Freeze modes

IGLOO nano Starter Kit

Part No.: AGLN-NANO-KIT

This kit provides a simple low-cost board with IGLOO nano AGLN250 device in the VQG100 package

- USB-to-UART connection for HyperTerminal on a PC
- Eight LEDs and four switches
- Ability to switch VCORE from 1.2 V to 1.5 V



Cortex-M1-enabled ProASIC3L Development Kit

Part No.: M1A3PL-DEV-KIT

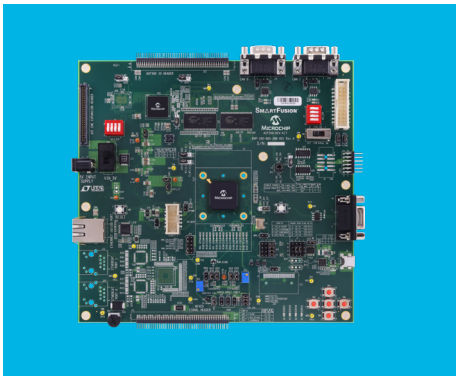
- This Kit comes with a ProASIC3L M1A3P1000L-FGG484 device
- Eight LEDs and eight switches
- Additional USB connection for USB-to-serial (RS232) interface
- 4 MB of SRAM, 16 MB of Flash memory and three 40-pin GPIO banks

SmartFusion Evaluation Kit

Part No.: A2F-EVAL-KIT-2

This Kit offers a simple, low-cost way to use FPGA with hard Arm Cortex-M3 and programmable analog.

- SPI-flash memory, RVI header, Mixed-signal header
- USB to UART connection to UART_0 for HyperTerminal examples
- 10/100 Ethernet interface with on-chip MAC and external PHY



SmartFusion Development Kit

Part No.: A2F500-DEV-KIT-2

This Kit offers a full-featured development board with hard Arm Cortex-M3 and programmable analog.

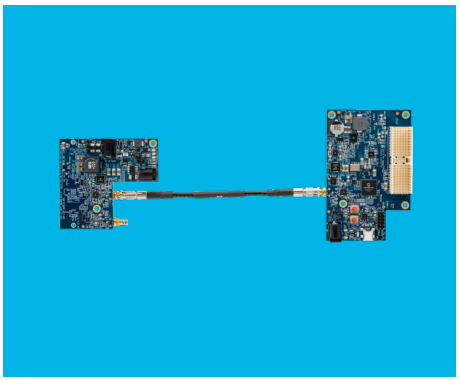
- On-chip flash, SRAM memory and PSRAM
- RVI header, Mixed-signal header, I^2C headers, SPI headers, DirectC header
- DB9 connector, RJ45 connector, IGLOO PLUS expansion header

Cortex-M1-enabled IGLOO Development Kit

Part No.: M1AGL1000-DEV-KIT

This Kit comes with M1AGL1000V2 device in FGG484 package & has a million system gates

- Eight LEDs and eight switches
- Additional USB connection for USB-to-serial (RS232) interface
- 4 MB of SRAM, 16 MB of Flash memory and three 40-pin GPIO banks
- Programmer built into board via USB 2.0 connection



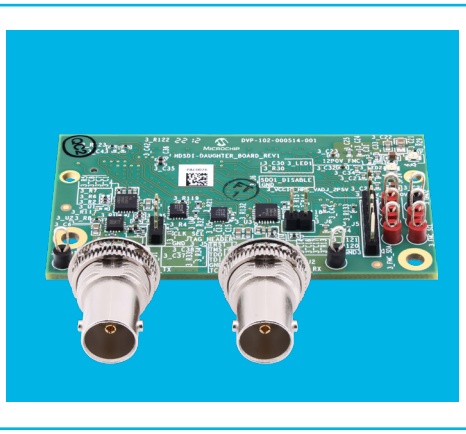
FMC Cards

CoaXPress FMC Daughter Card

Part No.: VIDEO-DC-CXP

The CoaXPress boards support a 12.5G CoaXPress PHY and include ready to use reference designs for quick prototyping. It is the hardware evaluation platform for evaluating and testing the CoaXPress protocol.

- 100k LE PolarFire device in FCSG325 package
- 12.5g CoaXPress PHY, JTAG – programming (FP4)
- Amphenol FCI connector, 1 Micro BNC Connectors –TX

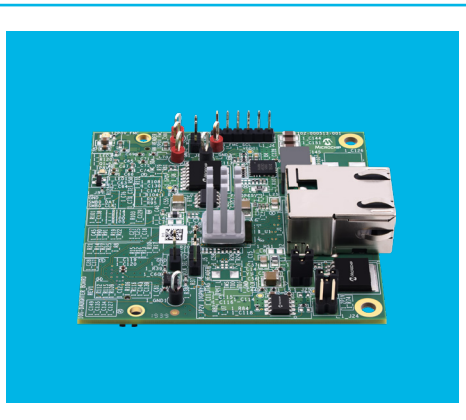


SDI FMC Daughter Card

Part No.: VIDEO-DC-SDI

This SDI FMC daughter card is the hardware evaluation platform for evaluating and testing the Serial Digital interface IP.

- HD/3G/6G SDI support
- Onboard 148.5MHz Oscillator
- Equalizer on RX path, Driver and Re-clocker on TX path



USXGMII FMC Daughter Card

Part No.: VIDEO-DC- USXGMII

- This USXGMII FMC daughter card is the hardware evaluation platform for evaluating and testing the quadrate PHY IP.
- Quadrate PHY (10 Gbps/5 Gbps/2.5 Gbps/1 Gbps/100 Mbps)
- RJ45 connector

Programmers

FLASHPRO6

Part No.: FLASHPRO6

FlashPro6 is the newest programmer, which along with Windows, supports Linux platforms, in conjunction with LiberoSoC, FlashPro Express, and SmartDebug software.

- It supports FPGA devices in PolarFire, PolarFire SoC, SmartFusion2, IGLOO2 and RTG4 series.
- Supports in-system programming, USB 2.0/3.0, SPI-Slave Programming
- Supports IEEE 1149 JTAG programming through STAPL

FLASHPRO5

Part No.: FLASHPRO5

FlashPro5 along with Windows, also supports Linux platforms also such as RedHat Enterprise Linux 6 and CentOS 6, in conjunction with FlashPro Express software.

- It supports all FPGA devices in PolarFire, PolarFire SoC, SmartFusion2, IGLOO2, RTG4, SmartFusion, Fusion, IGLOO, ProASIC3 and RT ProASIC3 series
- Supports in-system programming, USB 2.0, SPI-Slave Programming for SmartFusion2, IGLOO2 devices
- Supports IEEE 1149 JTAG programming through STAPL

FLASHPRO4

Part No.: FLASHPRO4

FlashPro4 is a programmer supporting all FPGAs in the PolarFire, SmartFusion2, IGLOO2, RTG4, IGLOO, ProASIC3, (including RT ProASIC3), SmartFusion and Fusion families.

- Supports in-system programming
- Supports IEEE 1149 JTAG programming through STAPL
- Supports USB 2.0

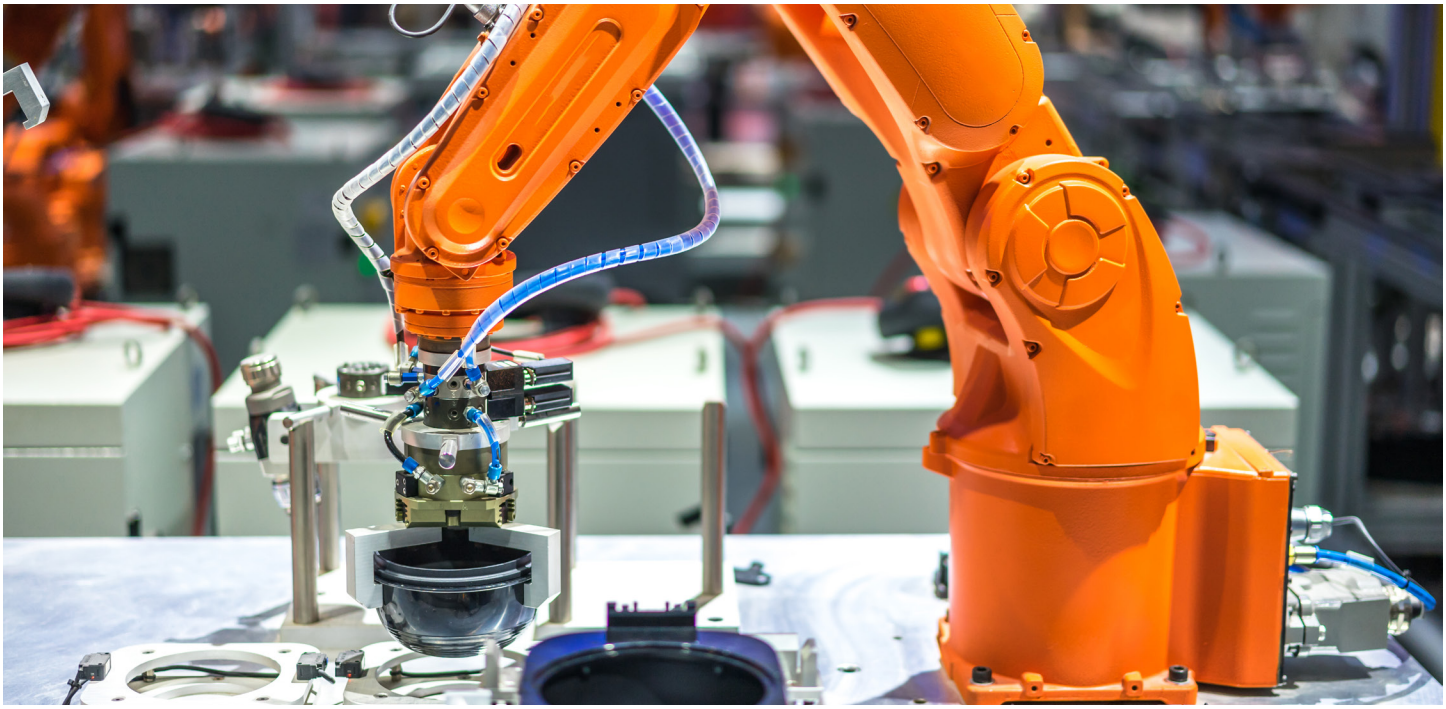
SILICON-SCULPTOR 4

Part No.: SILICON-SCULPTOR_4

Silicon Sculptor 4 offers increased memory size and fast data processing. With 2 GB of internal memory, it allows concurrent programming of large parts without performance degradation.

- Works with all Silicon Sculptor Adapter Module and allows self-test
- STAPL support for supported devices, ESD protection
- Overcurrent shutdown, Power failure shutdown

For more information on Kits, please visit: https://www.microchip.com/en-us/products/fpgas-and-plds/boards-and-kits



Highly Differentiated Features

Secured Production Programming Solution (SPPS) Prevents Overbuilding and Cloning

SPPS enables secured production programing of FPGAs and SoCs by generating and injecting cryptographic keys and configuration bitstreams. This enables prevention of cloning, reverse engineering, malware insertion, leakage of sensitive IP, overbuilding, and other security threats. It is an ideal solution to eliminate the risk of overbuilding customer's systems. It builds upon existing Hardware Security Modules (HSMs), custom firmware and the state-of-the-art security protocols, built into PolarFire FPGA, PolarFire SoC FPGA, SmartFusion SoC FPGA and IGLOO 2 FPGA families, to automatically prevent overbuilding.

- Supports multiple programming file formats
- Single- and chain-programming support using SPI and JTAG programming modes
- Auto-update and programming recovery modes
- Interfaces software and hardware security modules
- Allows initial key loading in unstructured environment
- Leverages underlying PolarFire, PolarFire SoC, SmartFusion SoC and IGLOO 2 security protocols
- Validates devices that can be programmed
- Controls the exact number of devices to be programmed

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