# Investigation of TID and Dynamic Burn-In-Induced $V_T$ Shift on RTG4 Flash-Based FPGA

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***Abstract*— RTG4 total ionizing dose (TID) tolerance is investigated postdynamic burn-in (DBI). A $V_T$ shift of the programmed Pflash cell is observed post-DBI and is due to programming voltage degradation resulting from the DAC aging. TID testing performed post-DBI shows DBI has minimum impact on RTG4 C-flash TID tolerance since it is dominated by Nflash $V_T$ shift. The programmed Pflash $V_T$ shift is the dominant effect post-DBI, whereas the erased Nflash $V_T$ shift is the dominant effect post-TID.**

***Index Terms*— Burn in (BI), field programmable gate array (FPGA), flash, total ionizing dose (TID).**

## I. Introduction

FOR space applications, dynamic burn-in (DBI) testing is used to evaluate the long term reliability (LTR) [1]–[3], of the device. Among all product screening tests employed by a large number of business categories, including automotive, aerospace, and defense, burn in (BI) test is one of the most effective tests for early failure detection. Production testing of space-flight field programmable gate array (FPGA) is a complicated matter. "Flight" units—those are shipped for integration into spacecraft—are subjected to temperature cycling and voltage stress prior to electrical testing. For space application, it appears logical to evaluate the LTR and total ionizing dose (TID) effects on the same device under test (DUT). In the literature, data is lacking, if not completely nonexistent, on what impact DBI would have on the TID response of flash cells (memories). Since the reliability of flash-based FPGAs is dominated by its flash cells, this topic is also critical to flash cell memories.

For the worst case evaluation, DBI should be performed before TID because the temperature during BI will anneal out, at least partially, some TID effects. In this paper, for the first time, the impact of DBI on the TID effects of flash cells in flash-based FPGA is investigated.

The focus is on the degradation of the flash cell through its threshold-voltage ($V_T$) shift. Microsemi is a qualified manufacturers list (QML)-certified manufacturer of high-reliability FPGAs for space applications. RTG4, Microsemi's fourth generation radiation tolerant flash-based FPGAs, manufactured in 65-nm technology uses a robust screening flow (which includes DBI) to verify that the devices are fit for deployment in space-based applications. RTG4 uses a novel complementary-flash (Cflash) cell which is composed of a Pflash and Nflash cell connected in series, and an nMOS switch controlled by the flash's output [4]–[6]. The switch has a significantly higher TID tolerance than flash cells, thus its radiation response can be ignored. DBI and TID are two different processes that may cause different $V_T$ shift in Pflash and Nflash within a C-flash cell. However, since all degradations are due to $V_T$ shift to the neutral state, if both DBI and TID favor the Nflash $V_T$ shift or both favor the Pflash $V_T$ shift, the effects of these two processes can be added and DBI will significantly degrade the device's TID tolerance.

In this paper, the TID tolerance of RTG4 devices post-DBI for different screening flows is compared with control RTG4 devices. Devices that went through 160, 240, and 4600 h of DBI are irradiated up to 125 krad($SiO_2$) and functionality of the parts is monitored. In addition to the functionality, $V_T$ distribution of the Nflash and Pflash cells is measured to understand the impact of DBI on the TID response of the device. Section II-A describes the BI design and BI test condition. Section II-B describes different screening flows used to screen and qualify RTG4 devices. In Section III-A, the BI results and its impact on the programmed Pflash cell are presented. Finally, in Section III-B, the TID results are presented.

## II. Experimental Procedure

DBI testing of the RT4G150 devices is performed at Microsemi in San Jose, CA, USA. Units from the "B flow" and "E/V flow" are tested. Details on different screening flows and corresponding BI hours are described in Section II-B. TID testing is performed at the defense microelectronics activity in McClellan, CA, USA. The FPGAs are irradiated at room temperature with a cobalt-60 gamma ray at a dose rate of 5 krad($SiO_2$)/min to a maximum dose of 125 krad($SiO_2$). The FPGA is biased during irradiation and to minimize annealing, measurements are performed within 5 min following radiation. An inverter chain design with 6000 stages is programmed into the FPGA for TID evaluation. The electrical parameters measured in this test are functionality, the propagation delay,

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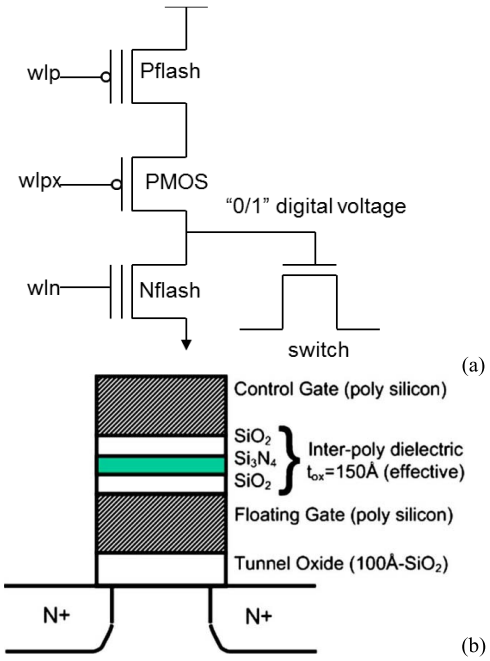


Fig. 1. (a) C-flash bit cell. (b) Gate-stack of the flash cell.

and power supply current. The propagation delay is the delta between the rising edges of both the input and output signals of the inverter chain and are measured *in situ* during irradiation. A square waveform input signal with a frequency of 1 kHz and 50% duty cycle is supplied from a function generator while the electrical parameters of the input–output signals are observed and recorded on the oscilloscope. Device failure is observed when the output signal can no longer be measured. For each FPGA the functionality and propagation delay are monitored, additionally the operation of "margin" is performed.

### *A. C-Flash Configuration Bit Cell and Margin Operation*

The operation of "margin" consists of measuring the threshold voltage ($V_T$) of each C-flash bit cell within the FPGA. The results are displayed using a $V_T$ histogram or distribution; the $V_T$ of each cell (both Nflash and Pflash) is measured and displayed in the histogram. Each FPGA DUT has millions of C-flash configuration bit cells and their $V_T$ distribution is measured for every DUT. The C-flash bit cell shown in Fig. 1 is composed of a Nflash and Pflash cell in a structure similar to a CMOS structure, in addition a pMOS device is introduced to mitigate a reliability issue, refer to [5] for details. Therefore since the C-flash is composed of both Nflash and Pflash, margin is performed on both cells in programmed and erased states simultaneously. The flash's output controls an nMOS switch, configured to ON ("1") or OFF ("0"). When the switch is OFF, the Nflash is erased (Nflash0 state) and the Pflash is programmed (Pflash0 state). Similarly when the switch is ON, the Nflash is programmed (Nflash1 state) and the Pflash is erased (Pflash1 state).

Because of the C-flash configuration, the FPGA TID tolerance is improved above 100 krad($SiO_2$), compared to the commercial 65-nm flash-based FPGA and SmartFusion2 [7]. This is due to the switch in the C-flash being decoupled from the flash cell. The switch performance does not degrade even when the individual Nflash and Pflash degrade significantly.

### *B. Burn-In Design*

A burn-in test is a method by which temperature and voltage loads are applied to devices aiming at reduction of initial failures by timely detection [1]–[3]. Carried out by operating the device under high temperature, dynamic BI is a screening simulating application conditions close to real use. It is also expected to help understand characteristic variations beforehand as commercial product failure recently comes up more frequently. The primary purpose of the BI design is to facilitate qualification and reliability experiments such as high-temperature operating lifetime or early life failure rate at junction temperature ($T_j$) ~125 °C, low-temperature operation lifetime at $T_j$ ~−55 °C, and biased highly accelerated stress testing. It will also be used to facilitate both dynamic and static BI as part of the production B/V flows.

The goals of the BI design are based on MIL-STD-883J Method 1016.2 to achieve high utilization of the fabric clusters and fabric IP blocks, high net toggle coverage in order to screen fabrication infant mortality defects, as well as dynamically exercise the RAM blocks during BI and enable propagation delay measurement through fabric ring oscillators. The BI also meets and exceeds recommended datasheet junction temperature. The BI design is divided into the following main blocks which can be dynamically exercised and monitored during BI:

1) fabric block;
   a) includes toggle coverage of the FPGA fabric and IP blocks;
   b) facilitates delay measurements;
2) high fan-out net utilization for increased toggle coverage;
3) long buffer chain for TID testing propagation delay analysis;
4) high-speed I/O block—toggle coverage of the serializer/deserializer IP blocks and external high-speed IO buffers.

The preferred method of design development is to utilize standard user flows through the production Libero software and Microsemi system-on-chip specific design development software tool. In some cases, engineering or manufacturing test modes are required in order to achieve BI goals.

### *C. Dynamic Burn-In*

Dynamic BI is a high-temperature operating life test at $T_j >$ 125 °C with a target $T_j = 135$ °C. The purpose of dynamic BI is to precipitate infant mortality defects, where the device is biased in the BI programmed state at maximum operating voltage per data sheet specification [8]. An external stimulus is supplied to the device in order to toggle the internal BI design nodes and real-time functional monitoring is performed on each device under test during BI.

For space-flight applications, the traditional qualification standards used are MIL-STD-883 Class-B or QML Class-V.

TABLE I
BI HOURS FOR EACH RTG4 SCREENING FLOW

| Flow | Production/Flight Units B (hrs) | E/V (hrs) | Qual Units B (hrs) |
|---|---|---|---|
| Dynamic BI | 160 | 240 | 4600 |
| Static BI | NA | 144 | NA |

TABLE II
DYNAMIC BI RESULTS POST-160 H

| Typical Bit | Shift post 160 hrs BI | BOL Limit |
|---|---|---|
| PFlash0 | -100 mV | -0.6V |
| PFlash1 | +60 mV | 2.3V |
| NFlash0 | -30 mV | 0.2V |
| NFlash1 | -10 mV | 3.3V |

Microsemi is a QML-certified manufacturer of high-reliability FPGAs for space applications. RTG4 devices use a robust screening flow to verify that the devices are fit for deployment in space-based applications. Microsemi offers three screening flows for radiation tolerant FPGAs [9]:

1) "B flow," which implements MIL-STD-883 Class-B screening and is compliant with QML Class-Q;
2) "E flow" for "extended flow" which implements additional tests beyond the requirement of MIL-STD-883 Class-B and is compliant with QML Class-Q;
3) "V flow," which is a full QML Class-V flow.

RTG4 achieved MIL-STD-883 Class-B qualification, meeting the industry's standard for qualifying microelectronic devices suitable for use within aerospace and defense electronic systems. Microsemi also announced the availability of RTG4 space flight models in various screening flows including the B flow and the extended flow (E flow), providing additional screening options and a higher level of reliability assurance required in many critical space applications. Adding Microsemi's E flow to these devices offers additional testing for space applications requiring a screening level beyond the MIL-STD-883 Class-B standard.Therefore, it is important to investigate the TID effects post-BI for different screening flows. Details of each screening flows can be found in [9].

Table I shows the various RTG4 screening flows with corresponding BI hours, including B flow and E/V flow for flight units. An internal screening is also performed as part of product qualification, where the parts go through approximately 4600 h of dynamic BI, called here "Qual" units. Generally, "Qual" units are for internal use only and are not shipped to customers; however, they are considered in this paper since they went through the highest amount of BI hours and represent the worst case units to perform TID testing on for this paper.

## III. BURN-IN AND GAMMA-RAY RESULTS

### A. Burn-In Results

The post-160-h DBI $V_T$ shift of the mean (typical) bit for both Nflash and Pflash in the programmed and erased states are summarized in Table II. The post-160-h BI results show that the programmed Pflash (Pflash0) $V_T$ loss is ~100 mV,

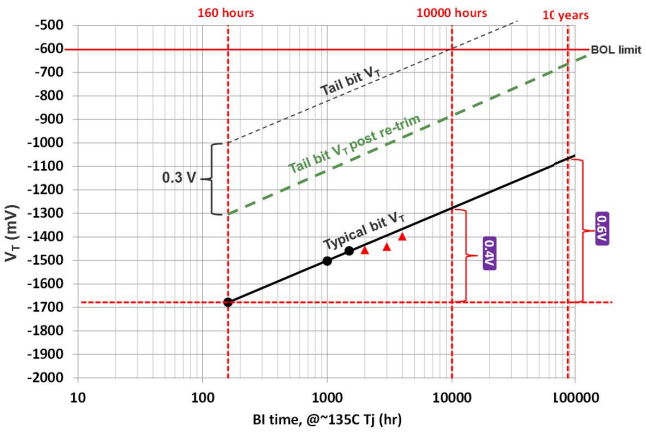


Fig. 2. Projection of Pflash0 $V_T$ with BI time (black line); The 2000-, 3000-, and 4000-h data points are represented by the triangle symbols.

both the peak and tail of the $V_T$ distribution move at similar rate. The Nflash $V_T$ loss is negligible (<100 mV) and the beginning of life (BOL) limit offers enough margin for Nflash cells in both programmed (Nflash1) and erased state (Nflash0). Pflash1 shows a $V_T$ gain of 60 mV, no $V_T$ loss is observed; therefore, the focus will be on the Pflash programmed state (Pflash0). The Pflash0 BOL limit is −0.6 V to account for the observed $V_T$ shift post-DBI and increase customer margin. A prediction model is used to verify that the BOL limit is sufficient and is shown in Fig. 2 by the black line. The 2000-, 3000-, and 4000-h data points (triangle symbols) show less degradation than the prediction. The prediction shows 0.4-V $V_T$ shift after 10 000 h and 0.6 V after ten years. However, the tail bit $V_T$ shows that we are failing the BOL limit at ten years, thus a retrimming of the programming voltage allowing to gain ~300 mV is performed and the tail bit $V_T$ post-retrimming is now passing the BOL limit at ten years as shown by the green dotted line in Fig. 2.

Although the original programming voltage parameters and BOL criteria did not adequately account for the circuit aging effect, there is no actual circuit or physical failure. In fact, the Pflash0 $V_T$ loss post-DBI has no performance or reliability impact and the samples passed the TID criteria of 100 krad($SiO_2$) as will be shown in Section III-B.

### B. Programmed Pflash $V_T$ Shift Post-DBI

The programmed Pflash (Pflash0) $V_T$ shift post-DBI is due to the programming voltage degradation, specifically due to the digital to analog converter (DAC) aging. A drop in the programming voltage will cause the observed $V_T$ shift. The programming voltage is controlled by the on-chip DAC, after BI, some of the DAC outputs reduce by 1%–1.75%. DAC drift is explained by very small changes in device matching, less than 2 mV in $V_T$ change, due to charge trapping as a result from imbalances in operating conditions during ON versus OFF bias. The pMOS transistors used in the DAC circuit, shown in Fig. 3 suffer $V_T$ shift during DBI due to the negative bias temperature instability (NBTI) mechanism [10]–[13]. NBTI is a gradual shift of threshold voltage over time and commonly observed in pMOS devices. This shift is caused by: voltage stress on the gate oxide, temperature, and the duty

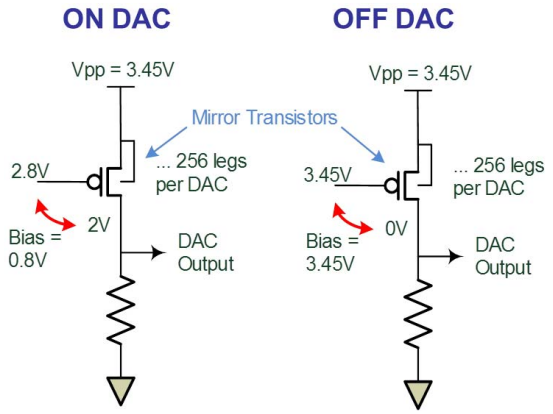


Fig. 3. Schematic of simplified current mirrors.

TABLE III
PREIRRADIATION AND POSTIRRADIATION PROPAGATION DELAY CHANGE

| Flow | DUT # | Functional | Pre-rad delay (us) | Post-rad delay (us) | Delay Change (%) |
|---|---|---|---|---|---|
| Control | 5195 | Yes | NA | NA | NA |
| B | 3773 | Yes | NA | NA | NA |
| B | 3776 | Yes | NA | NA | NA |
| E/V | 9738 | Yes | 0.461 | 0.461 | 0 |
| E/V | 9741 | Yes | 0.464 | 0.462 | -0.43 |
| E/V | 9752 | Yes | 0.460 | 0.457 | -0.65 |
| Qual | 3231 | Yes | 0.469 | 0.478 | 1.92 |
| Qual | 10427 | Yes | 0.476 | 0.464 | -1.05 |
| Qual | 3180 | Yes | 0.474 | 0.480 | 1.37 |
| Qual | 2393 | Yes | 0.468 | 0.474 | 1.28 |
| Qual | 2305 | Yes | 0.464 | 0.471 | 1.4 |

cycle of the stressing voltage (static stress as compared to dynamic stress). During DBI, the pMOS devices within the DAC are subjected to a high voltage stress on the gate oxide and temperature over a long period of time, which causes the $V_T$ shift and consequently a reduction in the output of the DAC. Each RTG4 device has 13 DACs for controlling the on-chip voltages. During BI, four DACs are ON and active and the remaining nine DACs are OFF. Only the OFF DACs show significant aging and two of the OFF DACs are used during programming the Pflash. Dissimilar bias of the primary mirror transistors causes a different aging, as shown in Fig. 3. DAC calibration checks performed before and after BI show that the nine of the thirteen programming DACs exhibit output aging, with reduced output by 1%–1.75%. Three worst cases die show DAC aging of 1.75%. At −55 °C and 75 °C, no Pflash distribution shift is evident, thus aging is only a concern at high temperatures.

### C. Gamma-Ray Results

TID testing is done on worst B flow units (post-160-h DBI) with typical bit Pflash0 $V_T \sim -1.7$ V as well as control unit (which did not go through DBI). Worst units represent units showing the largest Pflash0 $V_T$ shift post-DBI. For the control unit and B flow unit, functionality is monitored (the propagation delay is not recorded for these units) as shown in Table III. Fig. 4(a) and (b) shows a comparison of the

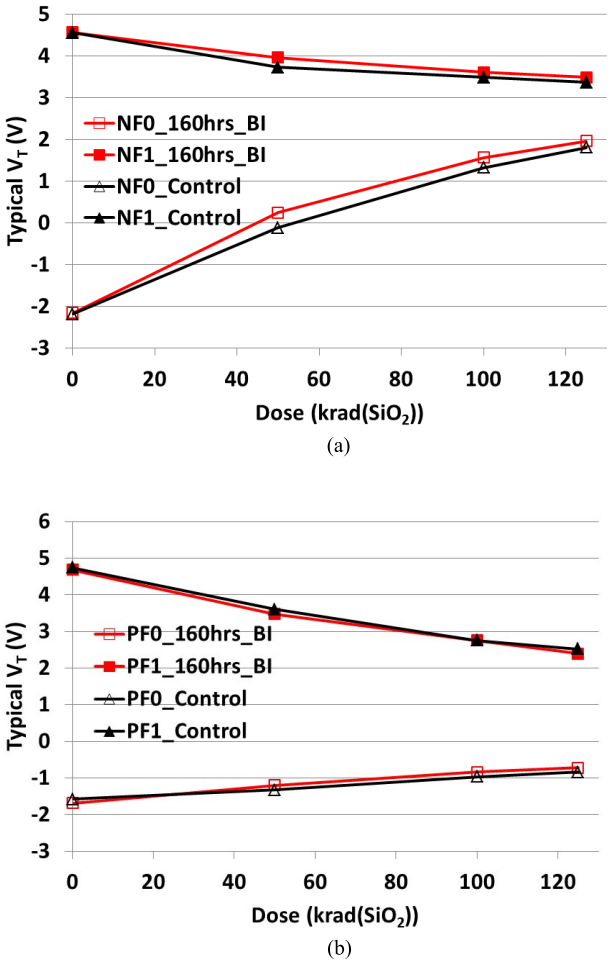


Fig. 4. (a) Comparison of the Nflash typical $V_T$ versus TID for the control unit (DUT 5195) and post-160-h DBI unit (DUT 3776). (b) Comparison of the Pflash typical $V_T$ versus TID for the control unit (DUT 5195) and post-160-h DBI unit (DUT 3776).

typical (or mean) $V_T$ of the control unit (DUT 5195) and B flow unit (DUT 3776) for both Nflash and Pflash cells, respectively. The results show small difference between the two parts and both parts are still functional after 125 krad($SiO_2$).

Three E/V flow units are tested and five "Qual" units are chosen for this test. The "Qual" units are selected based on Pflash0 $V_T$, two worst case units with $V_T$ of $\sim -1.3$ V, two average units with $V_T \sim -1.5$ V, and one best case unit with $V_T \sim -1.8$ V are tested. The results show that all parts are functional at 125 krad($SiO_2$) and show minimal propagation delay change, as shown in Table III. The negligible change in propagation delay versus TID for a "Qual" unit (DUT 3231) post-4600-h DBI is shown in Fig. 5. A maximum of approximately 2% propagation delay degradation is observed after 125 krad($SiO_2$) for all the parts tested. Therefore DBI did not degrade the TID tolerance.

To understand these results, a detailed investigation of the flash cell $V_T$ distribution is performed. The post-160- (DUT 3776) and post-4600-h (DUT 3231) DBI Nflash $V_T$ distribution versus TID for both the erased (NF0) and programmed (NF1) Nflash cells are shown in Figs. 6 and 7, respectively. The post-160- (DUT 3776) and post-4600-h (DUT 3231) DBI Pflash $V_T$ distribution versus TID for both

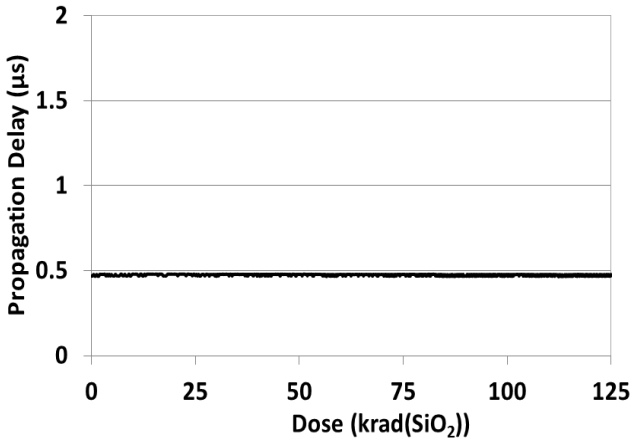


Fig. 5. Propagation delay versus TID post-4600-h DBI for DUT 3231.

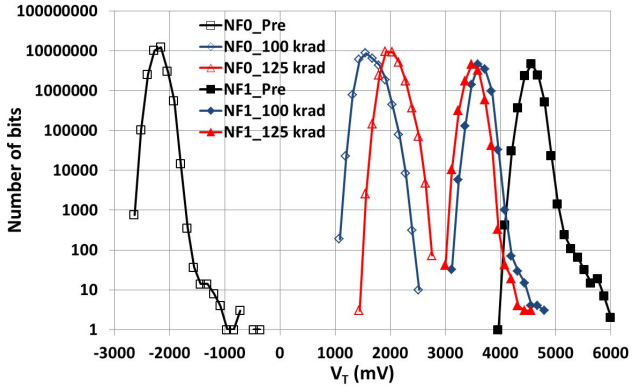


Fig. 6. Post-160-h DBI Nflash $V_T$ distributions versus TID for DUT 3776.

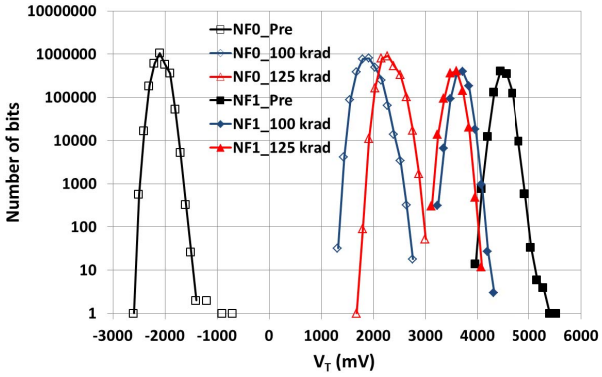


Fig. 7. Post-4600-h DBI Nflash $V_T$ distributions versus TID for DUT 3231.

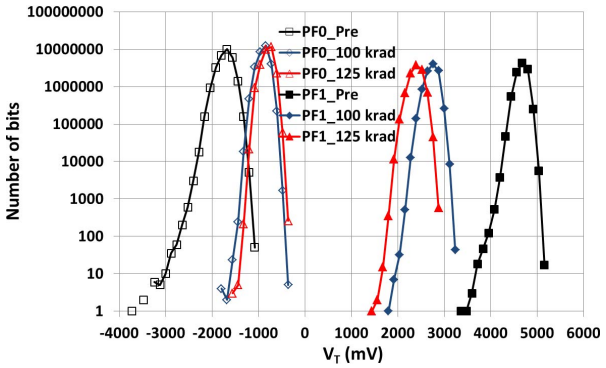


Fig. 8. Post-160-h DBI Pflash $V_T$ distributions versus TID for DUT 3776.

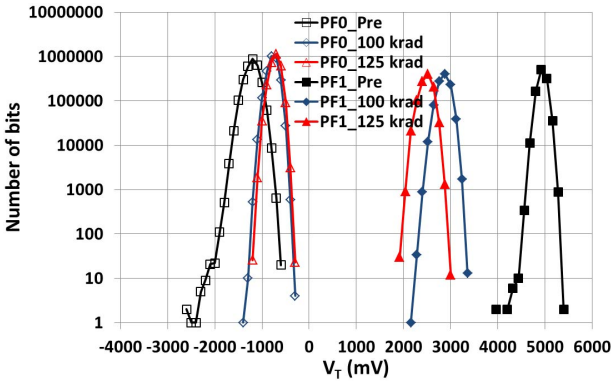


Fig. 9. Post-4600-h DBI Pflash $V_T$ distributions versus TID for DUT 3231.

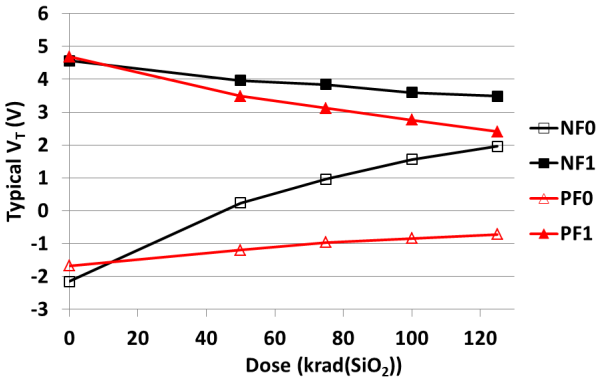


Fig. 10. Post-160-h DBI typical $V_T$ versus TID for Nflash and Pflash cells for DUT 3776.

the programmed (PF0) and erased (PF1) Pflash cells are shown in Figs. 8 and 9, respectively. Figs. 10 and 11 show the typical (or mean) $V_T$ shift with TID for both Nflash and Pflash in programmed and erased states post-160 (DUT 3776) and post-4600 h (DUT 3231) of DBI, respectively. TID-induced $V_T$ loss for Pflash0 saturates nearly 100–125 krad($SiO_2$) post-160 and post-4600 h of DBI.

The results show that the $V_T$ distribution of the Pflash cells does not cross the operation mode bias, whereas the erase state $V_T$ distribution of the Nflash cells cross the operation mode bias after 100 krad($SiO_2$). Even though the Nflash cells $V_T$ distribution cross the operation bias after 125 krad($SiO_2$) the part did not fail functionality. This is due to the C-flash bit cell design, where the device does not fail functionality, as long as the correct voltage is passed onto the gate of the switch device. The RTG4 C-flash bit cell is a radiation tolerant design developed specifically for RTG4 to reach a TID tolerance higher than 100 krad($SiO_2$) [4], [5]. Although the $V_T$ of the Pflash0 shifted post-DBI, the $V_T$ change did not affect the C-flash TID tolerance because the TID of the C-flash bit cell is dominated by the $V_T$ shift of the Nflash cell, which shifts by ~3.7 V after 100 krad($SiO_2$) (for NF0) versus ~0.84 V (for PF0). Any change in the threshold voltage of the Nflash and Pflash transistors caused by accumulation of charges in their floating gates, does not result in a change in the state of C-flash pair (and consequently the state of the switch device) until the threshold voltage degrades past the switching

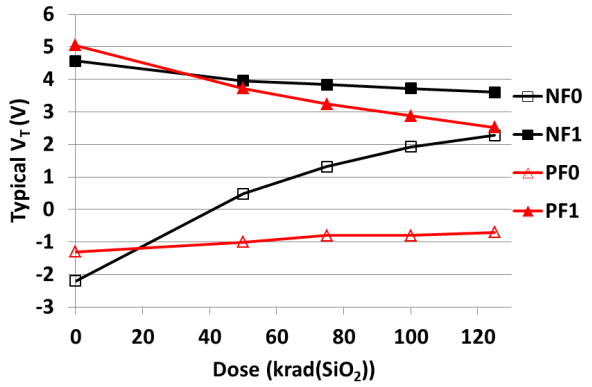


Fig. 11. Post-4600-h DBI typical $V_T$ versus TID for Nflash and Pflash cells for DUT 3231.

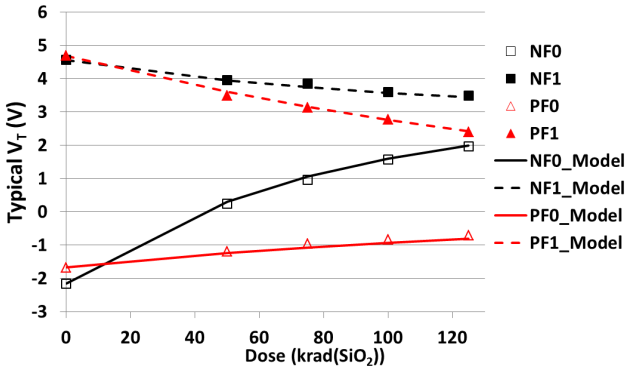


Fig. 12. Model prediction (solid line and dashed line) and experimental $V_t$ versus total dose for Nflash and Pflash cells in erased and programmed states.

threshold or operation mode bias of the transistors, which is at a TID level higher than 100 krad($SiO_2$). For flash cells, once we get close to neutral $V_T$ postradiation, a small $V_T$ shift is expected postbake. The $V_T$ decays fast at the beginning and slows down as we get close to the neutral $V_T$ [6] as shown by the results in Figs. 10 and 11. Therefore retention effect will be minimal after TID, especially for Nflash cells since we are very close to neutral $V_T$ after 125 krad($SiO_2$).

### *D. Modeling of Flash Cells $V_T$ as a Function of TID*

The results show that the Nflash cells, specifically the erased cells show the largest shift with TID compared to Pflash cells. In this section, we are using an analytical model to predict the immediate TID effects on the threshold voltage of floating gate devices including Nflash and Pflash cells to understand why Nflash cells shift more than Pflash cells. There are three radiation-induced mechanisms that can affect the threshold voltage of the floating gate devices [14]: 1) holes injected into the floating gate; 2) holes trapped into the oxides; and 3) electrons emitted over the polysilicon or oxide barriers. Electron–hole pairs generated from radiation results in the injection of holes into the floating gate and the trapping of holes in the oxides. Hole injection and trapping have a similar effect since they both reduce the threshold voltage in the floating gate device. The third radiation phenomenon: electron emission occurs mainly when radiation-induced photons possess an energy exceeding the potential barrier. The emitted electrons are then swept to the substrate or control gate by the electric field, which reduces the floating gate threshold voltage.

Fig. 12 shows the experimental data fitting to the analytical model [5], [6], [14], which predicts the immediate TID effect on the threshold voltage of floating gate devices. Both Nflash and Pflash cells $V_T$ versus total dose can be modeled by the following natural decay equations [14]:

$$V_T(\gamma) = V_T(\infty) + [V_T(0) - V_T(\infty)]e^{-A\gamma} \quad (1)$$

$$A = a + b + e_c \quad (2)$$

$$a = qG_h\alpha h(t_1, t_2) \quad (3)$$

$$b = qG_h\alpha\ (1-\alpha)h(t_1, t_2) \quad (4)$$

$$h(t_1, t_2) = \frac{t_1 k_1}{\epsilon_1 + \epsilon_2 \frac{t_1}{t_2}} + \frac{t_2 k_2}{\epsilon_1 \frac{t_1}{t_2} + \epsilon_2}. \quad (5)$$

TABLE IV
FIT DECAY CONSTANT FOR NFLASH AND PFLASH CELLS IN ERASED AND PROGRAMMED STATES

| Flash Cell | State | A (krad($SiO_2$)$^{-1}$) |
|---|---|---|
| NFlash0 | Erase | 0.013 |
| NFlash1 | Program | 0.01 |
| PFlash1 | Erase | 0.005 |
| PFlash0 | Program | 0.007 |

The $\gamma$ parameter is the total dose, $V_T(0)$ is the initial value, $V_T(\infty)$ is the saturation value when $\gamma$ approaches infinity, and $A$ is a decay constant. In (3)–(5), $q$ is the electron charge, $G_h$ is the number of electron–hole pairs generated, $\alpha$ is the fraction of holes injected into the floating gate, $(1-\alpha)$ is the fraction trapped in the oxide, $d_1$ is the tunnel oxide thickness between the floating gate and the silicon substrate and $\epsilon_1$ is the permittivity for that region, and $d_2$ is the effective oxide thickness between the control gate and floating gate as shown in Fig. 1(b) and $\epsilon_1$ is the permittivity for that region. Finally, $k$ is the slope of the collection efficiency [14].

The fitting of the decay constant $A$, in krad($SiO_2$)$^{-1}$, for Nflash and Pflash cells in erased and programmed state is presented in Table IV. The fitting shows that the decay constant for Nflash cells is larger than the decay constant for Pflash cells.

The decay constant $A$ is a function of the gate oxide $T_{ox}$, the electric field and other physical constant that depends on the electric field listed in (2). The parameter $a$ in (2) results from the hole injection, parameter $b$ results from hole trapping and the last parameter $e_c$ is due to electron emission. Since the gate-stack in the flash cell is the same for both N- and Pflash, including $d_1$ and $d_2$, the nitride layer as well as the floating gate for both N- and Pflash cells, the main parameter contributing to the difference observed is the electric field and the charge stored during programming and erase. Electron–hole pairs are generated during radiation, the number of electron–hole pairs depends on the material and volume available. A fraction of the electron–hole pairs will recombine; this fraction greatly depends on the electric field across the radiation oxide. During operation the voltage applied to the gate of the Nflash cells is 2 and 1 V for Pflash cells. Therefore we can conclude that the Nflash erased cells show the largest shift with TID due to a combination of the operation mode

gate bias and the charge stored in the floating gate during the erased state.

## IV. Discussion

This paper demonstrates a practical method to evaluate the combined effects of DBI and TID on a single DUT. Furthermore, since both N- and Pflash are measured in one setup, their individual characteristics can be studied simultaneously. The contrast of DBI and TID test results on Nflash and Pflash is an interesting finding. Further investigations on this topic to enhance the confidence level of RTG4's reliability in space should be worthwhile.

The results show no observable difference on the TID tolerance post-DBI, since the programmed Pflash $V_T$ shift is the dominant effect post-DBI, whereas the erased Nflash $V_T$ shift is the dominant effect post-TID. Thanks to the C-flash cell configuration, which was specifically designed for RTG4 to reach TID tolerance $>100$ krad($SiO_2$), a much higher dose is required to create a functional failure. The effect of BI or aging has been extensively studied on MOS devices, Shaneyfelt *et al.* [15], [16] showed that BI significantly affects the radiation response of MOS devices and Fleetwood *et al.* [17] showed that oxide and interface traps in MOS devices are affected by hydrogen-related species. For flash devices studied in this paper, we show that flash cells exposed to BI shift slightly more after TID than control unit (no BI), however, the shift is not significant enough to cause device failure. End of life limits are selected carefully with enough margin to include both the effect of TID and retention.

Although the results of this paper suggest that DBI has minimum impact on the TID tolerance of flash-based FPGAs, lot testing still needs to be performed to account for any lot to lot variation and is completed for each production lot from different screening flows before the units are shipped to customers.

## V. Conclusion

RTG4's TID tolerance is investigated post-DBI. A shift of the programmed Pflash cell $V_T$ post-DBI is observed. The programmed Pflash $V_T$ shift is due to programming voltage degradation, resulting from $\sim$1.75% degradation of the DAC's output. The $V_T$ shift of the pMOS devices within the DAC is due to NBTI, and results in the degradation of the output of the DAC. The TID results show no observable degradation of the TID tolerance post-DBI. DBI has minimum impact on RTG4 TID tolerance, since the TID tolerance of the C-flash is dominated by the Nflash cell. Therefore, we can conclude that Pflash $V_T$ shift is the dominant effect post-DBI, whereas Nflash $V_T$ shift is the dominant effect post-TID.

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