Software and Licensing

The Libero® SoC PolarFire Design Suite is required for designing with the PolarFire Evaluation Kit. Libero SoC PolarFire Design Suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools for designing with Microsemi's low power Flash FPGAs and SoC. The suite integrates industry standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management and debug capabilities.

Download the latest Libero SoC PolarFire release:

www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-soc-polarfire#downloads

A Gold license is required to program the PolarFire Evaluation Kit. A Software ID letter enclosed with the kit contains Software ID and instructions on how to generate a Libero Gold license. For more information, see www.microsemi.com/products/fpga-soc/design-resources/dev-kits/polarfire/polarfire-eval-kit#licensing

Documentation Resources

For more information about the PolarFire Evaluation Kit, including schematics and user's guides, see the documentation at https://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/ polarfire/polarfire-eval-kit#documentation.

Support

Technical support is available online at www.microsemi.com/soc/support and by email at soc_tech@microsemi.com.

Microsemi sales offices, including representatives and distributors, are located worldwide.

Microsemi Headquarters
One Enterprise, Aliso Viejo, CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
email: sales.support@microsemi.com
www.microsemi.com

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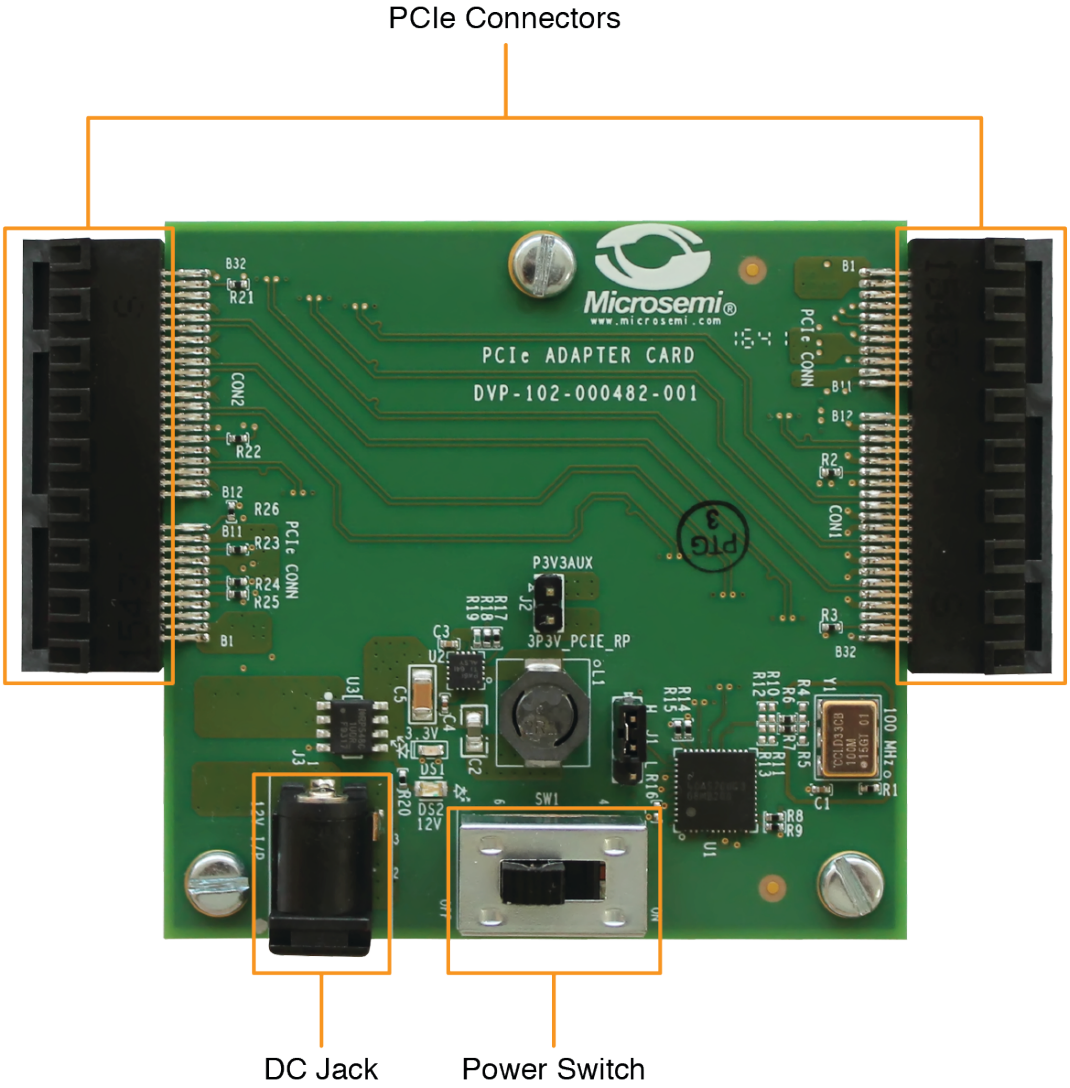
PCIe Root Port Adapter Card Quick Start Card

Kit Contents

Quantity	Description
1	PCIe root port adapter card
1	12 V, 5 A AC power adapter and cord
1	This quickstart card



Overview

Microsemi PolarFire® FPGAs support fully integrated PCIe Endpoint and Root Port subsystems with optimized embedded controller blocks that use the physical layer interface (PHY) of the transceiver. Each PolarFire device includes two embedded PCIe subsystem (PCIESS) blocks that can be configured either separately, or as a pair, using the PF_PCIE IP configurator in the Libero® System-on-Chip (SoC) PolarFire software. The PF_PCIE IP core is compliant with the PCI Express Base Specification, Revision 2.1. It implements memory-mapped advanced microcontroller bus architecture (AMBA) advanced extensible interface 4 (AXI4) access to the PCIe space, and the PCIe access to the memory-mapped AXI4 space. For more information, see UG0685: PolarFire FPGA PCI Express User Guide.

Microsemi's PCIe RootPort Adapter Card is a hardware evaluation platform for evaluating and testing the PolarFire FPGA PCIe Root Port capabilities like the enumeration of an Endpoint device, low-speed and high-speed data transfers.

Applications

PCIe interface is used across many applications, including the following:

- Automotive Applications
- Datacenter infrastructure
- Enterprise infrastructure
- Defense systems

Key Features

The PCIESS is a hard PCI Express protocol stack embedded within every PolarFire device and includes the following important features.

- PolarFire transceivers for 2.5 and 5.0 Gbps line speeds
- Native x1, x2, and x4 lane-support PCIe block (down-configurable/downgradable)
- Root port support for up to two 32-bit or one 64-bit BAR.
- PCI express base specification 1.1- and 2.1-compliant
- Legacy PCI power management support
- 64-bit AXI master and slave interface to the FPGA fabric
- End-to-end data integrity

Hardware Setup

To evaluate Microsemi's PCIe RootPort solution a three-board hardware setup is utilized. The adapter card is plugged into two PolarFire Evaluation boards, one running the root port design and another running the end point design. All development boards are required and must be purchased separately.

Pre-Programmed Demo Design

The PolarFire Evaluation Kits must be programmed before use. The root port design must be programmed on one kit and the endpoint design must be programmed on the other kit. See DG0802: Polarfire FPGA PCIe Root Port Demo Guide.

Jumper Settings

Jumper	Pin	Factory Default
J1	1–2	Open

Running the Demo

The demo requires Programming the PolarFire devices on the two evaluation boards with the end point and root port designs and connecting the two PolarFire evaluation boards though the PCIe Root Port Adapter card. In order to run the demo, set up the PCIe root port adapter card as outlined in the following steps. For detailed instructions, refer to DG0802: PolarFire FPGA PCIe Root Port Demo Guide.

1. Ensure that the pins 1 and 2 of the J1 jumper are closed.
2. Ensure that the pins 1 and 3 of the J2 jumper are open.
3. Connect CON1 of the adapter card to CON3 (PCIe slot) of board running the Root Port design.
4. Connect CON2 of the adapter card to CON3 (PCIe slot) of board running the Endpoint design.
5. Connect the USB cable from the Host PC to J5 (FTDI port) on board running the Root Port design.
6. Connect the USB cable from the Host PC to J5 (FTDI port) on board running the Endpoint design.
7. Connect the power supply cable to the J3 connector of the PCIe adapter card.
8. Power on Board A and B using the SW3 slide switch.
9. Power-up the PCIe adapter card using the SW1 slide switch

Programming

Microsemi's PolarFire Evaluation Kit provides feasible programmability using an on-board embedded FlashPro5 programmer.

The board can also be programmed with standalone FlashPro4/5 hardware.

IAP programming and debug support is also provided on the board.

See Documentation Resources for more information about programming procedures..