PolarFire FPGA CPRI

AN4949

Introduction (Ask a Question)

Common Public Radio Interface (CPRI) is an industry standard which defines the publicly available specification for the key internal interface of radio base stations between Radio Equipment Control (REC) and Radio Equipment (RE). Microchip provides the CPRI slave IP core that implements the transmitter and receiver interfaces of the CPRI standard.

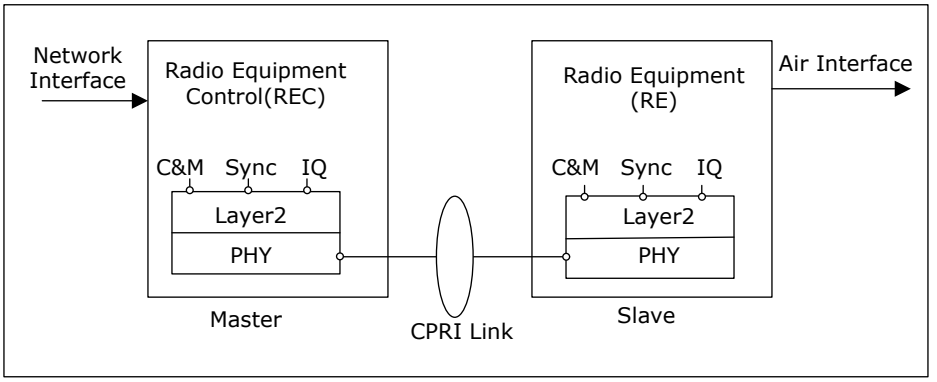
Important: The protocol standard uses the terminology “Master” and “Slave”. The equivalent Microchip terminology used in this document is **Initiator** and **Target**, respectively.

Table of Contents

1. Common Public Radio Interface Demo (Ask a Question)

CPRI IP cores are easy to integrate with CPRI-based data converters to develop high-bandwidth applications. Microchip® CPRI IP supports from Line Rate 1 (614.4 Mbps) to Line Rate 7 (9830.4 Mbps). The transceiver supports link rate from 250 Mbps to 12.5 Gbps per lane. The transceiver supports up to Line Rate 9 for CPRI protocol. The transceiver (PF_XCVR) module integrates several functional blocks to support multiple high-speed serial protocols within the FPGA.

Figure 1-1. Radio Base Station System



This demo design is created using the PolarFire® high-speed transceiver blocks and CPRI Slave IP core. The design operates in the loopback mode by sending the CPRI Master data to the CPRI Slave IP core through the transceiver lanes, which are looped back on the board. This loopback setup facilitates a stand-alone CPRI interface demo that does not require CPRI testers and other devices to validate the design.

The demo design shows CPRI loopback using transceiver on the evaluation board. The CPRI Slave IP is configured with the following settings:

- Line Rate 5: 4.9152 Gbps
- Number of Antenna carriers: 4
- The transceiver is configured in 8b10b mode running at 4.9152 Gbps data-rate
- 32-bit PCS fabric interface using a 122.88 MHz reference clock

2. Design Requirements (Ask a Question)

The following table lists the hardware and software requirements for running the demo.

Table 2-1. Design Requirements

Requirement	Version
Operating system	Windows® 10
Hardware	
PolarFire® Evaluation Kit (MPF300-EVAL-KIT)	Rev D or later
Software	
Libero® SoC	See the `readme.txt` file provided in the design files for the software versions used with this reference design.
FlashPro Express	

Important: Libero® SmartDesign and configuration screen shots shown in this guide are for illustration purpose only. Open the Libero design to see the latest updates.

3. Prerequisites (Ask a Question)

Before you begin, perform the following steps:

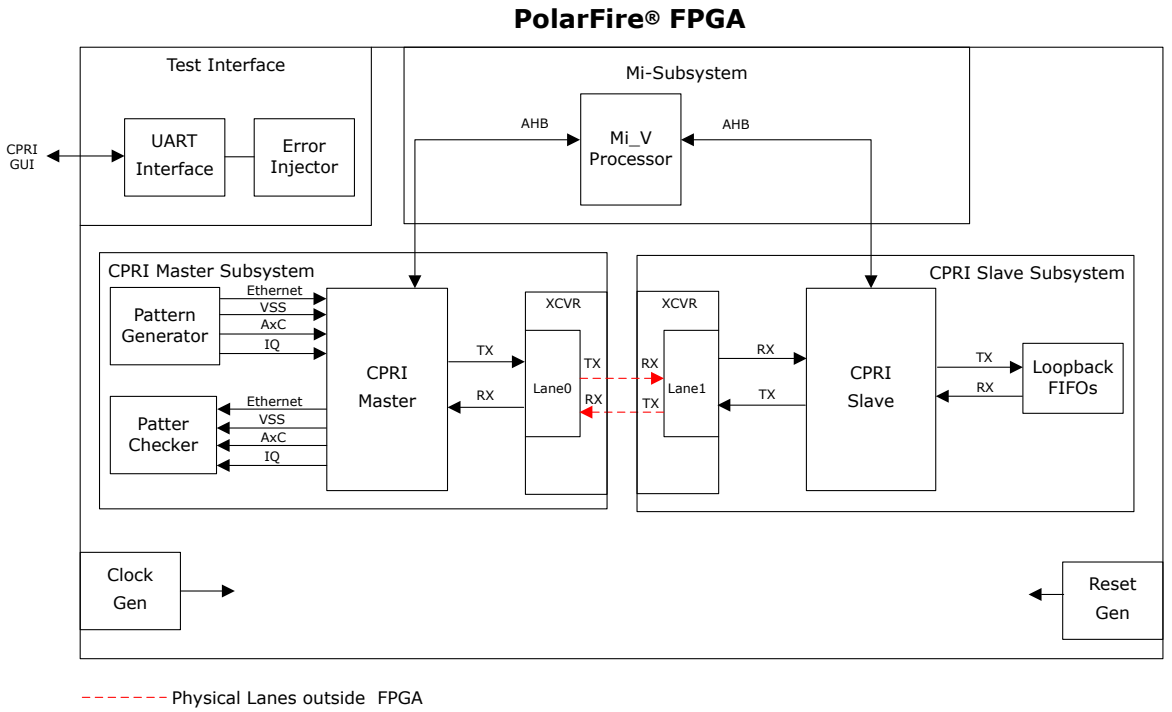
1. Download the **demo design** files from: www.microchip.com/en-us/application-notes/AN4949.
2. Download the Libero SoC (as indicated in the website for this design) from Libero SoC Documentation and install it on the host PC.
3. Download and install the SoftConsole on the host PC.

4. Demo Design (Ask a Question)

The PolarFire CPRI Loopback demo design is developed for demonstrating CPRI IP in Slave mode. The pattern generator in this demo design generates CPRI protocol data such as IQ data, VSS data, Ethernet data, and Antenna carrier control data which is provided to the CPRI master module. The CPRI master module frames the data according to the CPRI protocol. The generated frames from the CPRI master are loopbacked to CPRI slave IP using the XCVR. The CPRI slave IP unpacks the incoming data into IQ data, VSS data, Ethernet data, and Antenna carrier control data. This data is then loopbacked from CPRI slave IP to CPRI master module, therefore demonstrates Full duplex transmission of CPRI IP in Slave mode.

The following figure shows the top-level block diagram of the CPRI demo design.

Figure 4-1. CPRI Demo Design Block Diagram



The following steps describe the data flow in the demo design:

1. The Mi_V_module configures the registers of the CPRI Master module and CPRI slave IP blocks.
2. The reference design uses a transceiver interface (PF_XCVR_ERM) configured in 8b10b mode running at 4.9152 Gbps data rate, 32-bit PCS fabric interface, and 122.88 MHz reference clock.
3. The CPRI master module and CPRI IP are configured at Line Rate 5: 4.9152 Gbps with four Antenna carriers.
4. The CPRI master module receives the IQ data from the TX IQ Data Generator and control information such as Ethernet data, Vendor specific data, and Antenna carrier control from the respective pattern generators.
5. CPRI master module then frames the incoming data and transmits a 32-bit CPRI frame to the transceiver.
6. The differential serial data of TX and RX is looped back using an on-board loopback.

7. The CPRI slave IP receives the incoming frames and segregates the incoming data according to the CPRI protocol.
8. The segregated IQ data, Vendor specific data, Ethernet data, and Antenna carrier control information are written to the respective loop back FIFO's.
9. CPRI slave IP then reads the data from loopback FIFO's frames the data and transmits the a 32-bit CPRI frame to CPRI master module through the transceiver.
10. The CPRI master module receives the incoming frames, segregates and sends the incoming data to respective pattern checkers.
11. Incoming control information is compared with the control data for Vendor specific, Fast Ethernet, IQ data, and Antenna carrier control data. When the data is matched, the respective lock signals are asserted.
12. The IQ data and control information such as Ethernet, Vendor specific, and Antenna carrier control lock signals from CPRI slave IP and master module along with transceiver RX_Valid and RX_ready for both the lanes are sent to the UART_interface block.
13. The UART_interface block forwards these status signal and locks information on its TX interface to the GUI for display.

4.1 Design Implementation (Ask a Question)

Each CPRI link connects two ports that have asymmetrical functions and roles: a master and a slave. The CPRI Demo design shows the CPRI point to point link between CPRI REC Master and CPRI RE Slave.

The top-level design includes the following SmartDesign components:

- CPRI Master Subsystem
- CPRI Slave Subsystem
- Transceiver Subsystem
- Mi-V Subsystem
- Test Interface

4.1.1 CPRI Master Subsystem (Ask a Question)

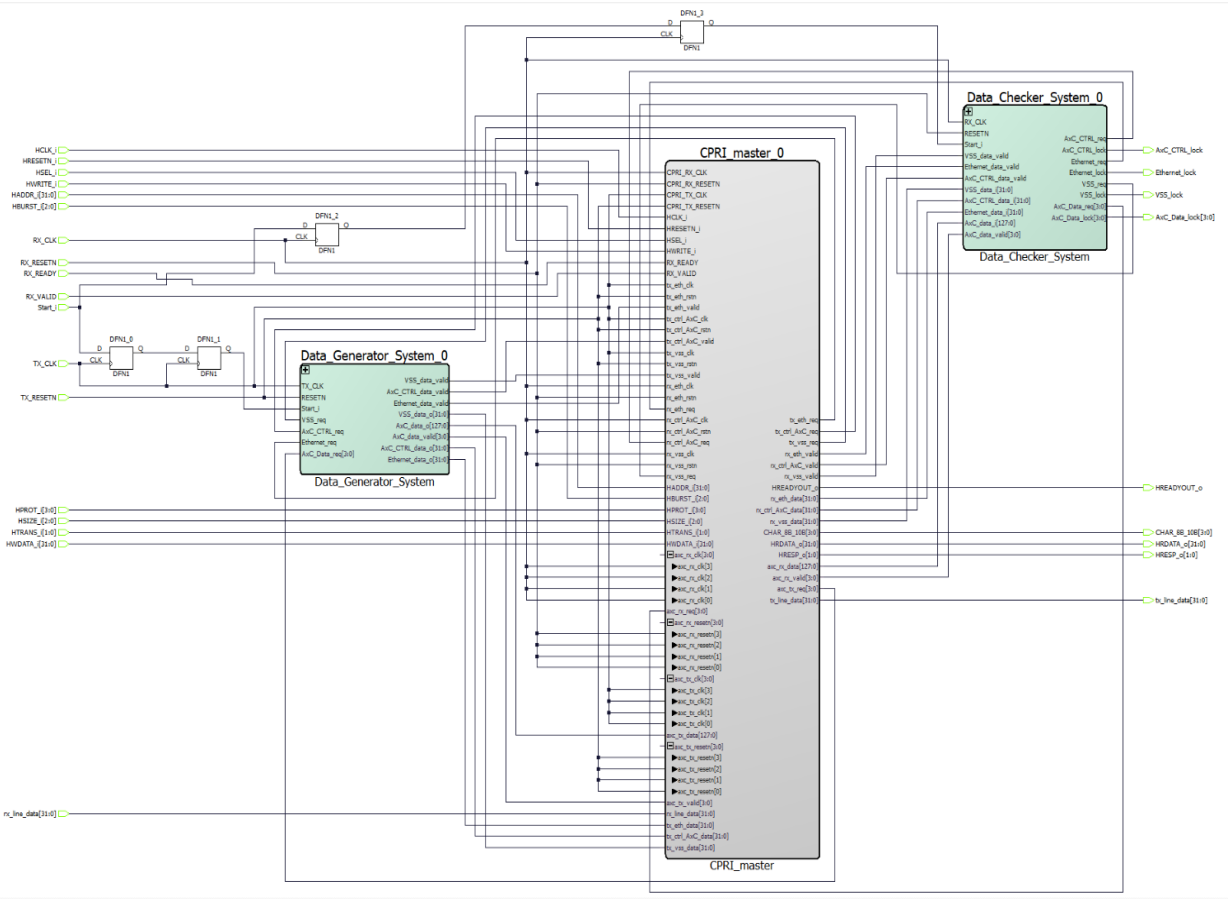
This sections gives the brief description about the CPRI REC Master.

The CPRI REC Master subsystem consists of the following modules:

- CPRI Master
- Pattern data generator
- Pattern checker modules

The following figure shows the implementation of CPRI master subsystem SmartDesign.

Figure 4-2. CPRI Master Subsystem SmartDesign



4.1.1.1 CPRI Master (Ask a Question)

When the CPRI master is configured, it receives IQ data, Vendor specific data, Antenna carrier control data, and Ethernet data from the respective pattern generator blocks. It then frames incoming data into the CPRI frame format at the rate of 4.9152 Gbps and transmits it to the serial lines through the XCVR interface.

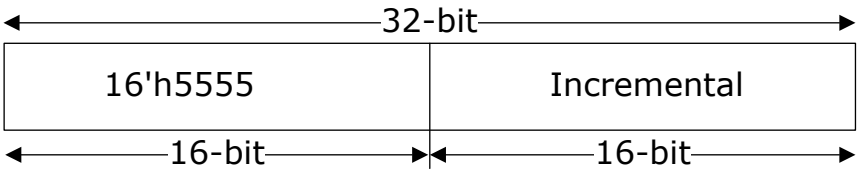
On the receive side, the CPRI master receives the data from the serial lines through the XCVR interface in the CPRI frame format, it then unpacks the data and sends the received IQ, VSS, and Ethernet data to the respective pattern checker block. For more information about register configuration, see 6. Register Configuration.

4.1.1.2 Pattern Data Generator (Ask a Question)

The pattern generator generates the following data:

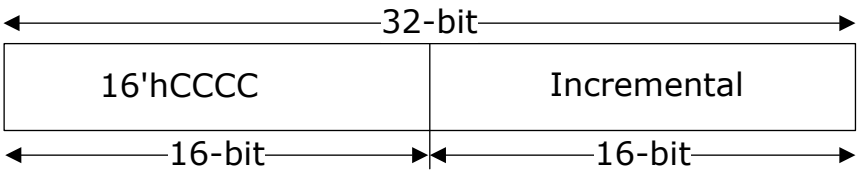
- 32-bit Ethernet data: The16-bit of MSB is constant and 16-bit of LSB is incremental data.

Figure 4-3. Ethernet Data Pattern



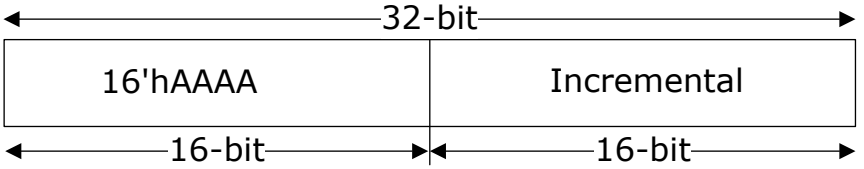
- 32-bit VSS data: The 16-bit of MSB is constant and the16-bit of LSB is incremental data.

Figure 4-4. VSS Data Pattern



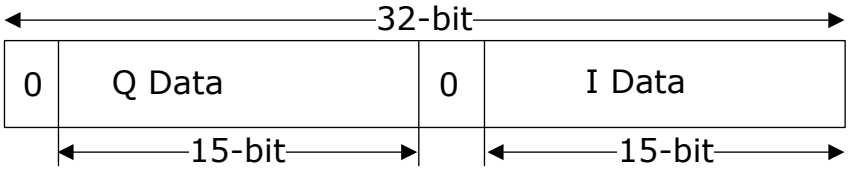
- 32-bit Antenna Carrier Control data: The 16-bit of MSB is constant and the 16-bit of LSB is incremental data.

Figure 4-5. Antenna Carrier Data Pattern



- In this demo four Antenna carriers are used, each antenna generates 32-bit data. The IQ data samples of each Antenna carrier control are fixed at 15-bit. The user-interface width is fixed at 32-bit, with zero appending on MSB. 15-bit IQ data samples are bit-stuffed in the 32-bit user interface for each Antenna carrier.

Figure 4-6. IQ Data Pattern



4.1.1.3 Pattern Checker (Ask a Question)

The pattern checker has individual pattern checker modules for VSS, Ethernet, Antenna carrier control, and IQ data, which checks for incremental, data and if the received data is matched, then the respective lock signals are asserted.

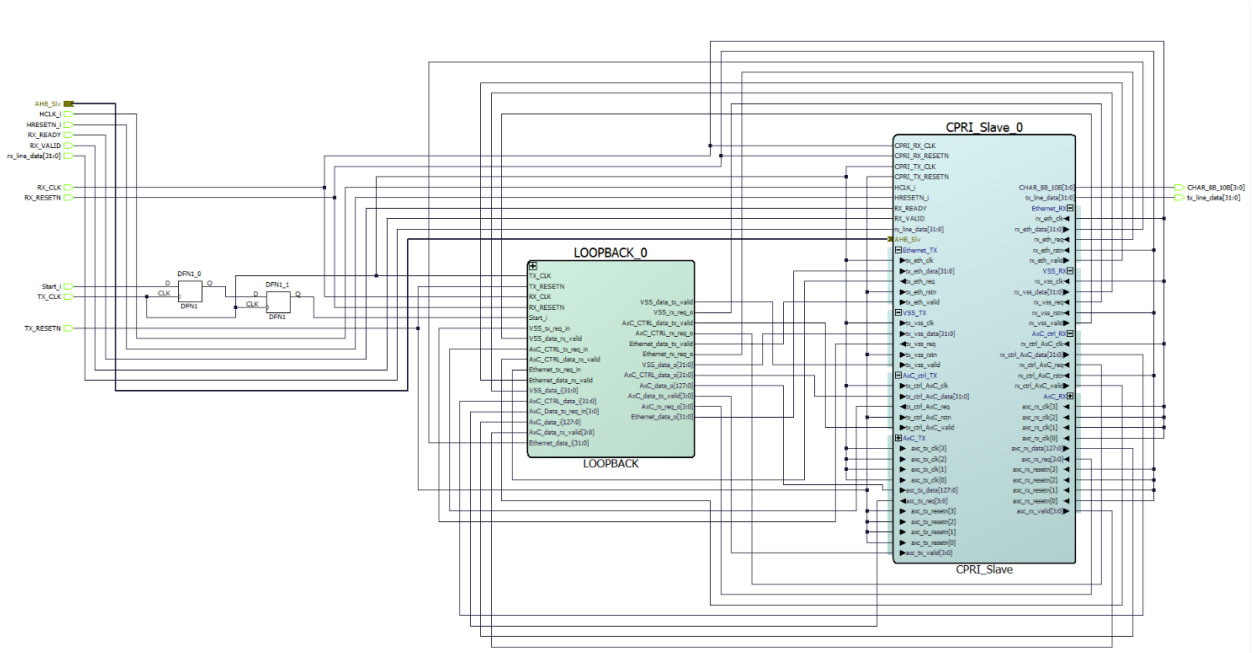
4.1.2 CPRI Slave Subsystem (Ask a Question)

The CPRI RE slave subsystem consists of the following modules:

- CPRI Slave
- Loopback FIFO

The following figure shows the CPRI Slave Subsystem SmartDesign implements CPRI Slave IP interface along with Ethernet, VSS, Antenna carrier control, and IQ data Loopback FIFO's.

Figure 4-7. CPRI Slave System



4.1.2.1 CPRI Slave (Ask a Question)

CPRI slave IP receives the data from the serial lines through the XCVR interface in the CPRI frame format. It then unpacks the data and sends the received IQ, VSS, Antenna carrier control, and Ethernet data to the respective Loopback FIFO's. On the transmit side, CPRI slave IP receives IQ, VSS, Antenna carrier control, and Ethernet data from the respective Loopback FIFO's, and then frames incoming data into the CPRI frame format at the rate of 4.9152 Gbps and transmits it to the serial lines through transceiver interface. For more information on CPRI register configuration, see 6. Register Configuration.

For more information about CPRI IP, see **Libero Catalog** > **Solution-Wireless** > **Microchip CPRI User Guide**.

4.1.2.2 Loopback FIFO (Ask a Question)

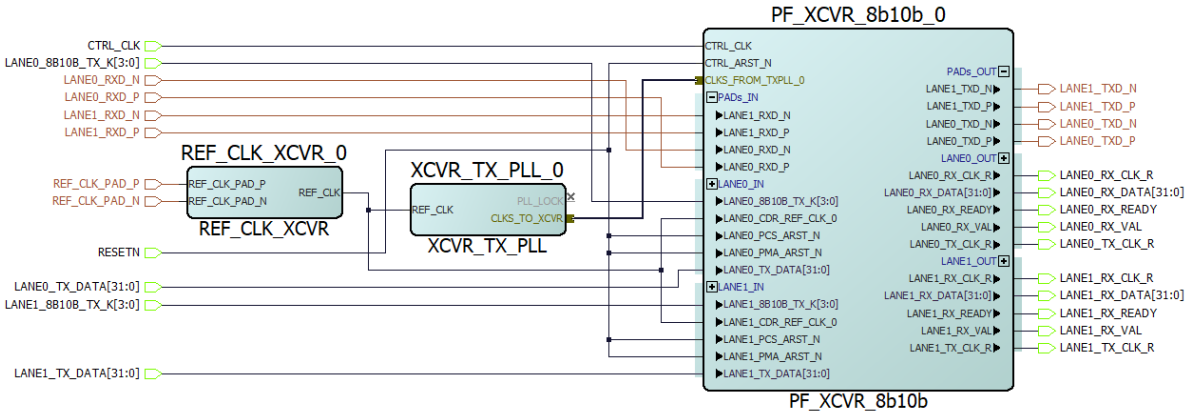
The Loopback FIFO module consists of individual loopback FIFO modules for VSS, Ethernet, Antenna carrier control, and IQ data, which loopback's the deframed data from the RX interface of CPRI IP to TX interface of CPRI IP.

4.1.3 Transceiver Subsystem (Ask a Question)

The transceiver is configured for the following characteristics:

- Two lanes at 122.88 MHz clock, each lane carries 32-bit IQ data
- 32-bit PCS interface
- Data rate of 4.9152 Gbps
- Lane 0 is configured for Master and Lane 1 is configured for Slave

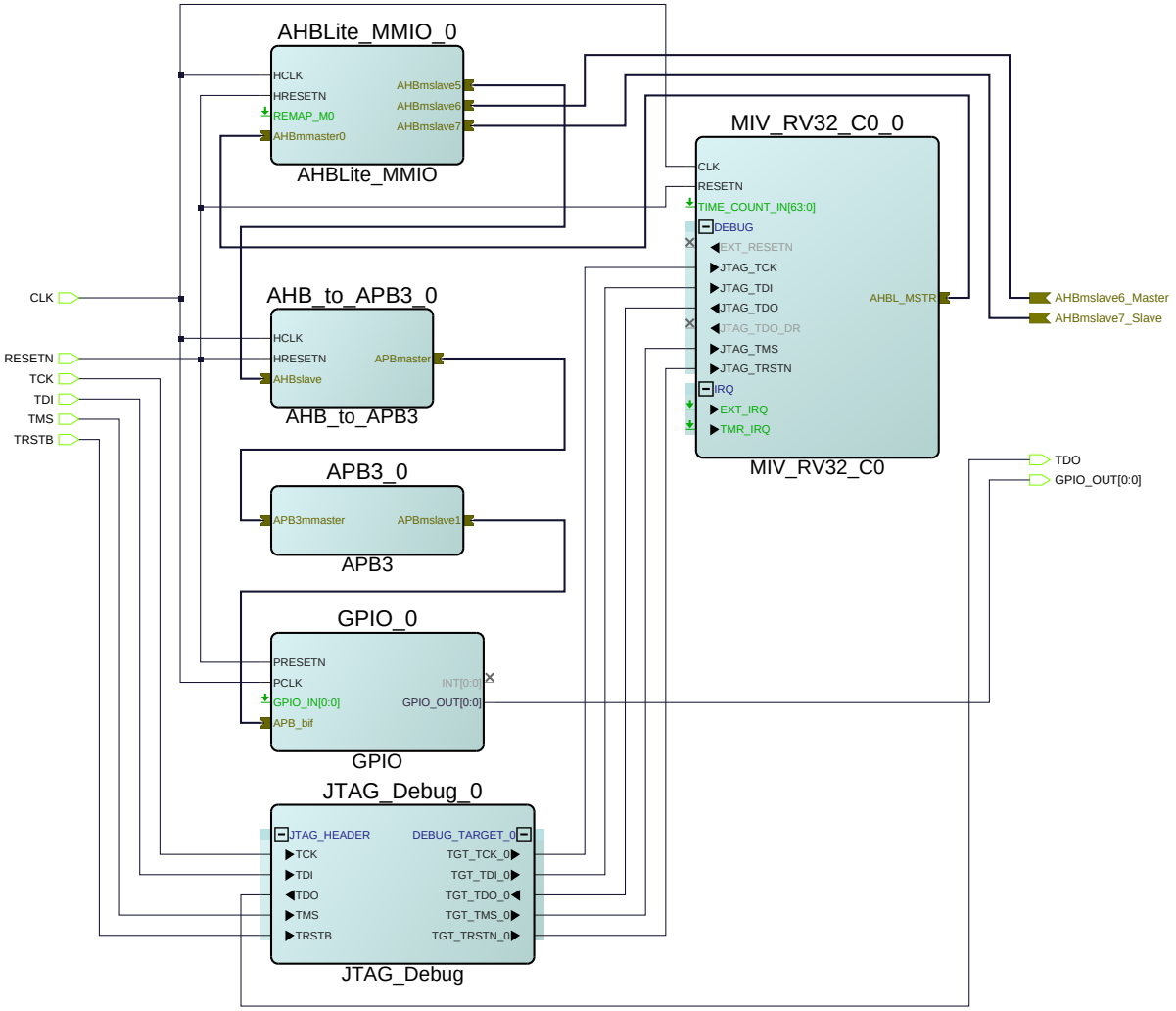
Figure 4-8. Transceiver Subsystem



4.1.4 Mi-V Subsystem (Ask a Question)

The Mi_V_Subsystem SmartDesign operates at 100 MHz. It implements an AHB interface and GPIO interface. The following figure shows how the AHB interface is used to access the CPRI configuration registers, and the GPIO interface is used to indicate configuration status.

Figure 4-9. Mi-V Subsystem



For more information about how to build the Mi-V subsystem, see TU0775 Tutorial PolarFire FPGA: Building a Mi-V Processor Subsystem.

The following table lists the address map of Mi-V processor.

Table 4-1. System Memory Map

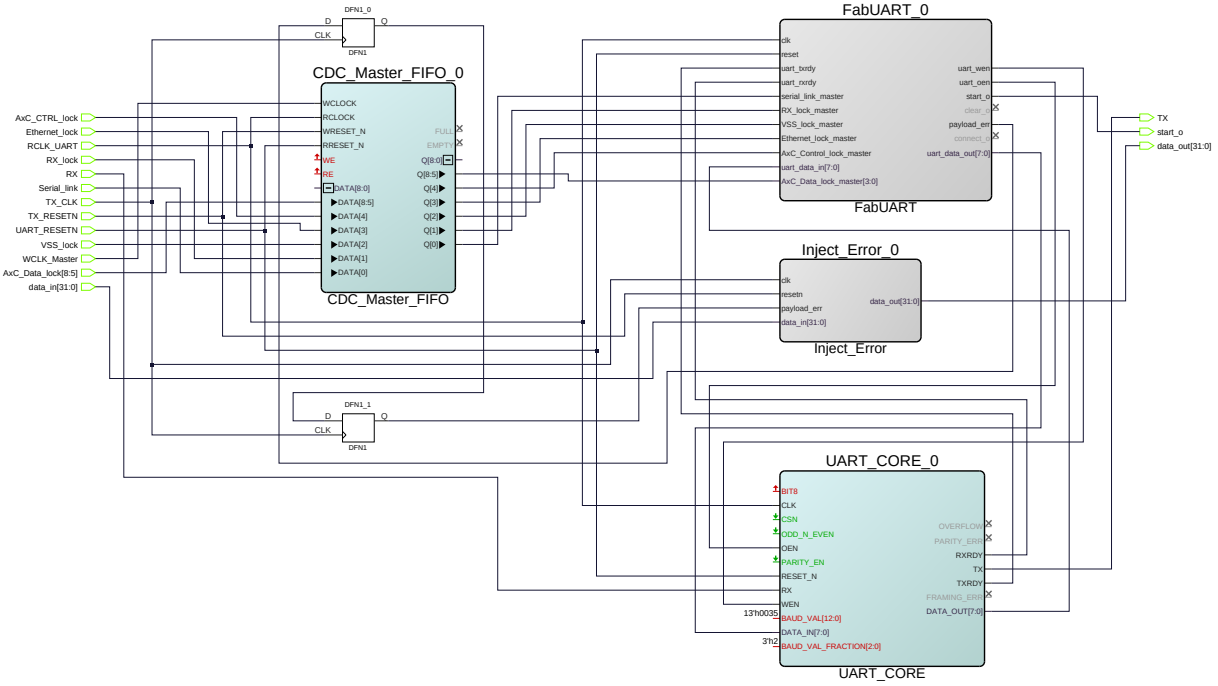
Component	Memory Map	Description
CoreGPIO	0x60051000	This bus interface is used to access the GPIO's through APB interface.
CPRI Slave IP	0x60060000	This bus interface is used to access CPRI slave IP configuration registers through the AHB interface.
CPRI Master module	0x60070000	This bus interface is used to access CPRI master configuration registers through the AHB interface.

4.1.5 Test Interface (Ask a Question)

The test interface system contains the UART interface and Inject error module.

The following figure shows the test interface SmartDesign implementations.

Figure 4-10. Test Interface SmartDesign



4.1.5.1 UART Interface (Ask a Question)

The UART_Interface SmartDesign interfaces Fabric UART logic with the GUI, which displays the lock signal.

4.1.5.2 Inject Error (Ask a Question)

The Inject error module induces an error in the CPRI frame that propagates through the serial interface. The presence of an error is validated using a pattern checker module.

5. Port Description (Ask a Question)

The following table lists the input and output ports of the design.

Table 5-1. Port Description

Signal	Direction	Description
RESETN	Input	External reset
REF_CLK_PAD_P and REF_CLK_PAD_N	Input	This is the differential reference clock generated from the on-board 122.88 MHz oscillator
LANE0_RXD_P and LANE0_RXD_N	Input	Transceiver Receiver differential input of Lane0
LANE1_RXD_P and LANE1_RXD_N	Input	Transceiver Receiver differential input of Lane1
RX	Input	This is the input signal received by the UART interface from the GUI
LANE0_TXD_P and LANE0_TXD_N	Output	Transceiver Receiver differential output of Lane0
LANE1_TXD_P and LANE1_TXD_N	Output	Transceiver Receiver differential output of Lane1
Config_done	Output	Indicates CPRI master and slave register configuration is completed by Mi-V processor
VSS_lock	Output	Indicates the Received Vendor specific data is correct
Ethernet_lock	Output	Indicates the Received Ethernet data is correct
AxC_Control_lock	Output	Indicates the received Antenna Control data is correct
AxC_Data_lock	Output	Indicates the received Antenna IQ data is correct
TX	Output	This is the output data received by the GUI from the UART interface

6. Register Configuration (Ask a Question)

The CPRI master module and CPRI slave IP are connected to the Mi-V processor using an AHB interface. The base address of CPRI master is 0x60070000 and the base address of CPRI slave IP is 0x60060000.

Tip: It is recommended to follow the register configuration order as described in the following table.

The following table lists the register configuration and these registers are configured in the SoftConsole project: `mpf_an4949_v2022p3_df\SoftConsole\CPRI_config\main.c`.

Table 6-1. Register Configuration

Offset	Value	Description
0x04	0x1F	TX Interface Sequence Number Register Line Rate 5: TX_SEQ_NUM: 0x1f
0x08	0x1F	RX Interface Sequence Number Register Line Rate 5: RX_SEQ_NUM: 0x1f
0x0C	0xBC	TX Framer K character Register TX_Z_0_0_SYNC: 0xBC which is K28.5 character
0x10	0xBC	RX Framer K character Register RX_Z_0_0_SYNC: 0xBC which is K28.5 character
0x14	0x50	TX Framer D character Register TX_Z_0_1_SYNC: 0x50 which is D16.2 character
0x18	0x50	RX Framer D character Register RX_Z_0_1_SYNC: 0x50 which is D16.2 character
0x1C	0x50	TX Framer D character Register TX_Z_0_Y_SYNC: 0x50 which is D16.2 character
0x20	0x50	RX Framer D character Register RX_Z_0_Y_SYNC: 0x50 which is D16.2 character
0x2C	0x14	TX Fast Ethernet pointer register TX_Z_194_0: 0x14 The Fast Ethernet data to be written from this location.
0x24	0x01	TX Protocol Version Register TX_Z_2_0_SYNC: 0x01 The current version of the IP supports only protocol version 1.
0x30	0x14	RX Fast Ethernet pointer register RX_Z_194_0: 0x14 The Fast Ethernet data to be written from this location.
0x100	0xF4240	Start Timer Register Time out value for L1 Sync state machine
0x104	0x1FFF	HFN Sync Counter Register Line 5: HFN_COUNT: 1FFF This value indicates the duration of one CPRI Hyperframe for the selected Line rate.
0x00	0xF	CPRI Control Register Enables IQ mapper, demapper, and L1 sync state machine and CPRI IP functionality.

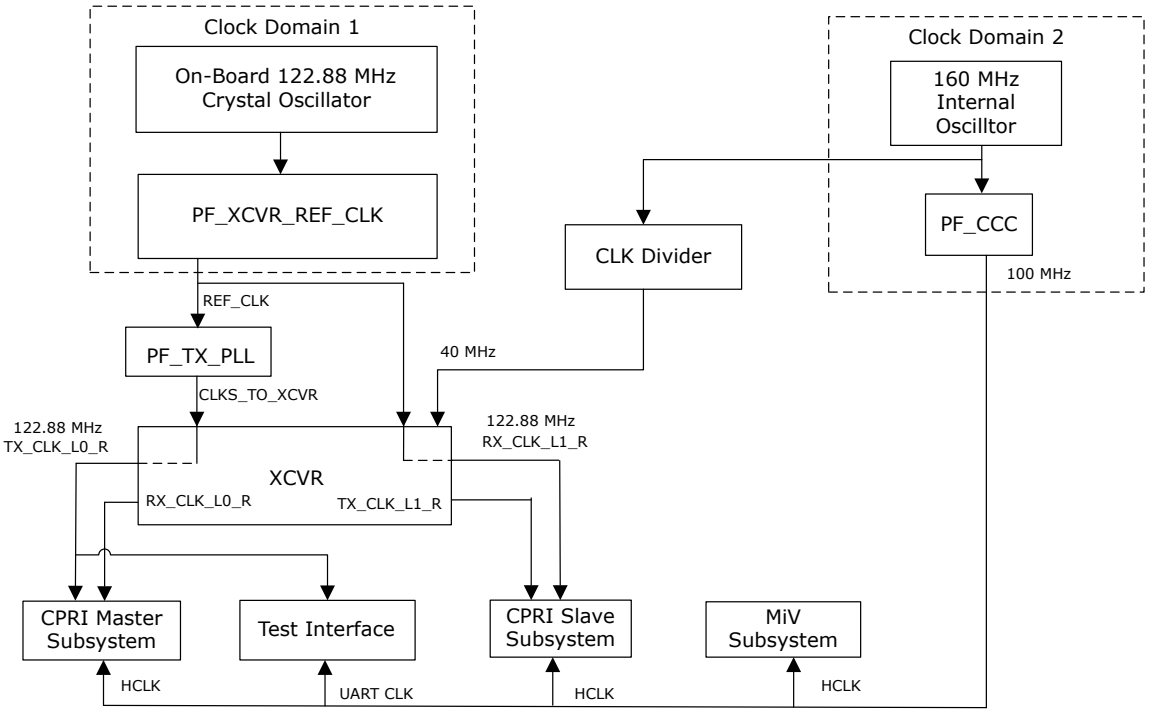
7. Clocking Structure (Ask a Question)

In this demo design, there are two clock domains. The on-board 122.88 MHz crystal oscillator drives the XCVR reference clock in 8b10b mode. This generates Lane0/1 RX clock and Lane0/1 TX clock. CPRI master system, CPRI slave Subsystem, and HDL modules use TX and RX clock (122.88 MHz).

The on-chip 160 MHz RC oscillator drives the CCC which generates 100 MHz clock. The UART_Interface, Mi-V system, and the AHB interface of the CPRI master subsystem and CPRI slave subsystem use 100 MHz clock. The clock divider generates 40 MHz clock for the XCVR_ERM.

The following figure shows the clocking structure in the reference design.

Figure 7-1. Clocking Structure



The following table lists the clocks used in the demo design.

Table 7-1. Clocks

Clock Name	Source	Frequency
Mi-V Clock	CCC_0	100 MHz
RX_CLK_L0_R	Transceiver RX recovered clock (Lane0)	122.88 MHz
RX_CLK_L1_R	Transceiver RX recovered clock (Lane1)	122.88 MHz
TX_CLK_L0_R	Transceiver TX PLL clock (Lane0)	122.88 MHz
TX_CLK_L1_R	Transceiver TX PLL clock (Lane1)	122.88 MHz
CTRL_CLK	CLK Divider	40 MHz

8. Reset Structure (Ask a Question)

In the demo design, the reset signal is generated using the Reset_Block module. CoreReset_FF (CoreReset_PF) module releases active-low reset signal of TEST_INTERFACE, Mi-V subsystem, CPRI master, and slave subsystem when PLL_lock output from PF_CCC block, RESETN (External active-low signal), and DEVICE_INIT_DONE signal from INIT_MONITOR block are asserted.

The CoreReset_L0_TX (CoreReset_PF) module releases an active-low reset signal of the CPRI master subsystem and Test Interface when the RESETN (External active-low signal) and DEVICE_INIT_DONE signals from the INIT_MONITOR block are asserted.

The CoreReset_L0_RX (CoreReset_PF) module releases an active-low reset signals of the CPRI master subsystem when RESETN (External active-low signal) and DEVICE_INIT_DONE signals from the INIT_MONITOR block are asserted.

The CoreReset_L1_TX (CoreReset_PF) module releases an active-low reset signal of the CPRI slave subsystem when the RESETN (External active-low signal) and DEVICE_INIT_DONE signals from the INIT_MONITOR block are asserted.

The CoreReset_L1_RX (CoreReset_PF) module releases an active-low reset signal of the CPRI slave subsystem when the RESETN (External active-low signal) and DEVICE_INIT_DONE signals from the INIT_MONITOR block is asserted.

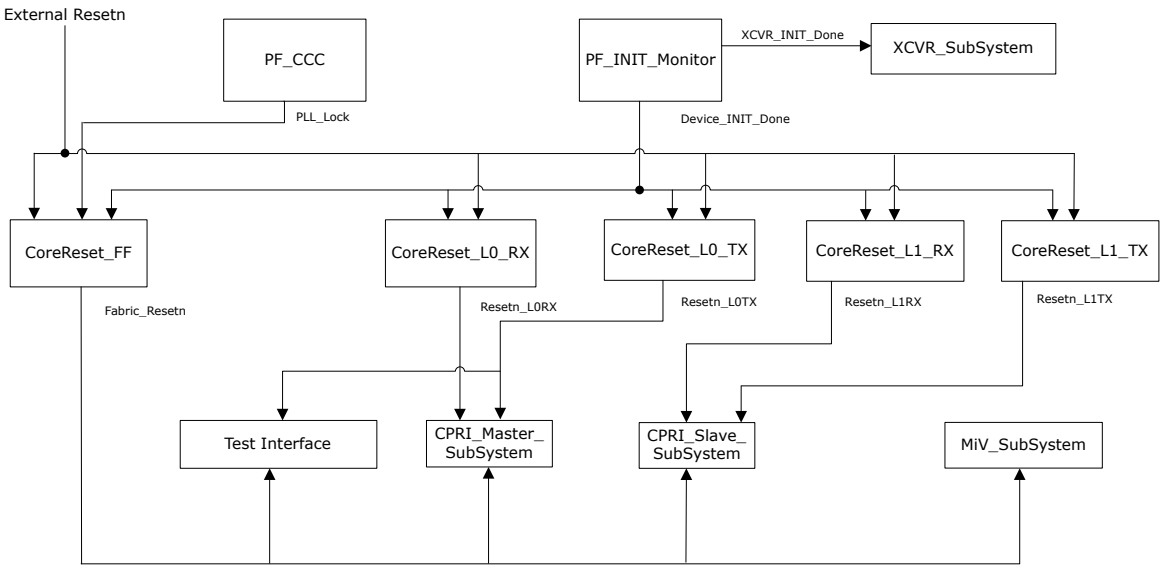
The INIT_MONITOR releases the active-low signal of XCVR_subsystem reset signals (PMA_ARST_N and PCS_ARST_N) when the XCVR_INIT_DONE signal from the INIT_MONITOR block is asserted.

DEVICE_INIT_DONE and XCVR_INIT_DONE signals are asserted when the device initialization is complete. For more information about device initialization, see PolarFire Family Power-Up and Resets User Guide.

For more information on CoreReset_PF IP core, see CoreReset_PF from the Libero catalog.

The following figure shows the reset structure in the demo design.

Figure 8-1. Reset Structure



9. Libero Design Flow (Ask a Question)

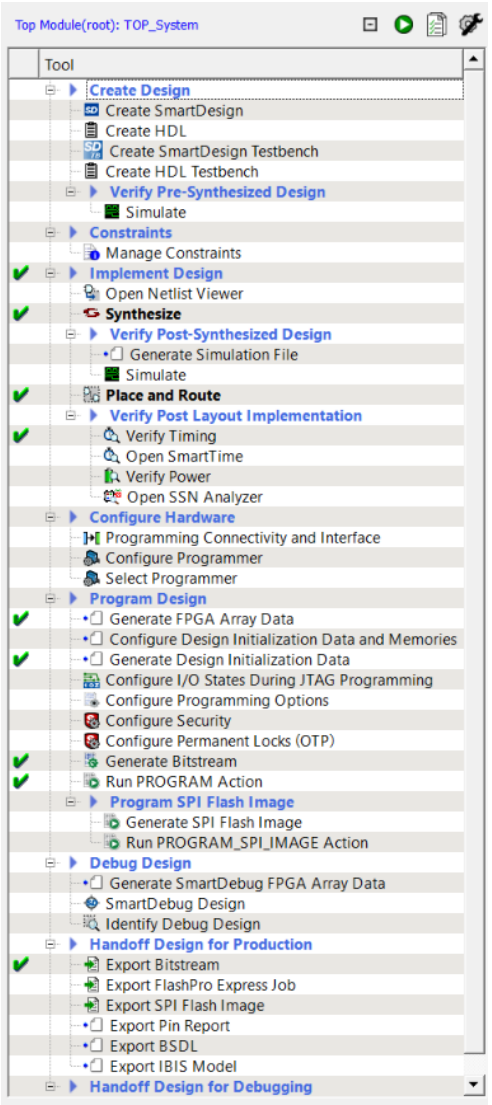
This section describes the Libero design flow, which involves the following processes:

- Synthesis
- Place and Route
- Verify Timing
- Design and Memory Initialization
- Generate Bitstream
- Run Program Action

Important: To initialize TCM in PolarFire using system controller, a local parameter, l_cfg_hard_tcm0_en, in the `miv_rv32_opsrv_cfg_pkg.v` file must be changed to 1'b1 prior to synthesis. See, MIV_RV32.

The following figure shows these options in the **Design Flow** window.

Figure 9-1. Libero® Design Flow Options



9.1 Synthesis (Ask a Question)

To synthesis the design, perform the following steps:

1. On the **Design Flow** window, double-click **Synthesize**.
2. When the synthesis is successful, a green tick mark appears next to Synthesize. See Figure 9-1.

The following table lists the resource utilization of the CPRI loopback design. These values vary slightly for different Libero runs, settings, and seed values.

Table 9-1. Resource Utilization—Synthesis

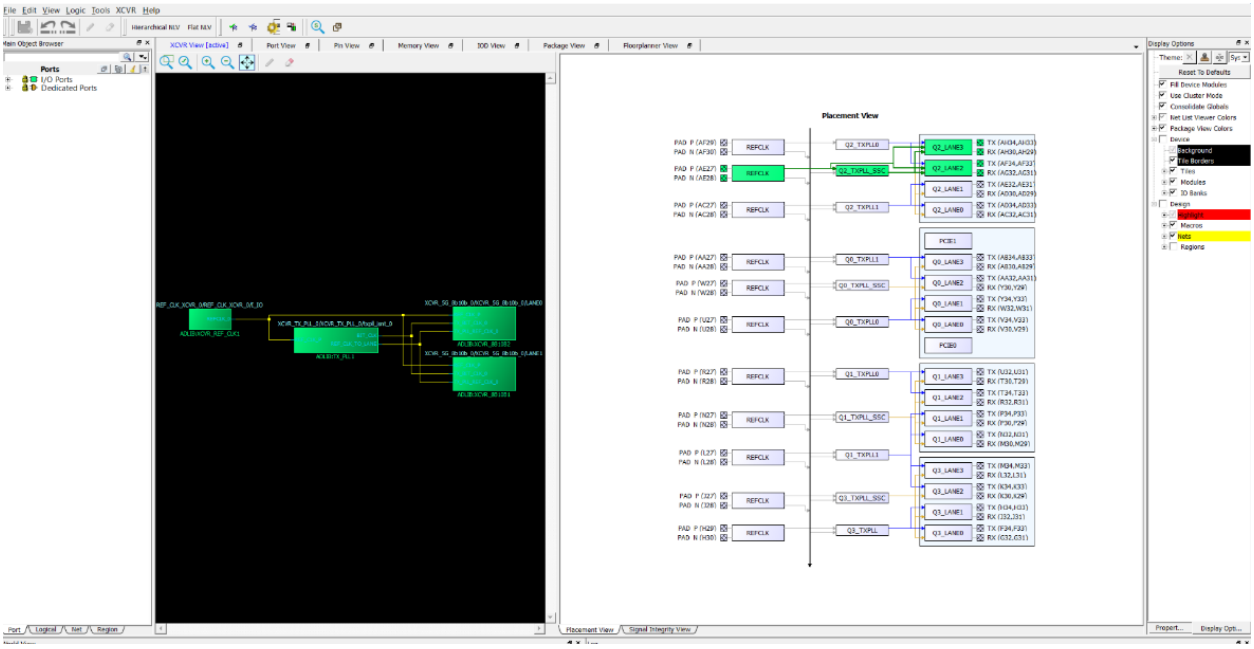
Type	Used	Total	Percentage
4LUT	26007	299544	8.68
DFF	15993	299544	5.34
I/O Register	0	1536	0
User VO	11	512	2.15
Single-ended I/O	11	512	2.15
Differential I/O Pairs	0	256	0

.....continued			
Type	**Used**	**Total**	**Percentage**
µSRAM	12	2772	0.43
LSRAM	75	952	7.88
Math	0	924	0
H-Chip Global	10	48	20 83
Local Global	4	1008	0.4
PLL	1	8	12.5
DLL	0	8	0
BANKEN	1	7	14.29
CRN INT	1	24	4.17
UJTAG	1	1	100
INIT	1	1	100
OSC RC160MHZ	1	1	100
Transceiver Lanes	2	16	12.5
Transceiver PCIe	0	2	0
TX PLL	1	11	9.09
XCVR REF CLK	1	11	9.09
ICB CLKDIV	1	24	4.17
ICB CLKINT	4	72	5.56
ICB INT	1	12	8.33

9.2 Place and Route (Ask a Question)

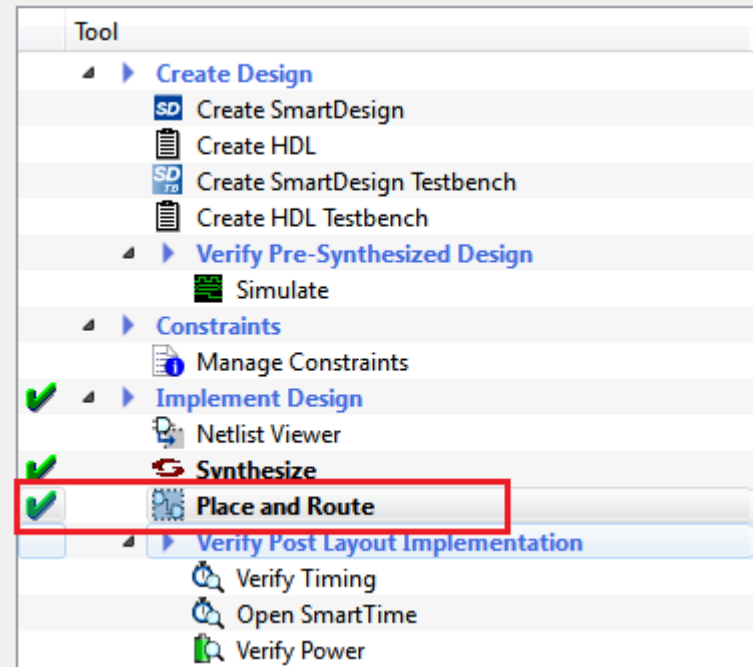
To place and route the design, TX_PLL, XCVR_REF_CLK, and PF_XCVR must be configured using the I/O Editor. For On-board transceiver loopback, the following figure shows how the Lane 2 and Lane 3 of Quard 2 are used.

Figure 9-2. I/O Editor Option—XCVR View



On the **Design Flow** window, double-click **Place and Route**. When place and route is successful, a green tick mark appears.

Figure 9-3. Place and Route



The following table lists the resource utilization after place and route.

Table 9-2. Resource Utilization—Place and Route

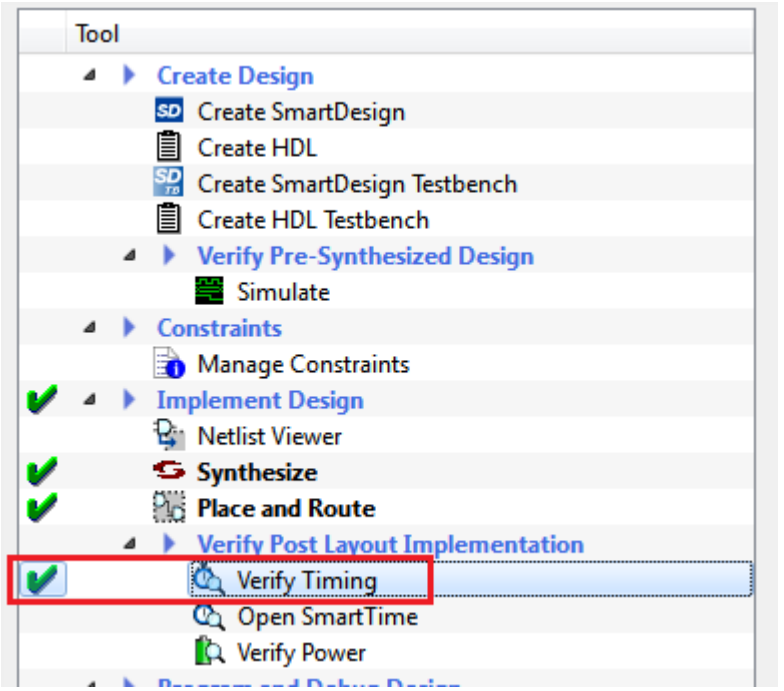
Type	Used	Total	Percentage
4 LUT	26471	299544	8.84
DEF	16099	299544	5.37
I/O Register	0	510	0
Logic Element	31843	299544	10.63

9.3 Verify Timing (Ask a Question)

To verify timing, perform the following steps:

1. On the **Design Flow** window, double-click **Verify Timing**. When the design meets the timing requirements, a green tick mark appears next to **Verify Timing**.
2. Right-click **Verify Timing** and select **View Report** to view the verify timing report and log files in the **Reports** tab.

Figure 9-4. Verify Timing



9.4 Design and Memory Initialization (Ask a Question)

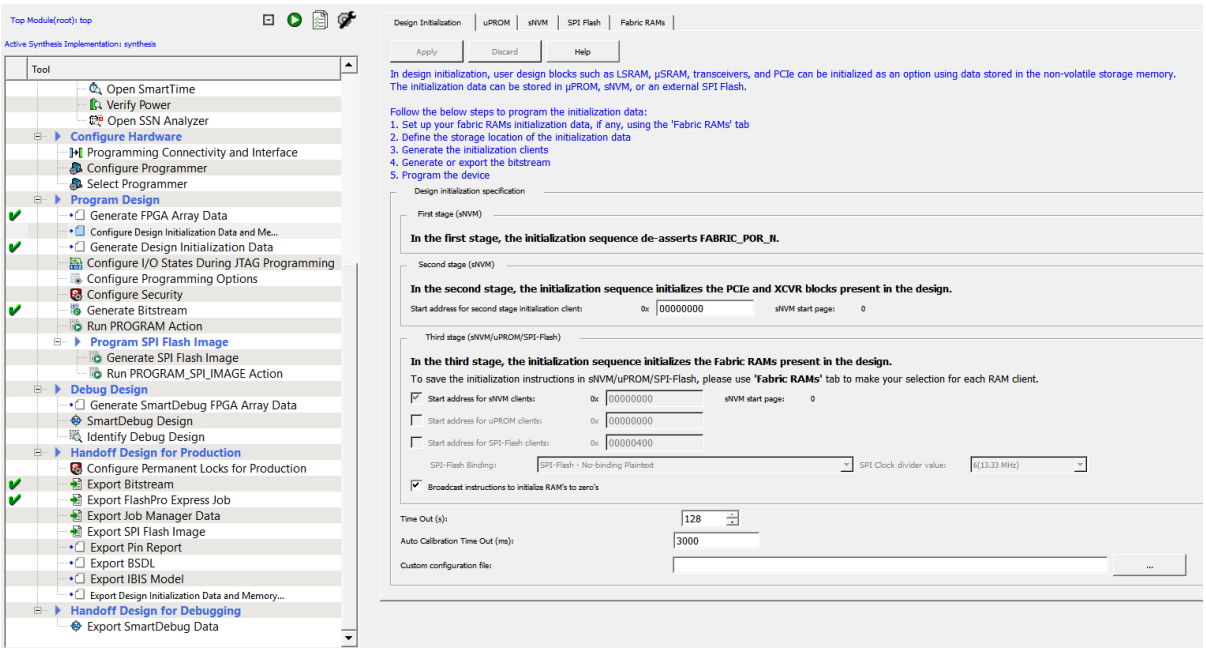
The **Configure Design Initialization Data and Memories** option generates the LSRAM initialization client and adds it to sNVM, µPROM, or an external SPI Flash, based on the type of nonvolatile memory selected. In this demo, the LSRAM initialization client is stored in the sNVM.

This process requires the user application executable file (hex file) to initialize the LSRAM blocks on device power-up. The hex file (`CPRI_config.hex`) is available in the `DesignFiles_Directory\mpf_an4949_v2022p3_df\Libero_Project` folder. When the hex file is imported, a memory initialization client is generated for LSRAM blocks.

To initialize the memory, perform the following steps:

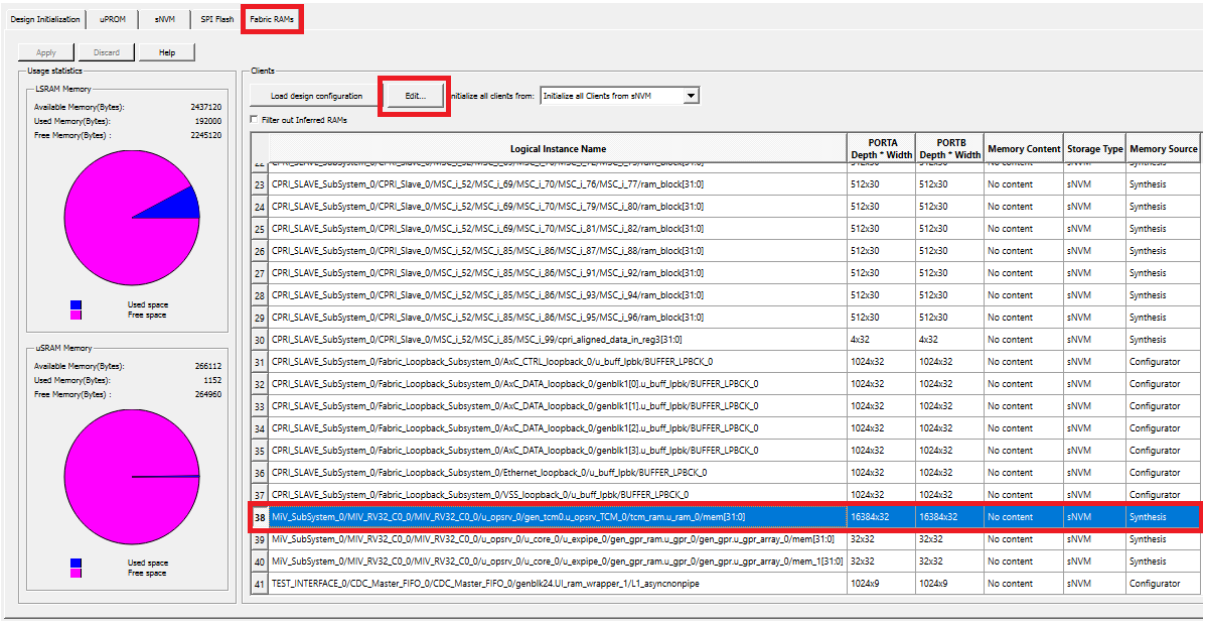
1. On the **Design Flow** window, double-click **Configure Design Initialization Data and Memories**. The **Design and Memory Initialization** window opens.

Figure 9-5. Design and Memory Initialization Window



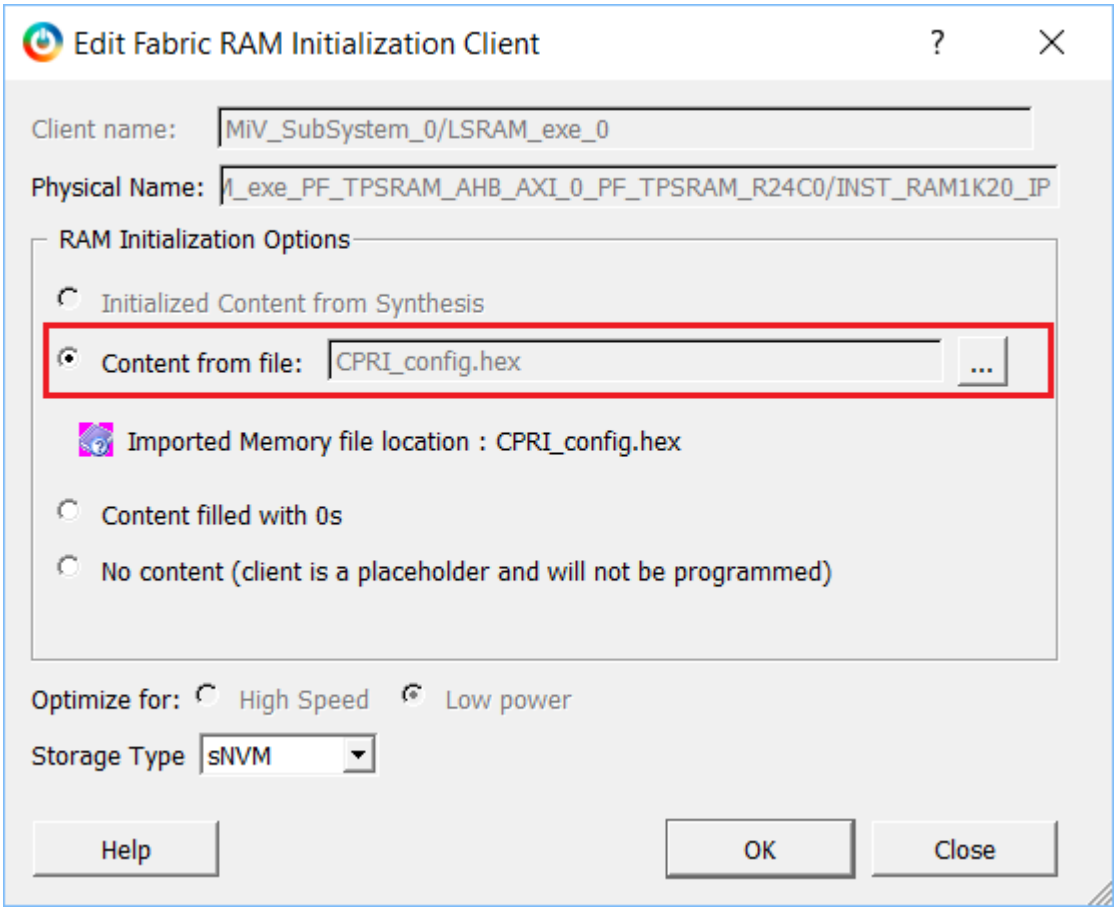
2. In the **Fabric RAM**s tab, select the LSRAM client from the list, and then click **Edit**.

Figure 9-6. Fabric RAM



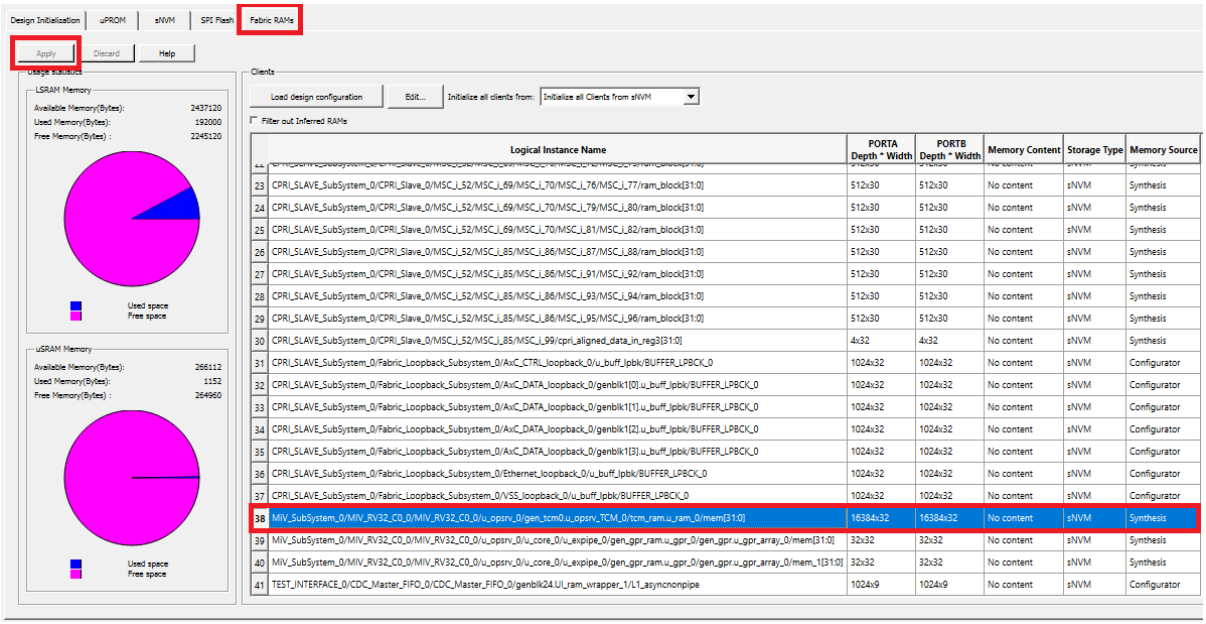
3. In the **Edit Fabric RAM Initialization Client** dialog box, select the **Content from file** option, and locate the `CPRI_config.hex` file from `DesignFiles_directory\mpf_an4949_v2022p3_df\Libero_Project` folder, and then click **OK**.

Figure 9-7. Edit Fabric RAM Initialization Client



4. Click **Apply**.

Figure 9-8. Design Initialization



5. To generate design initialization data, click **Generate Initialization Data** on the **Design Flow** window. After successful generation of the **Initialization** data, a green tick mark appears next to **Generate Initialization Data** option. See Figure 9-8.

9.5 Generate Bitstream (Ask a Question)

To generate bitstream, perform the following steps:

1. On the **Design Flow** window, double-click **Generate Bitstream**. When the bitstream is successfully generated, a green tick mark appears next to **Generate Bitstream**. See Figure 9-1.
2. Right-click **Generate Bitstream** and select **View Report** to view the corresponding log file in the **Reports** tab.

9.6 Run Program Action (Ask a Question)

To program the PolarFire device, perform the following steps:

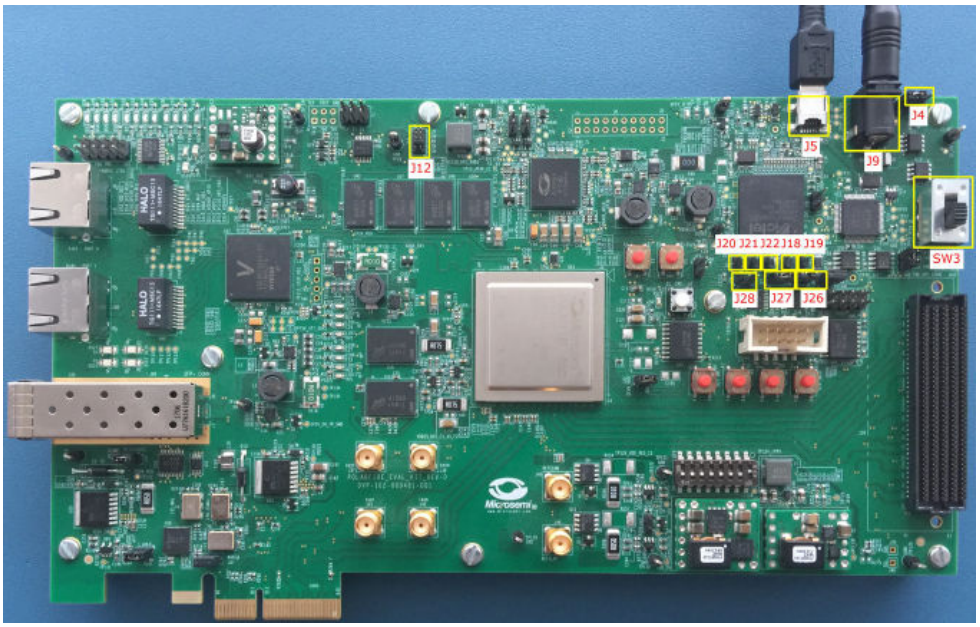
1. Ensure that the jumper settings on the board are as listed in the following table.

Table 9-3. PolarFire® Evaluation Board Jumper Settings

Jumper	Description
J18, J19, J20, J21, and J22	Short pin 2 and 3 for programming the PolarFire® FPGA through FTDI
J28	Short the pin 2 and 3 for programming through the on-board FlashPro5
J4	Short pin 1 and 2 for manual power switching using SW3
J12	Short pin 3 and 4 for 2.5V
J46	Short pin 1 and 2 for routing 125 MHz differential clock oscillator output to the side. Open pin 1 and 2 for routing 122.88 MHz differential clock oscillator to the line side.

2. Connect the power supply cable to the J9 connector.
3. Connect the USB cable from the host PC to the J5 (FTDI port).
4. Power **ON** the board using the SW3 slide switch.
   The following figure shows the board setup.

Figure 9-9. PolarFire® Evaluation Board Setup



5. On the **Design Flow** window, double-click **Run PROGRAM Action**.

The device is successfully programmed and a green tick mark appears next to **Run PROGRAM Action**, see Figure 9-1. LED 4 is asserted once the device is programmed.

10. Running the Demo (Ask a Question)

This section describes how to install and use the CPRI Demo application Graphic User Interface (GUI). The PolarFire CPRI demo application is a simple GUI that runs on the host PC to communicate with the PolarFire Device.

10.1 Installing CPRI Demo Application (Ask a Question)

To install CPRI demo application, perform the following step:

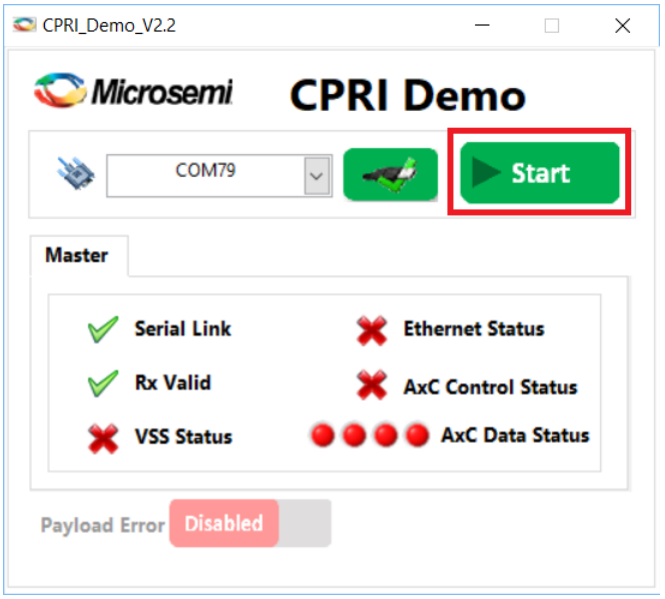
1. Install the GUI (`setup.exe`) from the following design files folder `mpf_an4949_v2022p3_df/GUI`.

The following steps describes how to install and use the GUI to run the CPRI Loopback demo. The following procedure assumes that the PolarFire evaluation board is connected and programmed with the CPRI Loopback design.

To run the CPRI Loopback demo, perform the following steps:

1. Extract the contents of the `mpf_an4949_v2022p3_df.zip` file.
2. From the `mpf_an4949_v2022p3_df\GUI\GUI Installer` folder, double-click the `setup.exe` file.
3. Follow the instructions displayed on the installation window.
4. After successful installation, **CPRI_GUI** appears on the **Start** menu of the host PC desktop.
5. From the **Start** menu, click **CPRI_GUI** to launch the application.
6. The GUI detects the COM port number and automatically connects to the board. The following figure shows COM port number and connection status. COM Port numbers may vary.

Figure 10-1. Selecting COM Port and Connecting Status

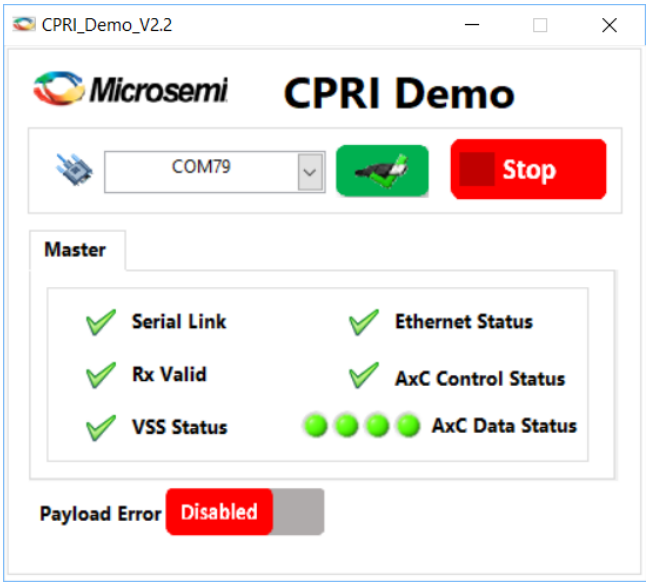


7. Click **Start**. The data is generated and framed using the CPRI master module and sent over the serial transmit link. It is then received by the receiver, and CPRI slave IP unpacks the data and loopbacks the data to the CPRI master module. The checker in the master system checks the incoming data for any errors. The status is monitored using the status signals on the GUI at any time. The following are the status signals:
   - Serial Link: Indicates transceiver link status

- Rx Valid: Indicates if the transmitter and receiver data are locked
- VSS status: Indicates the received VSS data is valid.
- Ethernet status: Indicates the received Ethernet data is valid.
- AxC Control status: Indicates the received Antenna carrier control data is valid.
- AxC Data Status: Indicates the received Antenna carrier data is valid.

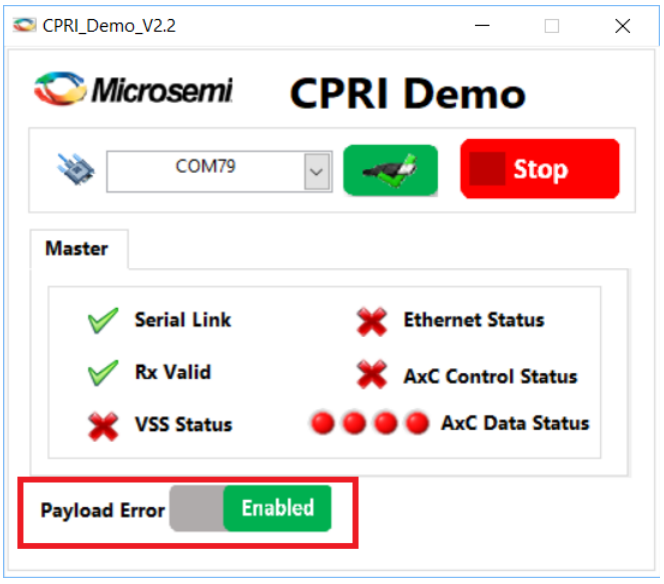
The following figure shows the status signals. The LED 4, LED 5, LED 6, LED 7, LED 8, LED 9, LED 10, and LED 11 are asserted at the same time.

Figure 10-2. Master Checker Status—Pass



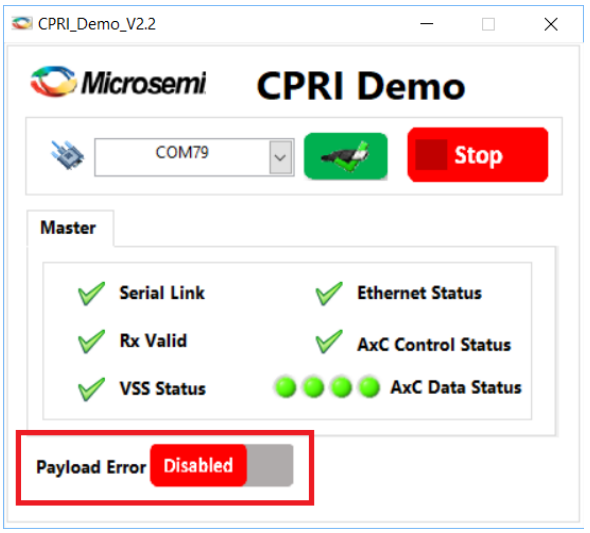
8. Click **Payload Error** to induce error in VSS data, Ethernet data, Antenna carrier control data, and Antenna carrier data. Observe the error status of **Master** tab. See the following figure. The LED 5, LED 6, LED 7, LED 8, LED 9, LED 10, and LED 11 are deasserted at the same time.

Figure 10-3. Payload Error Enabled—Master



9. Disable **Payload Error** to stop generating an error and observe that the Serial Link, Rx Valid, and all the status signals of **Master** turn green. See the following figure. When the error is cleared, the LED 5 to LED 11 is asserted at the same time.

Figure 10-4. Payload Error Disabled—Master



The CPRI demo is successfully run.

11. Appendix 1: Programming the Device Using FlashPro Express (Ask a Question)

This chapter describes how to program the PolarFire device with the Job programming file using a FlashPro programmer. The default location of the `.stp` file is `mpf_an4949_v2022p3_df\Programming_Job`.

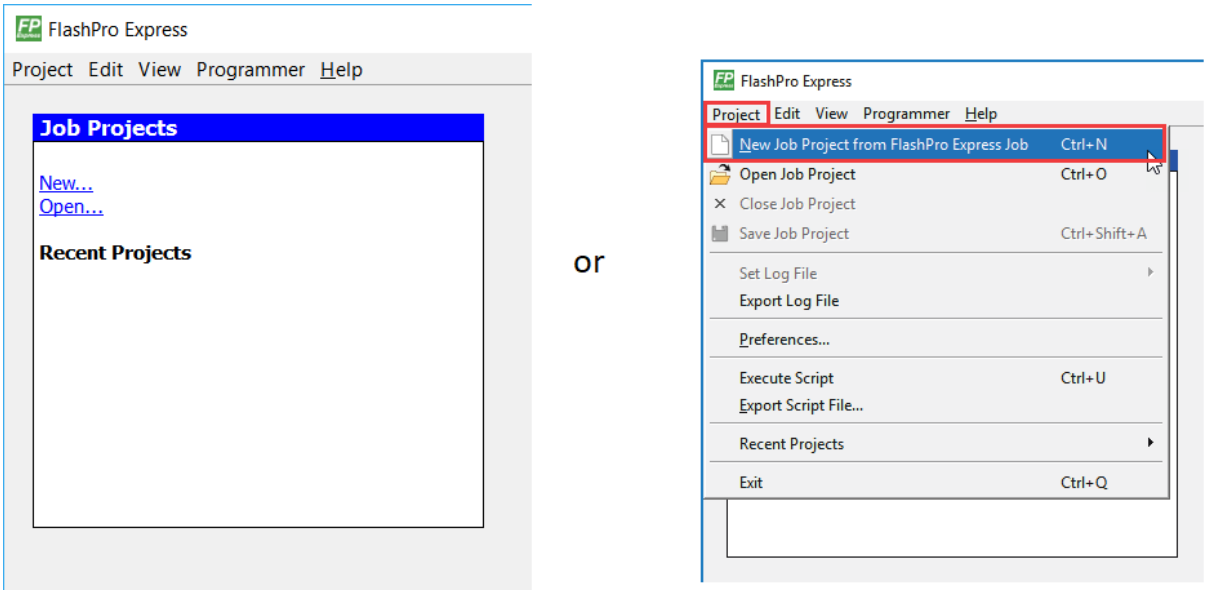
To program the PolarFire device using FlashPro Express, perform the following steps:

1. Ensure that the jumper settings on the board are the same as listed in Table 9-3.

> **Tip:** The power supply switch must be switched **OFF** while making the jumper connections.

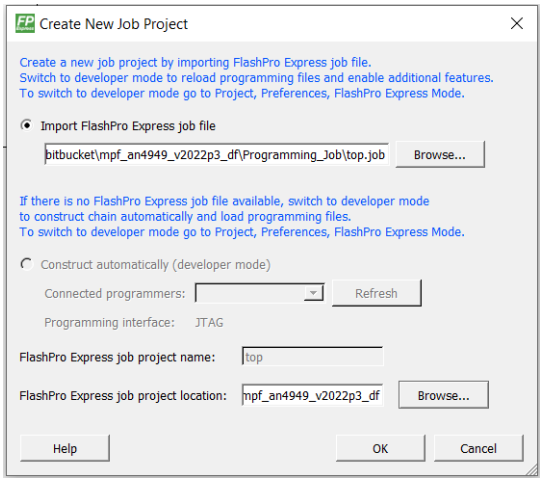
2. Connect the power supply cable to the **J9** connector on the board.
3. Connect the USB cable from the Host PC to the **J5** (FTDI port) on the board.
4. Power on the board using the **SW3** slide switch.
5. On the host PC, launch the FlashPro Express software.
6. Click **New** or select **New Job Project** from **FlashPro Express Job** from **Project** menu to create a new job project. See the following figure.

Figure 11-1. FlashPro Express Job Project



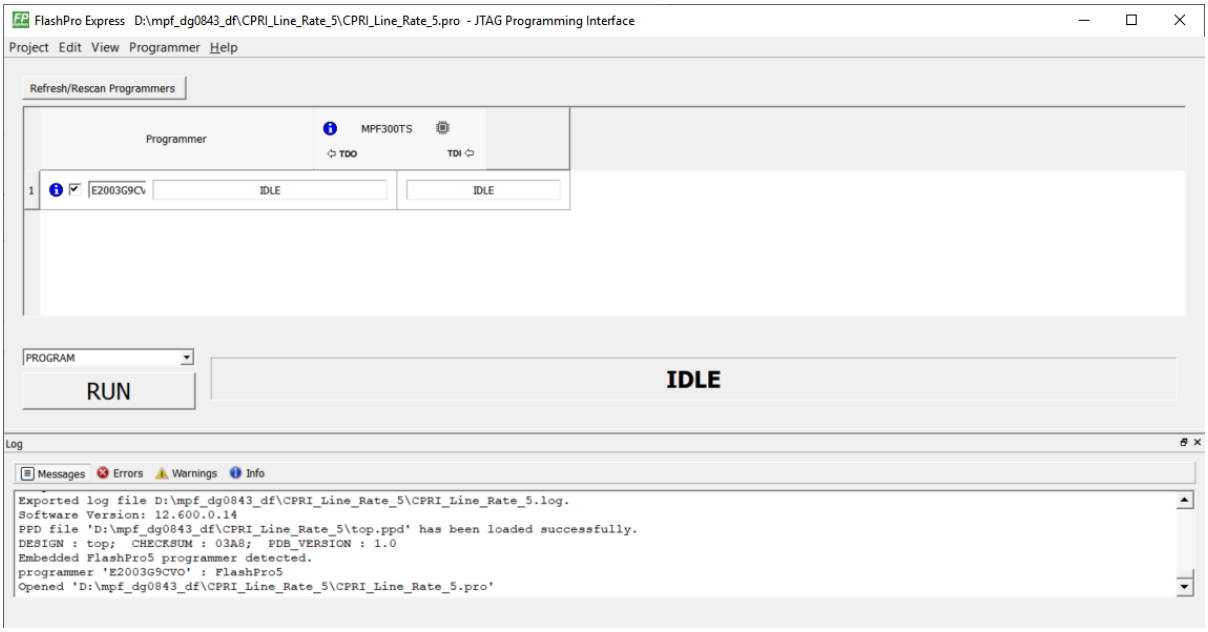
7. Enter the following in the **New Job Project** from FlashPro Express Job dialog box:
   - **Programming job file**: Click **Browse**, and navigate to the location where the `.job` file is located and select the file. The default location is `<download_folder>\mpf_an4949_v2022p3_df\Programming_Job`.
   - **FlashPro Express job project location**: Click **Browse** and navigate to the location where you want to save the project.

Figure 11-2. New Job Project from FlashPro Express Job



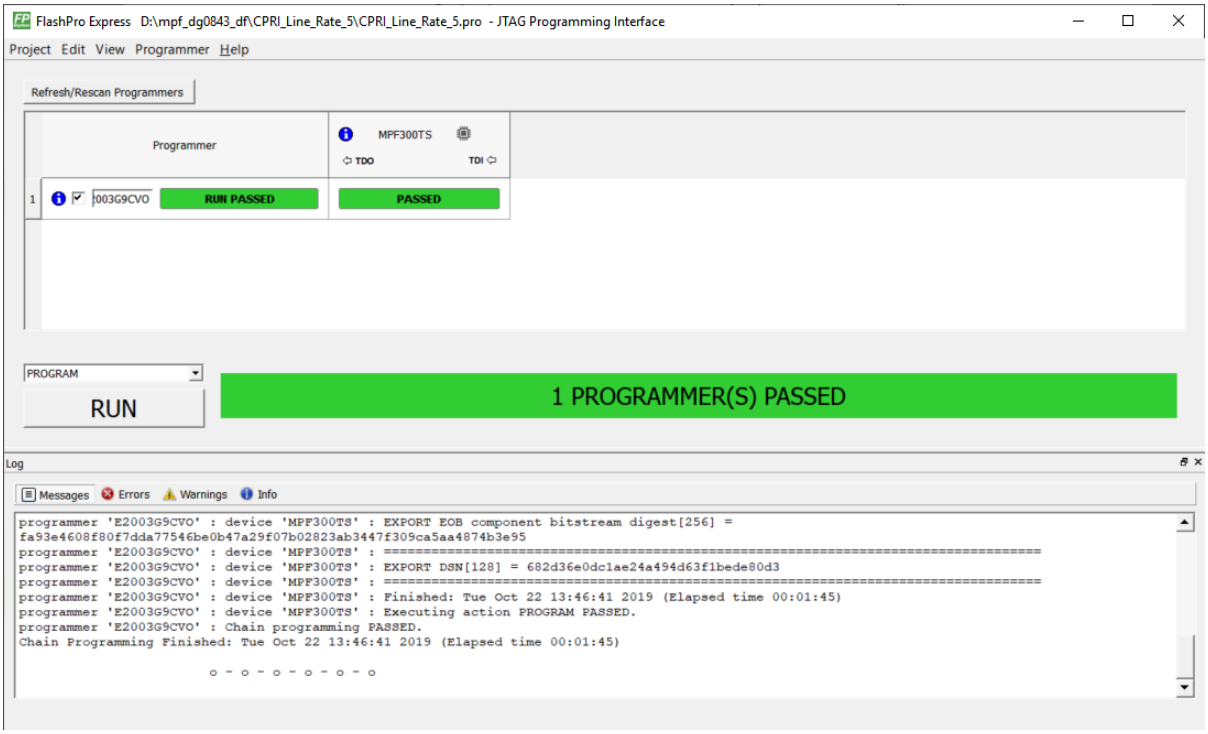
8. Click **OK**. The required programming file is selected and ready to be programmed in the device.
9. The FlashPro Express window appears. Confirm that a programmer number appears in the Programmer field. If it does not, confirm the board connections and click **Refresh/Rescan** Programmers.

Figure 11-3. Programming the Device



10. Click **RUN**. When the device is programmed successfully, a **RUN PASSED** status is displayed.

Figure 11-4. FlashPro Express—RUN PASSED



11. Close **FlashPro Express** or in the **Project** tab, click **Exit**.

12. Appendix 2: Running the TCL Script (Ask a Question)

TCL scripts are provided in the design files folder under directory `TCL_Scripts`. If required, the design flow can be reproduced from Design Implementation till generation of job file.

Following are the steps to run the TCL:

1. Launch the Libero software
2. Select **Project** > **Execute Script**
3. Click **Browse** and select `script.tcl` from the downloaded `TCL_Scripts` directory.
4. Click **Run**.

After successful execution of TCL script, Libero project is created within `TCL_Scripts` directory.

For more information about TCL scripts, see `mpf_an4949_v2022p3_df/TCL_Scripts/readme.txt`.

For more details on TCL commands, see Tcl Commands Reference Guide. Contact Technical Support for any queries encountered when running the TCL script.

13. Appendix 3: References (Ask a Question)

This section lists the documents that provide more information about the concepts and features covered in this demo guide.

- For more information about PolarFire transceiver blocks, see PolarFire Family Transceiver User Guide.
- For more information about Libero, ModelSim, and Synplify, see Libero SoC v12.0 and later.
- For more information about CPRI IP, see **Libero Catalog** > **Solution-Wireless** > **Microchip CPRI User Guide**.
- For more information about PolarFire Evaluation kit, see UG0747: PolarFire FPGA Evaluation Kit User Guide.
- For more information about Power-Up and Reset, see PolarFire Family Power-Up and Resets User Guide.
- For more information about the CoreJTAGDEBUG IP core, see CoreJTAGDebug from **Libero** > **Catalog**.
- For more information about the MIV_RV32 IP core, see MIV_RV32 from the **Libero SoC Catalog**.
- For more information about the CoreUARTapb IP core, see CoreUARTapb.
- For more information about the CoreAHBLite IP core, see CoreAHBLite.
- For more information about the CoreAPB3 IP core, see CoreAPB3.
- For more information about the CoreGPIO IP core, see CoreGPIO.

14. Revision History (Ask a Question)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 14-1. Revision History

Revision	Date	Description
A	05/2023	The following is a summary of the changes made in this revision A. • The document was migrated to the Microchip template. The document number was updated to DS00004949 from 50200843. • The document ID was updated to AN4949 from DG0843. • Updated the document for Libero® v2022.3. • Updated design filepath and `.job` throughout the document.
4.0	—	Added 12. Appendix 2: Running the TCL Script.
3.0	—	The following is a summary of the changes made in this revision. • Updated the document for Libero SoC v12.2. • Removed the references to Libero version numbers.
2.0	—	Updated the document for Libero SoC v12.0.
1.0	—	The first publication of this document.

Microchip FPGA Support (Ask a Question)

Microchip FPGA products group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, and worldwide sales offices. Customers are suggested to visit Microchip online resources prior to contacting support as it is very likely that their queries have been already answered.

Contact Technical Support Center through the website at www.microchip.com/support. Mention the FPGA Device Part number, select appropriate case category, and upload design files while creating a technical support case.

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

- From North America, call **800.262.1060**
- From the rest of the world, call **650.318.4460**
- Fax, from anywhere in the world, **650.318.8044**

Microchip Information (Ask a Question)

The Microchip Website (Ask a Question)

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service (Ask a Question)

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support (Ask a Question)

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Microchip Devices Code Protection Feature (Ask a Question)

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Legal Notice (Ask a Question)

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks (Ask a Question)

The Microchip name and logo, the Microchip logo, Adaptec, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet- Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, TrueTime, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, Clockstudio, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic

ISBN: 978-1-6683-2477-6

Quality Management System (Ask a Question)

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office	**Australia - Sydney**	**India - Bangalore**	**Austria - Wels**
2355 West Chandler Blvd.	Tel: 61-2-9868-6733	Tel: 91-80-3090-4444	Tel: 43-7242-2244-39
Chandler, AZ 85224-6199	**China - Beijing**	**India - New Delhi**	Fax: 43-7242-2244-393
Tel: 480-792-7200	Tel: 86-10-8569-7000	Tel: 91-11-4160-8631	**Denmark - Copenhagen**
Fax: 480-792-7277	**China - Chengdu**	**India - Pune**	Tel: 45-4485-5910
Technical Support:	Tel: 86-28-8665-5511	Tel: 91-20-4121-0141	Fax: 45-4485-2829
www.microchip.com/support	**China - Chongqing**	**Japan - Osaka**	**Finland - Espoo**
Web Address:	Tel: 86-23-8980-9588	Tel: 81-6-6152-7160	Tel: 358-9-4520-820
www.microchip.com	**China - Dongguan**	**Japan - Tokyo**	**France - Paris**
Atlanta	Tel: 86-769-8702-9880	Tel: 81-3-6880- 3770	Tel: 33-1-69-53-63-20
Duluth, GA	**China - Guangzhou**	**Korea - Daegu**	Fax: 33-1-69-30-90-79
Tel: 678-957-9614	Tel: 86-20-8755-8029	Tel: 82-53-744-4301	**Germany - Garching**
Fax: 678-957-1455	**China - Hangzhou**	**Korea - Seoul**	Tel: 49-8931-9700
Austin, TX	Tel: 86-571-8792-8115	Tel: 82-2-554-7200	**Germany - Haan**
Tel: 512-257-3370	**China - Hong Kong SAR**	**Malaysia - Kuala Lumpur**	Tel: 49-2129-3766400
Boston	Tel: 852-2943-5100	Tel: 60-3-7651-7906	**Germany - Heilbronn**
Westborough, MA	**China - Nanjing**	**Malaysia - Penang**	Tel: 49-7131-72400
Tel: 774-760-0087	Tel: 86-25-8473-2460	Tel: 60-4-227-8870	**Germany - Karlsruhe**
Fax: 774-760-0088	**China - Qingdao**	**Philippines - Manila**	Tel: 49-721-625370
Chicago	Tel: 86-532-8502-7355	Tel: 63-2-634-9065	**Germany - Munich**
Itasca, IL	**China - Shanghai**	**Singapore**	Tel: 49-89-627-144-0
Tel: 630-285-0071	Tel: 86-21-3326-8000	Tel: 65-6334-8870	Fax: 49-89-627-144-44
Fax: 630-285-0075	**China - Shenyang**	**Taiwan - Hsin Chu**	**Germany - Rosenheim**
Dallas	Tel: 86-24-2334-2829	Tel: 886-3-577-8366	Tel: 49-8031-354-560
Addison, TX	**China - Shenzhen**	**Taiwan - Kaohsiung**	**Israel - Ra'anana**
Tel: 972-818-7423	Tel: 86-755-8864-2200	Tel: 886-7-213-7830	Tel: 972-9-744-7705
Fax: 972-818-2924	**China - Suzhou**	**Taiwan - Taipei**	**Italy - Milan**
Detroit	Tel: 86-186-6233-1526	Tel: 886-2-2508-8600	Tel: 39-0331-742611
Novi, MI	**China - Wuhan**	**Thailand - Bangkok**	Fax: 39-0331-466781
Tel: 248-848-4000	Tel: 86-27-5980-5300	Tel: 66-2-694-1351	**Italy - Padova**
Houston, TX	**China - Xian**	**Vietnam - Ho Chi Minh**	Tel: 39-049-7625286
Tel: 281-894-5983	Tel: 86-29-8833-7252	Tel: 84-28-5448-2100	**Netherlands - Drunen**
Indianapolis	**China - Xiamen**		Tel: 31-416-690399
Noblesville, IN	Tel: 86-592-2388138		Fax: 31-416-690340
Tel: 317-773-8323	**China - Zhuhai**		**Norway - Trondheim**
Fax: 317-773-5453	Tel: 86-756-3210040		Tel: 47-72884388
Tel: 317-536-2380			**Poland - Warsaw**
Los Angeles			Tel: 48-22-3325737
Mission Viejo, CA			**Romania - Bucharest**
Tel: 949-462-9523			Tel: 40-21-407-87-50
Fax: 949-462-9608			**Spain - Madrid**
Tel: 951-273-7800			Tel: 34-91-708-08-90
Raleigh, NC			Fax: 34-91-708-08-91
Tel: 919-844-7510			**Sweden - Gothenberg**
New York, NY			Tel: 46-31-704-60-40
Tel: 631-435-6000			**Sweden - Stockholm**
San Jose, CA			Tel: 46-8-5090-4654
Tel: 408-735-9110			**UK - Wokingham**
Tel: 408-436-4270			Tel: 44-118-921-5800
Canada - Toronto			Fax: 44-118-921-5820
Tel: 905-695-1980			
Fax: 905-695-2078			