ER0217

Device Status and Errata

PolarFire FPGA Pre-Production Devices

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Microsemi

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Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.0

Revision 4.0 was published in December 2018. The following is a summary of changes.

- Added MPF500 updates. Updated table Supported Transceiver Protocols.

1.2 Revision 3.0

Revision 3.0 was published in August 2018. The following is a summary of changes.

- Added MPF100 updates.

1.3 Revision 2.0

Revision 2.0 was published in July 2018. The following is a summary of changes.

- Added MPF300 updates and MPF200 columns to transceiver and memory tables. For more information, see tables Supported Transceiver Protocols, MPF200 Supported Memory Standards, and MPF300 Supported Memory Standards.

1.4 Revision 1.0

Revision 1.0 was published in June 2018. It was the first publication of this document.

2 Overview

The PolarFire® MPF100T, MPF200T, MPF300T, and MPF500T pre-production (PP) FPGA devices are subject to the limitations described in this document. Pre-production devices are final silicon devices that are shipped to a pre-production test flow. These devices are expected to behave identical to production devices but are not to be used for qualified production systems. This document contains updated information about any known issues and provides the available limitations and workarounds. It provides a snapshot of the current validation status for feature sets. The document highlights dependencies that may exist between silicon device revisions and specific support by Libero® PolarFire SoC software versions. Contact Microsemi Technical Support at soc_tech@microsemi.com for more information.

2.1 Device Revisions

The following table lists the device revisions and package offerings listed, if not specified. These represent the devices covered by this document.

Table 1 • Sample Revisions Released per Device

Devices	Packages	Revisions
MPF100T, TL, TS, TLS	FCG484, FCVG484, and FCSG325	0
MPF200T, TL, TS, TLS	FCG784, FCG484, FCVG484, FCSG536, and FCSG325	0
MPF300T, TL, TS, TLS	FCG1152, FCG784, FCG484, FCVG484, and FCSG536	0
MPF500T, TL, TS, TLS	FCG1152 and FCG784	0

The following table lists the PolarFire FPGA device options for the MPF100T, MPF200T, MPF300T, and MPF500T pre-production offering.

Table 2 • PolarFire FPGA Device Options

Options	Extended Commercial 0 °C–100 °C	Industrial –40 °C– 100 °C	STD	–1	Transceivers T	Lower Static Power L	Data Security S
MPF100T, MPF200T, MPF300T, and MPF500T	Yes	Yes	Yes	Yes	Yes	N/A	N/A
MPF100T, MPF200TL, MPF300TL, and MPF500TL	Yes	Yes	Yes		Yes	Yes	
MPF100T, MPF200TS, MPF300TS, and MPF500TS		Yes	Yes	Yes	Yes		Yes
MPF100T, MPF200TLS, MPF300TLS, and MPF500TLS		Yes	Yes		Yes	Yes	Yes

For specifications, see DS0141: PolarFire FPGA Datasheet.

The following table lists the operating conditions for the PolarFire pre-production (PP) devices only. The operating conditions for production devices follow datasheet specifications (see DS0141: PolarFire FPGA Datasheet).

Table 3 • PolarFire Pre-Production Operating Conditions

Operation Temperature Range	Retention Lifetime
–40 °C to 100 °C (Industrial)	1 year

2.2 PCB Designs

For information on how to determine proper signal pinout, see UG0726: PolarFire FPGA Board Design User Guide. The proper signal pinout is required for all clocking, transceiver, and FPGA pin recommendations.

3 Errata Descriptions and Workarounds

The following sections provide a description of device errata and the workarounds wherever applicable. The following table lists the specific device erratas and the affected PolarFire production devices.

Table 4 • Summary of PolarFire FPGA Errata

Description	MPF100T , TL, TS, TLS	MPF200T , TL, TS, TLS	MPF300T, TL, TS, TLS	MPF500T , TL, TS, TLS
Bitstream compatibility	N/A	N/A	*	N/A
GPIO IOCDR SGMII only supports 0 ppm clocking	*	*	*	*
Incorrect transceiver RXPLL behavior /LANEx_RX_READY pin behavior	*	*	*	*
IBIS-AMI RX simulation model limitations	*	*	*	*
LPDDR3 electrical compliance limit	*	*	*	*
GPIO/HSIO glitches dependent on power supply sequences	*	*	*	*
JTAG TCK duty cycle deviates from datasheet specifications	*	*	*	*
Automated decision feedback equalizer (DFE) support (contact Microsemi)	*	*	*	*
Mutli-lane IO CDR limitation	*	*	*	*
IBIS models for LVDS outputs shows common mode drift	*	*	*	*
MIPI D-PHY support (contact factory)	*	*	*	*
Unsupported Features				
Device zeroization	*	*	X	*
Digest check	*	*	*	*
Feature Clarifications				
Supported transceiver protocols	For more information, see the Supported Transceiver Protocol Statuses.			
Supported memory standards	For more information, see the Supported Memory Standards.			

Note: * indicates that the errata exists for that particular device and revision number.

Note: X indicates that the errata is removed and no longer exists for that particular device and revision number (based on additional details).

3.1 Bitstream Compatibility

MPF300T-ES bitstreams cannot be used to program MPF300T-PP devices.

3.2 GPIO IOCDR SGMII Only Supports 0 ppm Clocking

IOD CDR interfaces cannot be used with a >0 ppm offset. For SGMII, the PHY device and PolarFire IOD CDR must use the same reference clock. SGMII interfaces using transceivers are not affected by this limitation. SGMII can be implemented with IOCDR using 0 ppm or a common clock using the same clock configuration for both Tx and Rx clocks. The device can manage 300 ppm operation; however, 300 ppm support is planned for a future software update.

3.3 Incorrect Transceiver RXPLL Behavior/LANEx_RX_READY Pin Behavior

The transceiver LANEx_RX_READY pin toggles when the Rx signal is open or disconnected, or while an out-of-range condition occurs. For example, incorrect Rx serial data rates, with serial input data >1.17% away, is considered out of range. Initially, the Rx CDR lock may not lock with missing or bad data stream.

The following conditions prevent the incorrect behavior.

- The Rx data rate is <±300 ppm of the Libero configured rate.
- Rx data is present when PMA_ARST is de-asserted.
- Data stream must not stop once locked.
- PMA_ARST can be used to restart.

Contact Microsemi Technical Support at soc_tech@microsemi.com for a workaround.

3.4 IBIS-AMI RX Simulation Model Limitations

Production IBIS-AMI simulation modeling is supported.

- TX IBIS-AMI model is full featured.
- RX IBIS-AMI model is CTLE only. For DFE support, contact factory.
  IBIS-AMI models are available online at IBIS Models: PolarFire.

3.5 GPIO/HSIO Glitches Dependent on Power Supply Sequences

The following sections describe GPIO and HSIO glitches dependent on power supply sequences.

3.5.1 GPIO

A glitch on GPIO can occur with VDDI = 1.8 V and 1.5 V modes when VDDI ramps up before VDDAUX regardless of ramp times. The issue can be avoided by bringing up VDDAUX before VDDI.

A glitch on GPIO can occur with VDDI = 1.8 V and 1. 5 V modes when VDDAUX ramps down before VDDI regardless of ramp times. The issue can be avoided by bringing down VDDI before VDDAUX.

GPIO requires 100-kΩ external pulldown resistor on pins requiring glitch immunity if power sequence mentioned above cannot be met.

In all mentioned GPIO cases above, VDD must reach its minimum trip point before VDDI and VDDAUX or an external pulldown resistor is required.

3.5.2 HSIO

A glitch on HSIO can occur with the following power sequence: VDD, then VDD18, then VDDI. In this case, HSIO requires a 100-kΩ external pulldown resistor on pins requiring glitch immunity.

3.6 LPDDR3 Electrical Compliance Limited

LPDDR3 electrical compliance per the JEDEC JESD79-3E and JESD79-3-1 DDR3 SDRAM specifications is not completely optimized with designs implemented in the Libero software. This impacts the electrical compliance test measurements and does not impact inter-operation with LPDDR3 memory devices. Optimized support is planned for a future Libero release.

3.7 JTAG TCK Input Duty Cycle

The minimum and maximum specifications for JTAG TCK input duty cycle require a 45%/55% duty cycle at 25 MHz.

3.8 Automated DFE Calibration

To initiate automated DFE calibration, please contact Microsemi Technical Support at soc_tech@microsemi.com.

3.9 Mutli-lane IO CDR Limitation

Multi-lane IO CDR (GPIO) designs requiring master/slave clocking is not supported with current solutions.

3.10 IBIS Models for LVDS Outputs Show Common Mode Drift

The initial common mode of LVDS output drivers has drift from 1.2 V to 0.875 V, though there is no change in the differential voltage. This is only a modeling issue and not observed by the actual device. Users should ignore the common mode drift and only look for the differential swing behavior of the model.

3.11 MIPI D-PHY Support

PolarFire supports MIPI D-PHY with MIPI25 and MIPIE25 IO types as well as IO digital functionality. Contact the factory for performance and solutions details.

3.12 Unsupported Features

The following features are not supported in PolarFire pre-production devices.

- Device zeroization
- Digest check

4 Supported Transceiver Protocol Statuses

Transceiver protocol capabilities are validated and tested for robustness as per the specifications listed in the DS0141: PolarFire FPGA Datasheet and UG0677: PolarFire FPGA Transceiver User Guide.

The following table summarizes the transceiver protocols and the validation states for PolarFire pre-production devices.

Table 5 • Supported Transceiver Protocols

Transceiver Protocol by Device	MPF100T/MPF200T /MPF300T/MPF500T Status	Details
SGMII/1000BASE-X	Complete	Transceiver: 1.25 Gbps with CoreTSE IP core TxPLL SyncE is supported
CPRI	Complete	Support for CPRI data rates 1–7 and 7A
CPRI8-9	In-Progress	
10GBASE-R	Complete	Transceiver: 10.3125 Gbps with Core10GMAC IP core TxPLL SyncE is supported IEEE 1588 time stamping is not supported
10GBASE-KR	Complete	Contact Microsemi for complete solution
Interlaken	Complete	
JESD204B	Complete	Up to 10G with CoreJESD20BTX/RX IP core
JESD204B at 12.5 Gbps	Complete	Contact Microsemi for complete solution
PCIE Endpoint Gen1/Gen2	Complete	
PCIE Rootport Gen1/Gen2	Complete	
LiteFast	Complete	Up to 5 Gbps
XAUI	Complete	
RXAUI	Complete	
HiGig/HiGig+	In-Progress	Contact Microsemi for complete solution
Display port	Complete	Per VESA DisplayPort Standard 1.2a
SRIO	Complete	
PMA only	Complete	
SATA	In-Progress	Contact Microsemi for complete solution
Fiber channel	In-Progress	Contact Microsemi for complete solution
SDI	In-Progress	HD-SDI (1.485 Gbps) and 3G-SDI (2.970 Gbps) are supported SD-SDI (270 Mbps) is in progress 6G-SDI and 12G-SDI are planned
OTN	Complete	Tested for electrical compliance

5 Supported Memory Standards

This following table describes PolarFire memory interface capabilities for the pre-production devices that deviate from the specifications published in the DS0141: PolarFire FPGA Datasheet and UG0676: PolarFire FPGA DDR Memory Controller User Guide.

The data rates for the various memory controller bus widths are listed as follows. The reduced performance for wider data bus widths are not a limitation of the pre-production devices and will be improved in subsequent Libero releases.

Table 6 • MPF100 Supported Memory Standards

Package	IO Type	Edge_ Anchor[1]	Memory Type	Maximum Interface Width vs. Performance					
				Interface Width (Max)	STD (Mbps)	–1 (Mbps)	Interface Width (Max)	STD (Mbps)	–1 (Mbps)
FCG484	HSIO	NORTH_NE	DDR3	40	1066	1066	8	1066	1333
FCG484	HSIO	NORTH_NE	DDR4	40	1333	1333	8	1333	1600
FCG484	HSIO	NORTH_NE	LPDDR3[2]	32	1066	1333	16	1066	1333
FCG484	HSIO	NORTH_NW	DDR3	40	1066	1066	8	1066	1333
FCG484	HSIO	NORTH_NW	DDR4	40	1333	1333	8	1333	1600
FCG484	HSIO	NORTH_NW	LPDDR3[2]	32	1066	1333	16	1066	1333
FCG484	GPIO	SOUTH_SW	DDR3	32	800	800	N/A	N/A	N/A
FCG484	GPIO	WEST_SW_OPT	DDR3	16	800	800	N/A	N/A	N/A
FCSG325	HSIO	NORTH_NE	DDR3	32	1066	1066	8	1066	1333
FCSG325	HSIO	NORTH_NE	DDR4	32	1333	1333	8	1333	1600
FCSG325	HSIO	NORTH_NE	LPDDR3[2]	32	1066	1333	16	1066	1333
FCSG325	HSIO	NORTH_NW	DDR3	32	1066	1066	N/A	N/A	N/A
FCSG325	HSIO	NORTH_NW	DDR4	32	1333	1333	N/A	N/A	N/A
FCSG325	HSIO	NORTH_NW	LPDDR3[2]	32	1066	1333	N/A	N/A	N/A
FCSG325	GPIO	SOUTH_SW	DDR3	8	800	800	8	800	800
FCVG484	HSIO	NORTH_NE	DDR3	40	1066	1066	16	1066	1333
FCVG484	HSIO	NORTH_NE	DDR4	40	1333	1333	16	1333	1600
FCVG484	HSIO	NORTH_NE	LPDDR3[2]	32	1066	1333	16	1066	1333
FCVG484	HSIO	NORTH_NW	DDR3	40	1066	1066	16	1066	1333
FCVG484	HSIO	NORTH_NW	DDR4	40	1333	1333	16	1333	1600
FCVG484	HSIO	NORTH_NW	LPDDR3[2]	32	1066	1333	16	1066	1333
FCVG484	GPIO	SOUTH_SW	DDR3	40	800	800	N/A	N/A	N/A
FCVG484	GPIO	WEST_NW	DDR3	16	800	800	N/A	N/A	N/A
FCVG484	GPIO	WEST_SW_OPT	DDR3	16	800	800	N/A	N/A	N/A

1. See the Package Pin Assignment Tables (PPAT) for information regarding anchor locations.
2. See LPDDR3 electrical compliance errata item.
3. Interface widths <16 are supported for DDR-PHY-only applications.

Table 7 • MPF200 Supported Memory Standards

Package	IO Type	Edge_ Anchor[1]	Memory Type	Maximum Interface Width vs. Performance					
				Interface Width (Max)	STD (Mbps)	–1 (Mbps)	Interface Width (Max)	STD (Mbps)	–1 (Mbps)
FCG484	HSIO	NORTH_NE	DDR3	40	1066	1066	8	1066	1333
FCG484	HSIO	NORTH_NE	DDR4	40	1333	1333	8	1333	1600
FCG484	HSIO	NORTH_NE	LPDDR3[2]	32	1066	1333	16	1066	1333
FCG484	HSIO	NORTH_NW	DDR3	40	1066	1066	8	1066	1333
FCG484	HSIO	NORTH_NW	DDR4	40	1333	1333	8	1333	1600
FCG484	HSIO	NORTH_NW	LPDDR3[2]	32	1066	1333	16	1066	1333
FCG484	GPIO	SOUTH_SW	DDR3	32	800	800	N/A	N/A	N/A
FCG484	GPIO	WEST_SW_OPT	DDR3	16	800	800	N/A	N/A	N/A
FCG784	HSIO	NORTH_NE	DDR3	64	1066	1066	16	1066	1333
FCG784	HSIO	NORTH_NE	DDR4	64	1333	1333	16	1333	1600
FCG784	HSIO	NORTH_NE	LPDDR3[2]	32	1066	1333	16	1066	1333
FCG784	HSIO	NORTH_NW	DDR3	64	1066	1066	16	1066	1333
FCG784	HSIO	NORTH_NW	DDR4	64	1333	1333	16	1333	1600
FCG784	HSIO	NORTH_NW	LPDDR3[2]	32	1066	1333	32	1066	1333
FCG784	GPIO	SOUTH_SW	DDR3	40	800	800	N/A	N/A	N/A
FCG784	GPIO	WEST_NW	DDR3	64	800	800	40	800	800
FCG784	GPIO	WEST_SW	DDR3	40	800	800	N/A	N/A	N/A
FCSG325	HSIO	NORTH_NE	DDR3	32	1066	1066	8	1066	1333
FCSG325	HSIO	NORTH_NE	DDR4	32	1333	1333	8	1333	1600
FCSG325	HSIO	NORTH_NE	LPDDR3[2]	32	1066	1333	16	1066	1333
FCSG325	HSIO	NORTH_NW	DDR3	32	1066	1066	N/A	N/A	N/A
FCSG325	HSIO	NORTH_NW	DDR4	32	1333	1333	N/A	N/A	N/A
FCSG325	HSIO	NORTH_NW	LPDDR3[2]	32	1066	1333	N/A	N/A	N/A
FCSG325	GPIO	SOUTH_SW	DDR3	8	800	800	8	800	800
FCSG536	HSIO	NORTH_NE	DDR3	40	1066	1066	16	1066	1333
FCSG536	HSIO	NORTH_NE	DDR4	40	1333	1333	16	1333	1600
FCSG536	HSIO	NORTH_NE	LPDDR3[2]	32	1066	1333	16	1066	1333
FCSG536	HSIO	NORTH_NW	DDR3	40	1066	1066	16	1066	1333
FCSG536	HSIO	NORTH_NW	DDR4	40	1333	1333	16	1333	1600
FCSG536	HSIO	NORTH_NW	LPDDR3[2]	32	1066	1333	16	1066	1333
FCSG536	GPIO	SOUTH_SW	DDR3	40	800	800	N/A	N/A	N/A
FCSG536	GPIO	WEST_NW	DDR3	32	800	800	16	800	800
FCSG536	GPIO	WEST_SW	DDR3	16	800	800	N/A	N/A	N/A
FCVG484	HSIO	NORTH_NE	DDR3	40	1066	1066	16	1066	1333
FCVG484	HSIO	NORTH_NE	DDR4	40	1333	1333	16	1333	1600
FCVG484	HSIO	NORTH_NE	LPDDR3[2]	32	1066	1333	16	1066	1333
FCVG484	HSIO	NORTH_NW	DDR3	40	1066	1066	16	1066	1333
FCVG484	HSIO	NORTH_NW	DDR4	40	1333	1333	16	1333	1600

FCVG484	HSIO	NORTH_NW	LPDDR3[2]	32	1066	1333	16	1066	1333
FCVG484	GPIO	SOUTH_SW	DDR3	40	800	800	N/A	N/A	N/A
FCVG484	GPIO	WEST_NW	DDR3	16	800	800	N/A	N/A	N/A
FCVG484	GPIO	WEST_SW_OPT	DDR3	16	800	800	N/A	N/A	N/A

1. See the Package Pin Assignment Tables (PPAT) for information regarding anchor locations.
2. See LPDDR3 electrical compliance errata item.
3. Interface widths <16 are supported for DDR-PHY-only applications.

Table 8 • MPF300 Supported Memory Standards

Package	IO Type	Edge_ Anchor[1]	Memory Type	Maximum Interface Width vs. Performance					
				Interface Width (Max)	STD (Mbps)	–1 (Mbps)	Interface Width (Max)	STD (Mbps)	–1 (Mbps)
FCG1152	HSIO	NORTH_NE	DDR3	72	1066	1066	16	1066	1333
FCG1152	HSIO	NORTH_NE	DDR4	72	1333	1333	16	1333	1600
FCG1152	HSIO	NORTH_NE	LPDDR3[2]	32	1066	1333	16	1066	1333
FCG1152	HSIO	NORTH_NW	DDR3	72	1066	1066	72	1066	1333
FCG1152	HSIO	NORTH_NW	DDR4	72	1333	1333	72	1333	1600
FCG1152	HSIO	NORTH_NW	LPDDR3[2]	32	1066	1333	32	1066	1333
FCG1152	HSIO	SOUTH_SE	DDR3	16	1066	1066	16	1066	1333
FCG1152	HSIO	SOUTH_SE	DDR4	16	1333	1333	16	1333	1600
FCG1152	HSIO	SOUTH_SE	LPDDR3[2]	32	1066	1333	32	1066	1333
FCG1152	GPIO	SOUTH_SW	DDR3	40	800	800	N/A	N/A	N/A
FCG1152	GPIO	WEST_NW	DDR3	72	800	800	40	800	800
FCG1152	GPIO	WEST_SW	DDR3	64	800	800	8	800	800
FCG484	HSIO	NORTH_NE	DDR3	40	1066	1066	8	1066	1333
FCG484	HSIO	NORTH_NE	DDR4	40	1333	1333	8	1333	1600
FCG484	HSIO	NORTH_NE	LPDDR3[2]	32	1066	1333	16	1066	1333
FCG484	HSIO	NORTH_NW	DDR3	40	1066	1066	8	1066	1333
FCG484	HSIO	NORTH_NW	DDR4	40	1333	1333	8	1333	1600
FCG484	HSIO	NORTH_NW	LPDDR3[2]	32	1066	1333	16	1066	1333
FCG484	GPIO	SOUTH_SW	DDR3	32	800	800	N/A	N/A	N/A
FCG484	GPIO	WEST_SW_OPT	DDR3	16	800	800	N/A	N/A	N/A
FCG784	HSIO	NORTH_NE	DDR3	64	1066	1066	16	1066	1333
FCG784	HSIO	NORTH_NE	DDR4	64	1333	1333	16	1333	1600
FCG784	HSIO	NORTH_NE	LPDDR3[2]	32	1066	1333	16	1066	1333
FCG784	HSIO	NORTH_NW	DDR3	64	1066	1066	16	1066	1333
FCG784	HSIO	NORTH_NW	DDR4	64	1333	1333	16	1333	1600
FCG784	HSIO	NORTH_NW	LPDDR3[2]	32	1066	1333	32	1066	1333
FCG784	GPIO	SOUTH_SW	DDR3	40	800	800	40	800	800
FCG784	GPIO	WEST_NW	DDR3	64	800	800	40	800	800
FCG784	GPIO	WEST_SW	DDR3	40	800	800	N/A	N/A	N/A
FCG784	HSIO	NORTH_NE_OPT	LPDDR3[2]	32	1066	1333	16	1066	1333

FCG784	HSIO	NORTH_NE_OPT	DDR4	72	1333	1333	16	1333	1600
FCG784	HSIO	NORTH_NW_OPT	DDR4	72	1333	1333	40	1333	1600
FCG784	HSIO	NORTH_NE_OPT	DDR3	72	1066	1066	16	1066	1333
FCG784	HSIO	NORTH_NW_OPT	DDR3	72	1066	1066	40	1066	1333
FCG784	GPIO	WEST_SW_OPT	DDR3	40	800	800	8	800	800
FCSG536	HSIO	NORTH_NE	DDR3	40	1066	1066	16	1066	1333
FCSG536	HSIO	NORTH_NE	DDR4	40	1333	1333	16	1333	1600
FCSG536	HSIO	NORTH_NE	LPDDR3[2]	32	1066	1333	16	1066	1333
FCSG536	HSIO	NORTH_NW	DDR3	40	1066	1066	16	1066	1333
FCSG536	HSIO	NORTH_NW	DDR4	40	1333	1333	16	1333	1600
FCSG536	HSIO	NORTH_NW	LPDDR3[2]	32	1066	1333	16	1066	1333
FCSG536	GPIO	SOUTH_SW	DDR3	40	800	800	40	800	800
FCSG536	GPIO	WEST_NW	DDR3	32	800	800	16	800	800
FCSG536	GPIO	WEST_SW	DDR3	16	800	800	N/A	N/A	N/A
FCVG484	HSIO	NORTH_NE	DDR3	40	1066	1066	16	1066	1333
FCVG484	HSIO	NORTH_NE	DDR4	40	1333	1333	16	1333	1600
FCVG484	HSIO	NORTH_NE	LPDDR3[2]	32	1066	1333	16	1066	1333
FCVG484	HSIO	NORTH_NW	DDR3	40	1066	1066	16	1066	1333
FCVG484	HSIO	NORTH_NW	DDR4	40	1333	1333	16	1333	1600
FCVG484	HSIO	NORTH_NW	LPDDR3[2]	32	1066	1333	16	1066	1333
FCVG484	GPIO	SOUTH_SW	DDR3	40	800	800	N/A	N/A	N/A
FCVG484	GPIO	WEST_NW	DDR3	16	800	800	N/A	N/A	N/A

1. See the Package Pin Assignment Tables (PPAT) for information regarding anchor locations.
2. See LPDDR3 electrical compliance errata item.
3. Interface widths <16 are supported for DDR-PHY-only applications.

Table 9 • MPF500 Supported Memory Standards

Package	IO Type	Edge_ Anchor[1]	Memory Type	Maximum Interface Width vs. Performance					
				Interface Width (Max)	STD (Mbps)	–1 (Mbps)	Interface Width (Max)	STD (Mbps)	–1 (Mbps)
FCG1152	HSIO	NORTH_NE	DDR3	72	1066	1066	16	1066	1333
FCG1152	HSIO	NORTH_NE	DDR4	72	1333	1333	16	1333	1600
FCG1152	HSIO	NORTH_NE	LPDDR3[2]	32	1066	1333	16	1066	1333
FCG1152	HSIO	NORTH_NW	DDR3	72	1066	1066	72	1066	1333
FCG1152	HSIO	NORTH_NW	DDR4	72	1333	1333	72	1333	1600
FCG1152	HSIO	NORTH_NW	LPDDR3[2]	32	1066	1333	32	1066	1333
FCG1152	HSIO	SOUTH_SE	DDR3	16	1066	1066	16	1066	1333
FCG1152	HSIO	SOUTH_SE	DDR4	16	1333	1333	16	1333	1600
FCG1152	HSIO	SOUTH_SE	LPDDR3[2]	32	1066	1333	32	1066	1333
FCG1152	GPIO	SOUTH_SW	DDR3	40	800	800	N/A	N/A	N/A
FCG1152	GPIO	WEST_NW	DDR3	72	800	800	40	800	800
FCG1152	GPIO	WEST_SW	DDR3	64	800	800	8	800	800

FCG784	HSIO	NORTH_NE	DDR3	64	1066	1066	16	1066	1333
FCG784	HSIO	NORTH_NE	DDR4	64	1333	1333	16	1333	1600
FCG784	HSIO	NORTH_NE	LPDDR3[2]	32	1066	1333	16	1066	1333
FCG784	HSIO	NORTH_NW	DDR3	64	1066	1066	16	1066	1333
FCG784	HSIO	NORTH_NW	DDR4	64	1333	1333	16	1333	1600
FCG784	HSIO	NORTH_NW	LPDDR3[2]	32	1066	1333	32	1066	1333
FCG784	GPIO	SOUTH_SW	DDR3	40	800	800	40	800	800
FCG784	GPIO	WEST_NW	DDR3	64	800	800	40	800	800
FCG784	GPIO	WEST_SW	DDR3	40	800	800	N/A	N/A	N/A
FCG784	HSIO	NORTH_NE_OPT	LPDDR3[2]	32	1066	1333	16	1066	1333
FCG784	HSIO	NORTH_NE_OPT	DDR4	72	1333	1333	16	1333	1600
FCG784	HSIO	NORTH_NW_OPT	DDR4	72	1333	1333	40	1333	1600
FCG784	HSIO	NORTH_NE_OPT	DDR3	72	1066	1066	16	1066	1333
FCG784	HSIO	NORTH_NW_OPT	DDR3	72	1066	1066	40	1066	1333
FCG784	GPIO	WEST_SW_OPT	DDR3	40	800	800	8	800	800

1. See the Package Pin Assignment Tables (PPAT) for information regarding anchor locations.
2. See LPDDR3 electrical compliance errata item.
3. Interface widths <16 are supported for DDR-PHY-only applications.

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