Total Ionizing Dose Test Report

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I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 100 and 125 krad(SiO_2)
2. Power Supply Current	Passed 100 and 125 krad(SiO_2)
3. Input Threshold (VTIL/VIH)	Passed 100 and 125 krad(SiO_2)
4. Output Drive (VOL/VOH)	Passed 100 and 125 krad(SiO_2)
5. Propagation Delay	Passed 100 and 125 krad(SiO_2) for 10% degradation criterion
6. Transition Time	Passed 100 and 125 krad(SiO_2)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the basis of an extensive database of TID testing for Radiation-Tolerant FPGAs including flash-based FPGAs. Microsemi TID reports can be found at http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/military-aerospace-radiation-reliability-data#tid-reports

Electrical parameters are measured pre-irradiation and post-irradiation using the burn in design and the Automatic Test Equipment (ATE) program. The report summarizes sample pins.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters.

Table. 1. DUT and Irradiation Parameters

Part Number	RT4G150
Package	LG1657
Foundry	United Microelectronics Corp.
Technology	65 nm
DUT Design	Burn in design with inverter string
Die Lot Number	KWJSL
Quantity Tested	5
Serial Number (Dose)	9738 (125 krad), 9741 (125 krad), 9752 (125 krad), 9774 (100 krad), 9793 (100 krad)
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	5 krad (SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias	Static at 1.2V/2.5V/3.3V/3.3V
IO Configuration	Single ended Differential Pair

B. Test Method

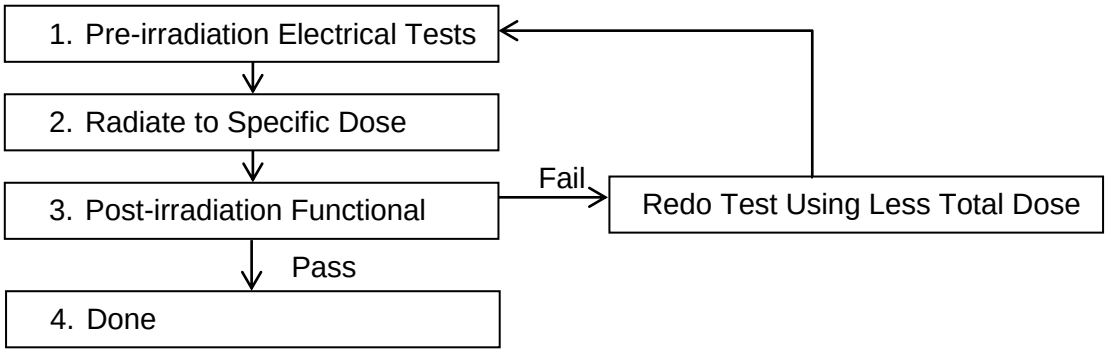

Fig. 1. Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 shows the flow chart describing the steps for the functional and parametric tests.

C. Design and Parametric Measurements

RTG4 FPGA devices have different types of I/Os, such as MSIO and MSIOD, double data rate I/Os (DDRIO), and dedicated I/Os based on functional usage. For more information on I/O naming conventions and I/O description, refer to the RTG4 FPGA Pin Description. All I/Os are tested pre and post-irradiation.

Fabric functionality coverage performed by the burn in design is summarized in table 2 below. In addition to the fabric coverage the supplemental test of propagation delay is also used to determine DUT functionality. These tests are performed pre and post-irradiation and recorded as a pass/fail.

Refer to appendix A for a graphical representation of fabric functional coverage blocks used to perform the functional tests.

Table. 2. Fabric Functional Coverage

Block	**Coverage**
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	Maximum output toggle rate(checker board) compared to reference
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 uRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
I/O Block	I/O utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

The core power supply current IDD, the I/Os power supply currents (IDDI_2.5/IDDI_3.3) and the charge pump/PLL power supply current (IPP_PLL) are also monitored during irradiation in real time.

The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential inputs, and is reported as a pass or fail, as part of the ATE test program. The output-drive voltage (VOL/VOH) is also measured on all pins on the MSIO MSIOD and DDRIO. This report contains the output-drive voltage measurements on selected IO pins used in the burn in design. LVTTL and LVCMOS 2.5V standard at different sourcing and sinking currents are reported.

A 2000 stage inverter string is used to measure the propagation delay. The propagation delay is defined as the time delay from the triggering edge at the Clock input to the switching edge at the output. The propagation delay is monitored real time during irradiation and the time difference between positive switching edges of the clock and output are reported. Additionally, the transition characteristics (rise and fall) at the output of the inverter chain are measured pre and post-irradiation. Oscilloscope screen captures are shown in section III. F.

III. TEST RESULTS

A. Functionality

Every DUT passed the pre-irradiation and post-irradiation functional tests mentioned in section II.C.

B. Power Supply Current

The core power supply current (IDD) is 1.2 V, the I/O bank power supply currents (IDDI) are 2.5 V (IDDI_2.5) and 3.3 V (IDDI_3.3). The charge pump and PLL power supply current (IPP_PLL) is 3.3 V. Figures 2-13 illustrate the plot of in-flux standby IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL versus total dose for every DUT. Tables 3-6 summarize the pre-irradiation and post-irradiation total current (static & dynamic) IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL. Due to testing malfunction the power supply current of DUT 9741 is not shown in this report.

Table. 3. Pre-irradiation and Post-irradiation I_{DD}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
9738	125 krad	0.313	0.331	5.75
9752	125 krad	0.333	0.349	4.80
9774	100 krad	0.349	0.361	3.43
9793	100 krad	0.343	0.361	5.24

Table. 4. Pre-irradiation and Post-irradiation $I_{DDI\_2.5}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
9738	125 krad	0.012	0.015	25
9752	125 krad	0.011	0.014	27.27
9774	100 krad	0.011	0.013	18.18

9793	100 krad	0.013	0.015	15.38

Table. 5. Pre-irradiation and Post-irradiation $I_{DDI\_3.3}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
9738	125 krad	0.042	0.047	11.90
9752	125 krad	0.038	0.045	18.42
9774	100 krad	0.036	0.041	13.88
9793	100 krad	0.038	0.046	21.05

Table. 6. Pre-irradiation and Post-irradiation I_{PP_PLL}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
9738	125 krad	0.0164	0.0173	5.48
9752	125 krad	0.0164	0.0167	1.82
9774	100 krad	0.0161	0.0159	-1.24
9793	100 krad	0.0162	0.0162	0

The following figures (2-17) show the in-beam monitoring of the currents mentioned above as a function of TID for the available DUTs.

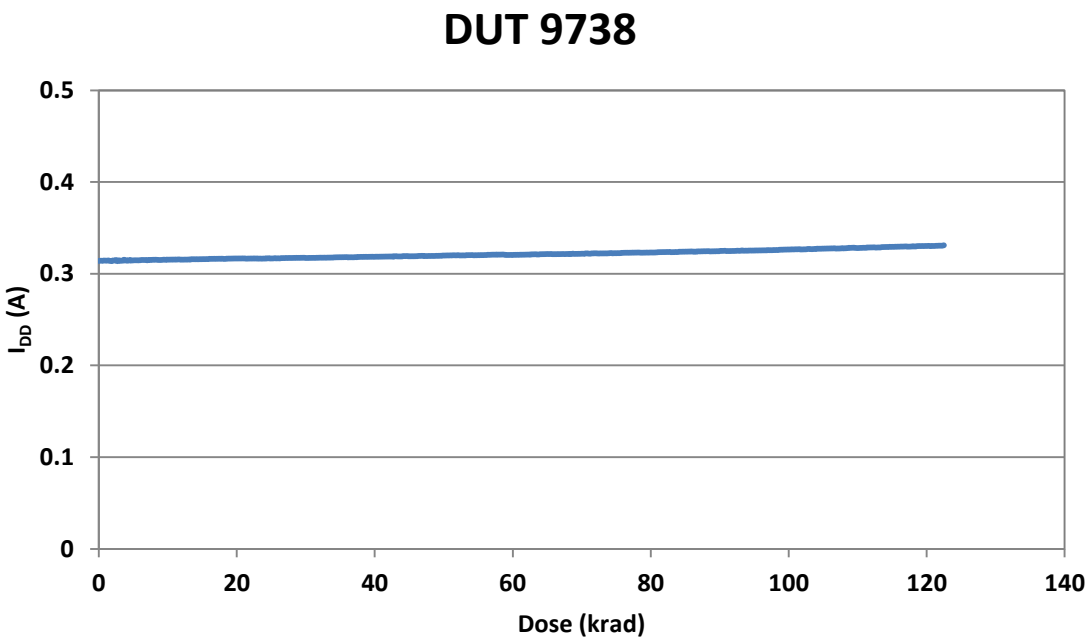

Fig. 2. DUT 9738 core power supply current (I_{DD}) versus TID

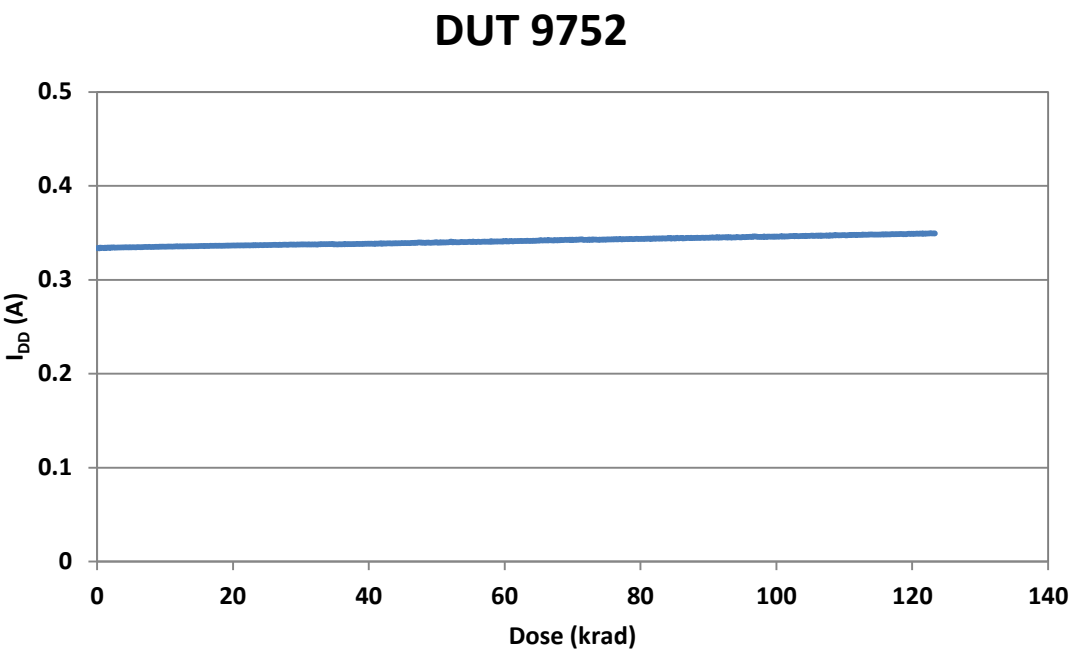

Fig. 3. DUT 9752 core power supply current (I_{DD}) versus TID

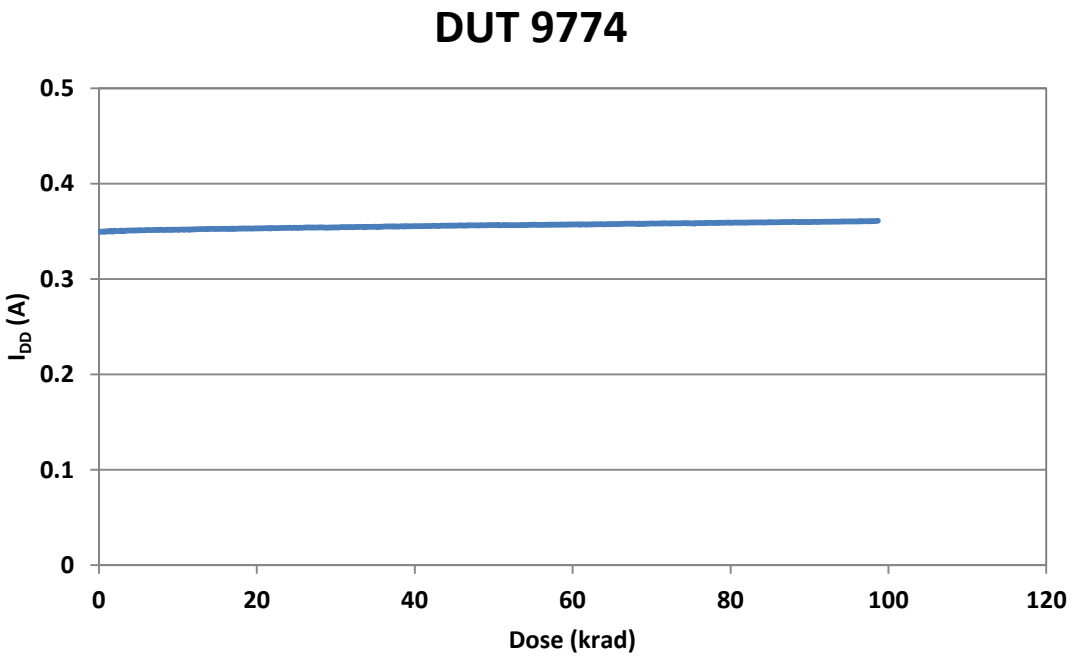

Fig. 4. DUT 9774 core power supply current (I_{DD}) versus TID

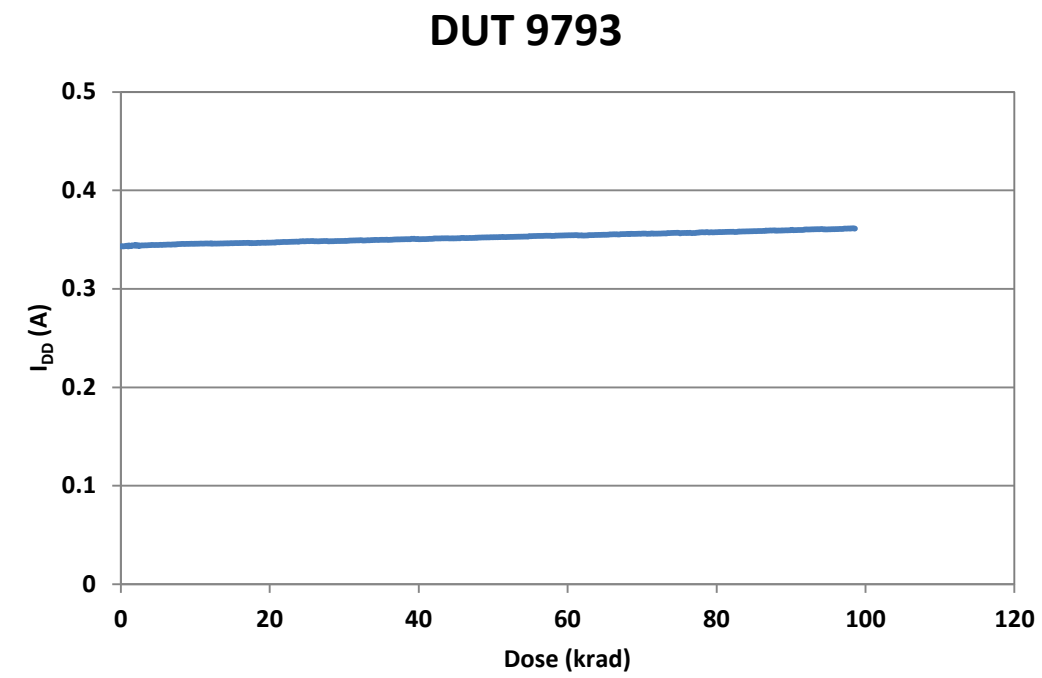

Fig. 5. DUT 9793 core power supply current (I_{DD}) versus TID

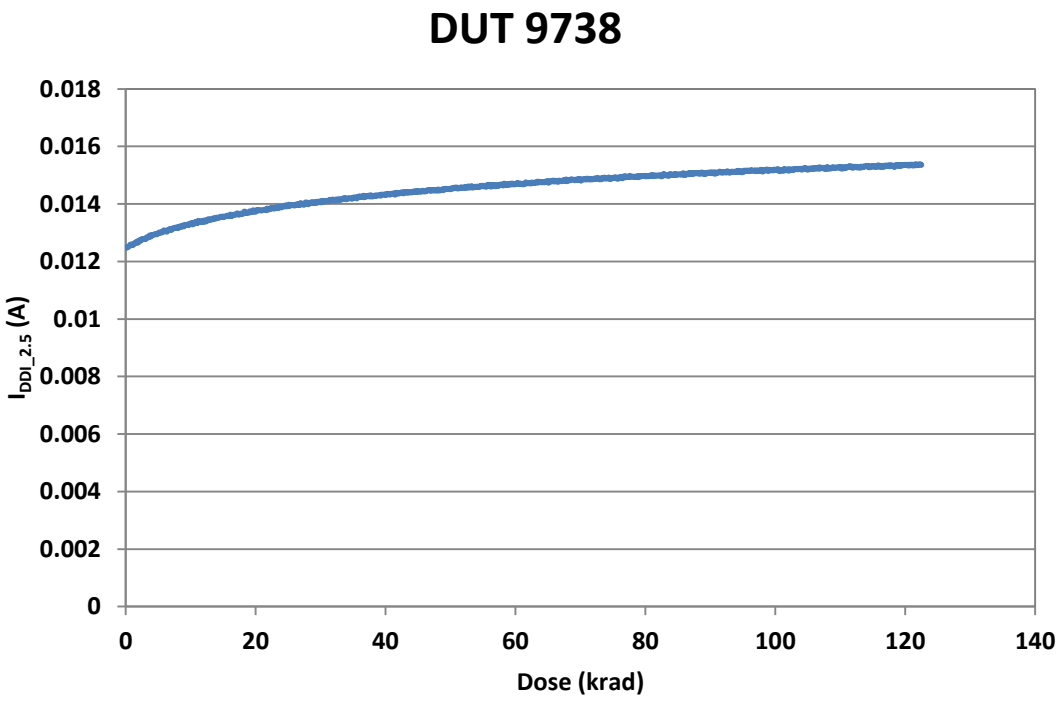

Fig. 6. DUT 9738 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

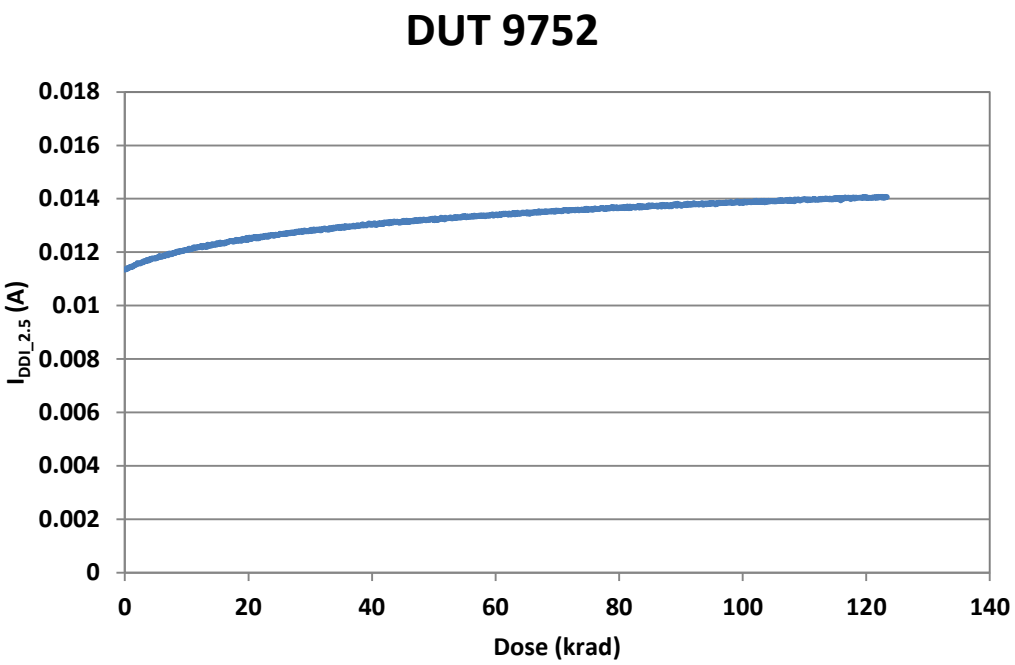

Fig. 7. DUT 9752 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

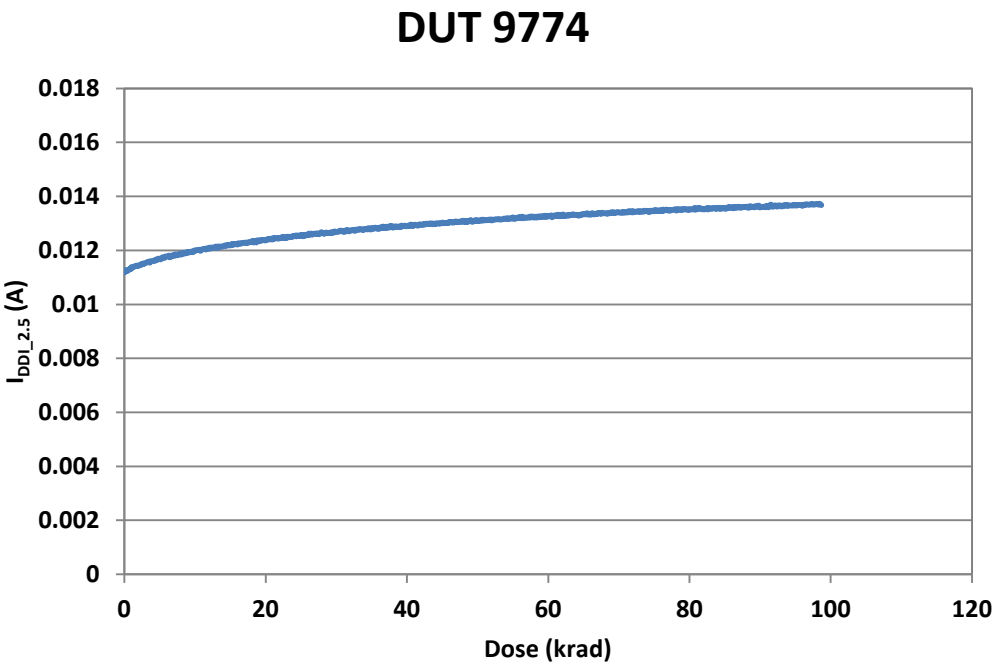

Fig. 8. DUT 9774 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

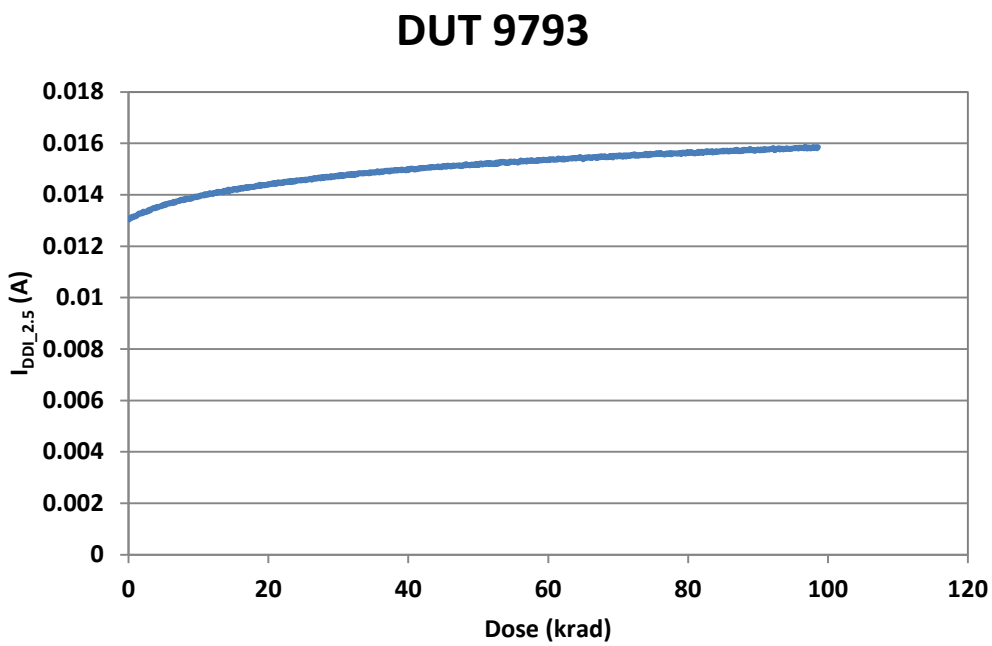

Fig. 9. DUT 9793 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

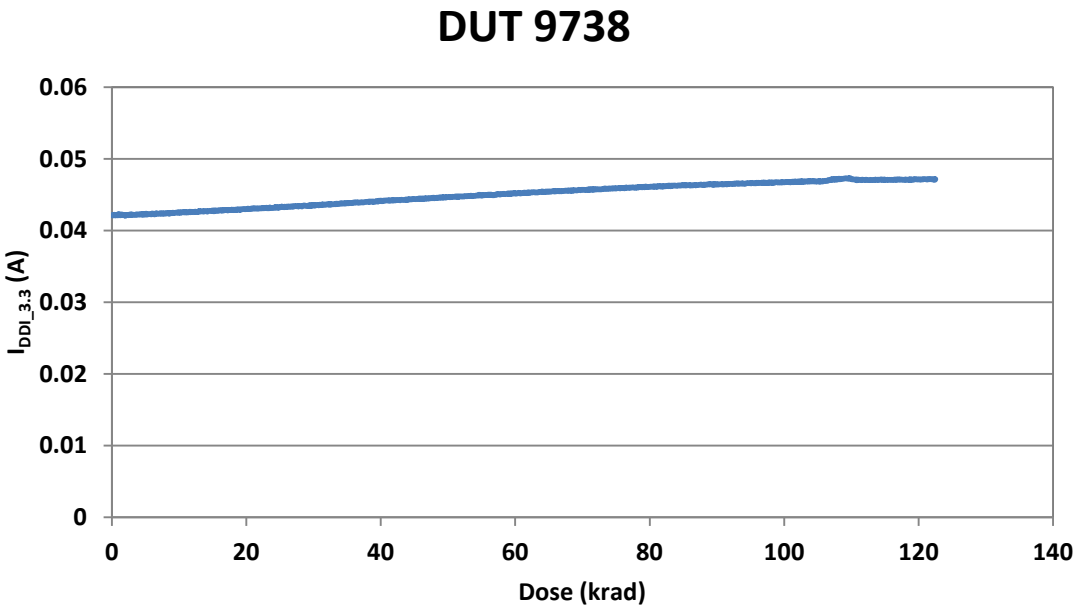

Fig. 10. DUT 9738 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

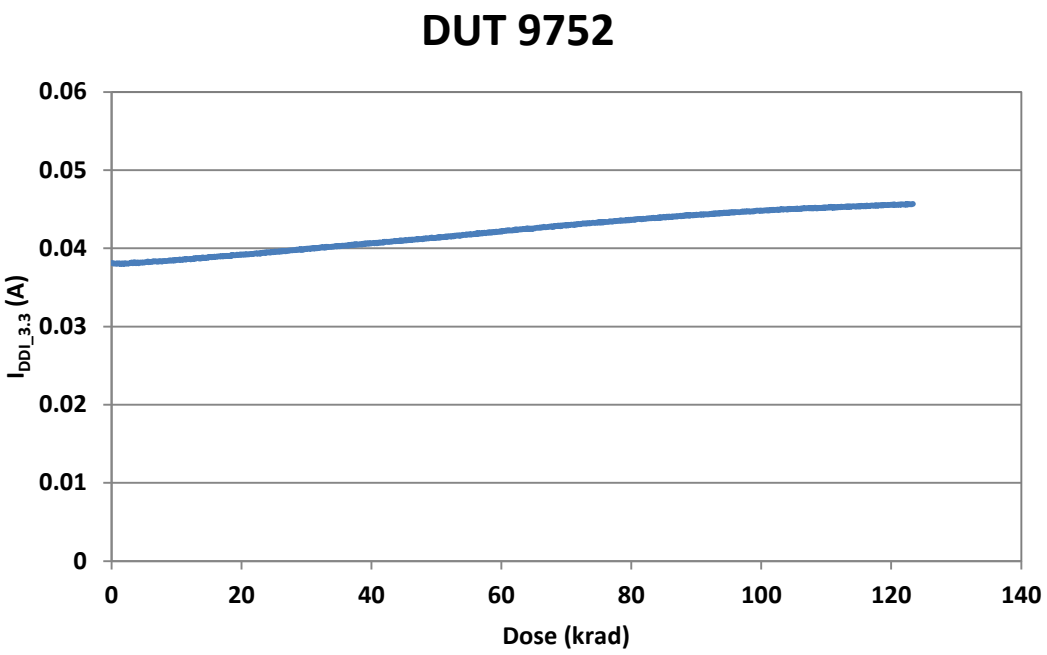

Fig. 11. DUT 9752 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

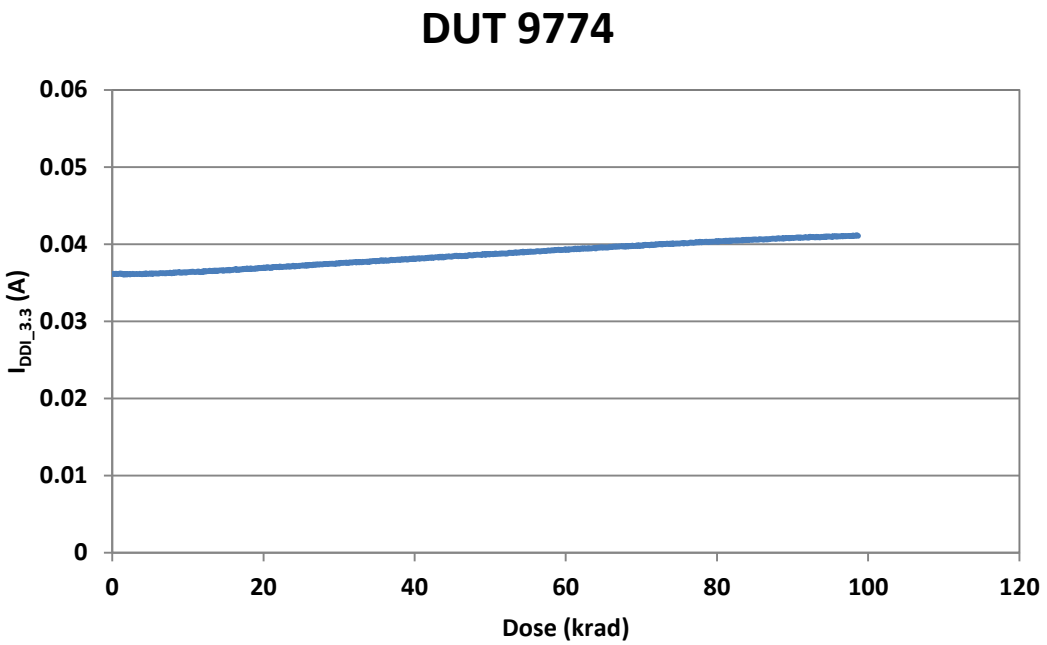

Fig. 12. DUT 9774 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

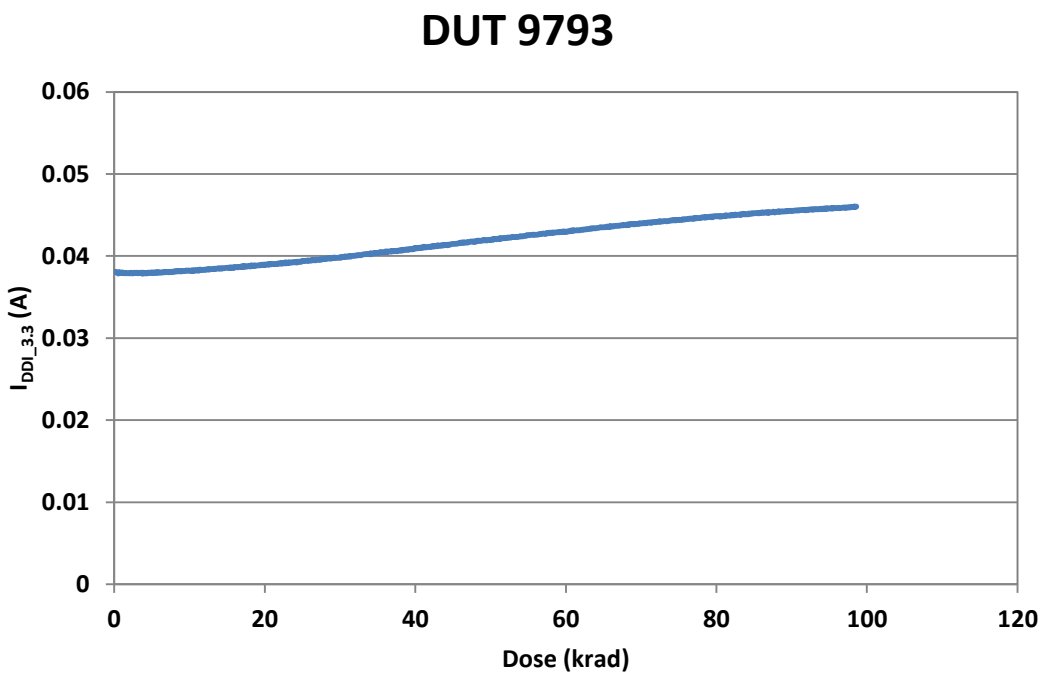

Fig. 13. DUT 9793 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

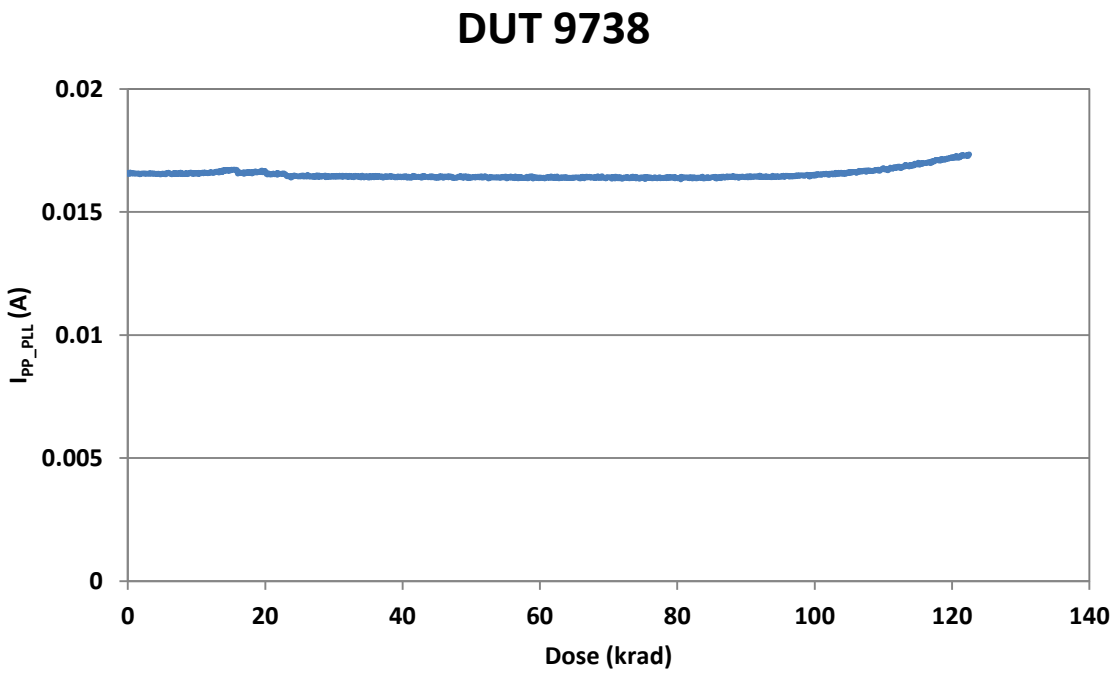

Fig. 14. DUT 9738 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

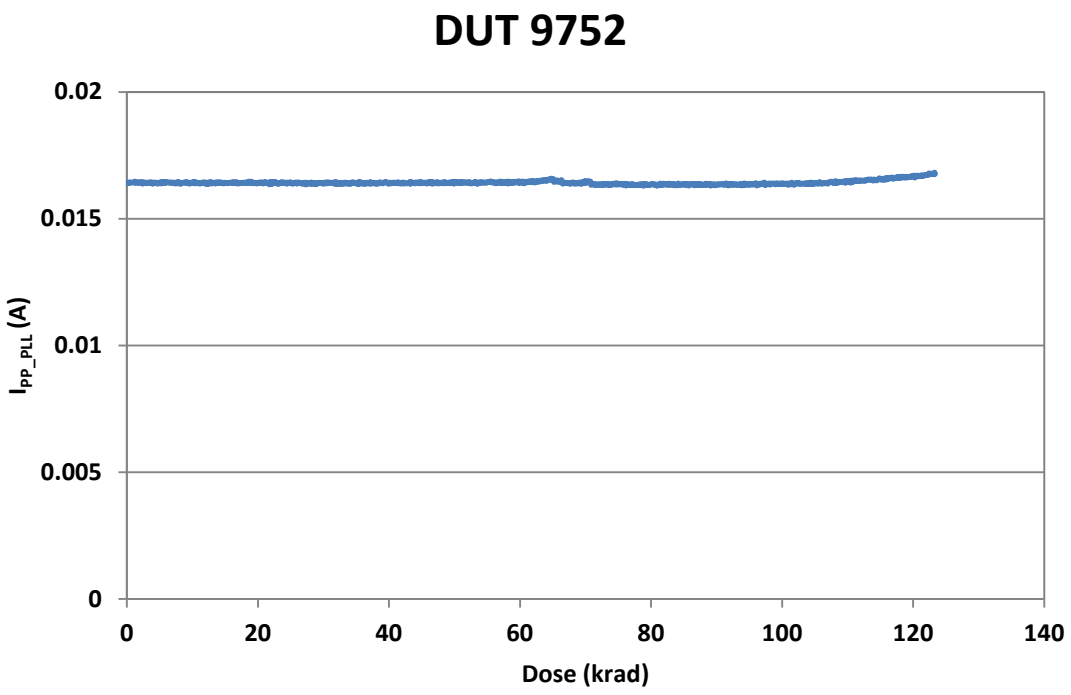

Fig. 15. DUT 9752 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

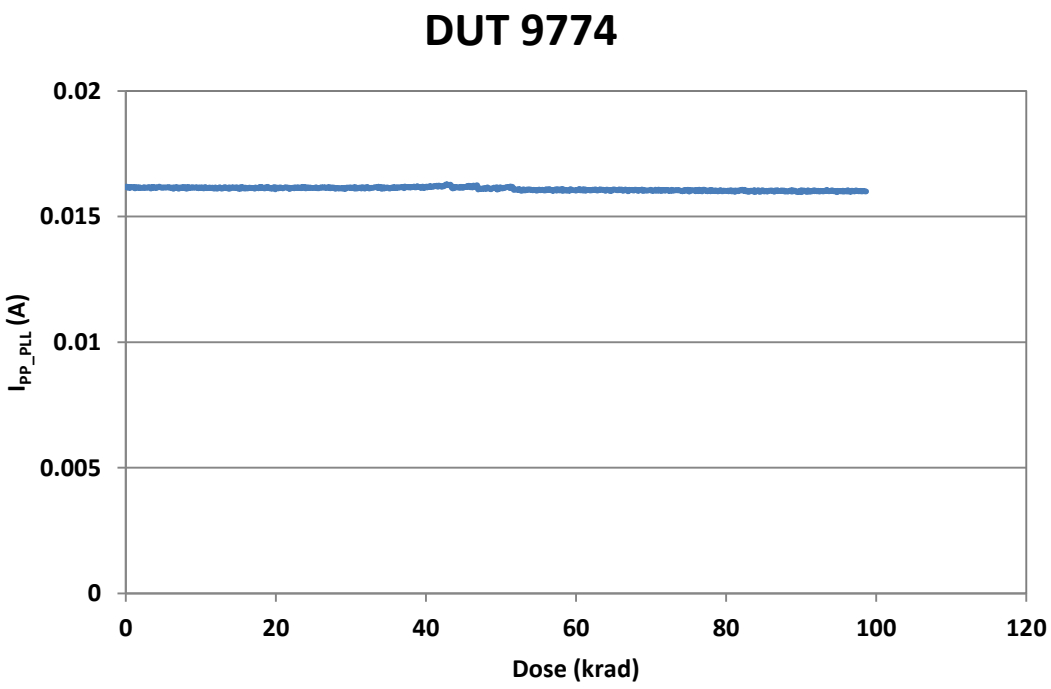

Fig. 16. DUT 9774 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

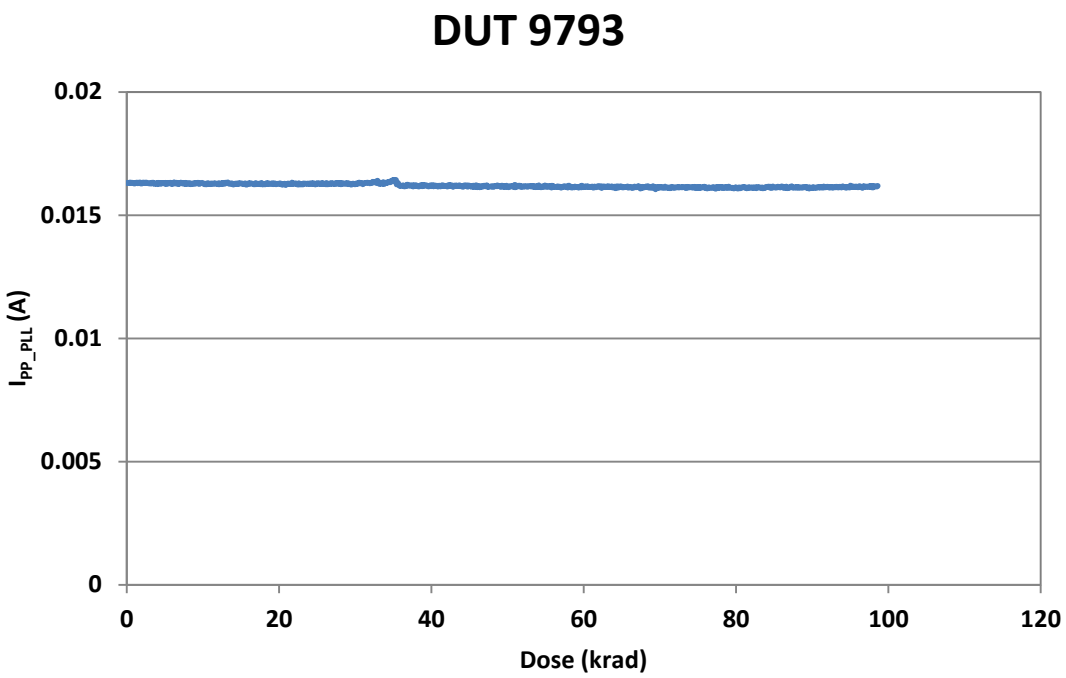

Fig. 17. DUT 9793 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

C. Single-Ended Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design starts to switch. VIH is the input trip point when the input is going high to low and VIL is the input trip point when the input is going low to high. The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential input and recorded as pass or fail. All I/Os are tested at their respective I/O standards and are compliant to the JEDEC specs. Refer to http://www.microsemi.com/document-portal/doc_view/135193-ds0131-rtg4-fpga-datasheet for more information.

The 3 DUTs tested passed with respect to the testing specification pre and post-irradiation. This pass/fail is determined as part of the ATE test program used to perform pre and post-irradiation electrical parametric measurements.

Table. 7. VIH Summary

DUT	Pre-irradiation	Post-irradiation
9738	Passed	Passed
9741	Passed	Passed
9752	Passed	Passed
9774	Passed	Passed
9793	Passed	Passed

Table. 8. VIL Summary

DUT	Pre-irradiation	Post-irradiation
9738	Passed	Passed
9741	Passed	Passed
9752	Passed	Passed
9774	Passed	Passed
9738	Passed	Passed

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-irradiation output-drive voltages (VOL/VOH) are performed on all available IOs. The measurements performed pre and post irradiation are within the specification limits; in each case, the radiation-induced degradation is within 10%. For the purpose of this report, the measurements presented below in tables 9 through 28 are sampled on several pins used in the burn in design.

Table. 9. LVCMOS 25 VOH – DUT 9738

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.1308	2.1345	2.1973	2.2029	2.1662	2.1739	2.1429	2.1547	2.1063	2.1216	2.0906	2.1074
EPCSRST_N_0	B31	2.1322	2.1351	2.2013	2.2030	2.1722	2.1738	2.1507	2.1545	2.1182	2.1208	2.1046	2.1066
EPCSRST_N_1	B32	2.1331	2.1356	2.2023	2.2047	2.1736	2.1765	2.1529	2.1566	2.1205	2.1254	2.1074	2.1123
EPCSRST_N_2	B34	2.1326	2.1349	2.2015	2.2034	2.1727	2.1747	2.1520	2.1544	2.1192	2.1225	2.1058	2.1088
EPCSRST_N_3	B35	2.1332	2.1355	2.2034	2.2048	2.1755	2.1772	2.1555	2.1571	2.1252	2.1273	2.1125	2.1144
EPCSRST_N_4	B36	2.1310	2.1345	2.1988	2.2025	2.1682	2.1739	2.1459	2.1526	2.1106	2.1200	2.0956	2.1057
EPCSRST_N_5	B37	2.1331	2.1354	2.2022	2.2042	2.1732	2.1760	2.1524	2.1558	2.1204	2.1247	2.1072	2.1114
MONITOR	K23	2.1329	2.1348	2.2023	2.2037	2.1741	2.1761	2.1534	2.1566	2.1226	2.1267	2.1094	2.1136
PLL_MON	L20	2.1329	2.1342	2.2035	2.2053	2.1761	2.1786	2.1577	2.1599	2.1281	2.1314	2.1158	2.1197
TOGGLE_MON	L22	2.1327	2.1340	2.2037	2.2048	2.1762	2.1776	2.1566	2.1581	2.1271	2.1293	2.1154	2.1170

Table. 10. LVCMOS 25 VOH – DUT 9741

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.1310	2.1349	2.1978	2.2033	2.1667	2.1747	2.1435	2.1552	2.1063	2.1216	2.0918	2.1083
EPCSRST_N_0	B31	2.1330	2.1355	2.2020	2.2033	2.1730	2.1745	2.1517	2.1551	2.1182	2.1208	2.1060	2.1077
EPCSRST_N_1	B32	2.1346	2.1372	2.2028	2.2054	2.1741	2.1774	2.1536	2.1575	2.1205	2.1254	2.1081	2.1133
EPCSRST_N_2	B34	2.1334	2.1359	2.2024	2.2042	2.1735	2.1758	2.1526	2.1552	2.1192	2.1225	2.1069	2.1098
EPCSRST_N_3	B35	2.1345	2.1368	2.2042	2.2060	2.1762	2.1781	2.1561	2.1583	2.1252	2.1273	2.1130	2.1154
EPCSRST_N_4	B36	2.1305	2.1357	2.1958	2.2033	2.1639	2.1744	2.1398	2.1536	2.1106	2.1200	2.0849	2.1071
EPCSRST_N_5	B37	2.1332	2.1359	2.2026	2.2046	2.1737	2.1767	2.1529	2.1567	2.1204	2.1247	2.1077	2.1123
MONITOR	K23	2.1334	2.1352	2.2030	2.2043	2.1752	2.1769	2.1548	2.1576	2.1226	2.1267	2.1113	2.1151
PLL_MON	L20	2.1346	2.1358	2.2048	2.2063	2.1778	2.1793	2.1593	2.1609	2.1281	2.1314	2.1184	2.1208
TOGGLE_MON	L22	2.1350	2.1358	2.2049	2.2057	2.1777	2.1785	2.1585	2.1594	2.1271	2.1293	2.1176	2.1186

Table. 11. LVCMOS 25 VOH – DUT 9752

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.1344	2.1378	2.1997	2.2054	2.1694	2.1766	2.1463	2.1576	2.1102	2.1250	2.0947	2.1109
EPCSRST_N_0	B31	2.1365	2.1382	2.2044	2.2052	2.1757	2.1763	2.1548	2.1570	2.1228	2.1239	2.1094	2.1095
EPCSRST_N_1	B32	2.1372	2.1394	2.2051	2.2073	2.1768	2.1796	2.1567	2.1597	2.1252	2.1293	2.1121	2.1162
EPCSRST_N_2	B34	2.1360	2.1378	2.2041	2.2056	2.1757	2.1773	2.1552	2.1569	2.1235	2.1254	2.1100	2.1117
EPCSRST_N_3	B35	2.1373	2.1388	2.2061	2.2071	2.1785	2.1796	2.1587	2.1599	2.1288	2.1299	2.1165	2.1171
EPCSRST_N_4	B36	2.1365	2.1380	2.2036	2.2048	2.1746	2.1763	2.1535	2.1553	2.1205	2.1229	2.1071	2.1090
EPCSRST_N_5	B37	2.1372	2.1388	2.2048	2.2065	2.1759	2.1785	2.1554	2.1585	2.1236	2.1273	2.1100	2.1142
MONITOR	K23	2.1363	2.1376	2.2050	2.2060	2.1773	2.1786	2.1570	2.1594	2.1265	2.1296	2.1139	2.1172
PLL_MON	L20	2.1375	2.1380	2.2067	2.2077	2.1800	2.1813	2.1618	2.1627	2.1331	2.1348	2.1213	2.1186
TOGGLE_MON	L22	2.1373	2.1380	2.2065	2.2070	2.1794	2.1800	2.1600	2.1607	2.1313	2.1319	2.1195	2.1201

Table. 12. LVCMOS 25 VOH – DUT 9774

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.1313	2.1350	2.1985	2.2032	2.1682	2.1745	2.1454	2.1554	2.1098	2.1229	2.0948	2.1090
EPCSRST_N_0	B31	2.1327	2.1350	2.2017	2.2031	2.1728	2.1742	2.1511	2.1546	2.1187	2.1213	2.1052	2.1072
EPCSRST_N_1	B32	2.1338	2.1359	2.2027	2.2051	2.1743	2.1770	2.1538	2.1571	2.1222	2.1267	2.1090	2.1136
EPCSRST_N_2	B34	2.1323	2.1346	2.2013	2.2034	2.1725	2.1749	2.1517	2.1545	2.1191	2.1229	2.1058	2.1094
EPCSRST_N_3	B35	2.1339	2.1354	2.2037	2.2050	2.1757	2.1771	2.1560	2.1574	2.1258	2.1273	2.1132	2.1147
EPCSRST_N_4	B36	2.1319	2.1338	2.2005	2.2022	2.1713	2.1731	2.1501	2.1520	2.1169	2.1195	2.1029	2.1051
EPCSRST_N_5	B37	2.1328	2.1348	2.2017	2.2038	2.1733	2.1753	2.1522	2.1552	2.1202	2.1241	2.1069	2.1105
MONITOR	K23	2.1326	2.1349	2.2010	2.2042	2.1723	2.1765	2.1507	2.1571	2.1184	2.1271	2.1050	2.1145
PLL_MON	L20	2.1344	2.1360	2.2047	2.2058	2.1776	2.1789	2.1592	2.1605	2.1303	2.1319	2.1187	2.1204
TOGGLE_MON	L22	2.1340	2.1347	2.2046	2.2051	2.1775	2.1779	2.1582	2.1584	2.1289	2.1297	2.1172	2.1176

Table. 13. LVCMOS 25 VOH – DUT 9793

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.1292	2.1332	2.1960	2.2023	2.1648	2.1735	2.1409	2.1540	2.1041	2.1215	2.0882	2.1073
EPCSRST_N_0	B31	2.1317	2.1341	2.2009	2.2023	2.1717	2.1733	2.1503	2.1539	2.1178	2.1204	2.1039	2.1059
EPCSRST_N_1	B32	2.1328	2.1350	2.2017	2.2042	2.1729	2.1755	2.1523	2.1557	2.1204	2.1244	2.1072	2.1112
EPCSRST_N_2	B34	2.1319	2.1336	2.2013	2.2028	2.1724	2.1742	2.1517	2.1536	2.1196	2.1218	2.1058	2.1083
EPCSRST_N_3	B35	2.1326	2.1343	2.2031	2.2043	2.1750	2.1765	2.1550	2.1564	2.1244	2.1265	2.1120	2.1136
EPCSRST_N_4	B36	2.1310	2.1335	2.1997	2.2018	2.1702	2.1722	2.1487	2.1513	2.1151	2.1186	2.1012	2.1043
EPCSRST_N_5	B37	2.1315	2.1338	2.2007	2.2030	2.1719	2.1746	2.1507	2.1543	2.1186	2.1228	2.1049	2.1094
MONITOR	K23	2.1315	2.1329	2.2019	2.2030	2.1737	2.1752	2.1529	2.1557	2.1226	2.1255	2.1100	2.1127
PLL_MON	L20	2.1326	2.1336	2.2034	2.2046	2.1763	2.1779	2.1575	2.1592	2.1287	2.1307	2.1166	2.1188
TOGGLE_MON	L22	2.1327	2.1335	2.2034	2.2041	2.1758	2.1765	2.1563	2.1569	2.1267	2.1279	2.1148	2.1156

Table. 14. LVCMOS 25 VOL – DUT 9738

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	238.901	234.381	173.067	167.345	203.560	195.652	226.179	218.228	262.148	249.842	277.947	263.343
EPCSRST_N_0	B31	237.030	234.193	169.287	167.646	197.658	196.130	218.480	218.857	250.543	250.999	264.408	264.713
EPCSRST_N_1	B32	237.123	233.181	168.671	165.645	196.697	193.049	217.274	213.197	249.031	243.990	262.423	256.794
EPCSRST_N_2	B34	237.839	234.613	169.839	167.252	197.790	194.907	218.631	215.456	250.564	246.940	263.955	260.083
EPCSRST_N_3	B35	236.896	234.161	167.478	165.733	194.826	192.898	214.586	212.732	244.798	242.621	257.210	255.150
EPCSRST_N_4	B36	239.321	235.378	172.339	168.181	202.074	196.350	224.209	217.465	259.044	249.714	273.993	263.460
EPCSRST_N_5	B37	237.248	234.098	168.985	166.336	196.986	193.940	217.714	214.327	249.195	244.956	262.448	257.861
MONITOR	K23	235.586	232.917	167.692	165.068	195.423	191.957	215.027	212.047	245.671	241.222	258.557	253.762
PLL_MON	L20	235.560	232.554	166.257	163.875	192.984	189.831	212.862	209.036	241.615	236.814	253.537	248.403
TOGGLE_MON	L22	235.973	233.115	166.252	164.275	192.959	190.810	212.217	210.055	240.797	238.284	252.894	250.303

Table. 15. LVCMOS 25 VOL – DUT 9741

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	238.436	233.853	172.515	166.880	202.769	194.999	225.337	217.474	261.067	248.937	276.665	262.463
EPCSRST_N_0	B31	236.251	233.212	168.533	166.905	196.854	195.162	217.212	217.939	249.074	249.880	262.788	263.493
EPCSRST_N_1	B32	235.376	231.512	167.716	164.754	195.655	191.957	216.119	212.004	247.738	242.659	260.878	255.488
EPCSRST_N_2	B34	236.633	233.382	168.771	166.587	196.760	194.041	217.538	214.615	249.119	245.986	262.561	259.229
EPCSRST_N_3	B35	235.276	232.491	166.762	164.829	194.084	191.894	213.895	211.690	243.931	241.554	256.531	254.020
EPCSRST_N_4	B36	239.622	234.060	175.115	167.541	206.421	195.622	230.188	216.435	268.176	248.735	284.796	262.342
EPCSRST_N_5	B37	236.570	233.571	168.294	165.846	196.333	193.187	216.835	213.473	248.215	243.990	261.380	256.819
MONITOR	K23	234.871	232.088	166.687	164.277	193.941	191.052	213.357	210.841	243.624	239.890	256.158	252.342
PLL_MON	L20	233.973	230.505	164.797	162.794	191.435	188.926	211.061	208.194	239.387	236.463	251.019	247.385
TOGGLE_MON	L22	233.749	231.095	164.907	163.146	191.301	189.568	210.094	208.638	238.523	236.879	250.168	248.684

Table. 16. LVCMOS 25 VOL – DUT 9752

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	234.279	230.145	169.927	164.629	199.931	192.284	222.173	214.696	257.651	245.644	273.086	259.044
EPCSRST_N_0	B31	232.383	229.868	165.934	165.007	193.827	193.088	214.147	215.639	245.494	247.416	259.020	261.092
EPCSRST_N_1	B32	231.909	228.600	165.154	162.620	192.665	189.559	212.802	209.255	243.856	239.508	256.958	252.099
EPCSRST_N_2	B34	233.354	230.696	166.360	164.528	194.022	191.831	214.398	212.331	245.715	243.387	258.931	256.568
EPCSRST_N_3	B35	231.821	229.679	164.262	163.059	191.220	189.772	210.717	209.468	240.288	239.345	252.687	251.609
EPCSRST_N_4	B36	232.990	230.759	167.226	165.470	195.265	193.413	216.068	214.214	248.491	246.224	262.071	259.857
EPCSRST_N_5	B37	232.437	229.604	165.970	163.700	193.846	190.990	214.146	211.088	245.728	241.831	258.843	254.547
MONITOR	K23	231.643	229.135	164.452	162.304	191.542	188.928	211.021	208.617	240.874	237.453	253.383	249.741
PLL_MON	L20	230.297	228.054	162.342	160.771	188.603	186.575	207.965	205.643	235.799	233.044	247.406	244.406
TOGGLE_MON	L22	230.759	228.573	162.734	161.402	189.052	187.585	207.871	206.530	236.425	234.947	248.033	246.677

Table. 17. LVCMOS 25 VOL – DUT 9774

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	236.929	232.998	171.045	166.125	200.760	194.207	222.788	216.582	257.526	247.743	272.684	260.942
EPCSRST_N_0	B31	235.372	232.722	168.069	166.716	196.289	194.949	216.860	217.613	248.860	249.603	262.499	263.053
EPCSRST_N_1	B32	234.886	231.612	167.339	164.654	195.077	191.630	215.289	211.502	246.532	241.755	259.458	254.434
EPCSRST_N_2	B34	236.256	233.395	168.885	166.486	196.961	193.990	217.726	214.402	249.597	245.647	262.950	258.765
EPCSRST_N_3	B35	235.163	232.817	166.309	164.867	193.419	191.869	213.204	211.828	242.964	241.504	255.074	253.831
EPCSRST_N_4	B36	237.198	234.763	169.751	167.930	198.381	196.200	219.372	217.151	251.845	249.438	265.802	263.184
EPCSRST_N_5	B37	236.231	233.583	168.294	166.122	196.295	193.589	216.885	213.988	248.516	244.881	261.757	257.861
MONITOR	K23	234.632	231.447	167.818	163.925	195.963	190.574	216.559	210.565	248.321	239.815	261.684	252.003
PLL_MON	L20	233.143	230.178	164.180	162.656	190.579	188.611	210.205	207.880	238.052	235.193	249.659	246.820
TOGGLE_MON	L22	233.787	231.459	164.744	163.409	191.125	189.781	209.931	208.750	238.322	236.966	249.930	248.948

Table. 18. LVCMOS 25 VOL – DUT 9793

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	239.039	234.934	173.356	167.420	203.987	195.389	226.769	218.090	263.077	249.201	279.102	262.576
EPCSRST_N_0	B31	236.578	233.916	168.960	167.508	197.193	195.829	217.814	218.631	249.953	250.659	263.629	264.461
EPCSRST_N_1	B32	236.243	233.018	168.307	165.871	196.283	193.187	216.835	213.335	248.177	243.751	261.506	256.781
EPCSRST_N_2	B34	237.273	234.700	169.211	167.315	197.099	194.907	217.714	215.381	249.295	246.789	262.435	259.895
EPCSRST_N_3	B35	236.620	234.449	167.440	165.972	194.725	193.262	214.536	213.109	244.522	243.048	256.971	255.539
EPCSRST_N_4	B36	238.090	235.567	170.643	168.683	199.461	197.091	220.628	218.168	253.441	250.492	267.460	264.213
EPCSRST_N_5	B37	237.612	234.826	169.375	167.114	197.627	194.543	218.317	215.055	250.150	245.998	263.566	258.991
MONITOR	K23	236.026	233.935	167.479	165.508	194.845	192.535	214.424	212.248	244.441	241.499	257.075	253.862
PLL_MON	L20	234.603	232.453	165.326	163.486	191.901	189.856	211.653	209.577	239.802	236.777	251.699	248.290
TOGGLE_MON	L22	234.591	232.412	165.573	164.262	192.432	191.010	211.300	210.143	240.156	238.798	252.103	250.817

Table. 19. LVTTL VOH – DUT 9738

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.9180	2.9209	2.9063	2.9112	2.8828	2.8919	2.8601	2.8730	2.8369	2.8547
EPCSRST_N_0	B31	2.9198	2.9209	2.9099	2.9112	2.8910	2.8918	2.8719	2.8721	2.8529	2.8534
EPCSRST_N_1	B32	2.9205	2.9217	2.9113	2.9130	2.8926	2.8952	2.8742	2.8777	2.8557	2.8601
EPCSRST_N_2	B34	2.9200	2.9209	2.9103	2.9115	2.8914	2.8932	2.8727	2.8748	2.8540	2.8566
EPCSRST_N_3	B35	2.9208	2.9214	2.9122	2.9130	2.8955	2.8962	2.8787	2.8794	2.8617	2.8627
EPCSRST_N_4	B36	2.9185	2.9203	2.9076	2.9110	2.8853	2.8915	2.8635	2.8720	2.8419	2.8528
EPCSRST_N_5	B37	2.9203	2.9212	2.9109	2.9124	2.8923	2.8946	2.8739	2.8768	2.8555	2.8593
MONITOR	K23	2.9196	2.9214	2.9106	2.9124	2.8929	2.8955	2.8754	2.8790	2.8580	2.8627
PLL_MON	L20	2.9196	2.9208	2.9118	2.9132	2.8958	2.8991	2.8802	2.8842	2.8651	2.8687
TOGGLE_MON	L22	2.9193	2.9208	2.9119	2.9132	2.8961	2.8978	2.8805	2.8821	2.8646	2.8665

Table. 20. LVTTL VOH – DUT 9741

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.9181	2.9213	2.9065	2.9119	2.8837	2.8927	2.8607	2.8734	2.8379	2.8554
EPCSRST_N_0	B31	2.9201	2.9213	2.9108	2.9118	2.8918	2.8924	2.8730	2.8730	2.8540	2.8546
EPCSRST_N_1	B32	2.9217	2.9229	2.9122	2.9140	2.8937	2.8966	2.8750	2.8790	2.8568	2.8613
EPCSRST_N_2	B34	2.9206	2.9217	2.9114	2.9125	2.8928	2.8942	2.8739	2.8756	2.8554	2.8572
EPCSRST_N_3	B35	2.9220	2.9228	2.9133	2.9143	2.8963	2.8973	2.8792	2.8806	2.8622	2.8637
EPCSRST_N_4	B36	2.9177	2.9217	2.9049	2.9119	2.8798	2.8924	2.8549	2.8732	2.8297	2.8539
EPCSRST_N_5	B37	2.9207	2.9218	2.9116	2.9129	2.8929	2.8954	2.8746	2.8779	2.8564	2.8602
MONITOR	K23	2.9201	2.9215	2.9114	2.9129	2.8944	2.8966	2.8773	2.8800	2.8601	2.8638
PLL_MON	L20	2.9211	2.9229	2.9135	2.9148	2.8977	2.9002	2.8824	2.8851	2.8677	2.8704
TOGGLE_MON	L22	2.9217	2.9223	2.9134	2.9146	2.8978	2.8989	2.8825	2.8835	2.8670	2.8680

Table. 21. LVTTL VOH – DUT 9752

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.9215	2.9239	2.9099	2.9146	2.8870	2.8955	2.8640	2.8766	2.8414	2.8586
EPCSRST_N_0	B31	2.9235	2.9243	2.9139	2.9142	2.8953	2.8949	2.8766	2.8753	2.8580	2.8568
EPCSRST_N_1	B32	2.9245	2.9252	2.9151	2.9163	2.8971	2.8991	2.8790	2.8819	2.8609	2.8646
EPCSRST_N_2	B34	2.9234	2.9238	2.9140	2.9146	2.8955	2.8963	2.8769	2.8778	2.8587	2.8596
EPCSRST_N_3	B35	2.9246	2.9248	2.9160	2.9161	2.8992	2.8995	2.8826	2.8825	2.8657	2.8657
EPCSRST_N_4	B36	2.9234	2.9239	2.9134	2.9140	2.8940	2.8949	2.8745	2.8754	2.8551	2.8563
EPCSRST_N_5	B37	2.9244	2.9249	2.9146	2.9159	2.8958	2.8979	2.8771	2.8799	2.8587	2.8622
MONITOR	K23	2.9229	2.9241	2.9140	2.9156	2.8971	2.8990	2.8799	2.8825	2.8628	2.8664
PLL_MON	L20	2.9236	2.9244	2.9162	2.9173	2.9007	2.9030	2.8859	2.8875	2.8711	2.8731
TOGGLE_MON	L22	2.9238	2.9245	2.9159	2.9168	2.9000	2.9008	2.8843	2.8852	2.8689	2.8696

Table. 22. LVTTL VOH – DUT 9774

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.9190	2.9212	2.9078	2.9119	2.8857	2.8930	2.8635	2.8743	2.8417	2.8566
EPCSRST_N_0	B31	2.9203	2.9212	2.9108	2.9117	2.8917	2.8921	2.8728	2.8727	2.8537	2.8544
EPCSRST_N_1	B32	2.9215	2.9222	2.9118	2.9134	2.8938	2.8961	2.8758	2.8790	2.8576	2.8619
EPCSRST_N_2	B34	2.9201	2.9210	2.9104	2.9116	2.8917	2.8934	2.8728	2.8752	2.8541	2.8572
EPCSRST_N_3	B35	2.9215	2.9215	2.9129	2.9136	2.8961	2.8968	2.8795	2.8797	2.8630	2.8632
EPCSRST_N_4	B36	2.9195	2.9202	2.9097	2.9103	2.8899	2.8910	2.8705	2.8716	2.8511	2.8526
EPCSRST_N_5	B37	2.9203	2.9211	2.9111	2.9123	2.8924	2.8943	2.8739	2.8761	2.8555	2.8585
MONITOR	K23	2.9194	2.9217	2.9101	2.9132	2.8909	2.8964	2.8720	2.8798	2.8530	2.8635
PLL_MON	L20	2.9212	2.9223	2.9135	2.9149	2.8980	2.9001	2.8830	2.8851	2.8685	2.8706
TOGGLE_MON	L22	2.9210	2.9216	2.9133	2.9141	2.8978	2.8981	2.8823	2.8828	2.8670	2.8673

Table. 23. LVTTL VOH – DUT 9793

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.9169	2.9203	2.9050	2.9105	2.8814	2.8920	2.8579	2.8730	2.8343	2.8550
EPCSRST_N_0	B31	2.9193	2.9206	2.9098	2.9108	2.8907	2.8915	2.8716	2.8716	2.8523	2.8531
EPCSRST_N_1	B32	2.9203	2.9212	2.9104	2.9121	2.8921	2.8945	2.8740	2.8771	2.8557	2.8596
EPCSRST_N_2	B34	2.9195	2.9201	2.9103	2.9111	2.8916	2.8929	2.8731	2.8745	2.8547	2.8562
EPCSRST_N_3	B35	2.9203	2.9207	2.9119	2.9122	2.8951	2.8954	2.8780	2.8785	2.8613	2.8617
EPCSRST_N_4	B36	2.9188	2.9197	2.9086	2.9099	2.8886	2.8901	2.8690	2.8710	2.8490	2.8515
EPCSRST_N_5	B37	2.9190	2.9201	2.9095	2.9109	2.8906	2.8932	2.8720	2.8752	2.8535	2.8575
MONITOR	K23	2.9188	2.9200	2.9104	2.9112	2.8930	2.8950	2.8758	2.8784	2.8587	2.8618
PLL_MON	L20	2.9198	2.9208	2.9123	2.9135	2.8964	2.8983	2.8812	2.8835	2.8663	2.8689
TOGGLE_MON	L22	2.9199	2.9207	2.9116	2.9126	2.8957	2.8967	2.8802	2.8809	2.8643	2.8655

Table. 24. LVTTL VOL – DUT 9738

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin #	Pre Rad	Post Rad	Pre Rad	Post Rad	Pre Rad	Post Rad	Pre Rad	Post Rad	Pre Rad	Post Rad
TID_BUF_OUT	A33	218.759	215.000	229.633	228.134	252.474	242.834	275.158	261.673	298.531	282.185
EPCSRST_N_0	B31	217.041	215.063	226.164	228.384	244.600	243.524	263.847	262.864	283.246	283.907
EPCSRST_N_1	B32	217.063	213.848	225.470	222.598	243.532	239.004	262.001	256.630	281.040	274.996
EPCSRST_N_2	B34	217.751	214.973	226.657	224.317	244.845	241.411	263.626	259.942	282.849	278.812
EPCSRST_N_3	B35	216.876	214.723	224.470	223.067	240.938	238.754	257.845	255.630	275.123	273.126
EPCSRST_N_4	B36	219.220	215.754	229.501	225.535	250.845	243.630	272.720	262.786	294.846	282.754
EPCSRST_N_5	B37	217.282	214.535	225.845	223.723	244.063	240.254	262.470	258.005	281.040	276.264
MONITOR	K23	215.592	213.472	223.686	222.601	241.625	237.702	258.970	254.304	276.529	271.528
PLL_MON	L20	215.401	213.137	224.309	221.168	238.344	234.949	253.910	249.543	270.645	265.347
TOGGLE_MON	L22	215.906	213.796	223.127	221.212	238.476	236.198	253.949	251.654	270.017	267.529

Table. 25. LVTTL VOL – DUT 9741

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin #	Pre Rad	Post Rad	Pre Rad	Post Rad	Pre Rad	Post Rad	Pre Rad	Post Rad	Pre Rad	Post Rad
TID_BUF_OUT	A33	218.290	214.467	228.945	227.726	251.817	242.239	274.252	260.983	297.375	281.494
EPCSRST_N_0	B31	216.478	214.279	225.227	227.538	243.850	242.458	262.347	261.955	281.626	282.789
EPCSRST_N_1	B32	215.532	212.348	224.157	221.410	242.407	237.817	260.907	255.380	279.671	273.640
EPCSRST_N_2	B34	216.688	214.098	225.095	223.348	243.782	240.536	262.313	258.848	281.216	277.921
EPCSRST_N_3	B35	215.438	212.910	223.188	221.785	239.813	237.629	256.813	254.661	274.420	271.946
EPCSRST_N_4	B36	219.532	214.410	231.688	224.348	256.532	242.567	281.407	261.567	306.692	281.474
EPCSRST_N_5	B37	216.813	214.066	224.751	222.817	243.095	239.473	261.407	256.848	279.909	275.184
MONITOR	K23	214.936	212.721	222.530	221.538	240.031	236.765	256.782	253.179	274.030	270.121
PLL_MON	L20	214.088	211.637	222.715	219.574	236.406	233.887	251.722	248.543	267.989	264.341
TOGGLE_MON	L22	213.687	211.919	221.220	219.710	236.600	234.978	251.636	250.121	267.240	265.948

Table. 26. LVTTL VOL – DUT 9752

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin #	Pre Rad	Post Rad	Pre Rad	Post Rad	Pre Rad	Post Rad	Pre Rad	Post Rad	Pre Rad	Post Rad
TID_BUF_OUT	A33	214.322	210.800	225.540	224.090	247.755	238.509	270.128	257.316	293.344	277.534
EPCSRST_N_0	B31	212.447	210.894	221.353	224.497	239.632	239.669	258.254	258.852	277.369	279.897
EPCSRST_N_1	B32	212.251	209.348	220.720	218.535	238.345	234.629	256.438	251.942	274.960	269.774
EPCSRST_N_2	B34	213.126	211.160	222.001	220.223	240.157	237.692	258.345	255.786	277.234	274.795
EPCSRST_N_3	B35	212.063	210.066	219.688	218.879	236.470	234.754	252.969	251.755	270.073	269.109
EPCSRST_N_4	B36	213.407	211.254	222.845	221.379	241.845	239.504	260.626	258.692	280.738	278.561
EPCSRST_N_5	B37	212.563	210.254	221.407	219.379	239.845	236.286	258.345	254.286	277.208	272.523
MONITOR	K23	211.998	209.908	219.499	218.975	236.656	233.826	253.500	249.771	270.953	267.017
PLL_MON	L20	210.806	208.543	219.308	217.324	232.811	230.730	247.721	245.324	263.834	260.960
TOGGLE_MON	L22	210.749	209.072	218.001	216.800	233.568	232.193	249.041	247.555	264.929	263.589

Table. 27. LVTTL VOL – DUT 9774

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin #	Pre Rad	Post Rad	Pre Rad	Post Rad	Pre Rad	Post Rad	Pre Rad	Post Rad	Pre Rad	Post Rad
TID_BUF_OUT	A33	216.541	213.433	226.852	226.347	248.630	240.734	270.440	259.416	292.502	279.382
EPCSRST_N_0	B31	215.197	213.276	224.102	226.692	242.850	241.800	261.629	260.983	281.023	281.959
EPCSRST_N_1	B32	214.813	211.910	223.470	221.098	241.126	237.254	258.970	254.067	277.560	272.172
EPCSRST_N_2	B34	216.376	213.629	225.345	223.067	243.532	240.192	262.376	258.255	281.517	276.967
EPCSRST_N_3	B35	214.970	213.004	222.563	221.473	239.157	237.286	255.532	254.067	272.849	271.356
EPCSRST_N_4	B36	216.907	214.879	226.438	224.817	245.220	243.036	264.532	262.005	284.658	281.963
EPCSRST_N_5	B37	216.063	213.848	224.470	222.598	242.688	239.661	261.376	257.411	279.997	276.000
MONITOR	K23	214.467	211.815	223.061	220.569	242.375	235.858	261.157	252.116	280.133	269.304
PLL_MON	L20	212.775	210.793	221.340	218.762	235.124	232.824	250.034	247.605	266.100	263.323
TOGGLE_MON	L22	213.437	211.888	220.439	219.553	235.631	234.477	250.761	249.870	266.424	265.898

Table. 28. LVTTL VOL – DUT 9793

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin #	Pre Rad	Post Rad	Pre Rad	Post Rad	Pre Rad	Post Rad	Pre Rad	Post Rad	Pre Rad	Post Rad
TID_BUF_OUT	A33	218.759	215.407	229.477	228.165	252.942	242.396	276.346	261.046	299.987	281.154
EPCSRST_N_0	B31	216.447	214.624	224.633	228.008	243.881	242.928	263.066	262.394	282.367	283.442
EPCSRST_N_1	B32	216.220	213.379	224.751	222.692	242.845	239.098	261.001	256.723	279.909	274.733
EPCSRST_N_2	B34	217.032	214.879	225.563	224.098	243.907	241.348	262.032	259.442	281.040	278.498
EPCSRST_N_3	B35	216.345	214.473	223.970	223.067	240.595	239.004	257.563	255.911	274.658	273.264
EPCSRST_N_4	B36	217.720	215.848	226.938	225.910	246.938	244.192	266.470	263.130	286.731	283.294
EPCSRST_N_5	B37	217.563	215.129	225.876	224.285	244.376	241.036	263.220	258.911	282.233	277.293
MONITOR	K23	215.873	214.035	223.030	222.945	240.875	238.203	257.844	254.492	274.733	271.402
PLL_MON	L20	214.276	212.762	222.903	220.824	237.031	234.699	252.159	249.543	268.354	265.045
TOGGLE_MON	L22	214.312	212.576	221.721	220.899	237.538	236.323	253.136	251.998	269.125	267.980

E. Propagation Delay

Table 29 lists the pre-irradiation and post-irradiation propagation delay measurements. It shows that the change due to radiation on each DUT is not significant and every DUT passes the 10% degradation criterion.

Table. 29. Pre-irradiation and Post-irradiation Propagation Delay Change

DUT	Total Dose	Pre-irradiation (µs)	Post-irradiation (µs)	Change Degradation (%)
9738	125 krad	0.461	0.461	0
9741	125 krad	0.464	0.462	-0.43
9752	125 krad	0.460	0.457	-0.65
9774	100 krad	0.458	0.457	-0.21
9793	100 krad	0.458	0.458	0

F. Transition Time

The figures below show the pre-irradiation and post-annealing transitions edges. In each case the radiation induced transition degradation is not observable.

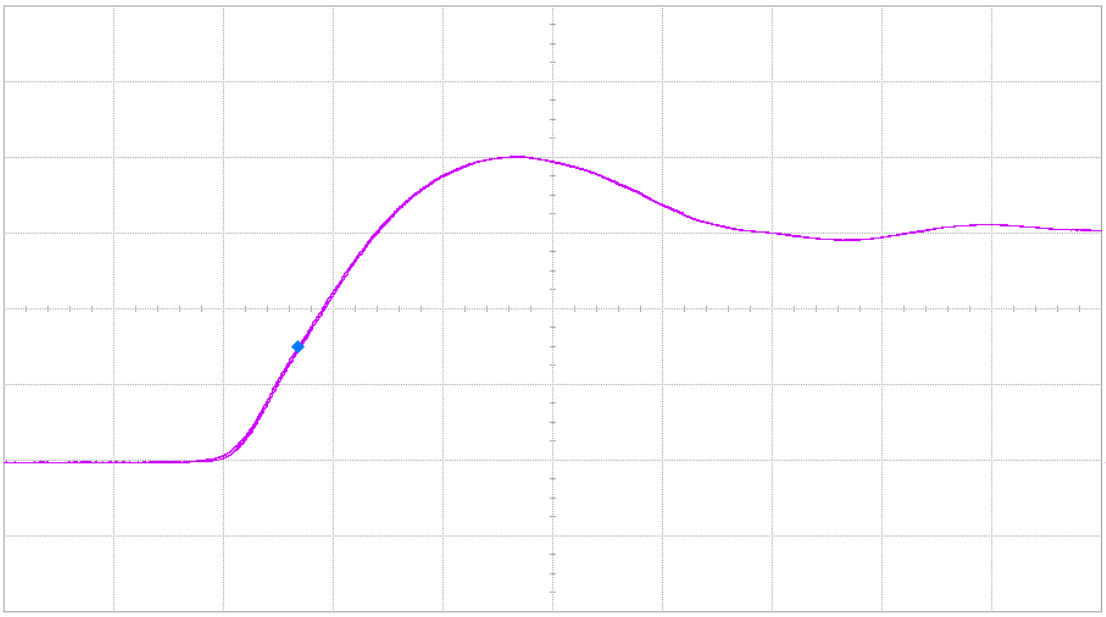

Fig. 18 (a). DUT 9738 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

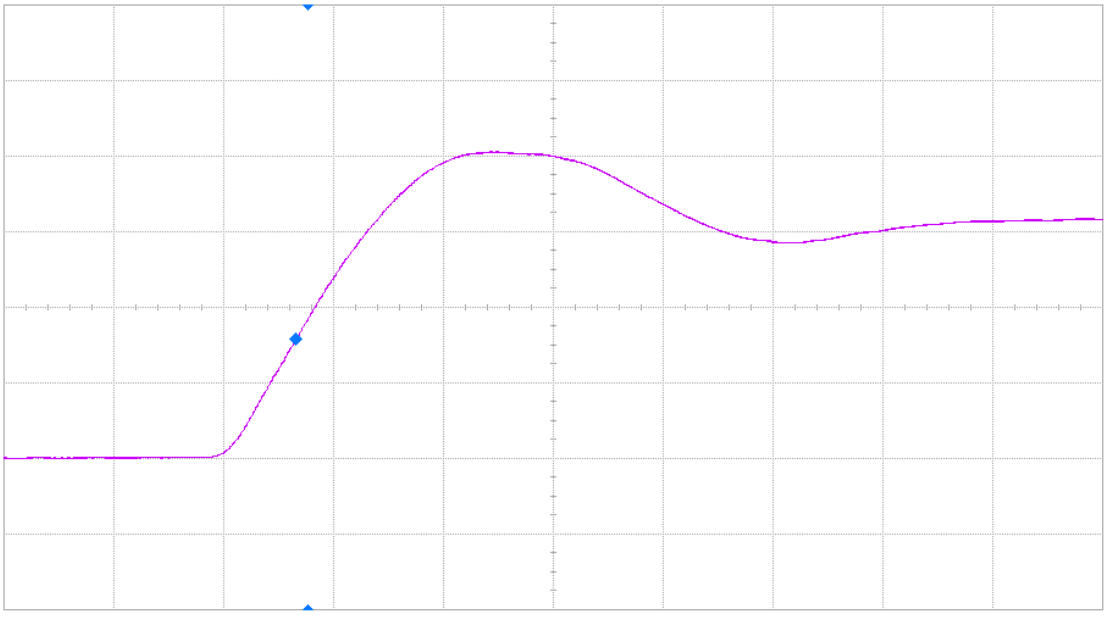

Fig. 18 (b). DUT 9738 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

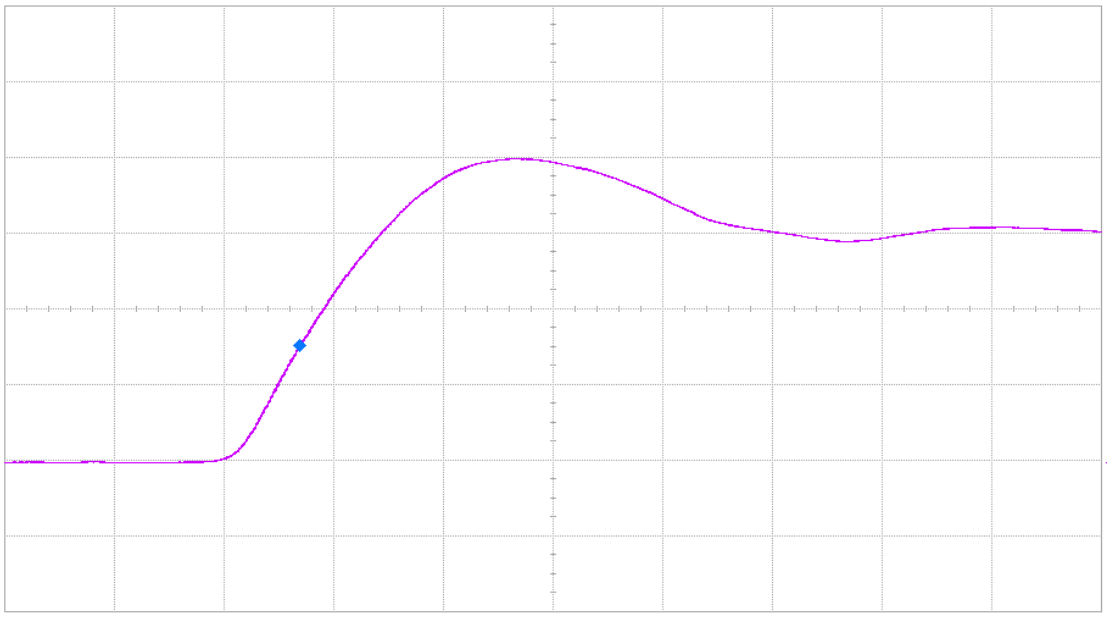

Fig. 19 (a). DUT 9741 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

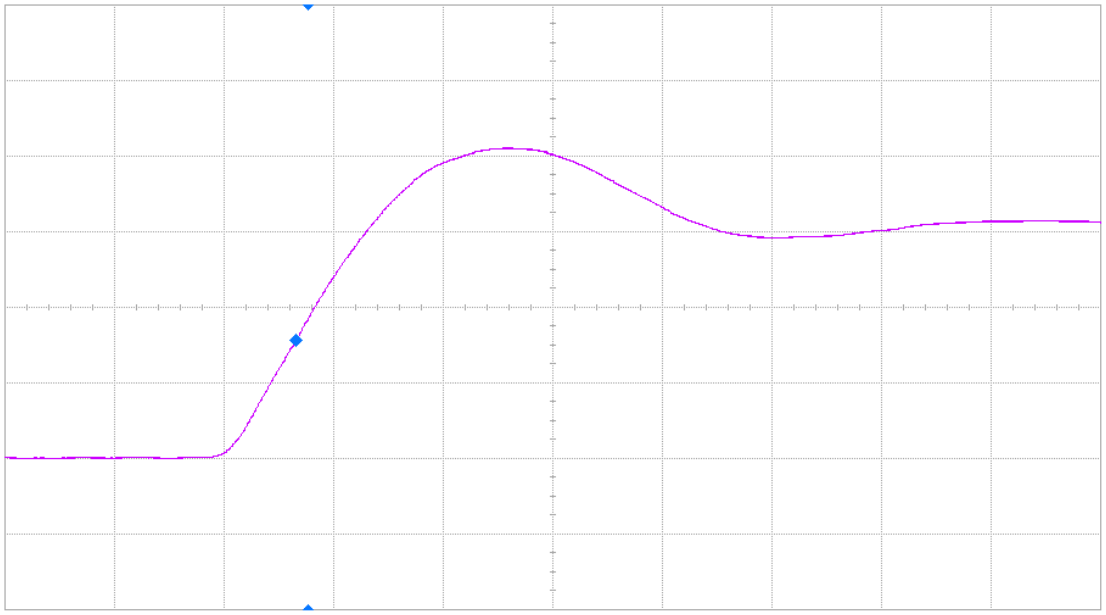

Fig. 19 (b). DUT 9741 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

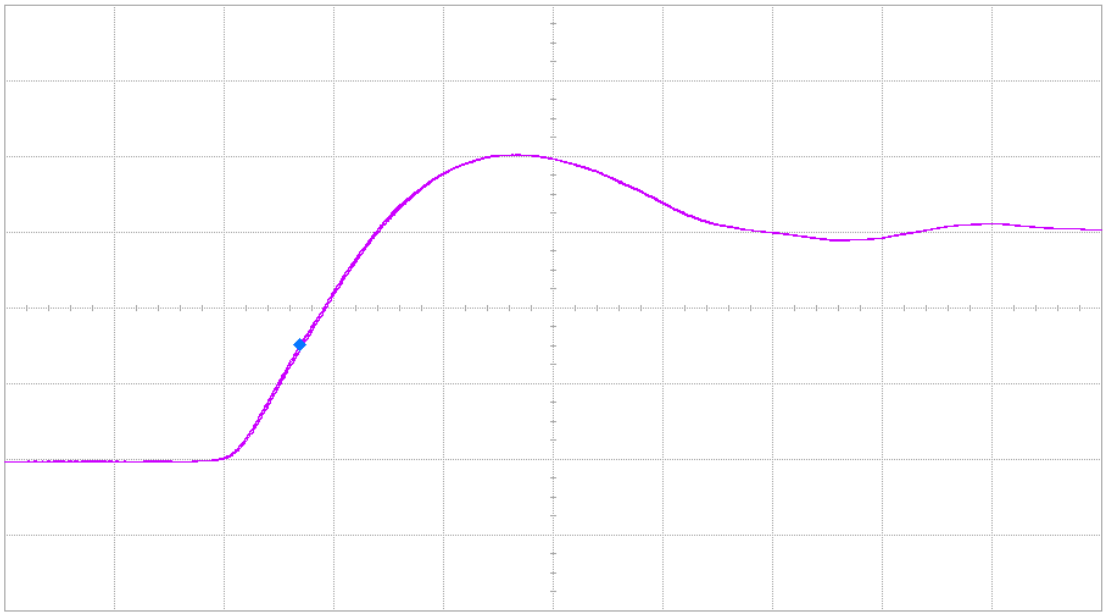

Fig. 20 (a). DUT 9752 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

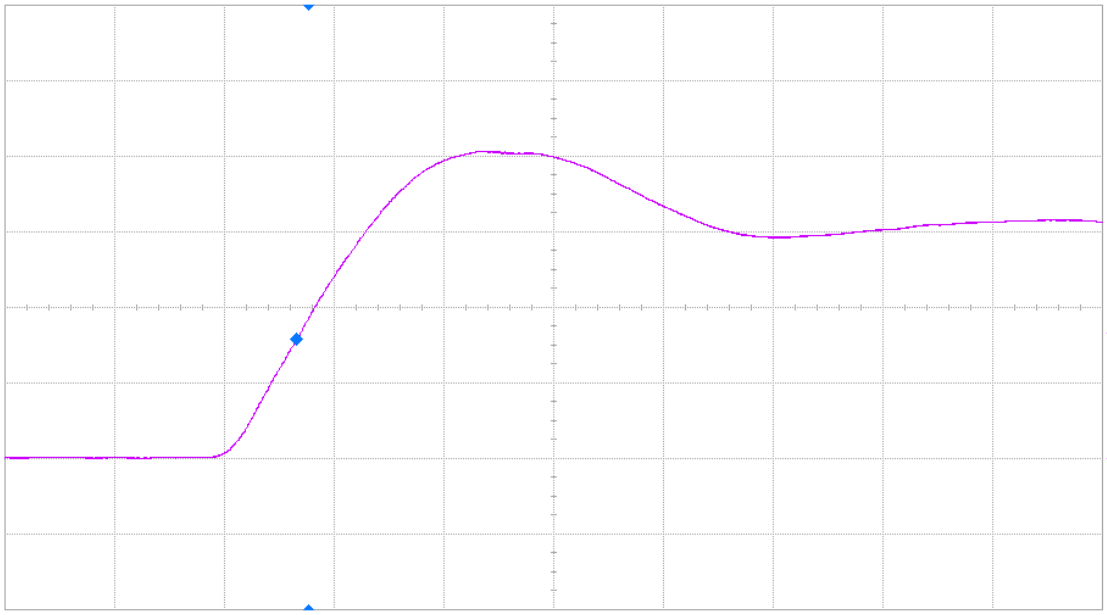

Fig. 20 (b). DUT 9752 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

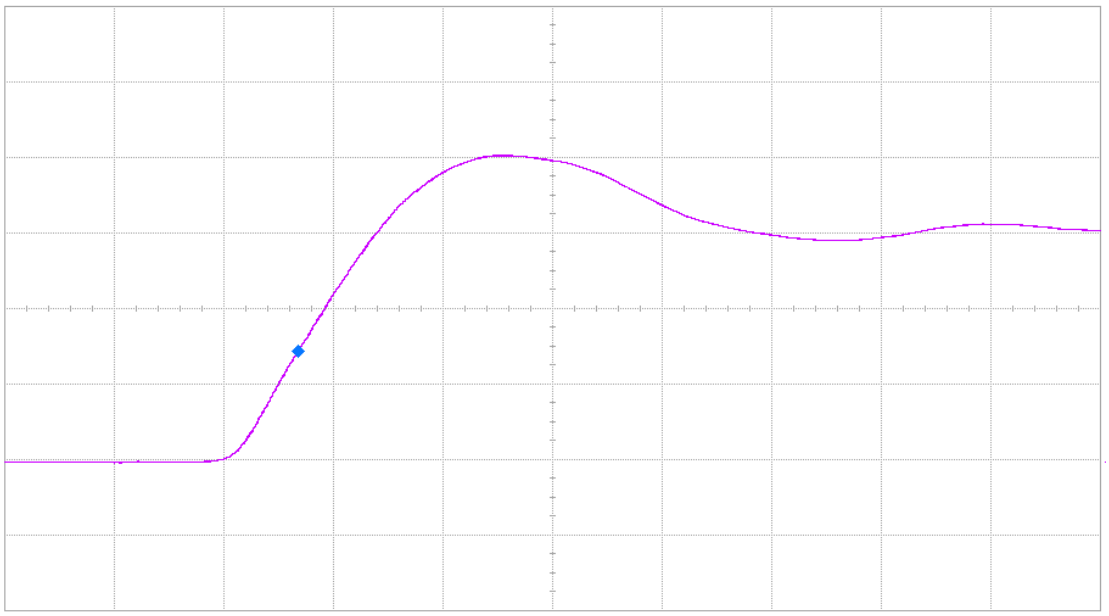

Fig. 21 (a). DUT 9774 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

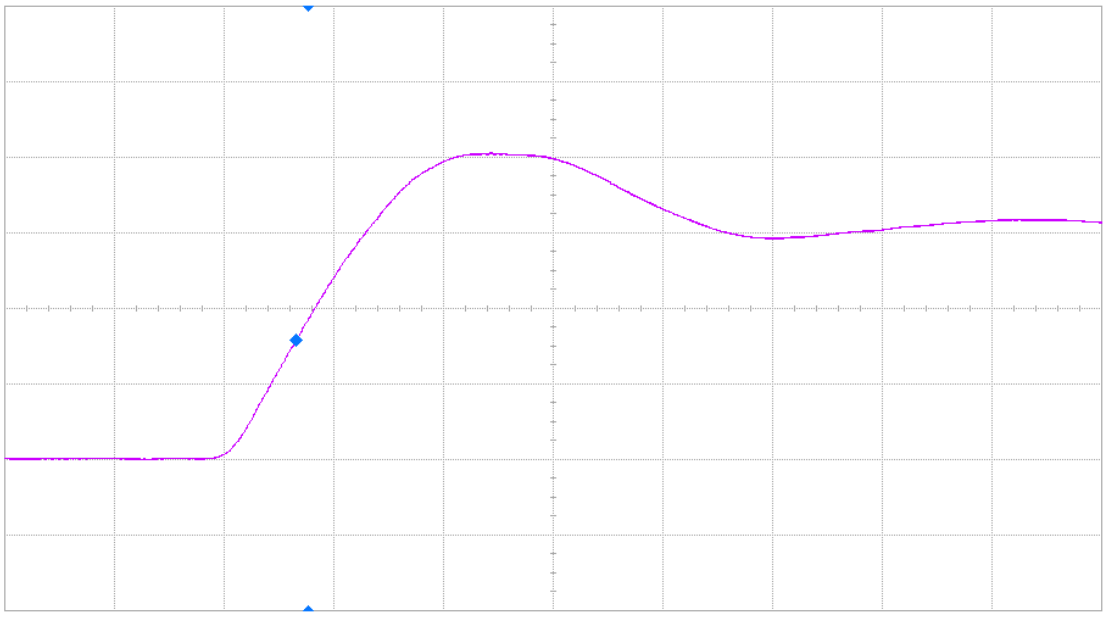

Fig. 21 (b). DUT 9774 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

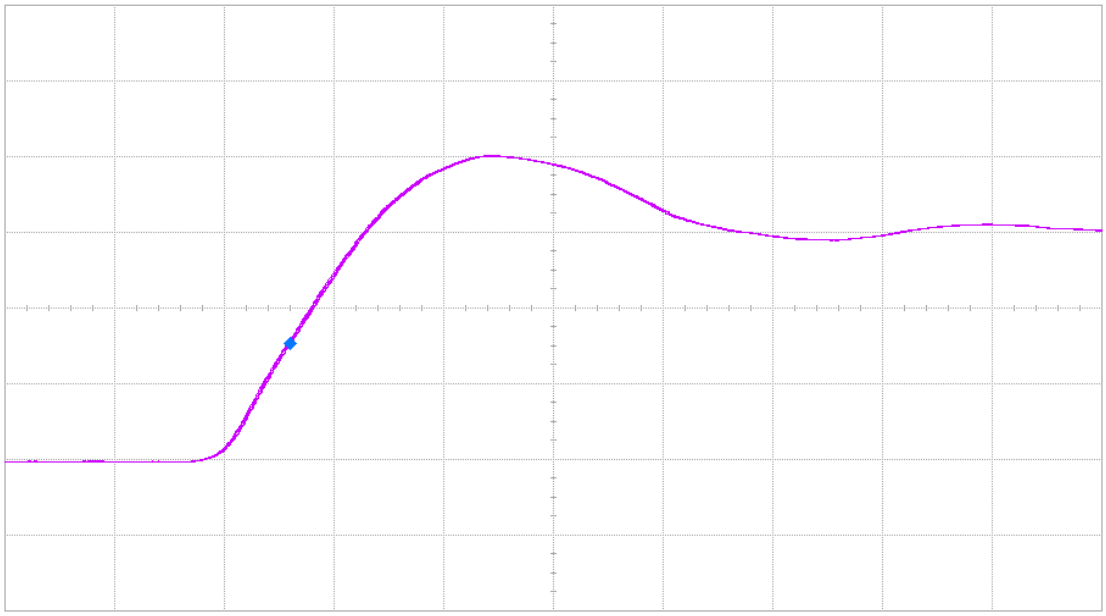

Fig. 22 (a). DUT 9793 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

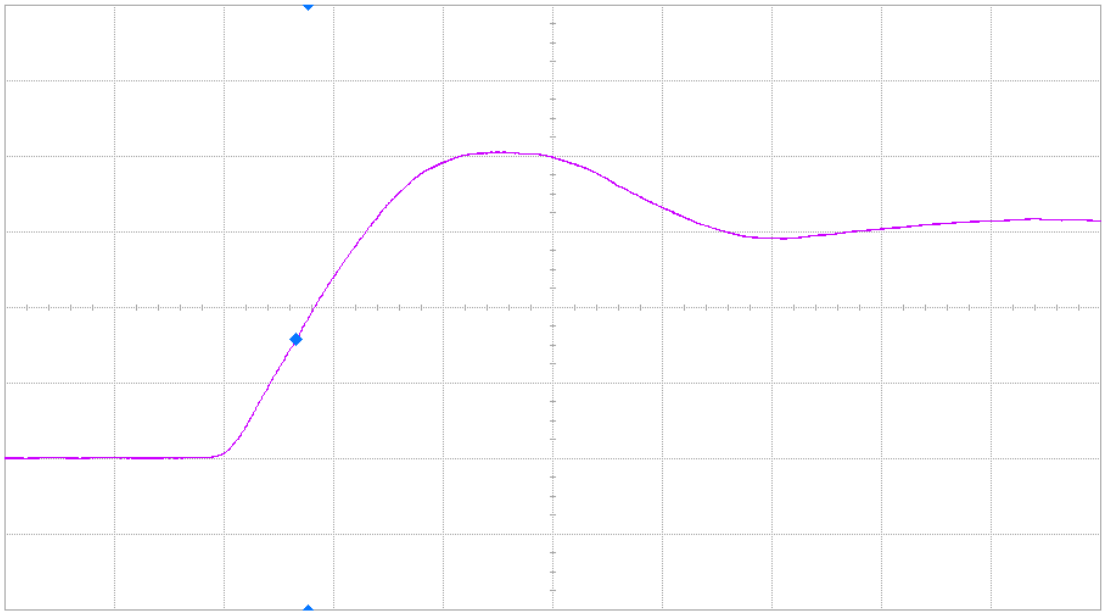

Fig. 22 (b). DUT 9793 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

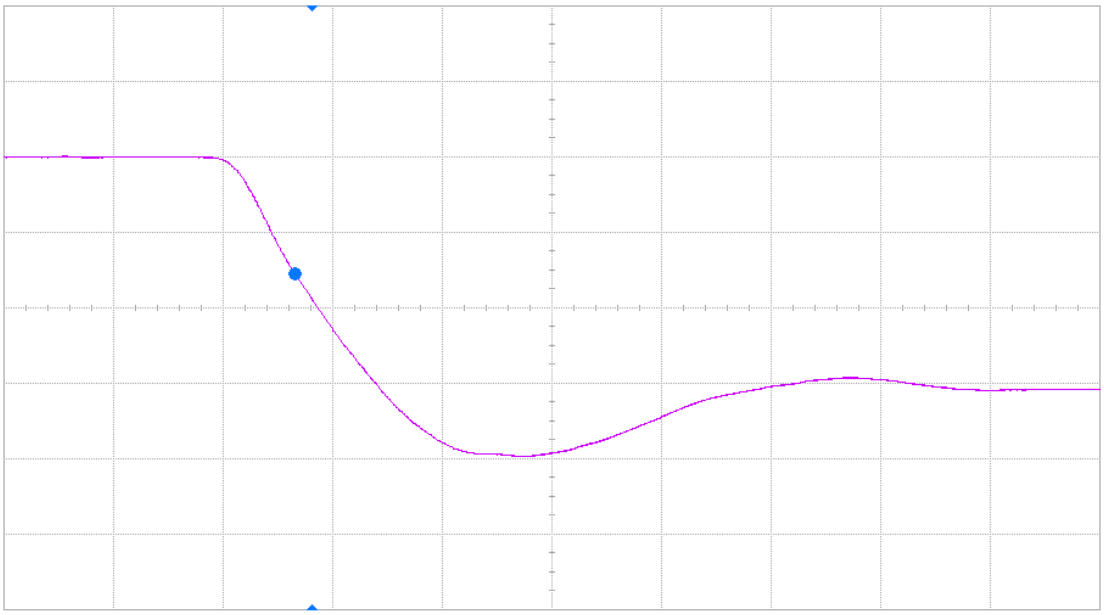

Fig. 23 (a). DUT 9738 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

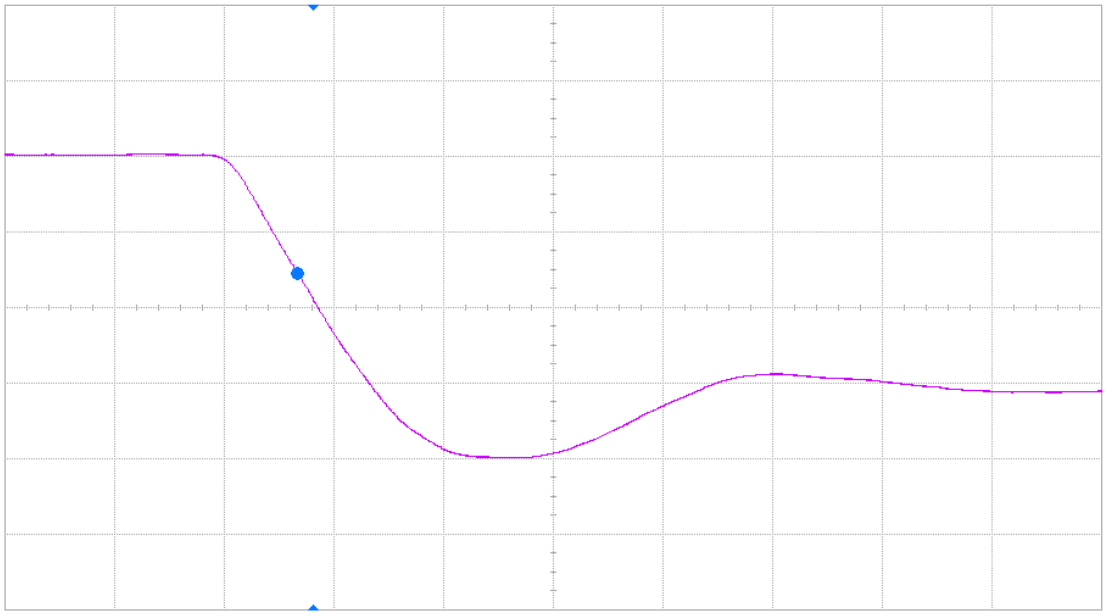

Fig. 23 (b). DUT 9738 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

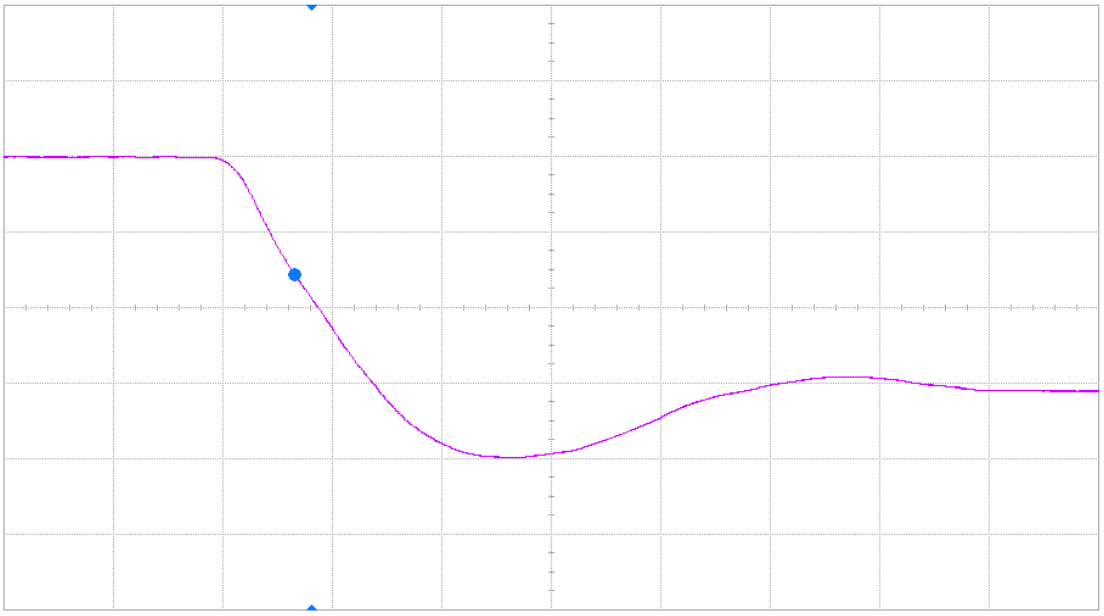

Fig. 24 (a). DUT 9741 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

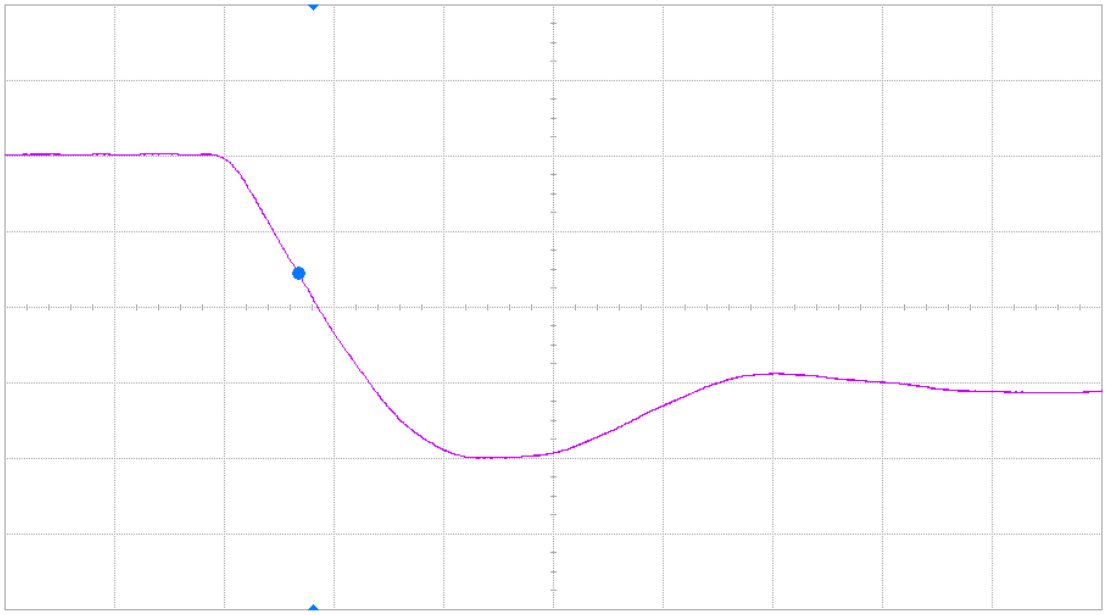

Fig. 24 (b). DUT 9741 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

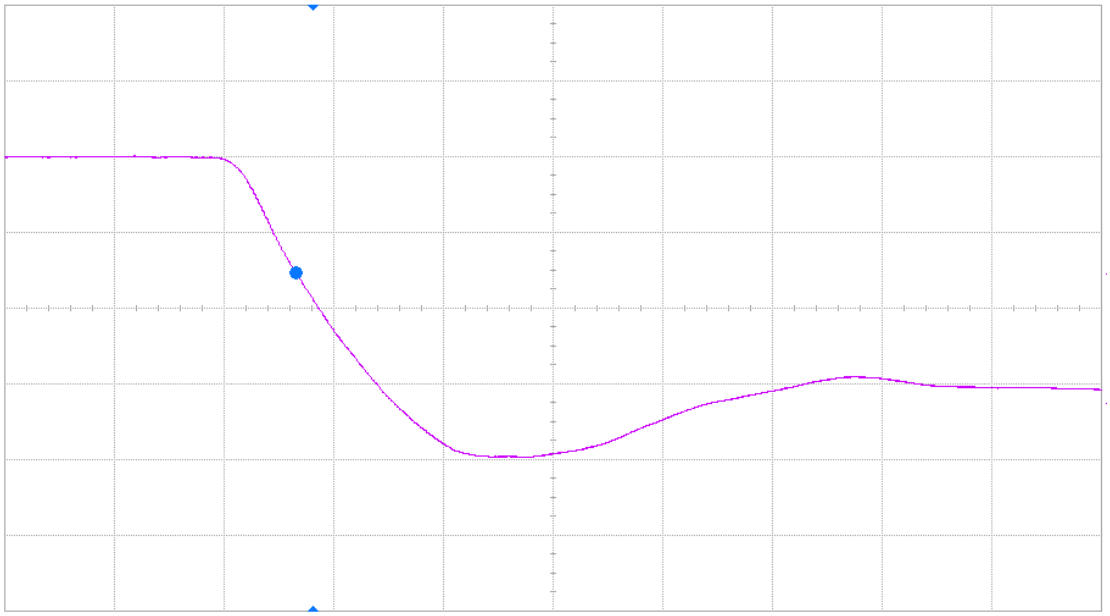

Fig. 25 (a). DUT 9752 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

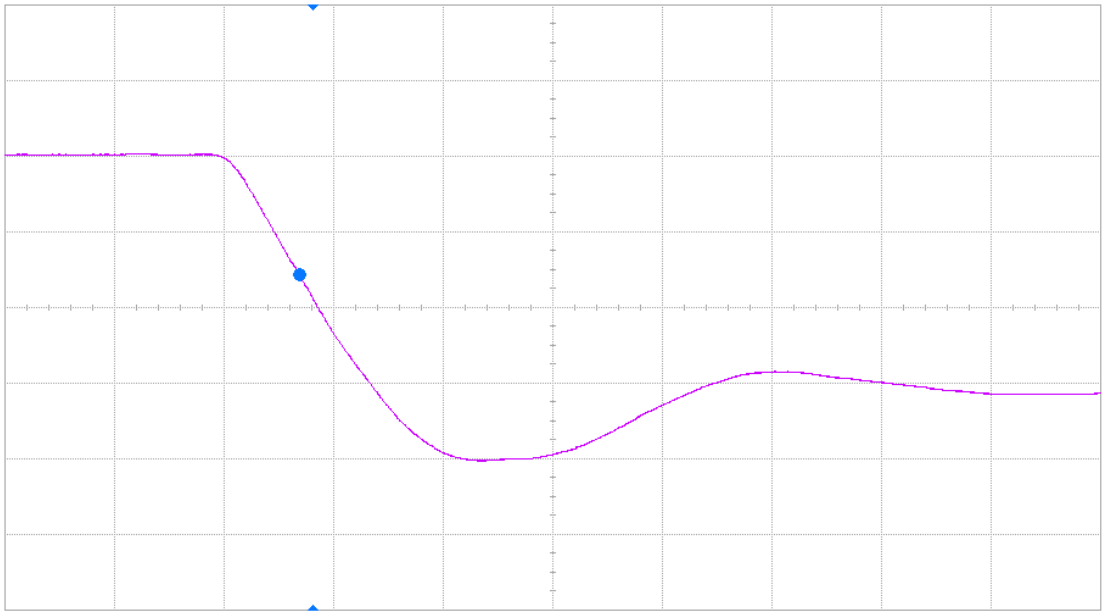

Fig. 25 (b). DUT 9752 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

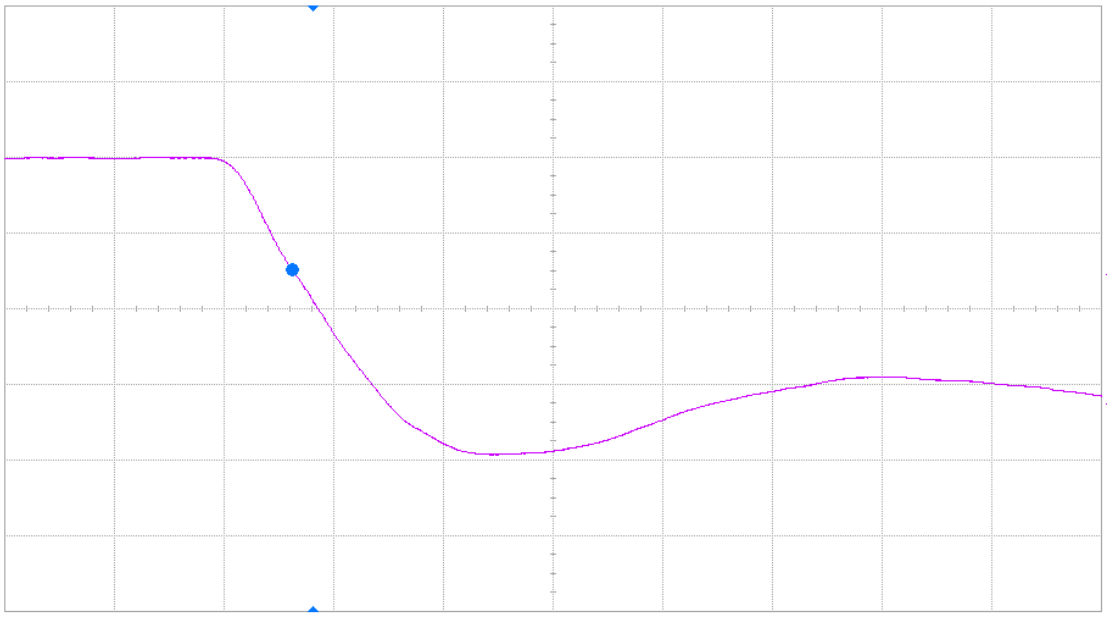

Fig. 26 (a). DUT 9774 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

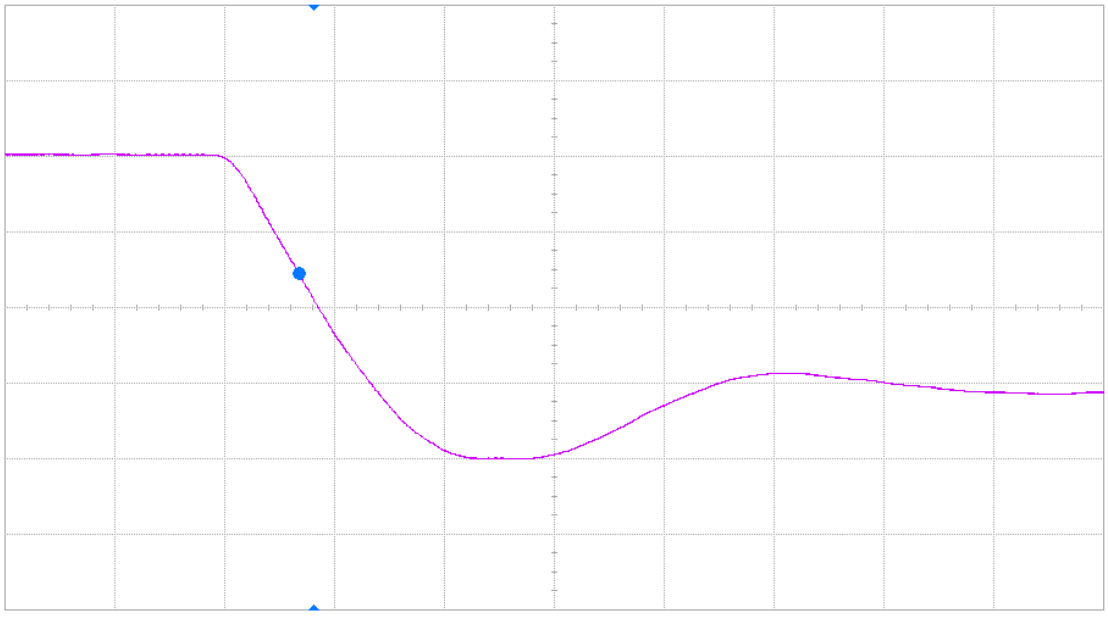

Fig. 26 (b). DUT 9774 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

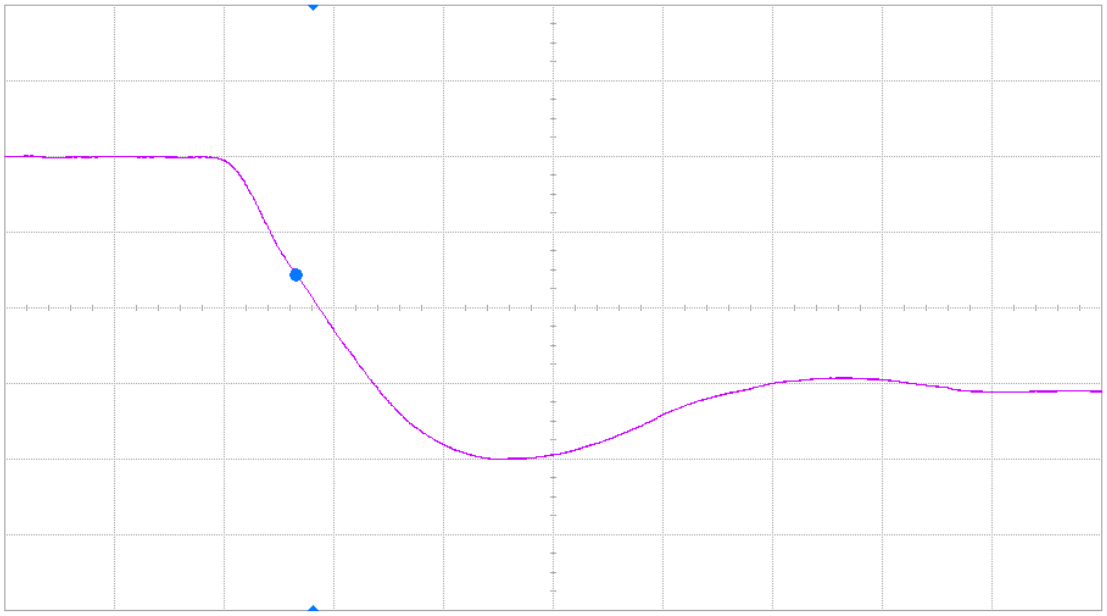

Fig. 27 (a). DUT 9793 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

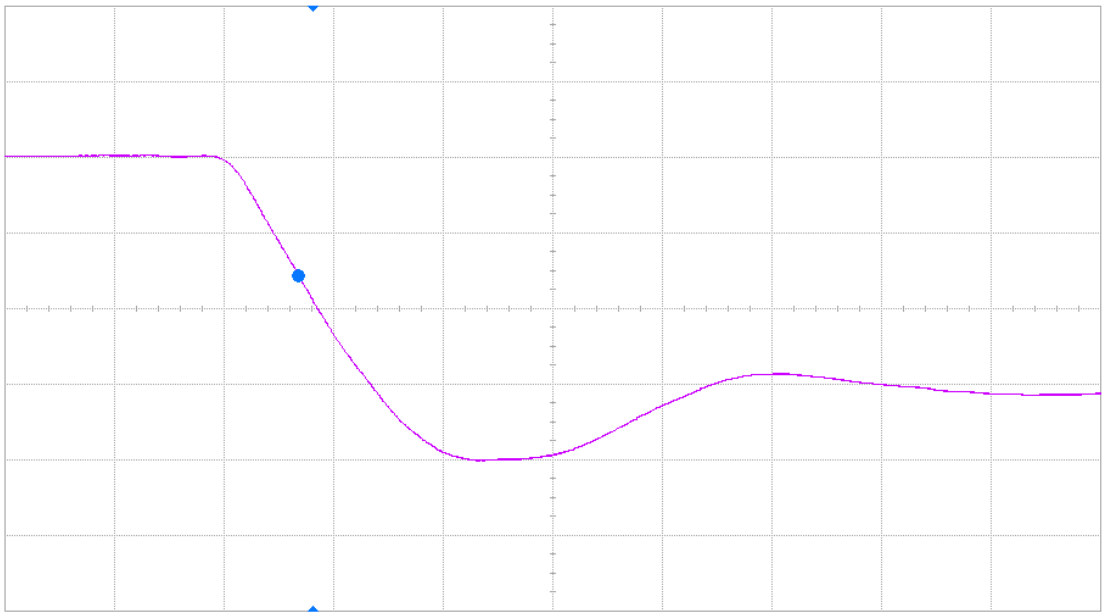

Fig. 27 (b). DUT 9793 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Appendix A

Table. 30. High level block diagrams of blocks used to perform fabric functional coverage pre and post-irradiation

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 uRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
IO Block	IO utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

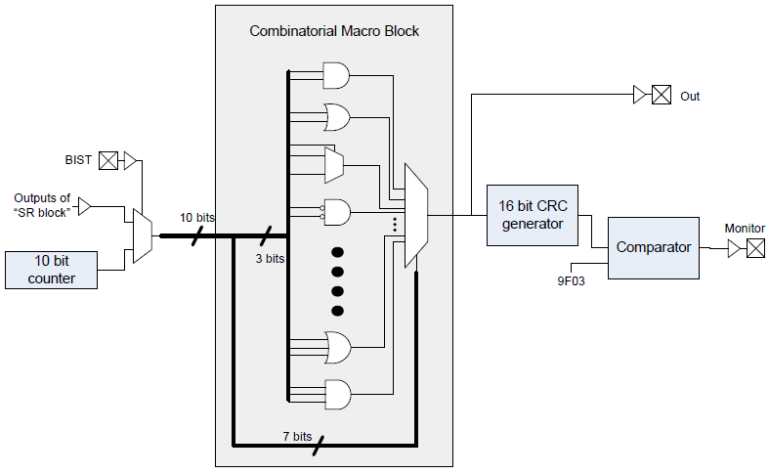

Fig. 28. Combo Block

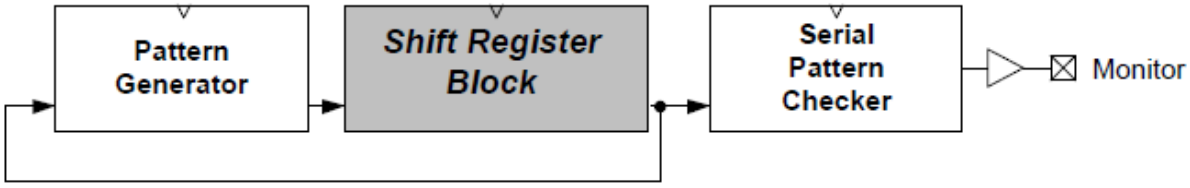

Fig. 29. Shift Register Block

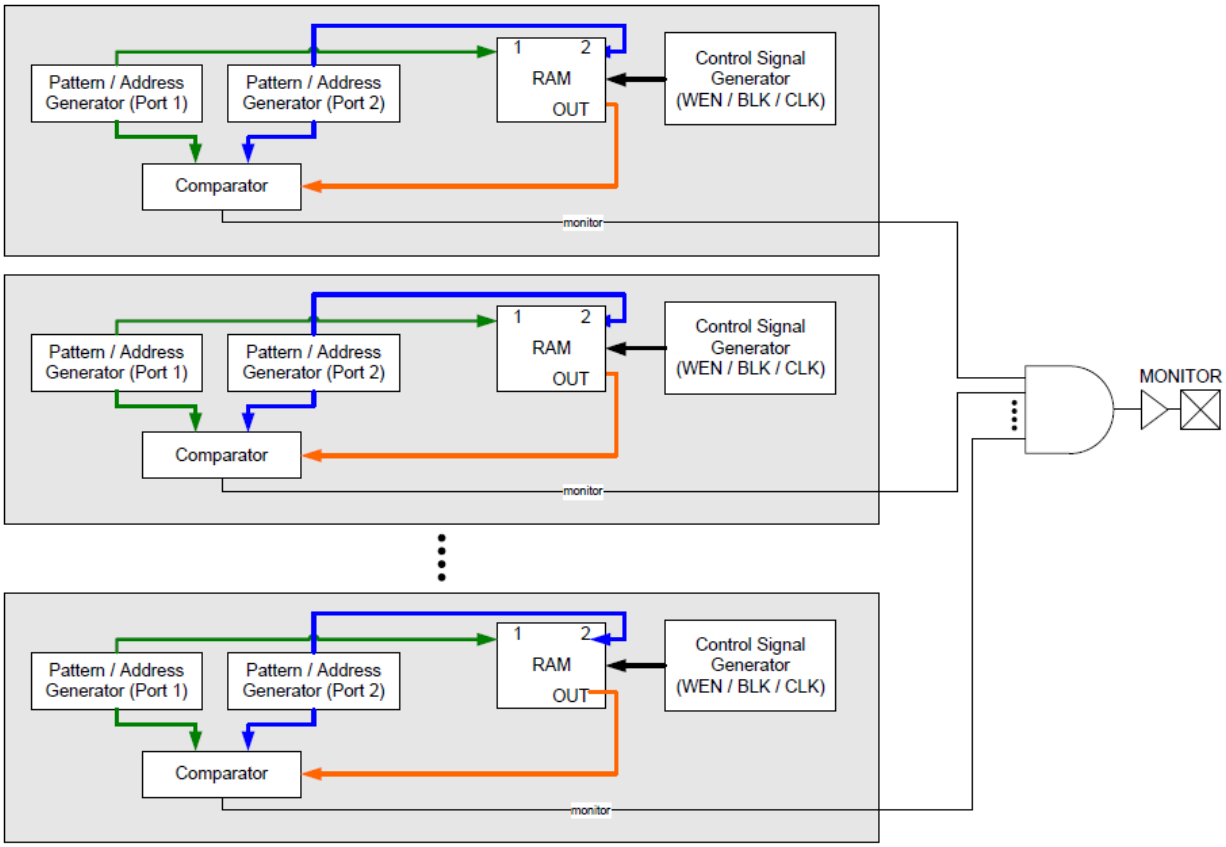

Fig. 30. Embedded Ram Blocks

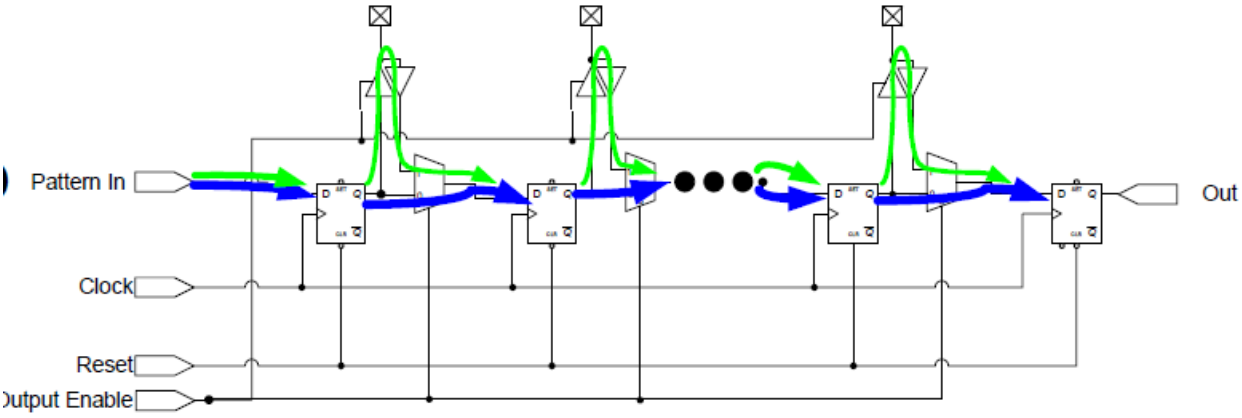

Fig. 31. IO Block

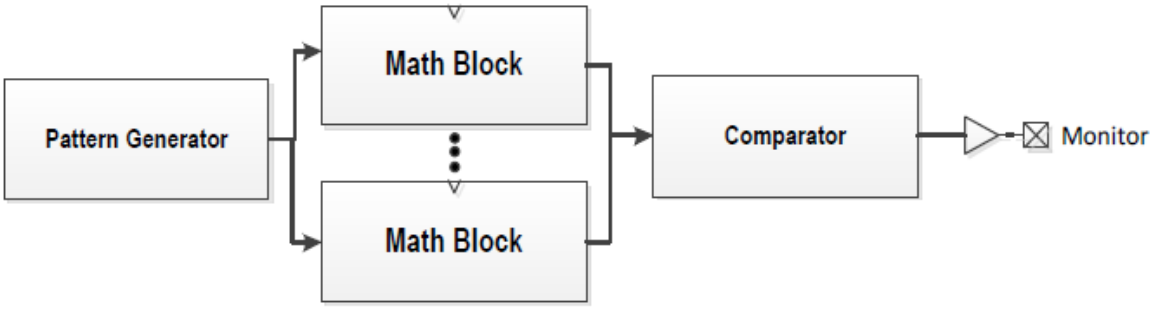

Fig. 32. Math Block