



Total Ionizing Dose Test Report

No. 16T-RT1460A-CQ196B-fp6128401

March 30, 2016

Table of Contents

I.	Summary Table	3
II.	Total Ionizing Dose (TID) Testing	3
A.	Device-Under-Test (DUT).....	3
B.	Irradiation.....	4
C.	Test Method.....	4
D.	Electrical Parameter Measurements	4
III.	Test Results	5
A.	Functional Test.....	5
B.	In-Flux and Post-Annealing ICC	5
C.	Input Logic Threshold.....	6
D.	Output Characteristic.....	6
E.	Propagation Delays	7
F.	Transition Characteristics	8

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I. Summary Table

Parameter	Tolerance
1. Gross Functionality	Pass 7.5 krad(SiO ₂)
2. I _{DDSTDBY}	Pass 7.5 krad(SiO ₂)
3. V _{IL} /V _{IH}	Pass 7.5 krad(SiO ₂)
4. V _{OL} /V _{OH}	Pass 7.5 krad(SiO ₂)
5. Propagation Delays	Pass 7.5 krad(SiO ₂)
6. Rising/Falling Edge Transient	Pass 7.5 krad(SiO ₂)

II. Total Ionizing Dose (TID) Testing

This section describes the device under test (DUT), the irradiation parameters, and the test method.

A. Device-Under-Test (DUT)

Table 1 lists the DUT information

Table 1 DUT Information

Part Number	RT1460A
Package	CQ196B
Foundry	MEC
Technology	0.8µm CMOS
Die Lot Number	FP6128401
Quantity Tested	6
Serial Numbers	9259, 9261, 9276, 9303, 9307, 9360

B. Irradiation

Table 2 lists the irradiation parameters.

Table 2 Irradiation Parameters

Facility	DMEA
Radiation Source	Co-60
Dose Rate	1krad(SiO ₂)/min(±10%)
Data Mode	Static
Temperature	Room
Bias	5.0V

C. Test Method

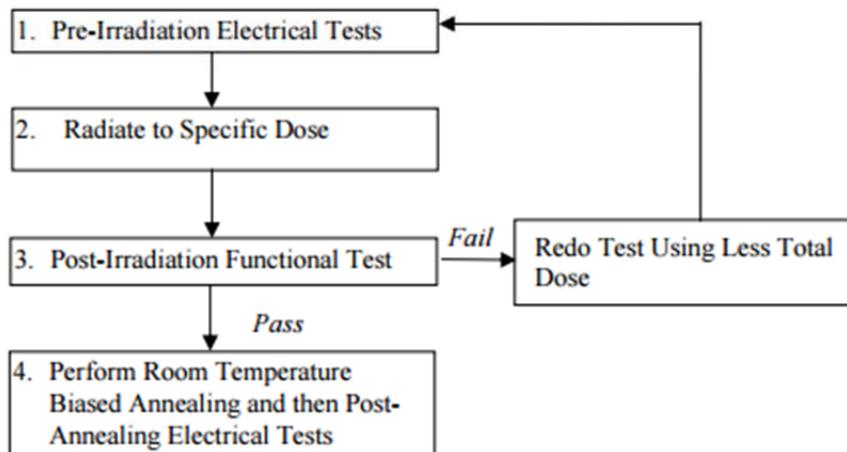


Figure 1 TID test flow chart

The test method is based on military standard TM1019.6. Figure 1 shows the flow chart of the testing sequence. The accelerated annealing test in section 3.12 is not performed lot-to-lot. This is because, for the CMOS technology used by the RT1460A product, the adverse effects due to interface state at the gate SiO₂/Si interface are negligible; the dominant annealing effect in this device is the reduction of trapped holes in the SiO₂. Therefore, the accelerated annealing alleviates the radiation effects on the DUT.

TM1019.6 section 3.11 extended room temperature anneal test is also applied; room temperature annealing for approximately 5 days was done on each device before the final parameter measurements.

D. Electrical Parameter Measurements

The electrical parameters were measured on the bench. Compared to an automatic tester, this bench setup has less noise, while it samples selected pins for threshold voltage measurements. The conservative dose level used to measure the parameters usually is too low to show any threshold voltage changes. I_{CC} usually dictates the dose level for parameter measurements, and consequently determines the radiation tolerance. Therefore, sampling few pins is sufficient to prove that the radiation effects cause no concerns on the threshold voltages. Other advantages for this bench setup are the in-flux measurement of I_{CC} and the measurement of the signal transient characteristic. Table 3 lists the corresponding logic design for each electrical measurement.

Table 3 Logic Design for each Measured Parameter

Parameter/Characteristics	Logic Design
1. Functionality	All key architectural Functions
2. I_{cc}	DUT power supply
3. V_{IL}/V_{IH}	TTL compatible input buffer
4. V_{OL}/V_{OH}	TTL compatible output buffer
5. Propagation Delays	String of inverters
6. Rising/Falling Edge	TTL compatible output

III. Test Results

A. Functional Test

Referring to Figure 1, the post irradiation functional test is performed on one IO design. Based on extensive database, the functionality versus total dose is determined by the TID tolerance of the charge pump; this test provides a fast and effective test for on-site post-irradiation functional test. The post annealing functional test is performed on key architectural functions includes IO, combinational logic, and shift registers. Power Supply Current (ICC)

Every DUT passed the post-irradiation and post-annealing functional tests.

B. In-Flux and Post-Annealing ICC

Table 4 Pre-irradiation, Post-irradiation and Post-annealing ICC

DUT	Total Dose krad(SiO ₂)	I_{cc} (mA)		
		Pre-irrad	Post-Irrad	Post-ann
9259	7.5	0.675	10.35	0.852
9261	7.5	0.762	9.63	0.809
9276	7.5	0.654	9.33	1.00
9303	7.5	0.72	10.05	1.33
9307	7.5	0.688	21.59	1.89
9360	7.5	0.651	21.30	1.79

Table 4 shows the pre-irradiation and post-irradiation ICC.

C. Input Logic Threshold

Table 5 lists the input logic threshold of each DUT for pre-irradiation and post-annealing; every data is within the spec, and the radiation-induced Δ is within $\pm 10\%$.

Table 5 Input Logic Threshold (V_{IL}/V_{IH}) Results (V)

DUT	$V_{IL}(V)$		$V_{IH}(V)$	
	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
9259	1.2600	1.2650	1.2550	1.2600
9261	1.2600	1.2650	1.2550	1.2600
9276	1.2650	1.2700	1.2600	1.2650
9303	1.2600	1.2650	1.2550	1.2600
9307	1.2550	1.2600	1.2500	1.2550
9360	1.2600	1.2650	1.2550	1.2600

D. Output Characteristic

Table 6 shows the V_{OL} characteristics for the pre-irradiated and post-annealed DUT; every data is within the spec. The spec is that when $I_{OL} = 6$ mA, V_{OL} cannot exceed 0.4 V

Table 6 VOL for various drive currents

DUT	V_{OL} (mV)	
	Pre-Irrad	Post-Ann
9259	94.4339	93.3028
9261	93.8684	94.8109
9276	95.1879	94.9994
9303	96.5074	94.4339
9307	93.4913	100.2776
9360	95.7534	95.9419

Table 7 shows the V_{OH} characteristic for the pre-irradiated and post-annealed DUT; every data point is within the spec. The spec is that when $I_{OH} = -4$ mA, V_{OH} cannot be lower than 3.7 V.

Table 7 VOH for various drive currents

DUT	V_{OH} (V)	
	Pre-Irrad	Post-Ann
9259	4.7660	4.7632
9261	4.7626	4.7611
9276	4.7634	4.7615
9303	4.7658	4.7683
9307	4.7658	4.7647
9360	4.7660	4.7645

E. Propagation Delays

Tables 8a and 8b list the pre-irradiation and post-annealing propagation delays. The results show small radiation effects; in any case the percentage change is below $\pm 10\%$

Table 8a Radiation-Induced Propagation Delay Degradations (L to H Transition)

DUT	Pre-Irradiation (ns)	Post-Irradiation(ns)	Post-Anneal (ns)	Degradation (%)
9259	79.8	82	80.6	1.00%
9261	79.8	84	80.0	0.24%
9276	79.3	83	79.4	0.19%
9303	78.1	89	80.0	2.43%
9307	79.2	96	81.3	2.66%
9360	79.8	97	82.1	2.83%

Table 8b Radiation-Induced Propagation Delay Degradations (H to L Transition)

DUT	Pre-Irradiation (ns)	Post-Irradiation(ns)	Post-Anneal (ns)	Degradation (%)
9259	109.1	111	109.6	0.46%
9261	109.2	112	108.8	-0.32%
9276	108.4	111.4	107.8	-0.54%
9303	108.4	110.4	108.3	-0.10%
9307	109.1	113	109.1	0.00%
9360	109.5	113.5	109.5	0.05%

F. Transition Characteristics

The rising and falling edge transient of an output is measured pre-irradiation and post-annealing. Figures 2 to 13 show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition time degradation is not observable.

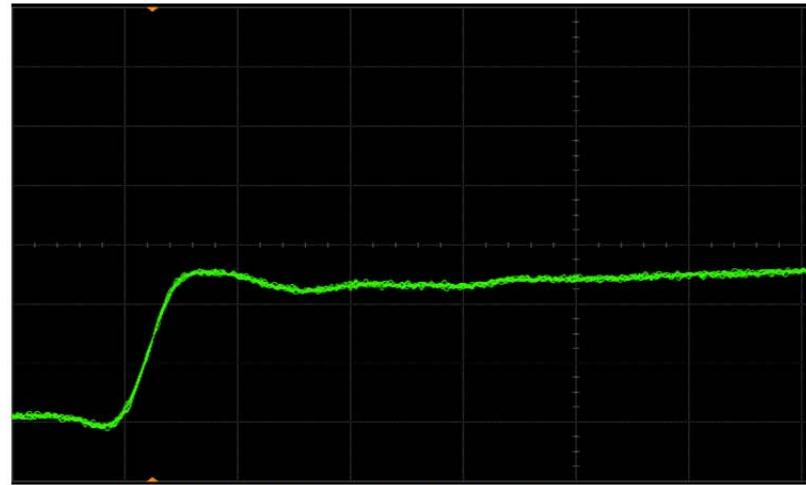


Figure 2a DUT 9259 Pre-Irradiation Rising Edge

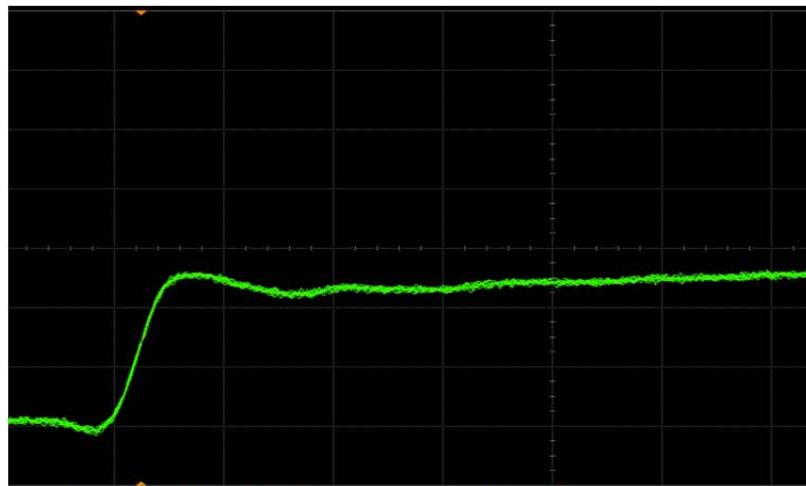


Figure 2b DUT 9259 Post-Annealing Rising Edge

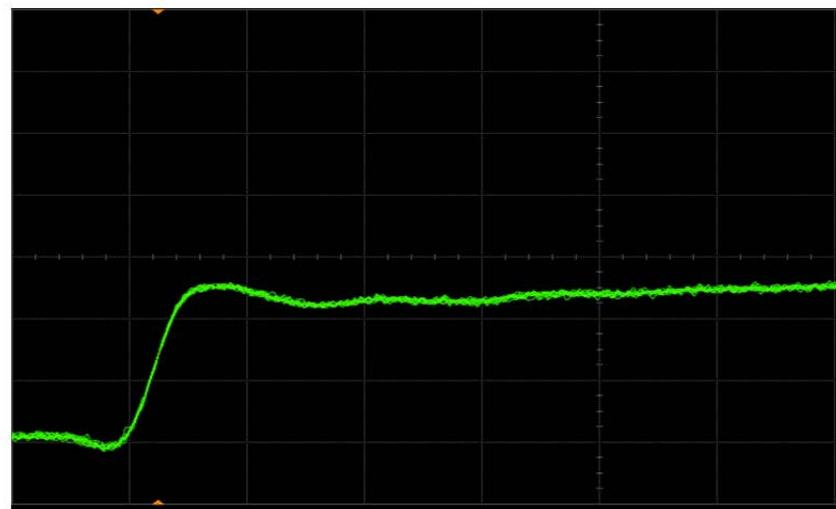


Figure 3a DUT 9261 Pre-Irradiation Rising Edge



Figure 3b DUT 9261 Post-Annealing Rising Edge

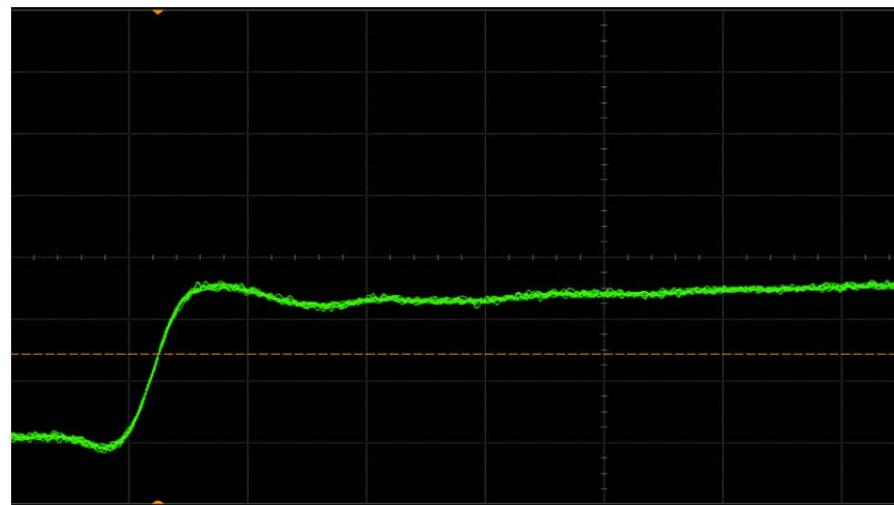


Figure 4a DUT 9276 Pre-Radiation Rising Edge

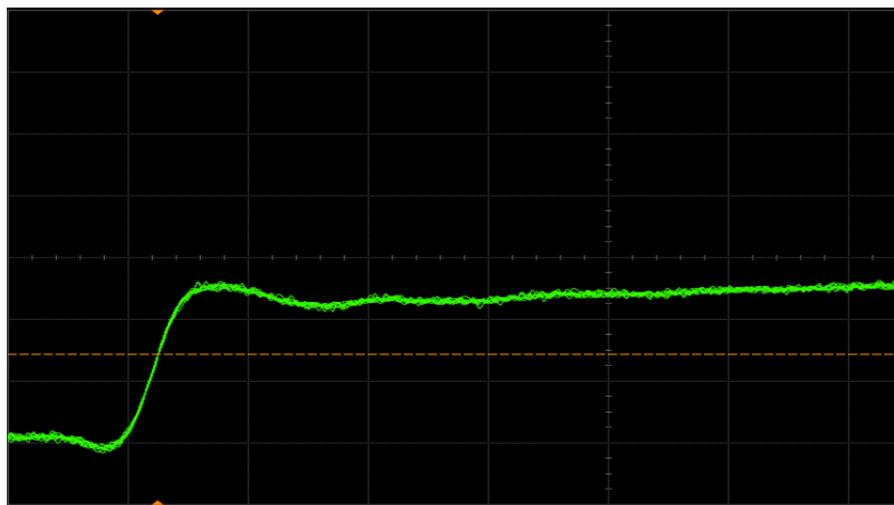


Figure 4b DUT 9276 Post-Annealing Rising edge

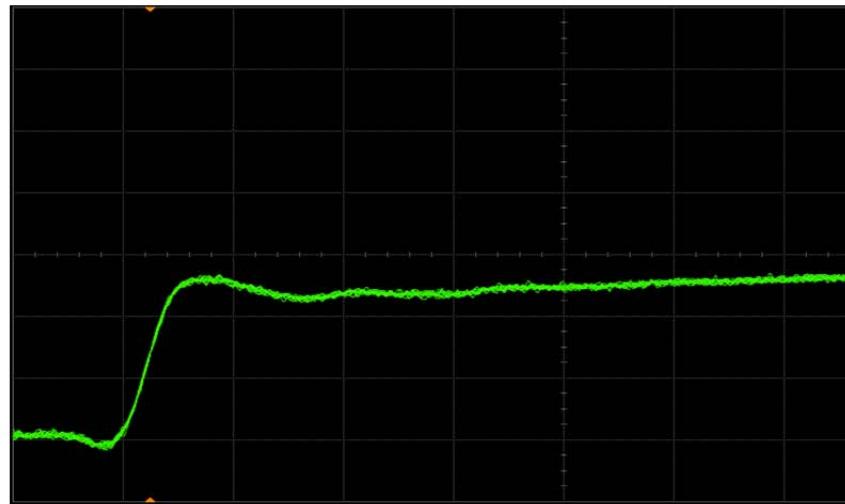


Figure 5a DUT 9303 Pre-Irradiation Rising Edge

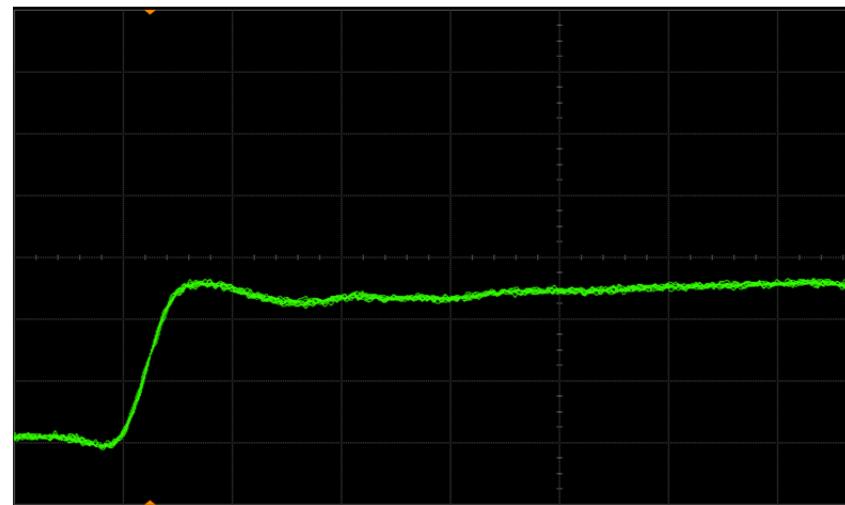


Figure 5b DUT 9303 Post-Annealing Rising Edge

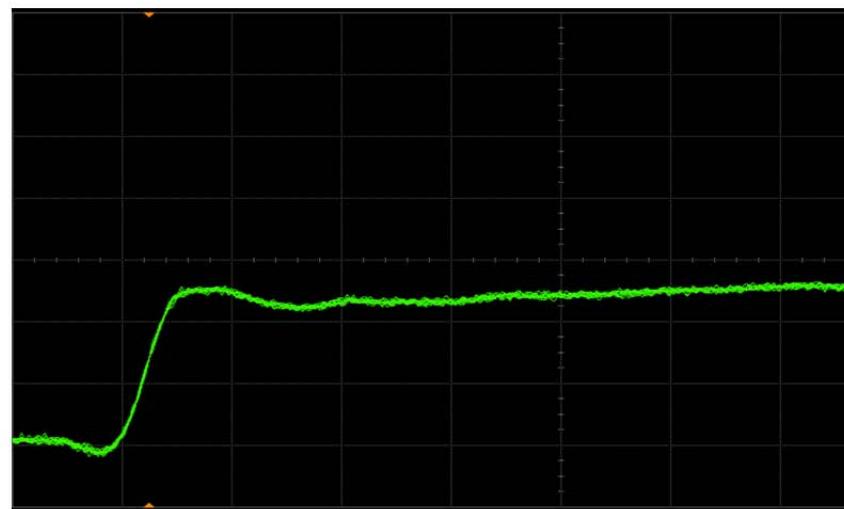


Figure 6a DUT 9307 Pre-Irradiation Rising Edge

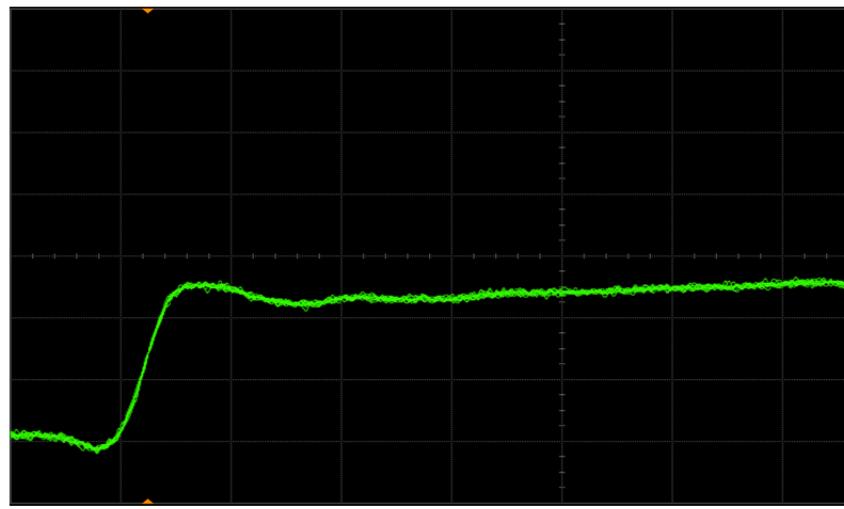


Figure 6b DUT 9307 Post-Annealing Rising Edge

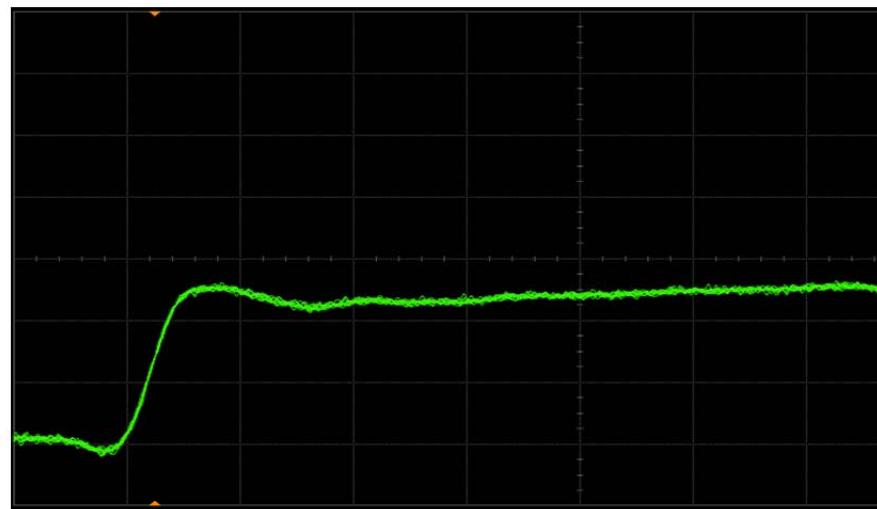


Figure 7a DUT 9360 Pre-Irradiation Rising Edge

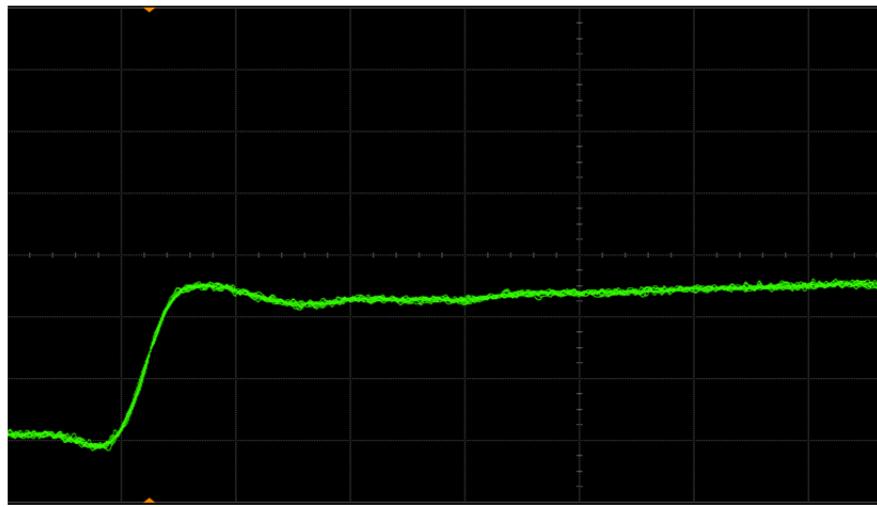


Figure 7b DUT 9360 Post-Annealing Rising Edge

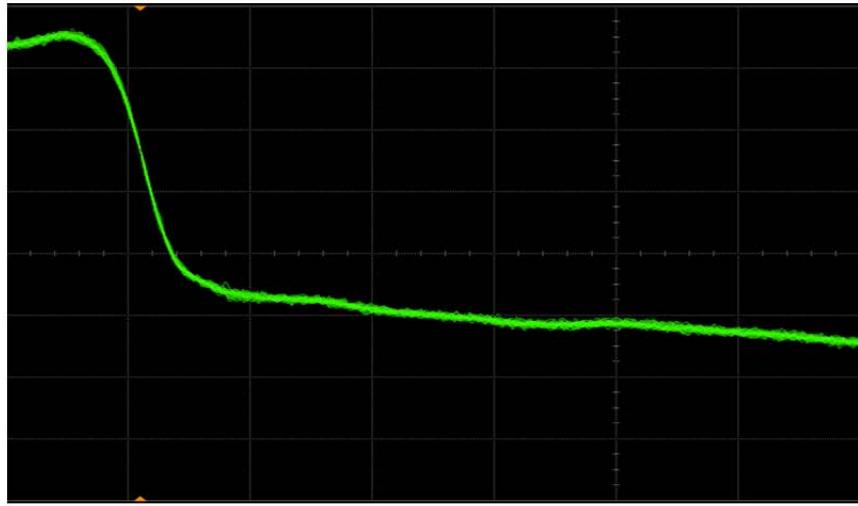


Figure 8a DUT 9259 Pre-Radiation Falling Edge

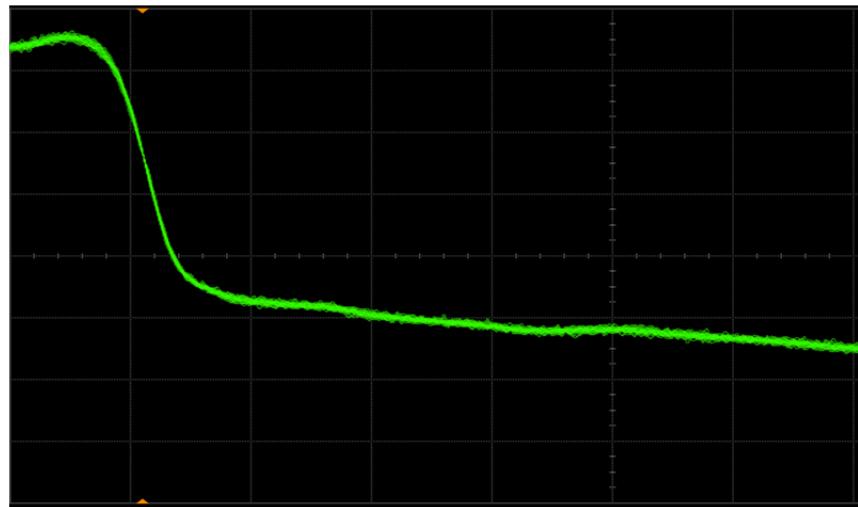


Figure 8b DUT 9259 Post-Annealing Falling Edge

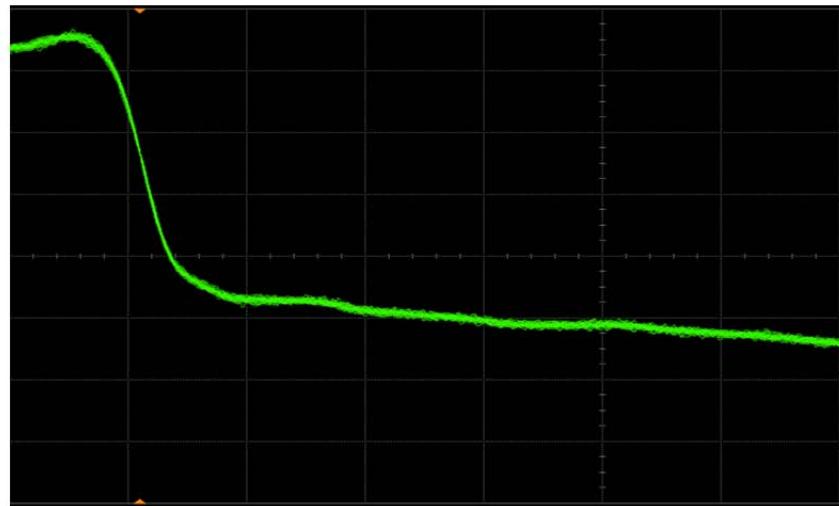


Figure 9a DUT 9261 Pre-Irradiation Falling Edge

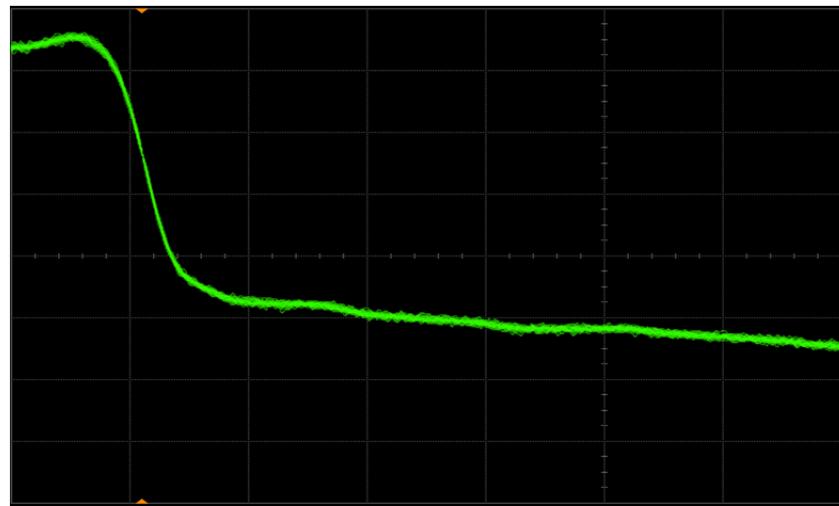


Figure 9b DUT 9261 Post-Annealing Falling Edge

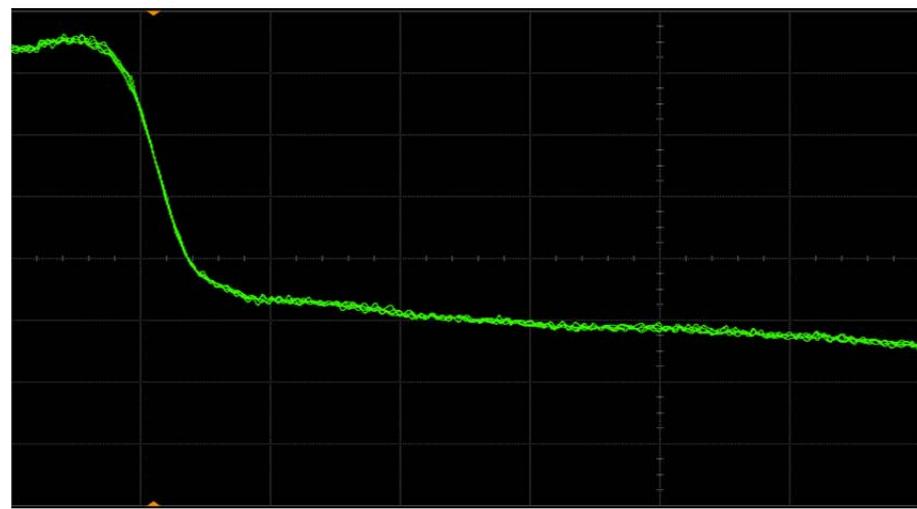


Figure 10a DUT 9276 Pre-Irradiation Falling Edge

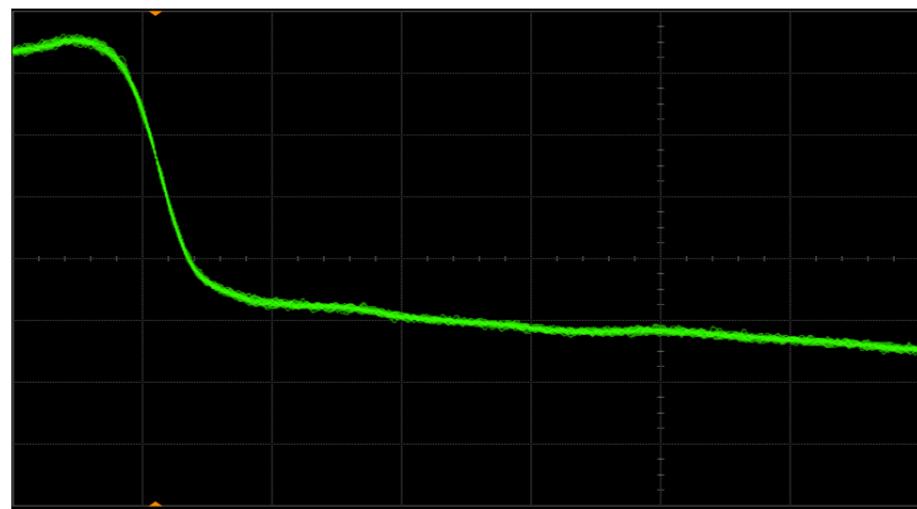


Figure 10b DUT 9276 Post-Annealing Falling Edge

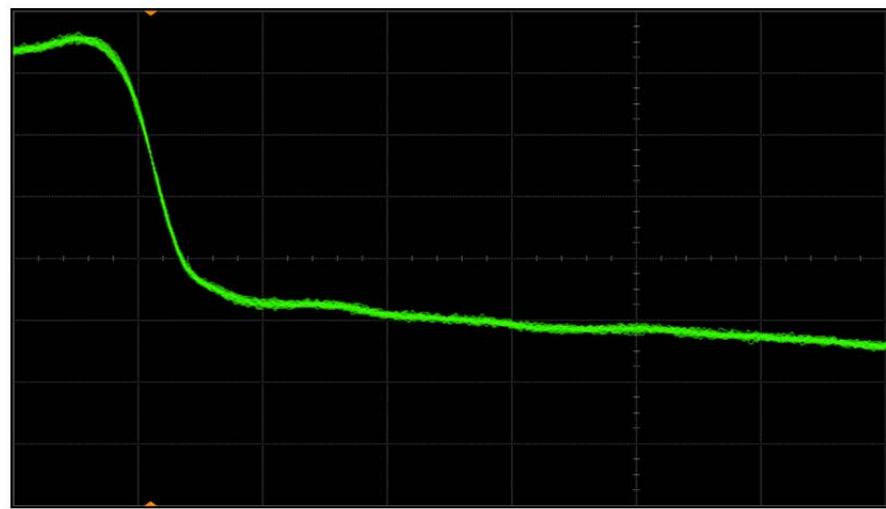


Figure 11a DUT 9303 Pre-Irradiation Falling Edge

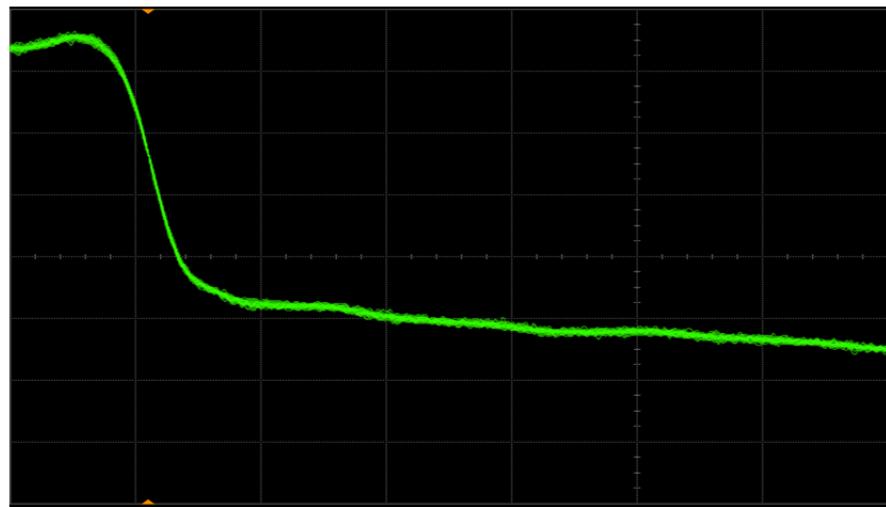


Figure 11b DUT 9303 Post-Annealing Falling Edge

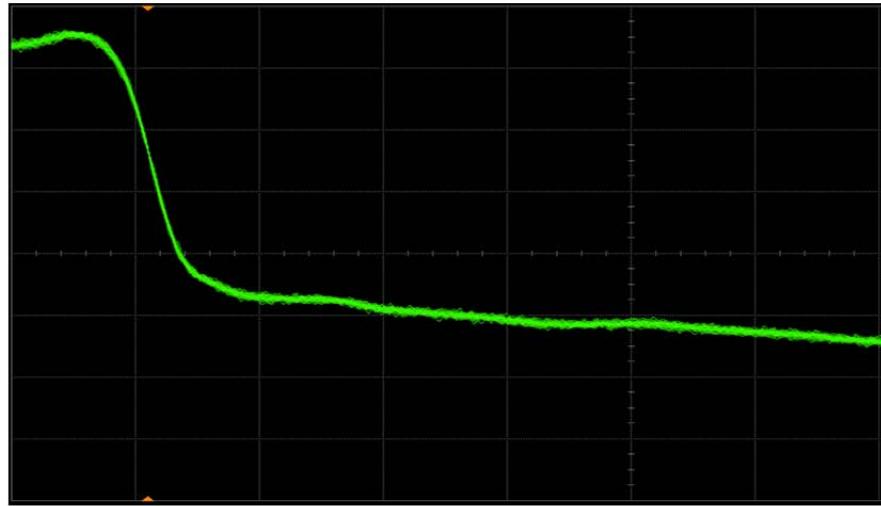


Figure 12a DUT 9307 Pre-Irradiation Falling Edge

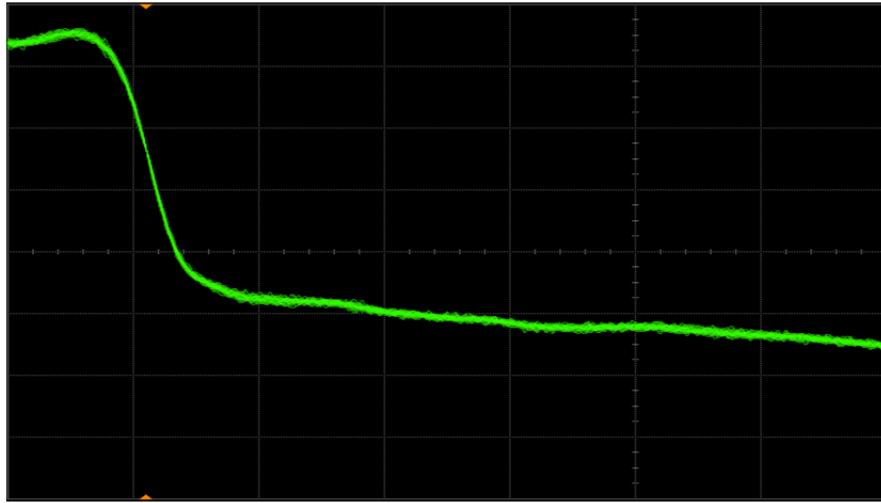


Figure 12b DUT 9307 Post-Annealing Falling Edge

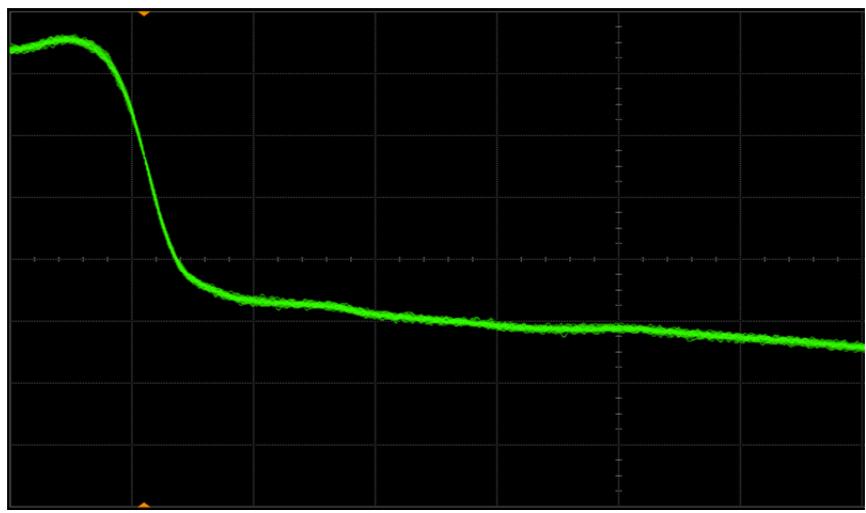


Figure 13a DUT 9360 Pre-Irradiation Falling Edge

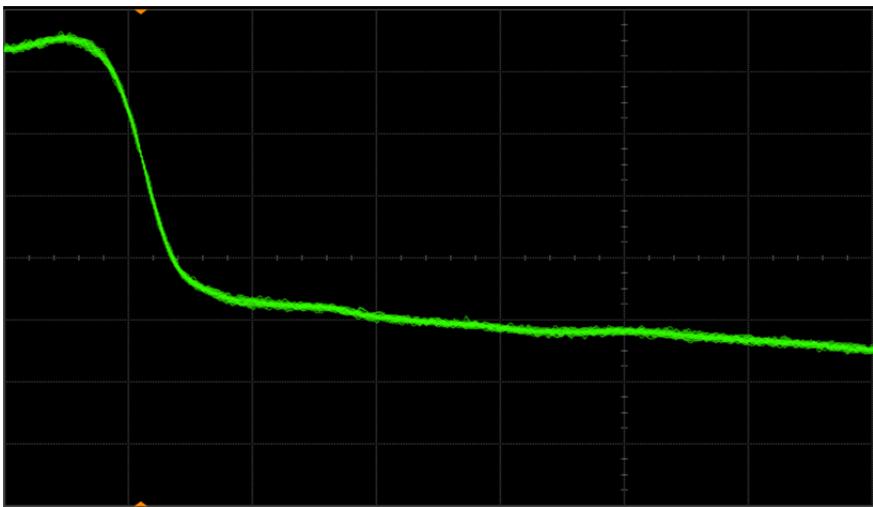


Figure 13b DUT 9360 Post-Annealing Falling Edge



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