AC393
Application Note
Board and Layout Design Guidelines for SmartFusion2
SoC and IGLOO2 FPGAs

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51900393. 15.0 10/20

Contents

Figures

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 15.0

The following is a summary of changes made in this revision.

- Renamed Table 4 to Table 7 as "Requirements for Bank Supplies".
- Information about I/O glitch at auto-update during POR was added, see I/O Glitch at Auto-Update During POR.
- Updated the note in Power Supplies to include Aux. PLL PCIe Supply in the power supply settings description for PLLs.
- Internal pull-up clamp diode is not present in MSIO. Hence, removed MSIO from Figure 20.
- In Table 21 (Design Checklist -> Power Supplies -> VDDI Bank Supplies), added reference to Table 4 to Table 7 for verifying the requirements for VDDI Bank supplies.
- Updated the pull-down resistor requirement to 150 ohms for the xDDR_IMP_CALIB_ECC pin of LPDDR and DDR2 interface. See Figure 16 and Figure 17.

1.2 Revision 14.0

The following is a summary of changes made in this revision.

- Information about I/O glitches during power-up, power-down, and on blank devices was updated. For more information, see I/O Glitch.
- A figure was added to illustrate SPI master mode programming. For more information, see SPI Master Programming.
- Information about simultaneous switching noise support was added. For more information, see Simultaneous Switching Noise.
- The design checklist from *CL0034: SmartFusion2/IGLOO2 Hardware Board Design Checklist* was merged into this document.
- List of device-package combinations that do not have SERDES_x_VDD pins was added. For more information, see Table 1.
- Design checklist was added in Board Design and Layout Checklist.
- Information about the de-coupling capacitor and SmartFusion2/IGLOO2 placement was added in Component Placement.
- Figures were updated in LPDDR and DDR2 Design and DDR3 Guidelines.

1.3 Revision 13.0

The following is a summary of changes made in this revision.

- Updated Figure 3, Figure 16, Figure 17, Figure 18, and Figure 19.
- Updated Table 4, Table 5, Table 6, Table 7, and Table 15.
- AC408: Creating Schematic Symbols using Cadence OrCAD Capture CIS for SmartFusion2 and IGLOO2 Designs is merged with this document.

1.4 Revision 12.0

The following is a summary of changes made in this revision.

- Recommended bank supplies are updated for the FG484 package. See Table 5.
- Recommended bank supplies are updated for VF400 and FCS325 Packages. See Table 6.
- Recommended bank supplies are updated for VF256 and TQ144 Packages. See Table 7.
- Added a note about DQ pins that all 4- and 8-bit pins are interchangeable in LPDDR, DDR2, and DDR3 memories. See Figure 16.
- Added that the SERDES_x_L[01/23]_VDDAPLL pin supports only 2.5 V, and removed 1.2 V references from all occurrences. For more information, see Figure 1 and Table 17.

- AC394: Layout Guidelines for SmartFusion2- and IGLOO2-Based Board Design was added as a part of Board Design guidelines itself.

1.5 Revision 11.0

The following is a summary of changes made in this revision.

- The filter circuit for SERDES_x_VDD was removed. Even if it was used in the board design previously, it does not affect the functionality of the board. See Figure 1.
- Information about VDDI2 was updated. See Table 6 and Table 7.
- Information about reset circuit was updated. see Reset Circuit.
- Changed the document to the new template.

1.6 Revision 10.0

The following is a summary of the changes made in this revision.

- Updated Power Supplies (SAR 77745 and SAR 79670).
- Updated Table 4 (SAR 78887).
- Updated SPI Master Programming (SAR 75910).
- Updated SerDes (SAR 78504).
- Updated User I/O and Clock Pins (SAR 61314).

1.7 Revision 9.0

The following is a summary of the changes made in this revision.

- Updated Figure 1 (SAR 72533).
- Added CCC_PLL_VDDA and MSS_xDDR_PLL_VDDA details under Power Supplies (SAR 72533).
- Deleted the RC Values for Filter Circuitry table (SAR 72533).
- Added the M2S060T/M2GL060T device column in Table 7 (SAR 70484).

1.8 Revision 8.0

The following is a summary of the changes made in this revision.

- Updated Figure 1 (SAR 66682).
- Updated the RC Values for Filter Circuitry table (SAR 66682 and SAR 65367).
- Updated Table 4 (SAR 70545).
- Updated Table 7 (SAR 67599).
- Updated Table 15 to replace pin SC_SPI_SS with SC_SPI_SDO.
- Updated PLL Filter (SAR 60798).
- Updated Figure 16 (SAR 65438, SAR 69743 and SAR 69580).
- Updated Figure 17 (SAR 65438).
- Updated Figure 19 (SAR 65438).
- Added Figure 20 (SAR 64377).

1.9 Revision 7.0

The following is a summary of the changes made in this revision.

- Updated Figure 1 and Figure 3 (SAR 62858).
- Updated Power Supply Sequencing (SAR 64117).
- Updated Power Supply Flow.
- Added Table 7.
- Updated Table 4, Table 18, and Table 11 (SAR 62858).
- Updated Reset Circuit.
- Updated AC Coupling.
- Updated Figure 16, Figure 17, Figure 18, and Figure 19 (SAR 65438).
- Replaced all instances of VQ144 with TQ144 Package.
- Removed all instances of and references to M2S100 and M2GL100 device (SAR 62858).

1.10   Revision 6.0

The following is a summary of the changes made in this revision.

- Updated Design Considerations (SAR 58055).
- Updated Power Supplies and Figure 1 (SAR 52580).
- Updated Power Supply Sequencing (SAR 59593 and SAR 57004).
- Updated Figure 3 (SAR 52580).
- Added M2S090T/M2GL090T-FCS325 information for power supplies in Table 4 (SAR 58241).
- Added a foot note to Table 15 (SAR 59563).
- Updated SerDes Reference Clock Requirements (SAR 60213).
- Updated Table 14 (SAR 58085).
- Updated Brownout Detection (BOD) and Figure 22 (SAR 56598).
- Updates made to maintain the style and consistency of the document.

1.11   Revision 5.0

The following is a summary of the changes made in this revision.

- Updated Power Supply Sequencing, Figure 1, Figure 3, and Table 4 (SAR 52580).
- Updated main crystal oscillator pins naming convention (SAR 53177).
- Updated Figure 1 (SAR 54177).
- Updated Figure 1, Figure 3, and Table 18 (SAR 55659).
- Updated Figure 1, and Figure 3 (SAR 55705).
- Updated Figure 16, Figure 17, Figure 18, and Figure 19 (SAR 53161).
- Updated Table 4 (SAR 53348).

1.12   Revision 4.0

The following is a summary of the changes made in this revision.

- Corrected the ramp rate description to 50 us in the Power Supply Sequencing (SAR 50245) (SAR 50844).
- Updated Figure 10. (SAR 50725).
- Added the Configuring Pins in Open Drain section.

1.13   Revision 3.0

The following is a summary of the changes made in this revision.

- Updated the content for IGLOO2 devices (SAR 48630).
- Updated Power Supply Sequencing.
- Updated DDR3 Guidelines.
- Updated the Temperature Sensing section.

1.14   Revision 2.0

The following is a summary of the changes made in this revision.

- Modified the SmartFusion2 Unused Pin Configurations section (SAR 47904).
- Updated Table 17 (SAR 47548).
- Updated the Brownout Detection (BOD) section (SAR 47904).
- Added Figure 22 (SAR 47904).

1.15   Revision 1.0

The following is a summary of the changes made in this revision.

- Added the Power Supply Sequencing and Power-on Reset section (SAR 47223).
- Updated Figure 3 (previously Figure 2) and added Figure 4 (SAR 47223).
- Updated Table 4 and Table 17, and added Table 18 (SAR 47223).

1.16 Revision 0

The first publication of this document.

2 Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs

This application note provides board-level design guidelines for SmartFusion®2 and IGLOO®2 devices. This document can be used along with the Layout Guidelines for SmartFusion2 and IGLOO2 Based Board Design, page 36 that describes the PCB design. These guidelines must be treated as a supplement to standard board-level design practices.

Good board design practices are required to obtain expected performance from both PCB and SmartFusion2/IGLOO2 devices. High quality and reliable results depend on minimizing noise levels, preserving signal integrity, meeting impedance and power requirements

This document assumes that the reader has a good understanding of the SmartFusion2/IGLOO2 device, is experienced in digital and analog board design, and knows about the electrical characteristics of systems.

2.1 Design Considerations

The SmartFusion2/IGLOO2 device supports various high-speed interfaces using both double data rate input/output (DDRIO) and SerDes I/O. DDRIO is a multi-standard I/O optimized for low-power DDR, DDR2, and DDR3 performance. SerDes I/O are dedicated to high-speed serial communication protocols. The SerDes I/O supports protocols such as PCI Express 2.0, 10 Gbps attachment unit interface (XAUI), serial gigabit media independent interface (SGMII), JESD204B, and user-defined high-speed serial protocol implementation in fabric.

Routing high-speed serial data over a PCB is a challenge as losses, dispersion, and crosstalk effects increase with speed. Channel losses and crosstalk decrease the signal-to-noise ratio and limit the data rate on the channel.

Subsequent sections discuss the following:

- Power supplies
- Limiting surge current during device reset
- Clocks
- Reset circuit
- JTAG
- Special pins
- Device programming
- SerDes
- LPDDR, DDR2, and DDR3
- User I/O and clock pins
- SerDes
- Brownout detection (BOD)

To verify the board design, see the Board Design and Layout Checklist, page 80.

2.2 Power Supplies

The following figure illustrates the typical power supply requirements for SmartFusion2/IGLOO2 devices. For more information about decoupling capacitors associated with individual power supplies, see Table 2, page 7.

Figure 1 • **Power Supplies**
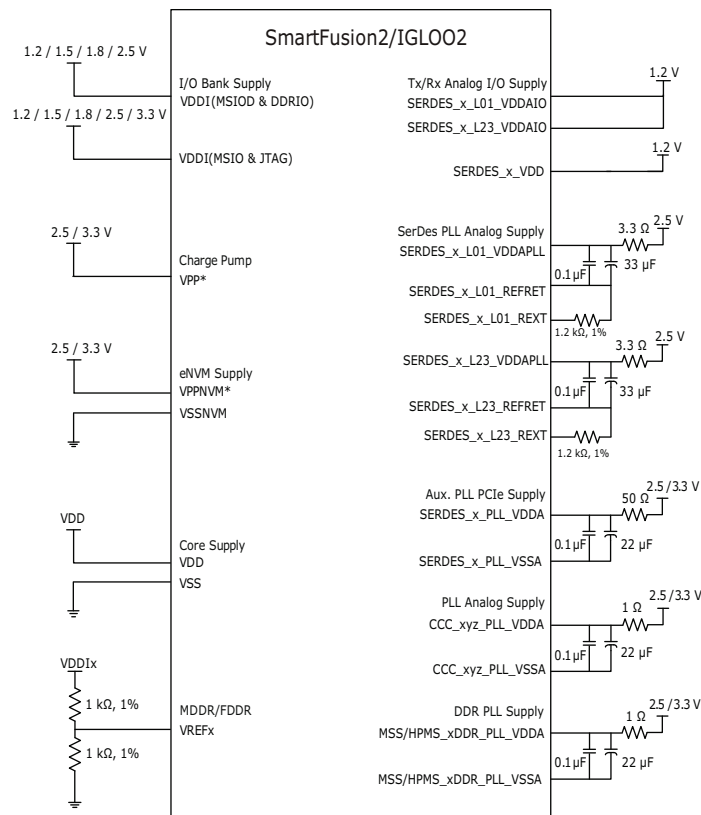
Note: The power supply settings for all the PLLs (Auxiliary PLL PCIe Supply, MDDR, FDDR, and CCC) must be the same in Libero SoC and on the board. The PLLs (Auxiliary PLL PCIe Supply, MDDR, FDDR, and CCC) can be connected to a 2.5 V or 3.3 V supply.

For M2S090T(S), M2GL090T(S), M2S150T(S), and M2GL150T(S) devices, the VPP and VPPNVM must be connected to a +3.3 V supply.

For the CCC_xyz_PLL supplies, xy refers to the location of the PLL in the device (NE/ NW/ SW) and z refers to the number associated with the PLL (0 or 1).

The PLL RC values shown in the figure are applicable to all variants of SmartFusion2/IGLOO2 devices.

When the power rails are in use, follow Figure 1, page 6. For unused cases, follow Figure 3, page 11. The power supply needed for IGLOO2 and SmartFusion2 FPGAs is Core VDD (Fabric voltage). Serdes_VDD is tied to VDD internally, so the same regulator should be used to drive SERDES_x_VDD, SERDES_x_Lyz_VDDAIO, and Core VDD together.

For the device-package combinations listed in the following table, the SERDES_x_VDD pins are shorted with VDD pins inside the package substrate to free up the package pins.

Table 1 • **Device-Package Combinations Without SERDES_x_VDD Pin**

Device	Package
M2S025T, M2GL025T	FCS325
M2S050T(S), M2GL050T(S)	FCS325
M2S060T(S), M2GL060T(S)	FCS325
M2S90T(S), M2GL90T(S)	FCS325
M2S10T(S), M2GL010T(S)	VF256

Table 1 •   **Device-Package Combinations Without SERDES_x_VDD Pin**

Device	Package
M2S025TS, M2S025T, M2GL025TS, M2GL025T	VF256
M2S150T(S), M2GL150T(S)	FCV484
M2S150TS, M2S150T M2GL150TS, M2GL150T	FCS536

For detailed pin descriptions, see *DS0115: SmartFusion2 Pin Descriptions Datasheet* or *DS0124: IGLOO2 Pin Descriptions Datasheet*.

2.2.1   Power Supply Decoupling

To reduce any potential fluctuation on the power supply lines, decoupling capacitors, bypass capacitors, and other power supply filtering techniques must be used.

- For values ranging from 1 nF to 100 µF, use X7R or X5R (dielectric material) type capacitors.
- For values ranging from 100 µF to 1000 µF, use tantalum capacitors.

The following table lists the recommended number of PCB decoupling capacitors for an M2S050T/M2GL050T-FG896 device.

Table 2 •   **Power Supply Decoupling Capacitors**

Pin Name	Number of Pins	Ceramic Caps						Tantalum Caps		
		0.01 µF	0.1 µF	10 µF	33 µF	22 µF	47 µF	100 µF	220 µF[1]	330 µF
VDD	24	12	12					1	3	1
VDDI0	29	14	14				2			
VDDI1	4	2	2	1						
VDDI2	4	2	2	1						
VDDI3	5	2	3	1						
VDDI4	3	2	1	1						
VDDI5	29	14	14				2			
VDDI6	1	1		1						
VDDI7	6	3	3	1						
VDDI8	5	2	3	1						
VDDI9	1	1	1							
VPP	4	2	2	1						
VREF0	3	2	1	1						
VREF5	3	2	1	1						
VPPNVM	1	1		1						
SERDES_0_VDD	2	1	1	1[2]						
SERDES_1_VDD	2	1	1	1[2]						
SERDES_0_L01_VDDAIO	1	1[2]	1[2]	1[3]						
SERDES_0_L23_VDDAIO	1	1[2]	1[2]	1[3]						
SERDES_1_L01_VDDAIO	1	1[2]	1[2]	1[3]						
SERDES_1_L23_VDDAIO	1	1[2]	1[2]	1[3]						
CCC_NE0_PLL_VDDA	1		1			1				

Table 2 • **Power Supply Decoupling Capacitors** *(continued)*

Pin Name	Number of Pins	Ceramic Caps				Tantalum Caps				
		0.01 µF	0.1 µF	10 µF	33 µF	22 µF	47 µF	100 µF	220 µF[1]	330 µF
CCC_NE1_PLL_VDDA	1		1			1				
CCC_NW0_PLL_VDDA	1		1			1				
CCC_NW1_PLL_VDDA	1		1			1				
CCC_SW0_PLL_VDDA	1		1			1				
CCC_SW1_PLL_VDDA	1		1			1				
MSS_FDDR_PLL_VDDA	1		1			1				
MSS_PLL_MDDR_VDDA	1		1			1				
PLL_SERDES_0_VDDA	1		1			1				
PLL_SERDES_1_VDDA	1		1			1				
SERDES_0_L01_VDDAPLL	1		1	1						
SERDES_0_L23_VDDAPLL	1		1	1						
SERDES_1_L01_VDDAPLL	1		1	1						
SERDES_1_L23_VDDAPLL	1		1	1						

1. 220 µF is used to limit surge current for the VDD supply.
2. Single ceramic decoupling capacitor is required for both pins at the device.
3. Single ceramic decoupling capacitor is required for four pins at the device.

The following table lists the recommended decoupling capacitors for the SmartFusion2/IGLOO2 devices. For placement and routing details, see Layout Guidelines for SmartFusion2 and IGLOO2 Based Board Design, page 36.

Table 3 • **Recommended Capacitors**

Part Number	Manufacturer	Description
GRM155R71C103KA01D	Murata	Ceramic 0.01 µF, 16 V, 10%, X7R, 0402
GRM155R71C104KA88D	Murata	Ceramic 0.1 µF, 16 V, 10%, X7R, 0402
GRM188R60J106ME47D	Murata	Ceramic 10 µF, 6.3 V, X5R, 0603
T491B475M016AT	KEMET	Tantalum 4.7 µF, 16 V, 20%, 1411
T491B226M016AT	KEMET	Tantalum 22 µF, 16 V, 20%, 1411
T491B476M010AT	KEMET	Tantalum 47 µF, 10 V, 20%SMD
T520V107M010ATE050	KEMET	Tantalum 100 µF, 10 V, 20%, 2917
TPSD337K010R0050	AVX	Tantalum 330 µF, 10 V, 10%, 2917

2.2.2   Power Supply Sequencing

On detection of a power-up event, the POR circuit sends the power-on reset signal to the system controller and reset controller in the SmartFusion2/IGLOO2 device. The power-on reset circuitry in SmartFusion2/IGLOO2 devices require the VDD and VPP supplies to ramp monotonically from 0 V to the minimum recommended operating voltage within a predefined time. There is no sequencing requirement on VDD and VPP. Four ramp rate options are available during design generation: 50 µs, 1 ms, 10 ms, and 100 ms. Each selection represents the maximum ramp rate to apply to VDD and VPP. The ramp rates can be configured by using the Libero software.

The SERDES_VDD pins are shorted to VDD on silicon die; therefore, Microsemi recommends using the same regulator to power up the VDD, SERDES_VDD and SERDES_VDDAIO pins. These three voltage

supplies must be powered at the same voltage and must be ramped up and ramped down at the same time.

For information about the power-up to functional time sequence, see *DS0128: IGLOO2 and SmartFusion2 Datasheet*.

2.3 I/O Glitch

Glitches were observed in SmartFusion2 and IGOOL2 devices during power-up and power-down cases in different scenarios. The following sections describe the glitch observations.

2.3.1 I/O Glitch During Power-Up

I/O Glitches can occur in some power-up sequences, and they can be ignored if good design practices are used.

To mitigate the I/O glitch:

1. Use the following power-up sequence:
   - Ensure VDD/VDDIOx powers-up before VPP (VDD/VDDIOx --> VPP). During this time, DEVRST_N should also be de-asserted along with VPP.
   - Assert DEVRST_N (Keep signal Low) until all the power rails are up. Only after all power rails are up de-assert DEVRST_N.
2. If power sequencing is not possible, add a 10 KΩ resistor to ground on all critical signal outputs like clocks and resets.

2.3.2 I/O Glitch During Power-Down

I/O glitches can occur in some power-down sequences, and they can be ignored if good design practices are used.

To mitigate the I/O glitch:

1. Use the following power-down sequence:
   - Ensure that the DEVRST_N is kept de-asserted at 3.3V while the power down of all the rails take place. DEVRST_N be asserted to 0V only after all the rails are powered down.
2. If power sequencing is not possible, add a 10 KΩ resistor to ground on all critical signal outputs like clocks and resets.

2.3.3 I/O Glitch in a Blank Device

I/O glitch was observed on bank 2 of a blank device before programming. On a blank device, the I/Os are placed in the Flash*Freeze state (tristate with weak pull-ups). When the programming starts, the I/Os transition to the boundary scan mode. On I/O bank 2, there is a race condition between exiting the Flash*Freeze mode and the entering boundary scan mode. During this transition, the outputs on bank 2 briefly drive high until the boundary scan mode is enabled. This transition results in an I/O glitch.

To prevent this glitch, use the JTAG command to adjust the I/O drive strength to zero before programming starts.

2.3.3.1 Application Impact Due to Glitch

Application Impact: There is no reliability impact because the duration of the I/O glitch does not exceed the datasheet overshoot specifications. The glitch amplitude tracks the VDDI bank voltage and rises slightly above the VDDI. For example, at 3.3 V of VDDI, the glitch rises above 3.3 V by approximately 0.3 V for 5 ns. The the glitch amplitude is directly proportional to the VDDI value.

Resolution: Regenerate the bitstream using Libero 11.8 SP1.

2.3.4 I/O Glitch at Auto-Update During POR

I/O glitches are observed during Power-On Reset (POR) with designs where the auto-update option is enabled. As the device powers up along with the DEVRSTb which is then in the state of being de-asserted and the I/O glitch occurs at the end of the auto-update process.

The glitch is observed only on bank 0, 1, and 2 of M2S005, M2S010, and M2S025 devices. The glitch is independent of the type of packages being used.

To avoid this glitch:

- Place critical signal like clocks and resets on I/O bank 4, 5, 6, and 7 across the dies M2S005, M2S010, M2S025.
- Use in-application programming (IAP) option instead of auto-update.
- No banks on M2S060, M2S090, M2S0150 experience any glitches.

2.3.5   Power Supply Flow

SmartFusion2/IGLOO2 FPGA devices require multiple power supplies. Figure 2, page 10 illustrates a topology for generating the required power supplies from a single 12 V source. This example power supply topology is based on SmartFusion2 M2S050T-FG896 device with two SerDes channels (SERDES0 and SERDES1) and a DDR3 interface.

Figure 2 • **Example Power Supply Topology**
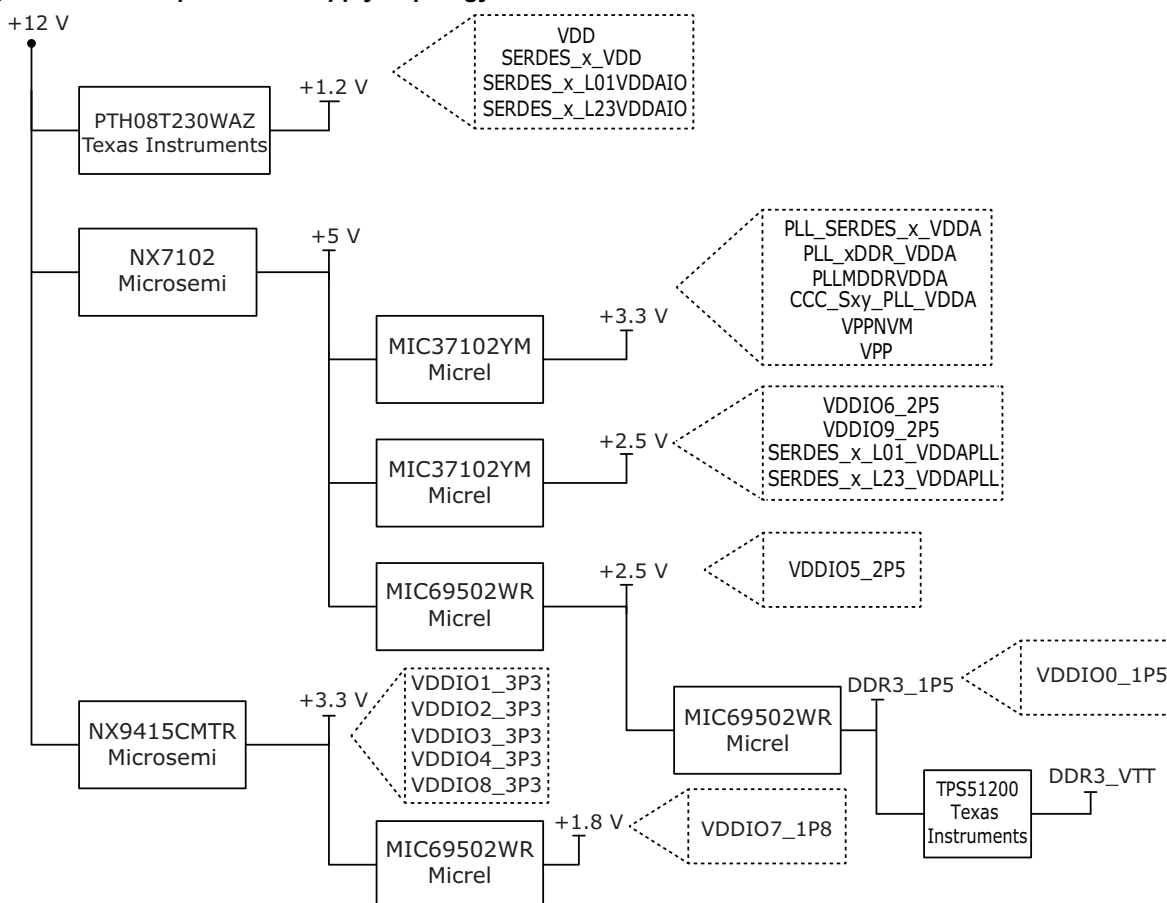
2.3.6   Unused Pin Configurations

In cases where certain interfaces are not used, the associated pins need to be configured properly. For example, the pins of an unused crystal oscillator can be left floating (DNC) and must not be grounded. If a PLL is not used or bypassed, and only the divider circuitry is used, then the PLL's pins can be powered without RC filter circuitry.

For SmartFusion2/IGLOO2 devices with multiple SerDes blocks, designers should tie off unused SerDes blocks, as shown in Figure 3, page 11.

For banks configured as LPDDR or single-ended I/O (and MDDR or FDDR functionalities are not being used), VREFx can be left floating (DNC) even though the corresponding bank supply is still powered.

To allow a SmartFusion2/IGLOO2 device to exit from reset, some of the bank supplies (VDDIx) must always be powered, even if associated bank I/O are unused (as shown in Table 4, page 13 and Table 7, page 15).

For details on bank locations for all the devices, see *DS0115: SmartFusion2 Pin Descriptions Datasheet* or *DS0124: IGLOO2 Pin Descriptions Datasheet*.

Figure 3 • **Recommendations for Unused Pin Configurations**
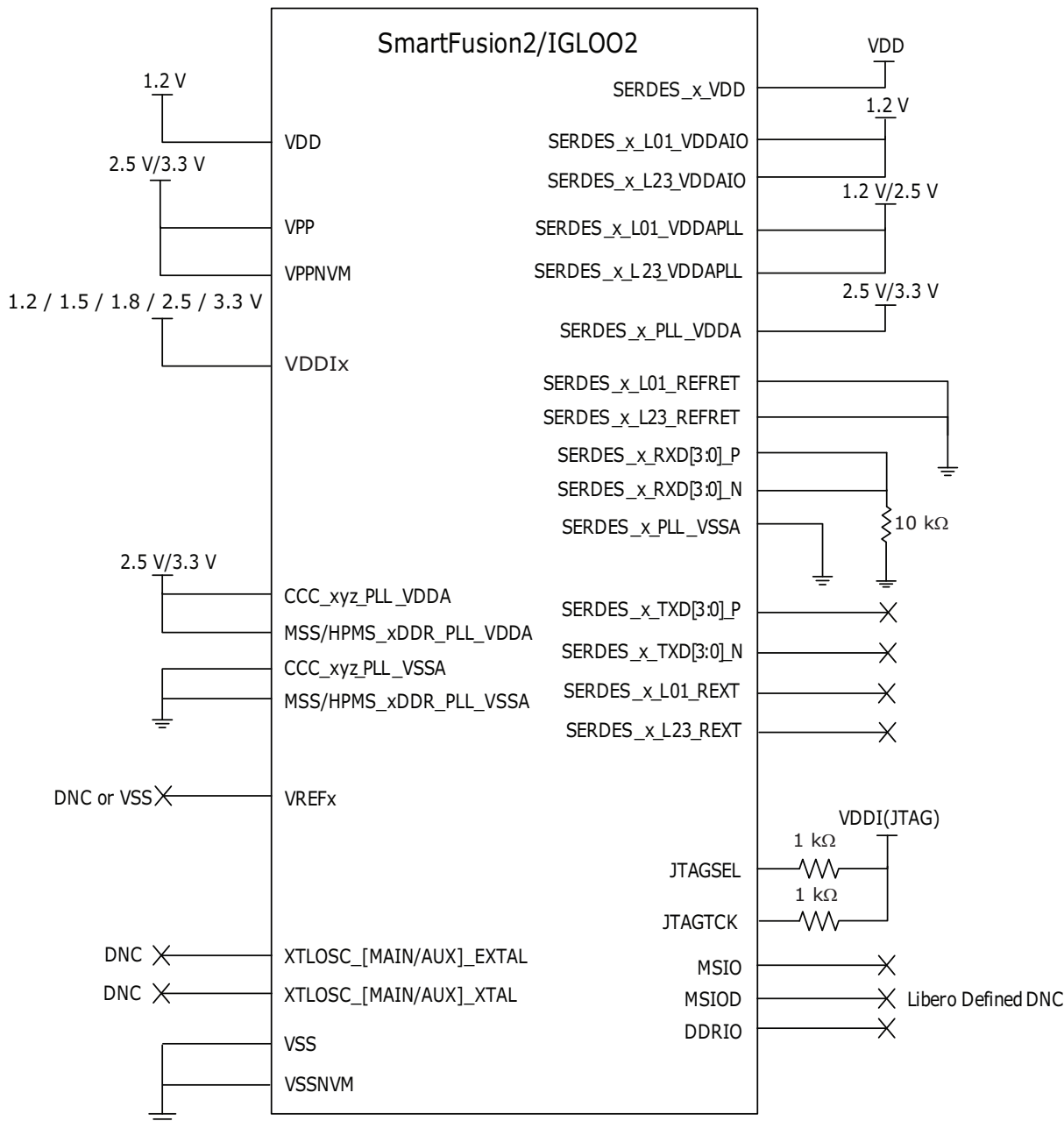
Note: For M2S090T(S), M2GL090T(S), M2S150T(S), and M2GL150T(S) devices, the VPP and VPPNVM must be connected to a +3.3 V supply.

Note: SERDES_RXD pin connections are changed to VSS through a 10 kΩ resistor to reduce the latch-up risk. This change does not effect the old board design functionality.

For recommendations on unused VDDI supplies, see the following tables.

SmartFusion2/IGLOO2 devices have multiple bank supplies. In cases where specific banks are not used, Microsemi recommends connecting them as listed in the following tables.

If there is no recommendation provided for a device-bank supply combination, it means the bank is not pinned out.

Table 4 • **Requirements for Bank Supplies for FC1152, FG896, FG676, FCS536, FCV484 Packages[1]**

Bank Supply Names	FC1152 M2S150T/ M2GL050T	FG896 M2S050T/ M2GL050T	FG676 M2S090T/ M2GL090T	M2S060T/ M2GL060T	FCS536 M2S150T/ M2GL150T	FCV484 M2S150T/ M2GL150
VDDI0	Connect to VSS through a 10 kΩ resistor					–
VDDI1	Connect to VSS through a 10 kΩ resistor	Must connect to VDDI1	Connect to VSS through a 10 kΩ resistor			
VDDI2	Connect to VSS through a 10 kΩ resistor	Must connect to VDDI2	Must connect to VDDI2	Must connect to VDDI2	Connect to VSS through a 10 kΩ resistor	
VDDI3	Connect to VSS through a 10 kΩ resistor	Must connect to VDDI3	Must connect to VDDI3	Must connect to VDDI3	Connect to VSS through a 10 kΩ resistor	
VDDI4	Connect to VSS through a 10 kΩ resistor			Must connect to VDDI4	Connect to VSS through a 10 kΩ resistor	
VDDI5	Connect to VSS through a 10 kΩ resistor					
VDDI6	Must connect to VDDI6	Connect to VSS through a 10 kΩ resistor			Must connect to VDDI6	Must connect to VDDI6
VDDI7	Must connect to VDDI7	Connect to VSS through a 10 kΩ resistor			Must connect to VDDI7	Must connect to VDDI7
VDDI8	Connect to VSS through a 10 kΩ resistor					–
VDDI9	Connect to VSS through a 10 kΩ resistor	–	Connect to VSS through a 10 kΩ resistor			
VDDI10	Connect to VSS through a 10 kΩ resistor	–	–	–	Connect to VSS through a 10 kΩ resistor	
VDDI11	Connect to VSS through a 10 kΩ resistor	–	–	–	Connect to VSS through a 10 kΩ resistor	
VDDI12	Connect to VSS through a 10 kΩ resistor	–	–	–	Connect to VSS through a 10 kΩ resistor	
VDDI13	Connect to VSS through a 10 kΩ resistor	–	–	–	Connect to VSS through a 10 kΩ resistor	
VDDI14	Connect to VSS through a 10 kΩ resistor	–	–	–	Connect to VSS through a 10 kΩ resistor	
VDDI15	Connect to VSS through a 10 kΩ resistor	–	–	–	Connect to VSS through a 10 kΩ resistor	–
VDDI16	Connect to VSS through a 10 kΩ resistor	–	–	–	Connect to VSS through a 10 kΩ resistor	
VDDI17	Connect to VSS through a 10 kΩ resistor	–	–	–	Connect to VSS through a 10 kΩ resistor	
VDDI18	Connect to VSS through a 10 kΩ resistor	–	–	–	Connect to VSS through a 10 kΩ resistor	–

1. The unused VDDI# pins must be connected to VSS through a 10 KΩ resistor. The VDDI# pins can be grouped and connected to one 10 KΩ resistor or a 10 K Ω resistor can be used for each VDDI# bank, it completely depends on the board layout. For the previous design the unused VDDI# pins were DNC, and cannot create functionality issue. Microsemi recommends connecting to Ground to improve the board reliability.

Table 5 • **Requirements for Bank Supplies for FG484 Package**[1]

Bank Supply Names	FG484					
	M2S090T/ M2GL090T	M2S060T M2GL060T	M2S050T/ M2GL050T	M2S025T/ M2GL025T	M2S010T/ M2GL010T	M2S005/ M2GL005
VDDI0	–	–	Connect to VSS through a 10 kΩ resistor			
VDDI1	Connect to VSS through a 10 kΩ resistor		Must connect to VDDI1	Must connect to VDDI1	Must connect to VDDI1	Must connect to VDDI1
VDDI2	Must connect to VDDI2	Must connect to VDDI2	–	Must connect to VDDI2	Must connect to VDDI2	Must connect to VDDI2
VDDI3	Must connect to VDDI3	–	Must connect to VDDI3	Connect to VSS through a 10 kΩ resistor	Must connect to VDDI3	Connect to VSS through a 10 kΩ resistor
VDDI4	Connect to VSS through a 10 kΩ resistor	Must connect to VDDI4	Connect to VSS through a 10 kΩ resistor	Must connect to VDDI4	Connect to VSS through a 10 kΩ resistor	Must connect to VDDI4
VDDI5	Connect to VSS through a 10 kΩ resistor					
VDDI6	Connect to VSS through a 10 kΩ resistor					
VDDI7	Connect to VSS through a 10 kΩ resistor					–
VDDI8	Connect to VSS through a 10 kΩ resistor			–	–	–
VDDI9	–	Connect to VSS through a 10 kΩ resistor	–	–	–	–

1. The unused VDDI# pins must be connected to VSS through a 10 KΩ resistor. The VDDI# pins can be grouped and connected to one 10 KΩ resistor or a 10 K Ω resistor can be used for each VDDI# bank, it completely depends on the board layout. For the previous design the unused VDDI# pins were DNC, and cannot create functionality issue. Microsemi recommends connecting to Ground to improve the board reliability.

Table 6 • **Requirements for Bank Supplies for VF400 and FCS325 Packages**[1]

Bank Supply Names	VF400					FCS325			
	M2S060T/ M2GL060T	M2S050T/M2GL050T	M2S025T/ M2GL025T	M2S010T/ M2GL010T	M2S005/ M2GL005	M2S090T/ M2GL090T	M2S060T/ M2GL060T	M2S050T/M2GL050T	M2S025T/ M2GL025T
VDDI0	–	Connect to VSS through a 10 kΩ resistor				–	–	Connect to VSS through a 10 kΩ resistor	
VDDI1	Connect to VSS through a 10 kΩ resistor	Must connect to VDDI1	Must connect to VDDI1	Must connect to VDDI1	Must connect to VDDI1	Connect to VSS through a 10 kΩ resistor		Must connect to VDDI1	Must connect to VDDI1
VDDI2	Must connect to VDDI2	–	Must connect to VDDI2	Must connect to VDDI2	Must connect to VDDI2	Must connect to VDDI2	Must connect to VDDI2	Must connect to VDDI2	–
VDDI3	–	Must connect to VDDI3	Connect to VSS through a 10 kΩ resistor			Must connect to VDDI3	Must connect to VDDI3	Must connect to VDDI3	Connect to VSS through a 10 kΩ resistor
VDDI4	Must connect to VDDI4	Connect to VSS through a 10 kΩ resistor			Must connect to VDDI4	Connect to VSS through a 10 kΩ resistor	Must connect to VDDI4	Connect to VSS through a 10 kΩ resistor	Must connect to VDDI4
VDDI5	Connect to VSS through a 10 kΩ resistor								

Table 6 • **Requirements for Bank Supplies for VF400 and FCS325 Packages[1]** *(continued)*

VDDI6	Connect to VSS through a 10 kΩ resistor						
VDDI7	Connect to VSS through a 10 kΩ resistor		–	Connect to VSS through a 10 kΩ resistor			
VDDI8	Connect to VSS through a 10 kΩ resistor	–	–	–	Connect to VSS through a 10 kΩ resistor		–	
VDDI9	Connect to VSS through a 10 kΩ resistor	–	–	–	–	–	Connect to VSS through a 10 kΩ resistor	–	–

1. The unused VDDI# pins must be connected to VSS through a 10 KΩ resistor. The VDDI# pins can be grouped and connected to one 10 KΩ resistor or a 10 K Ω resistor can be used for each VDDI# bank, it completely depends on the board layout. For the previous design the unused VDDI# pins were DNC, and cannot create functionality issue. Microsemi recommends connecting to Ground to improve the board reliability.

Table 7 • **Requirements for Bank Supplies for VF256 and TQ144 Packages[1]**

	VF256			TQ144	
Bank Supply Names	**M2S025T/ M2GL025T**	**M2S010T/ M2GL010T**	**M2S005S/ M2GL005S**	**M2S010S/ M2GL010S**	**M2S005S/ M2GL005S**
VDDI0	Connect to VSS through a 10 kΩ resistor				
VDDI1	Must connect to VDDI1	Must connect to VDDI1	Must connect to VDDI1	–	–
VDDI2	Must connect to VDDI2	Must connect to VDDI2	Must connect to VDDI2	Must connect to VDDI2	Must connect to VDDI2
VDDI3	Connect to VSS through a 10 kΩ resistor				
VDDI4	Must connect to VDDI4	Must connect to VDDI4	Must connect to VDDI4	Must connect to VDDI4	Must connect to VDDI4
VDDI5	Connect to VSS through a 10 kΩ resistor			–	Connect to VSS through a 10 kΩ resistor
VDDI6	Connect to VSS through a 10 kΩ resistor				
VDDI7	Connect to VSS through a 10 kΩ resistor		–	Connect to VSS through a 10 kΩ resistor	–

1. The unused VDDI# pins must be connected to VSS through a 10 KΩ resistor. The VDDI# pins can be grouped and connected to one 10 KΩ resistor or a 10 K Ω resistor can be used for each VDDI# bank, it completely depends on the board layout. For the previous design the unused VDDI# pins were DNC, and cannot create functionality issue. Microsemi recommends connecting to Ground to improve the board reliability.

2.4 Limiting Surge Current During Device Reset

After device power-up, if the application asserts the DEVRST_N pin and there are no decoupling capacitors on the board, additional surge current on VDD may be observed during assertion of DEVRST_N or during a digest check operation. This section describes how to minimize additional surge current during SmartFusion2/IGLOO2 device reset operation. This additional surge current does not occur during device power-up; it is applicable only when DEVRST_N is asserted.

SmartFusion2/IGLOO2 device reset can be activated either directly through an external DEVRST_N pin or indirectly through the tamper macro IP. When the device reset is asserted, the system controller immediately puts the FPGA core in inactive state. The additional surge current has no effect on device reliability. This surge current is for a very short duration and is normally handled by bulk decoupling capacitors on the power plane in a typical system. In cases where Microsemi-recommended board design guidelines cannot be implemented for decoupling capacitors for VDD (due to limited board spacing or other reasons), higher-than-expected surge current may occur during device reset.

The following table provides characterized surge current data for VDD during DEVRST_N assertion. This data represents the worst-case condition with no decoupling capacitors on the board.

Table 8 • **Surge Current on VDD during DEVRST_N Assertion (No Decoupling Capacitors on Board)**

Device	Width of Surge at 50% of Pulse (µS)	Surge Current on VDD			Units
		0 °C to 85 °C	–40 °C to 100 °C	–55 °C to 125 °C	
M2S005/M2GL005	2	0.5	0.6	0.6	A
M2S010/M2GL010	3	0.9	0.9	0.9	A
M2S025/M2GL025	6	1.7	1.7	1.7	A
M2S050/M2GL050	12	3.2	3.2	3.2	A
M2S060/M2GL060	12	3.2	3.2	3.2	A
M2S090/M2GL090	22	4.4	4.6	4.6	A
M2S150/M2GL150	42	7.0	7.3	7.3	A

However, the surge current data in the preceding table does not represent a typical system. To illustrate this, surge current during device reset was measured at room temperature separately for the M2S090 security evaluation kit and the M2S150 advanced development kit. These kits have decoupling capacitors according to the Microsemi-recommended board design guidelines. The following table lists the surge currents observed on the M2S090 security evaluation kit and the M2S150 advanced development kit. The surge current values were found to be within acceptable limits.

Table 9 • **M2S090 and M2S150 Surge Current During DEVRST_N Assertion (With Decoupling Capacitors on Board)**

Kit	Width of Surge at 50% of Pulse	Surge Current
M2S090 Security Evaluation Kit	5 µs	150 mA
M2S150 Advanced Development Kit	40 µs	1.5 A

The digest check system service performs on-chip NVM data integrity check on SmartFusion2 devices. The use of system services by digest check may cause additional surge current on VDD. For more information on digest check service, see the *UG0450: SmartFusion2 SoC and IGLOO2 FPGA System Controller User Guide.*

The following table provides surge current data recorded for VDD when system services were being used by the digest check service. To limit surge current during digest check, follow the Microsemi-recommended board design guidelines.

Table 10 • **Surge Current on VDD During Digest Check Using System Services (No Decoupling Capacitors on Board)**

| Device | Width of Surge at 50% of Pulse (µS) | Surge Current on VDD | | | |
		0 °C to 85 °C	–40 °C to 100 °C	–55 °C to 125 °C	Units
M2S005/M2GL005	12	0.2	0.2	0.2	A
M2S010/M2GL010	12	0.5	0.5	0.5	A
M2S025/M2GL025	13	0.6	0.6	0.6	A
M2S050/M2GL050	13	0.9	0.9	0.9	A
M2S060/M2GL060	13	0.9	0.9	0.9	A
M2S090/M2GL090	20	1.0	1.0	1.0	A
M2S150/M2GL150	26	1.0	1.0	1.0	A

2.5 Clocks

SmartFusion2 devices have two on-chip RC oscillators and up to two crystal oscillators for generating clocks for the on-chip resources and logic in the FPGA fabric, as listed in the following table.

RC Oscillators:

- 1-MHz RC oscillator
- 50-MHz RC oscillator

Crystal Oscillators:

- Main crystal oscillator
- Auxiliary (RTC) crystal oscillator

All IGLOO2 devices and the M2S050 SmartFusion2 device only have a main crystal oscillator; they do not have an auxiliary (RTC) crystal oscillator.

Table 11 • **Clock Circuit**

| Resource | | SmartFusion2 SoC Part Number | | | | | IGLOO2 Part Number | | | | |
		M2S005	M2S010	M2S025	M2S050	M2S150	M2GL005	M2GL010	M2GL025	M2GL050	M2GL150
On-Chip Oscillators	RC Oscillators	2	2	2	2	2	2	2	2	2	2
	Crystal Oscillators	2	2	2	1	2	1	1	1	1	1

2.5.1   Main Crystal Oscillator

The main crystal oscillator works with an external crystal, ceramic resonator, or a resistor-capacitor network to generate a high-precision clock in the range of 32 kHz to 20 MHz and is connected via the pins XTLOSC_[MAIN/AUX]_EXTAL and XTLOSC_[MAIN/AUX]_XTAL.

The following table lists the output frequency range of the main crystal oscillator with different possible sources.

Table 12 •   **Crystal Oscillator Output Frequency Range**

Source	Output Frequency Range
Crystal	32 kHz to 20 MHz
Ceramic resonator	500 kHz to 4 MHz
RC circuit	32 kHz to 4 MHz

The main crystal oscillator is operated in medium gain mode when a ceramic resonator is connected between the XTLOSC_[MAIN/AUX]_EXTAL and XTLOSC_[MAIN/AUX]_XTAL pins.

When a crystal is used, the load capacitance is determined by the external capacitors C_1 and C_2, internal capacitance, and stray capacitance (C_S), as shown in the following figure.

Figure 4 •   **Crystal Oscillator**
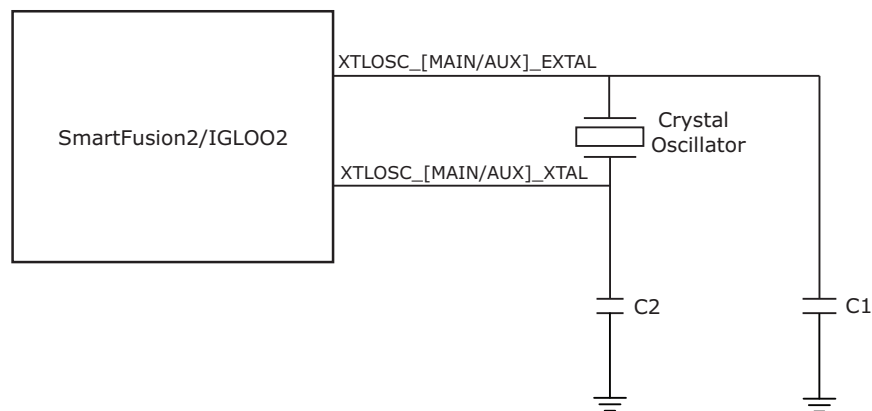
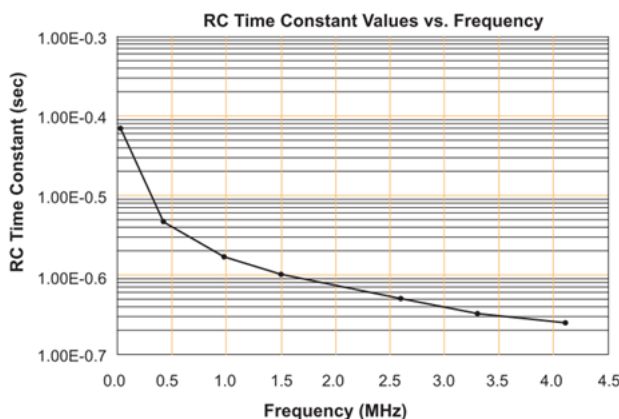The oscillator and the load capacitance should be used as per the recommendation of the manufacturer.

Suggested Crystal Oscillator

CRYSTAL 32.768 kHz 12.5 pF SMD	Citizen	CM519-32.768KEZF-UT

The frequency generated by an RC network is determined by the RC time constant of the selected components, as shown in the following figure.

Figure 5 • **RC Time Constant**

The R and C components are connected to the XTLOSC_[MAIN/AUX]_EXTAL pin, with the XTLOSC_[MAIN/AUX]_XTAL pin connected to the power pin VPP, as shown in the following figure.

Figure 6 • **RC Oscillator**
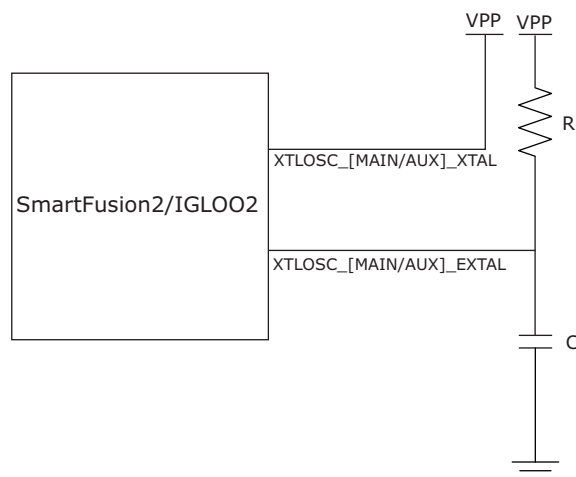
The operating mode of the main crystal oscillator is configured by the oscillator's macro available in Libero SoC.

2.5.2 Auxiliary (RTC) Crystal Oscillator

The SmartFusion2 devices, except M2S050, have an auxiliary crystal oscillator dedicated to real-time clocking as an alternative source for the 32 kHz clock. The RTC can take its 32 kHz clock source from the auxiliary crystal oscillator when the main crystal oscillator is being used.

Similar to the main crystal oscillator, the auxiliary crystal oscillator can work with an external crystal, ceramic resonator, or an RC circuit to generate a high-precision clock in the range of 32 kHz to 20 MHz. There are two I/O pads for connecting the external frequency source to the auxiliary crystal oscillator: XTLOSC_AUX_EXTAL and XTLOSC_AUX_XTAL. The output frequency range, operating modes, and characteristics for the auxiliary crystal oscillator are the same as those for the main crystal oscillator.

For detailed information, see the *UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide*.

Auxiliary (RTC) crystal oscillator is not available in the IGLOO2 device.

2.6 Reset Circuit

SmartFusion2/IGLOO2 devices have a dedicated asynchronous Schmitt-trigger reset input pin (DEVRST_N) with a maximum slew rate not faster than 1 μs. This active-low signal should be asserted only when the device is unresponsive due to some unforeseen circumstances. It is not recommended to

assert this pin during a programming (including eNVM) operation, as it may cause severe consequences including corruption of the device configuration. Asserting this signal tristates all user I/O and resets the system. Deasserting DEVRST_N enables the system controller to begin its startup sequence.

The following figure shows an example of a reset circuit using the Maxim DS1818 reset device, which maintains reset for 150 ms after the 3.3 V supply returns to an in-tolerance condition. Adding a capacitor to ground on DEVRST_N avoids high-frequency noise and unwanted glitches that could reset the device.
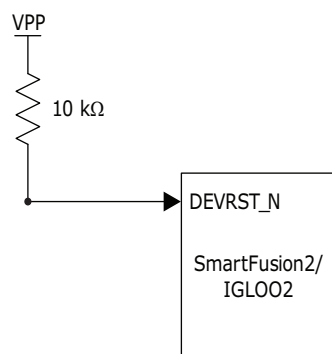
Note: Use DEVRST_N only for IAP or auto update. Do not use DEVRST_N for user logic reset.

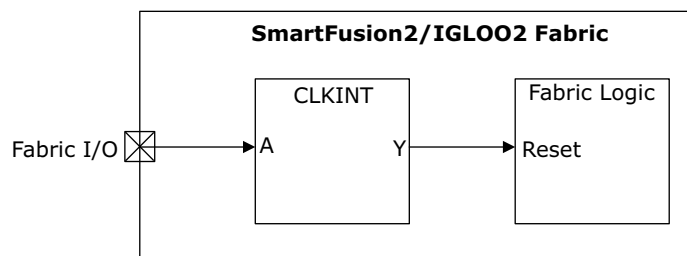*Figure 7 •* **Reset Circuit**
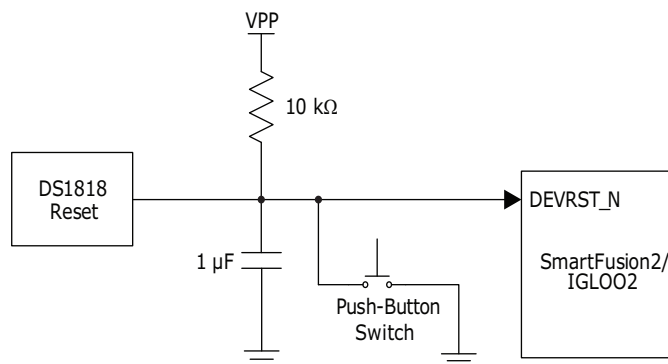
If the reset device is not used, DEVRST_N must be pulled up to VPP through a 10 kΩ resistor, as shown in the following figure.

Figure 8 • **Without Reset Circuit**

If the user logic needs to be reset, any FPGA I/O can be used as an asynchronous reset for the user logic, as shown in the following figure.

Figure 9 • **Fabric Logic Reset**

Use the fabric logic reset for CM3 Reset, fabric logic reset, MSS reset (including all peripherals), FDDR reset, SERDES reset. For more information about fabric reset, see the *MSS Reset Controller Configuration Guide*.

2.7 Device Programming

The SmartFusion2/IGLOO2 device can be programmed via one of two dedicated interfaces: JTAG or SPI. These two interfaces support the following programming modes:

- Auto-programming (master) mode
- In-system programming:
    - JTAG programming mode
    - SPI Slave programming mode
- In-application update:
    - Cortex-M3 update mode (only for SmartFusion2 devices)
   - Auto update mode

For detailed information about programming the device, see the *UG0451: IGLOO2 and SmartFusion2 Programming User Guide*.

2.7.1 JTAG Programming

The JTAG interface is used for device programming and testing or for debugging the Cortex-M3 firmware, as listed in the following table. These functions are enabled depending on the state of the JTAGSEL input. When the device reset is asserted, JTAG I/O are still enabled but cannot be used as the TAP controller is in reset. JTAG I/O are powered by VDDI in the I/O bank where they reside. JTAG pins must be connected as shown in the following figure.

Table 13 • **JTAG Pins**

| Pin Names	Direction	Weak Pull-up	Description
JTAG_TMS	Input	Yes	JTAG test mode select.
JTAG_TRSTB	Input	Yes	JTAG test reset.
JTAG_TDI	Input	Yes	JTAG test data in.
JTAG_TCK	Input	No	JTAG test clock. Microsemi recommends that TCK be tied to VSS or VDDI through a resistor on the board when unused per IEEE 1532 requirements. This prevents totem-pole current on the input buffer.
JTAG_TDO	Output	No	JTAG test data out.
JTAGSEL	Input	Connect the JTAGSEL pin to an external pull-up resistor. The default configuration should enable the FPGA fabric TAP.	JTAG controller selection. Depending on the state of the JTAGSEL pin, an external JTAG controller connects to either the FPGA fabric TAP (high) or the Cortex-M3 JTAG debug interface (low). For SmartFusion2-based designs, this signal must be held high or low through jumper settings. For IGLOO2-based designs, this signal must be held high through a pull-up resistor.

Figure 10 • **JTAG Programming**
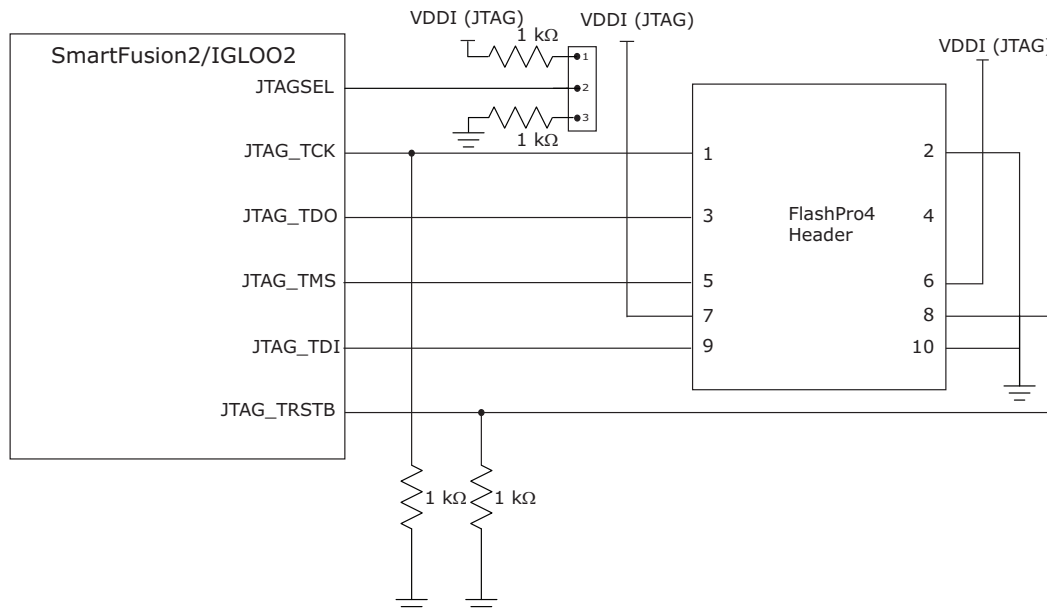
2.7.2   SPI Master Programming

The SmartFusion2/IGLOO2 devices have dedicated pins for programming the device and probing the fabric I/O.

The embedded system controller contains a dedicated SPI block for programming, which can operate in master or slave mode. In master mode, the SmartFusion2/IGLOO2 device interfaces with the external SPI flash from which programming data is downloaded. In slave mode, the SPI block communicates with a remote device that initiates download of programming data to the device.

page 23 shows the board-level connectivity for SPI master mode programming in SmartFusion2 and IGLOO2 devices.

Figure 11 • **SPI Master Mode Programming**
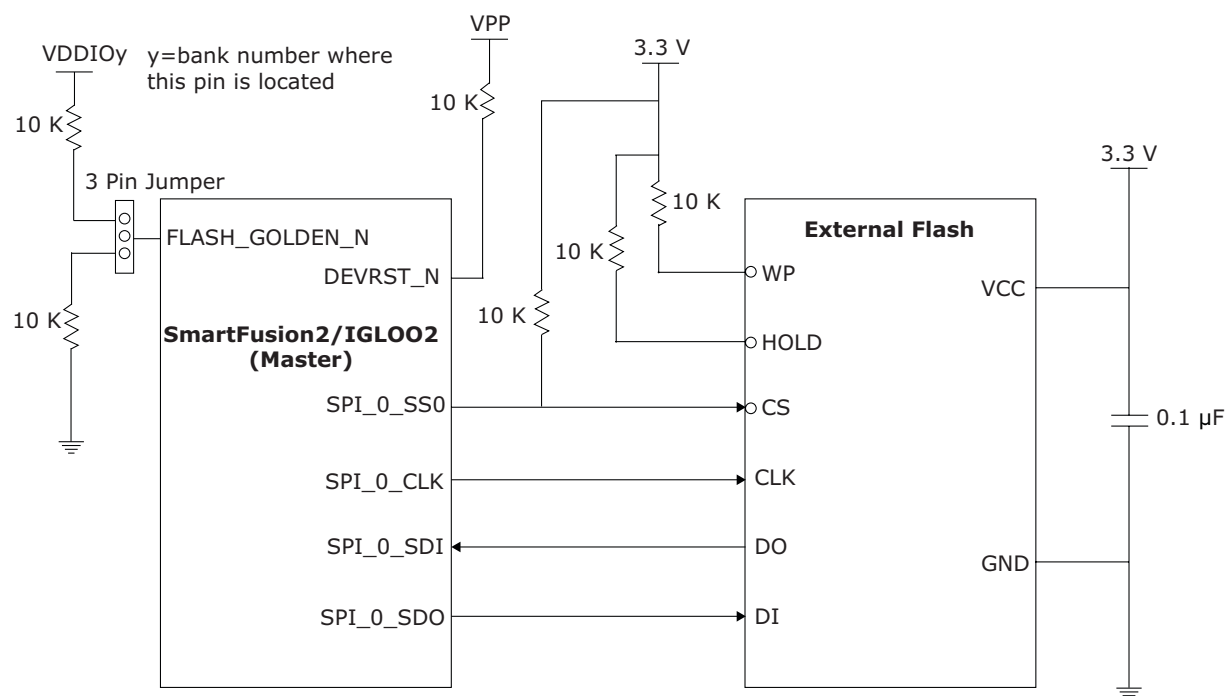
The following table lists the dedicated pins used for programming the device and probing the fabric I/O.

Table 14 • **Dedicated Pins**

| Special Pins	Direction	Description
SPI_0_SDI	Input	Serial data input
SPI_0_SDO	Output	Serial data output
SPI_0_CLK	Output	Serial clock. It is a serial programmable bit rate clock out signal.
SPI_0_SSO[1]	Output	Slave select
FLASH_GOLDEN_N[1]	Input	If pulled low, the SPI_0 port is put into master mode, which indicates that the device is to be reprogrammed from an image in the external SPI flash attached to the SPI_0 interface.
NC		No connect. Indicates the pin is not connected to circuitry within the device. NC pins can be driven to any voltage or can be left floating with no effect on the operation of the device.
DNC		Do not connect. Must not be connected to any signals on the PCB. DNC pins must be left unconnected.
PROBE_A		The two live probe I/O pins are dual-purpose:
PROBE_B		- Live probe functionality
		- User I/O
		The unused live probe I/Os can be configured as weak pull-up resistors, and these pins can be connected to the 10 kΩ external resistor. The 10 kΩ external resistor power supply must be the same as the I/O bank power supply (VDDI).
		Ensure to power up the Bank where the Live Probe signals are assigned. That Bank may be different across die/package combination.

1. Active Low Signal.

For more information about programming, see *UG0451: SmartFusion2 and IGLOO2 Programming User Guide*.

2.7.3 SPI Slave Programming

The following figure shows the SmartFusion2/IGLOO2 SPI slave programming configuration when an external processor is the master.

Figure 12 • **SPI Slave Programming by External Microprocessor**
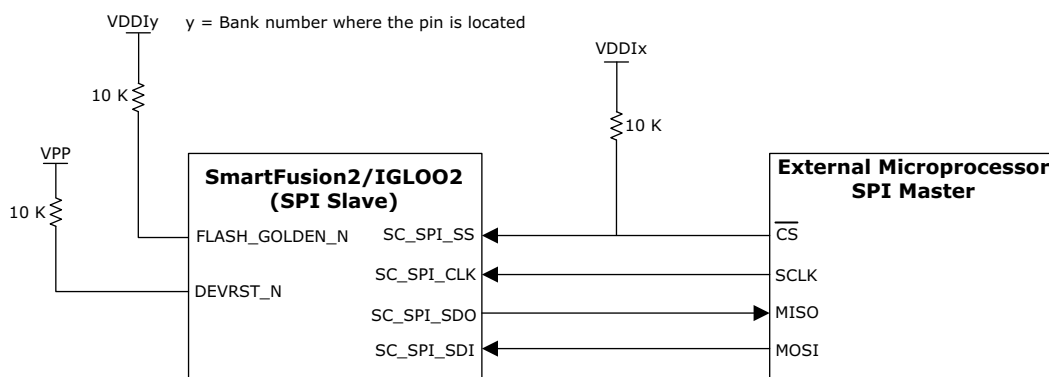
The following figure shows the SmartFusion2/IGLOO2 SPI slave programming configuration when an external programmer is the master.

Figure 13 • **SPI Slave Programming by External Programmer**
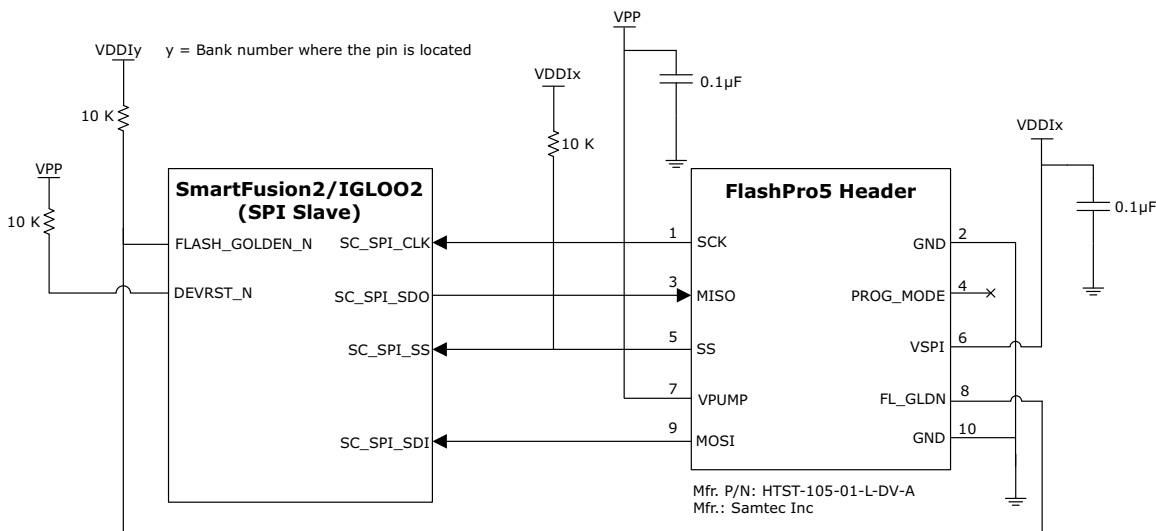

2.8 SerDes

SmartFusion2/IGLOO2 SerDes I/O reside in dedicated I/O banks. The number of SerDes I/O depends on the device size and pin count.

2.8.1 PCI Express (PCIe)

PCIe is a point-to-point serial differential low-voltage interconnect supporting up to four channels. Each lane consists of two pairs of differential signals: a transmit pair, TXP/TXN, and receive pair, RXP/RXN. The following figure illustrates the connectivity between the SmartFusion2/IGLOO2 SerDes interface and the PCIe edge connector.

Figure 14 • **SerDes Schematics**
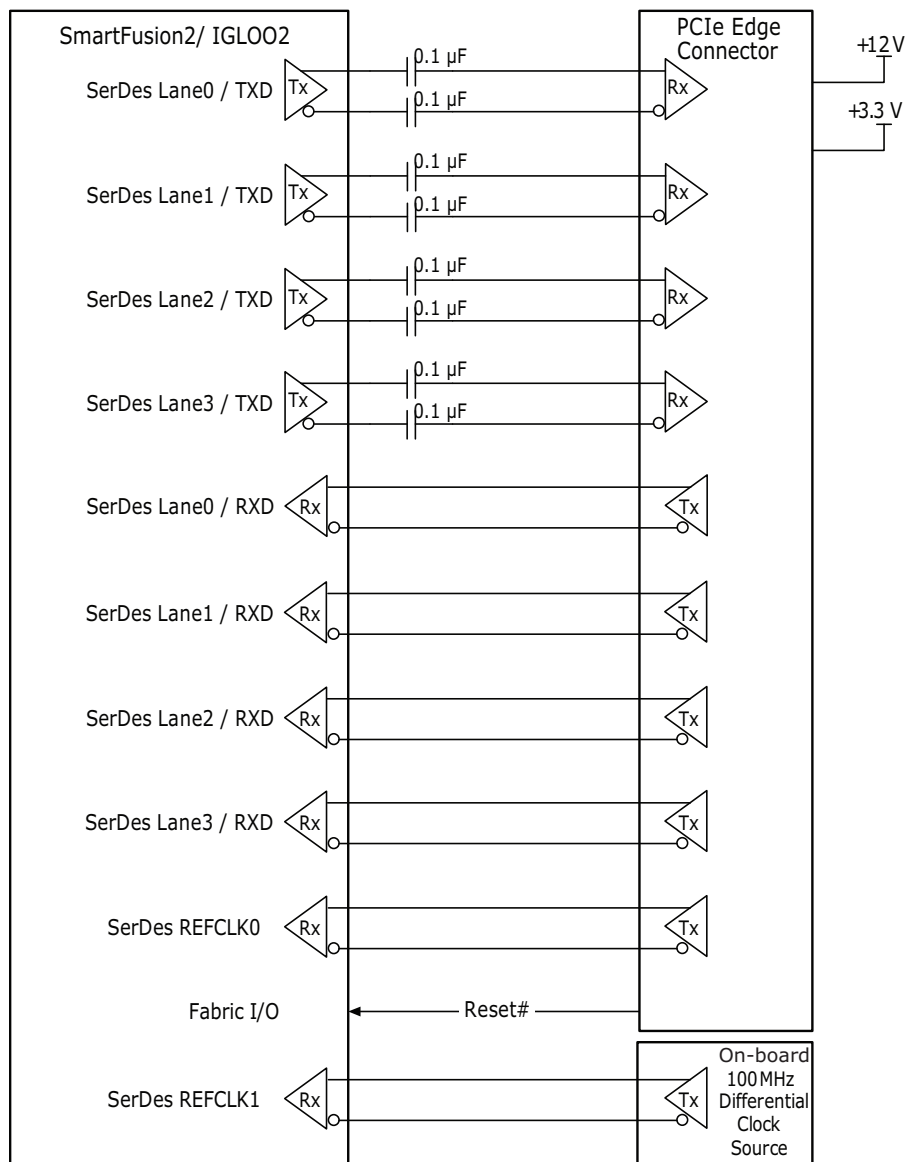
2.8.2 AC Coupling

Each transmit channel of a PCIe lane must be AC coupled to allow link detection.

For non-PCIe applications, the SmartFusion2/IGLOO2 device requires the receive inputs to be AC coupled to prevent common-mode mismatches between devices. Suitable values (for example, 0.1 µF) for AC-coupling capacitors must be used to maximize link signal quality and must conform to *DS0128: IGLOO2 and SmartFusion2 Datasheet* electrical specifications.

2.8.3 SerDes Reference Clock Requirements

The selection of the reference clock source or clock oscillator is driven by many parameters such as frequency range, output voltage swing, jitter (deterministic, random, and peak-to-peak), rise and fall times, supply voltage and current, noise specification, duty cycle and duty cycle tolerance, and frequency stability.

For SerDes reference clock pins, the internal ODT option should be enabled, and therefore, external termination is not required.

Following are the requirements for the SerDes reference clock:

- Must be within the range of 100 MHz to 160 MHz.
- Must be within the tolerance range of the I/O standard.
- The input clock for PCIe is typically a 100 MHz reference clock provided by the host slot for an end point device through the PCIe connector of the motherboard. If two components connected through the PCIe bus use the same 100 MHz clock source, it is called common clock mode. In any other case, the PCIe device is in separated clock mode where one component either does not use a 100 MHz reference clock or uses a 100 MHz reference clock that does not have the same source and phase as the one used by the connected component.

See the PCI Express Base specification Rev 2.1 for detailed PHY specifications. Also see the PCIe Add-in Card Electro-Mechanical (CEM) specifications.

2.8.4 PLL Filter

To obtain a reasonable level of long-term jitter, it is vital to supply the PLL with analog-grade power. Typically, an RC or RLC filter is used, where C is composed of multiple devices to obtain a wide spectrum of noise absorption. Although the circuit is simple, its effectiveness depends on specific board layout requirements. See Figure 1, page 6 for an illustration of a typical power supply connection.

- The DC series resistance of this filter should be limited. Microsemi recommends limiting the voltage drop across this device to less than 5% under worst-case conditions.
- Place a main ceramic or tantalum capacitor (see Figure 1, page 6), in the filter design to obtain good low-frequency cut-off. At least one low equivalent series inductance (ESL) and low ESR capacitor in parallel (~0.1 µF ceramic capacitor in 0402 package) enables the filter to maintain its attenuation through moderately high frequencies.
- The package ball grid array (BGA) pattern allows the placement of 0402 or 0201 components across the SERDES_x_Lyz_VDDAPLL and SERDES_x_Lyz_REFRET pins on the backside of the board.
- For the SerDes block, SERDES_x_Lyz_REFRET serves as the local on-chip ground return path for SERDES_x_Lyz_VDDAPLL. Therefore, the external board ground must not get shorted with SERDES_x_Lyz_REFRET under any circumstances.
- High-quality series inductors must not be used without a series resistor when there is a high-gain series resonator. In general, avoid using inductive chokes in any supply path unless care is taken to manage resonance.

See Figure 1, page 6 for SerDes analog power connections. A high-precision 1.2 KΩ, 1% resistor in either a 0402 or 0201 package is required for the external reference resistor connected between SERDES_x_Lyz_REXT and SERDES_x_Lyz_REFRET.

2.9 LPDDR, DDR2, and DDR3

DDRIO is a multi-standard I/O buffer optimized for LPDDR, DDR2, and DDR3 performance. SmartFusion2/IGLOO2 devices include two DDR subsystems: the fabric DDR controllers (FDDR) and microcontroller subsystem (MSS) DDR (MDDR) controllers. All DDRIO can be configured as differential I/O or two single-ended I/O. DDRIO can be connected to the respective DDR sub-system PHYs or can be used as user I/O.

For more information on FDDR and MDDR, see the *SmartFusion2 FPGA Fabric DDR Controller Configuration Guide* and *SmartFusion2 MSS DDR Controller Configuration Guide.*

The following table lists the differences between LPDDR, DDR2, and DDR3.

Table 15 • **LPDDR/DDR2/DDR3 Parameters**

Parameter	LPDDR	DDR2	DDR3
VDDQ	1.8 V	1.8 V	1.5 V
VTT, VREF		0.9 V	0.75 V
Clock, address, and command (CAC) layout	Asymmetrical tree branch	Symmetrical tree branch	Daisy chained (fly-by)
Data strobe	Single-ended	Differential	Differential
ODT	None	Static	Dynamic
Match Addr/CMD/Ctrl to clock tightly	Yes	Yes	Yes
Match DQ/DM/DQS tightly	Yes	Yes	Yes
Match DQS to clock loosely	Yes	Yes	Not required
Interface	LVCMOS_18 or SSTL18 for LPDDR1	SSTL_18	SSTL_15
Impedance Calibration	LVCMOS18 - Not required SSTL18 - Required	150_1%	240_1%

One major difference between DDR2 and DDR3 SDRAM is the use of data leveling. To improve signal integrity and support higher frequency operations, a fly-by termination scheme is used with the clocks, command, and address bus signals. Fly-by termination reduces simultaneous switching noise by deliberately causing flight-time skew between the data strobes at every DDR3 chip. Fly-by termination requires controllers to compensate for this skew by adjusting the timing per byte lane. To obtain length matching, short TMATCH_OUT to TMATCH_IN with the shortest loop.

For more information about DDR memories, refer to the following documents:

- JESD209B-JEDEC STANDARD—Low Power Double Data Rate (LPDDR) SDRAM Standard
- JESD79-2F-JEDEC STANDARD—DDR2 SDRAM Specification
- JESD79-3F-JEDEC STANDARD—DDR3 SDRAM Standard

2.9.1 MDDR/FDDR Impedance Calibration

The MDDR and FDDR have a DDRIO calibration block. DDRIO can use fixed impedance calibration for different drive strengths, and these values can be programmed using the Libero SoC software for the selected I/O standard.

Before initiating DDRIO impedance calibration, either of the following must be done:

- Power sequencing, where the DDRIO bank VDDIx supply must be up and stable before VDD core supply.
- DDRIO re-calibration through the APB interface after DDRIO- VDDIx and VDD are up and stable.

For more information on impedance calibration, see the *UG0445: SmartFusion2 SoC and IGLOO2 FPGA Fabric User Guide*.

2.9.2 VREF Power

VREF is a low-power reference voltage equal to half of VDDQ. It must also be equal to VTT ± 40 mV. The following figure shows the VREF generation circuit.

Figure 15 • **VREF Generation**
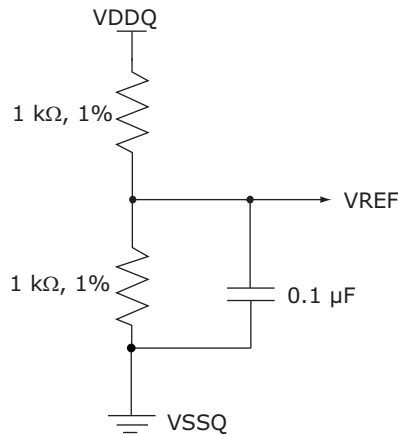
The following are the guidelines for connecting VREF power:

- For light loads (less than four DDR components), connect VDDQ to VSSQ through a simple resistor divider composed of two equivalent 1% 1 kΩ resistors (Figure 15, page 28).
- Generate a local VREF at every device, rather than generating a single VREF with one divider and routing it from the controller to the memory devices.
- Decouple at each device or connector to minimize noise.

Note: Use discrete resistors, not a resistor pack, to generate VREF.

2.9.3 VTT Power

VTT is memory bus termination voltage. To maintain noise margins, VTT must be equal to VDDQ/2, with an accuracy of ± 3%. VTT terminates command and address signals to VDDQ/2 using a parallel resistor (RT) tied to a low impedance source.

VTT is not used to terminate any DDR clock pairs. Rather, the xDDR_CLK and xDDR_CLK_N termination consists of a parallel 100-121 Ω resistor between the two lines.

- VTT islands require a 10µF capacitor.
- Since each data line is connected to VTT with relatively low impedance, this supply must be extremely stable. Any noise on this supply directly affects the data lines.
- Sufficient bulk and bypass capacitance must be provided to keep this supply at VDDQ/2. VREF power should not be derived from VTT, but must be derived from VDDQ with a 1% or better resistor divider.

2.9.4 LPDDR and DDR2 Design

This document assumes that the designer is familiar with the specification and the basic electrical operation of the LPDDR/DDR2 interface. Data bus, data strobe, and data mask (byte enable) signals are point-to-point, whereas all other address, control, and clock signals are not point-to-point. Figure 16, page 29 and Figure 17, page 30 show the connectivity of the SmartFusion2/IGLOO2 LPDDR interface and a 32-bit DDR2 interface respectively.

Figure 16 • **LPDDR Interface**
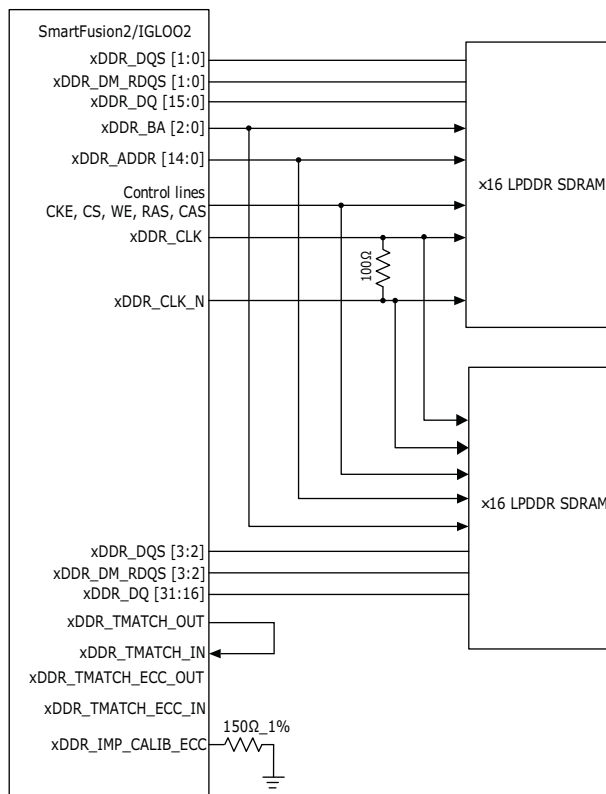
Note: Impedance calibration is optional for LPDDR operating in LVCMOS mode and is required for LPDDR1 operating in SSTL18 mode.

Note: For a 4- or 8-bit DRAM, all DQ pins are interchangeable. All 4- and 8-bit DQ pins are interchangeable in LPDDR, DDR2, and DDR3 memories. For a 16-bit DRAM, DQ0 through DQ7 are interchangeable. Also, DQ8 through DQ15 are interchangeable. However, DQ0-7 pins or signals *must not* be interchanged with the DQ8-15 pins or signals.

Note: Short ECC_TMATCH_ OUT and ECC_TMATCH_ IN when using ECC bits.

Figure 17 • **DDR2 Interface**
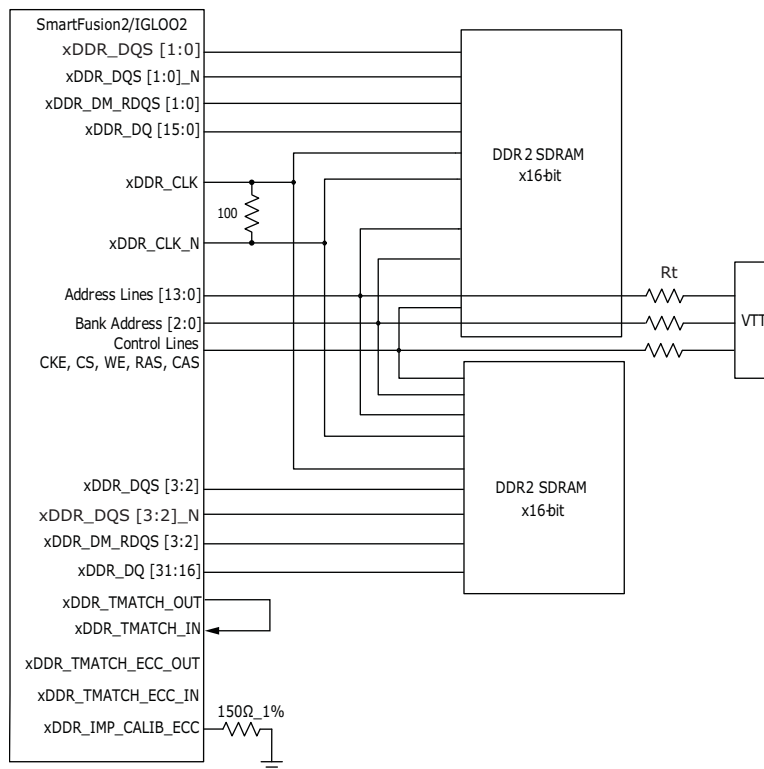
With short traces, the address, control, and command signals may not require both parallel (RT) and series (RS) termination. In a worst-case scenario, a small series resistor (RS) of about 10 Ω or less is required. This series termination is not used for impedance matching, but for dampening the signals.

Note: To get length matching, short the TMATCH_OUT to TMATCH_IN with the shortest loop.

Note: Short ECC_TMATCH_ OUT and ECC_TMATCH_ IN when using ECC bits.

2.9.5 DDR3 Guidelines

The following are the guidelines for connecting to the DDR3 memory:

- DDR3 data nets have dynamic on-die termination (ODT) built into the controller and SDRAM. The configurations are 40 Ω, 60 Ω, and 140 Ω. VTT pull-up is not necessary.
- Characteristic impedance: Zo is typically 50 Ω, and Zdiff (differential) is 100 Ω.

DDR3 interfacing with SmartFusion2/IGLOO2 devices for 8-bit and 16-bit interfaces is shown in Figure 18, page 31 and Figure 19, page 31.

Figure 18 • **8-Bit DDR3 Interface**
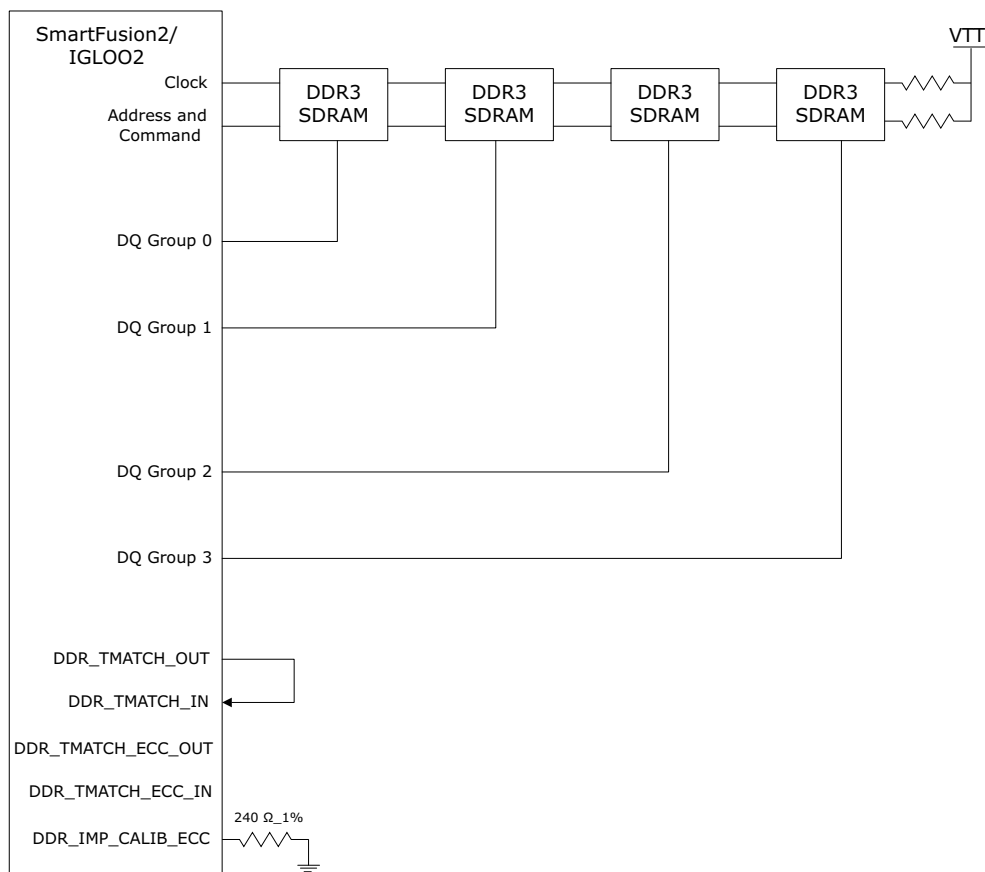
Figure 19 • **16-Bit DDR3 Interface**
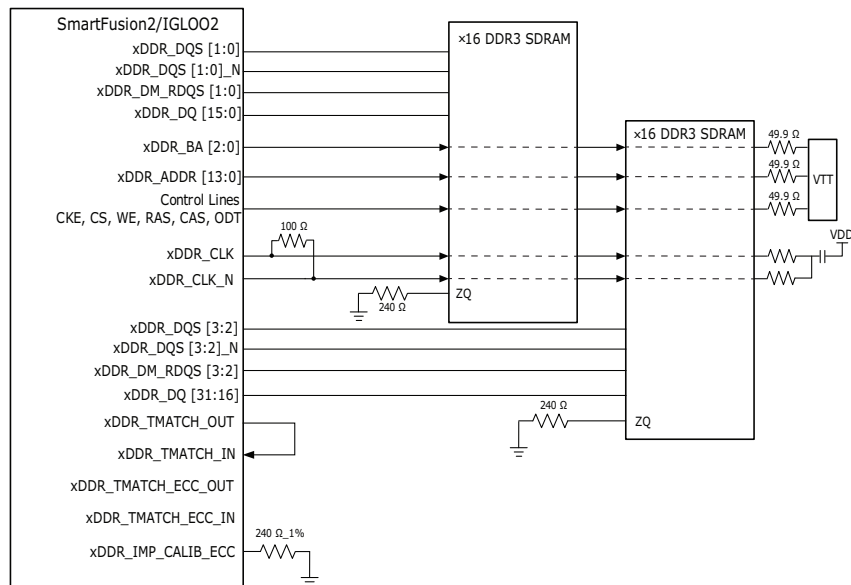
Note: Short ECC_TMATCH_ OUT and ECC_TMATCH_ IN when using ECC bits.

2.10　User I/O and Clock Pins

The following table lists recommendations for unused I/O and clock pins in a SmartFusion2/IGLOO2 device.

*Table 16 •*　**Recommendations for Unused I/O and Clock Pins**

I/O	Unused Condition	Remarks
MSIO	Libero-Defined DNC[1]	Internal weak pull-up is available
MSIOD		
DDRIO		
Programming SPI pins		
Crystal oscillator pins	Must be left floating and must not connect to ground (VSS)	Internal weak nominal 50 kΩ pull-up to VPP

1.　Libero configures unused user I/O (MSIO, MSIOD, and DDRIO) as: input buffer disabled, output buffer tristated with weak pull-up.

2.10.1　Internal Clamp Diode Circuitry

All user I/Os have an internal clamp diode control circuitry, as shown in the following figure. A pull-up clamp diode must not be present in the I/O circuitry if the hot-swap feature is used. The 3.3 V PCI standard requires a pull-up clamp diode and, therefore, cannot be selected if hot-swap capability is required.

Figure 20 •　**Internal Clamp Diode Control Circuitry**
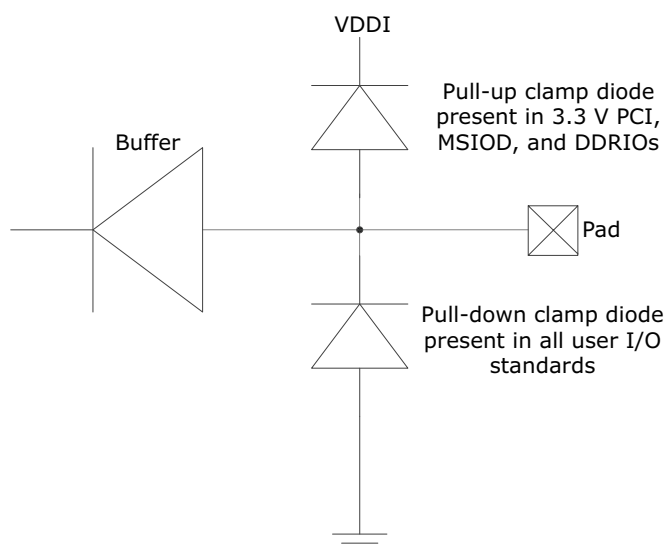
For more information about hot swapping and cold sparing applications, see the *AC396: SmartFusion2 and IGLOO2 in Hot Swapping and Cold Sparing Application Note*.

2.11 Obtaining a Two-Rail Design for Non-SerDes Applications

SmartFusion2/IGLOO2 devices require multiple power supplies for functional operation, programming, and high-speed serial interfaces. It is possible to design an application with only two voltage rails using SmartFusion2/IGLOO2 devices.

I/O banks in SmartFusion2 and IGLOO2 devices support a wide range of I/O standards. I/O bank supplies can operate at +1.2 V, +1.5 V, +1.8 V, +2.5 V, or +3.3 V. To obtain a two-voltage-rail design, the core voltage should be connected to +1.2 V, and the mandatory I/O bank supplies and VPP supplies can be connected to +2.5 V or +3.3 V.

2.11.1 Operating Voltage Rails

SmartFusion2/IGLOO2 devices require +1.2 V for the core supply and either +2.5 V or +3.3 V for I/O and analog supplies. The following table lists operating voltage requirements for the devices.

Table 17 • **Operating Voltage Rails**

| Pin Name	Description	Operating Voltage
VDD	DC core supply voltage.	+1.2 V
VDDIx[1]	I/O bank supply.	+1.2 V, +1.5 V, +1.8 V, +2.5 V, or +3.3 V
SERDES_x_VDD	PCIe/PCS supply.	+1.2 V
SERDES_x_L[01/23]_VDDAIO	Tx/Rx analog I/O voltage. Low-voltage power for lanes 0, 1, 2, and 3 of the SerDes interface.	+1.2 V
VPP[2]	Power supply for charge pump.	+2.5 V or +3.3 V
VPPNVM[1]	Analog sense-circuit supply for the embedded non-volatile memory (eNVM).	+2.5 V or +3.3 V
CCC_xyz_PLL_VDDA	Analog power pad for CCC PLL.	+2.5 V or +3.3 V
MSS/HPMS_xDDR_PLL_VDDA	Analog power pad for xDDR PLL.	+2.5 V or +3.3 V
SERDES_x_PLL_VDDA	High supply voltage for SerDes PLL.	+2.5 V or +3.3 V
SERDES_x_L[01/23]_VDDAPLL	Analog power for SerDes PLL of lanes 0, 1, 2, and 3.	+2.5 V

1. The 3.3 V supply can be connected to MSIO VDDIx bank only.
2. For M2S090T(S), M2S150T(S) devices, VPP, and VPPNVM must be connected to +3.3 V.

2.12 Configuring Pins in Open Drain

To configure fabric pins in open-drain mode, the input port of the tristate buffer must be tied low, and the enable port of the buffer must be driven from the user logic via the fabric port, as shown in the following figure. For more information about the bank supplies, see Table 4, page 13 to Table 7, page 15 and Table 16, page 32.

Figure 21 • **Configuring Pins in Open Drain**
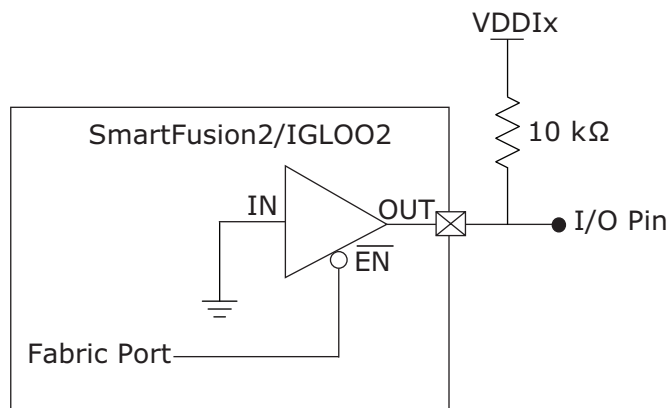
The following table lists the truth table for configuring pins in open-drain mode.

Table 18 • **Truth Table**

Buffer Enable Port	Buffer In Port	Buffer Out Port
0 (low)	0 (low)	0 (low)
1 (high)	0 (low)	$VDDI_X$

2.13 Brownout Detection (BOD)

SmartFusion2/IGLOO2 functionality is guaranteed only if VDD is above the recommended level specified in the datasheet. Brownout occurs when VDD drops below the minimum recommended operating voltage. As a result, it is not possible to ensure proper or predictable device operation. The design might continue to malfunction even after the supply is brought back to the recommended values, as parts of the device might have lost functionality during brownout. The VDD supply must be protected by a brownout detection circuit.

To recover from VDD brownout, the device must either be power-cycled, or an external brownout detection circuit must be used to reset the device for correct operation. The recommended guideline for the threshold voltage of brownout detection is mentioned in "Table 14" of *DS0128: IGLOO2 and SmartFusion2 Datasheet*. The brownout detection circuit must be designed such that when the VDD falls below the recommended voltage mentioned in the datasheet, the device is held in power-down mode via the DEVRST_N pin.

Note: Brownout detection must be implemented through a standalone circuit or included as part of power management circuitry.

SmartFusion2/IGLOO2 devices do not have a built-in brownout detection circuitry, but an external brownout detection circuitry can be implemented as shown in the following figure.

Figure 22 • **BOD Circuit Implementation**
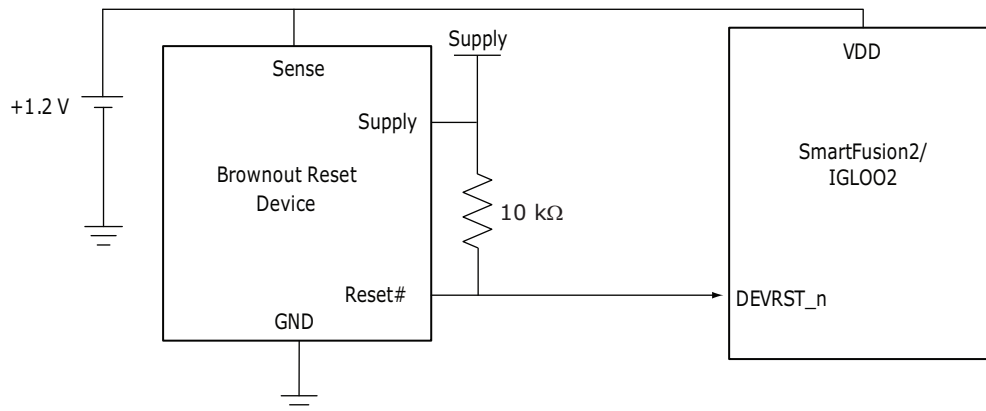
The BOD device must have an open-drain output to connect to VPP through a 10 kΩ resistor externally. During power-on, the brownout reset keeps the device powered down until the supply voltage reaches the threshold value. Thereafter, the brownout reset device monitors VDD and keeps RESET# output active as long as VDD remains below the threshold voltage. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset.

The delay time is in milliseconds and starts after VDD has risen above the threshold voltage. When the supply voltage drops below the threshold voltage, the output becomes active (low) again.

2.14 Simultaneous Switching Noise

When multiple output drivers switch simultaneously, they induce a voltage drop in the chip or package power distribution. The simultaneous switching momentarily raises the ground voltage within the device relative to the system ground. This apparent shift in the ground potential to a non-zero value is known as simultaneous switching noise (SSN) or, more commonly, ground bounce.

For SSO guidelines for SmartFusion2 and IGLOO2 I/Os, see *UG0445: SmartFusion2 SoC FPGA and IGLOO2 FPGA Fabric User Guide*.

3 Layout Guidelines for SmartFusion2 and IGLOO2 Based Board Design

This chapter provides guidelines for the hardware board layout that incorporates SmartFusion2 SoC FPGA or IGLOO2 FPGA devices. Good board layout practices are required to achieve the expected performance from the printed circuit boards (PCB) and SmartFusion2/IGLOO2 devices. These are essential to achieve high quality and reliable results such as low-noise levels, signal integrity, impedance, and power requirements. The guidelines mentioned in this document act as a supplement to the standard board-level layout practices.

This chapter assumes that the users have a good understanding of the SmartFusion2/IGLOO2 chip, experience in digital and analog board layout, and knowledge of transmission line theory and signal integrity. For more information about the recommended guidelines for designing SmartFusion2/IGLOO2-based boards, see Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs, page 5.

3.1 Power Supply

In power supply design, it is important to know the target impedance of the power planes. The target impedance varies depending on the design. This helps in planning the requirement of the number of decoupling capacitors based on the target impedance. The number of decoupling capacitors varies based on the design.

Complex FPGA designs have increasing amounts of current transients switching across the power bus. Simultaneously switching outputs (SSO) contribute a major share of instantaneous current issues. Decoupling is necessary to prevent the instantaneous currents. Decoupling is only effective when inductance is minimized. Low inductance decoupling provides localized high frequency energy to decouple noise from the switching currents of the device power bus. This is most effective when capacitors are in close proximity to the device. Some of these high-frequency de-coupling capacitors must be placed directly under the FPGA or on single side. These capacitors must be placed close to the power and ground pins of the device and routed with thick trace.

To calculate the number of decoupling capacitors, it is important to know the target impedance of the power plane. Target impedance is calculated as follows:

$$Z_{Max} = \% \ Ripple \times \frac{V_{supply}}{I_{trans}}$$

Where,

V_{supply}: Supply voltage of the power plane.

% Ripple: % of ripples allowed on the power plane; see *DS0128: IGLOO2 and SmartFusion2 Datasheet* for more information about ripple in Recommended Operating Conditions table.

I_{trans}: Transient current drawn on the power plane. Generally, the transient current is half of the maximum current. Maximum current is taken from the power calculator sheet.

Z_{max}: Target impedance of the plane.

Subsequent sections display simulation results based on target impedance calculated using preceding equation. Microsemi recommends calculating the target impedance and performing simulations for the impedance profile of the power plane. These simulations help in optimizing the decoupling capacitors to reduce the production cost and have the optimal placement. The plane shapes given in this document are with reference to the *UG0557: SmartFusion2 SoC FPGA Advanced Development Kit User Guide.* This may vary depending on the design. For simulation topology, see Appendix: Power Integrity Simulation Topology, page 92.

SmartFusion2/IGLOO2 power supplies are classified as:

- Core power supply
- I/O power supply
- Serializer/deserializer (SerDes) power supply
- Double data rate (DDR) power supply
- Phase-locked loop (PLL) power supply

3.2 Core Supply (VDD)

The core power supply must have a low-noise and low-ripple voltages, as per datasheet. Proper care should be taken while designing the power supply (VDD) for core. Proper placement of decoupling capacitors and plane geometry greatly influences the power supply distribution going into SmartFusion2/IGLOO2 device.

3.2.1 Component Placement

- The bulk capacitors (330 µF and 100 µF) should be placed near by the SmartFusion2/IGLOO2 device.
- The bypass capacitors (47 µF and 22 µF) should be placed near or if possible, on the periphery of the device. The placement on the SmartFusion2 Development Kit board is shown in the following figure.

Figure 23 • **Placement of Capacitors for VDD Plane**
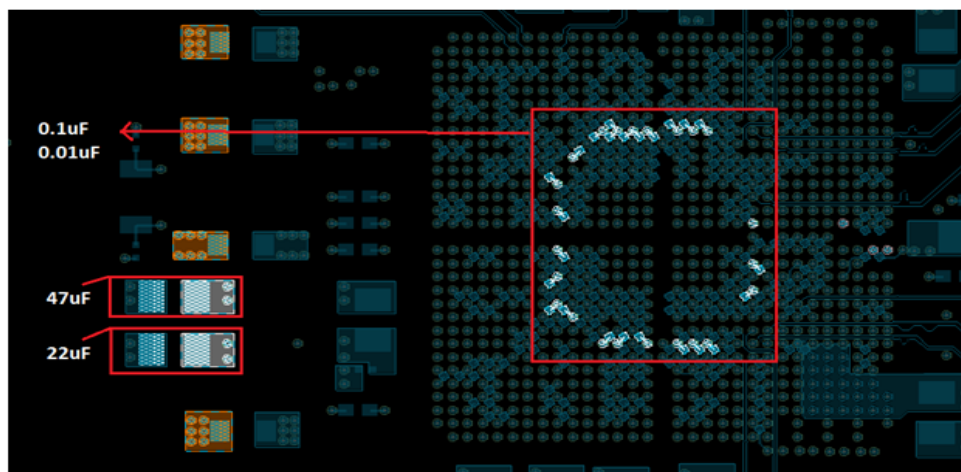
- All decoupling capacitors (0.1 µF and 0.01 µF) should be 0402 or of a smaller package size, as they are required to be mounted on the back side of the board. They should be fit between the adjacent vias of ball grid array (BGA) package pins. These decoupling capacitors are selected to have a low impedance over operating frequency and temperature range. Capacitor pad to via trace should be as small as possible. The following figure shows how these capacitors need to be mounted. Microsemi recommends keeping the capacitor pad directly on the corresponding vias. The capacitors should not share ground vias. Each decoupling capacitor should have its own via connection to the PCB ground plane.
- The De-coupling capacitor and the Smart Fusion2\IGOOL2 device can be placed side by side. If placed side by side, route the power with thick traces. Microsemi does not guarantee on noise on power rails. User must run the power simulation.

Figure 24 • **Capacitor Placement under BGA Vias**
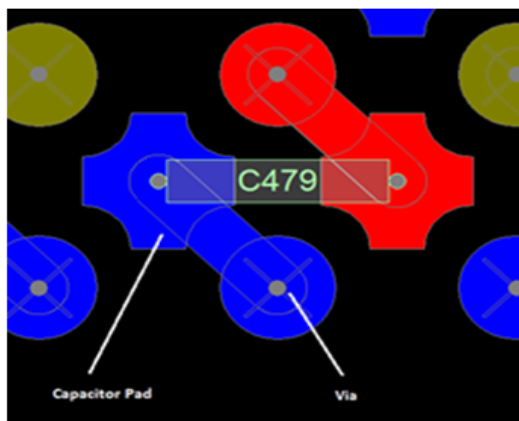
3.2.2 Plane Layout

Microsemi recommends using the VDD plane, as shown in the following figure.

**Note:** The plane can be routed in multiple ways. The goal is to have a dedicated and low-impedance plane.

Figure 25 • **VDD Plane**
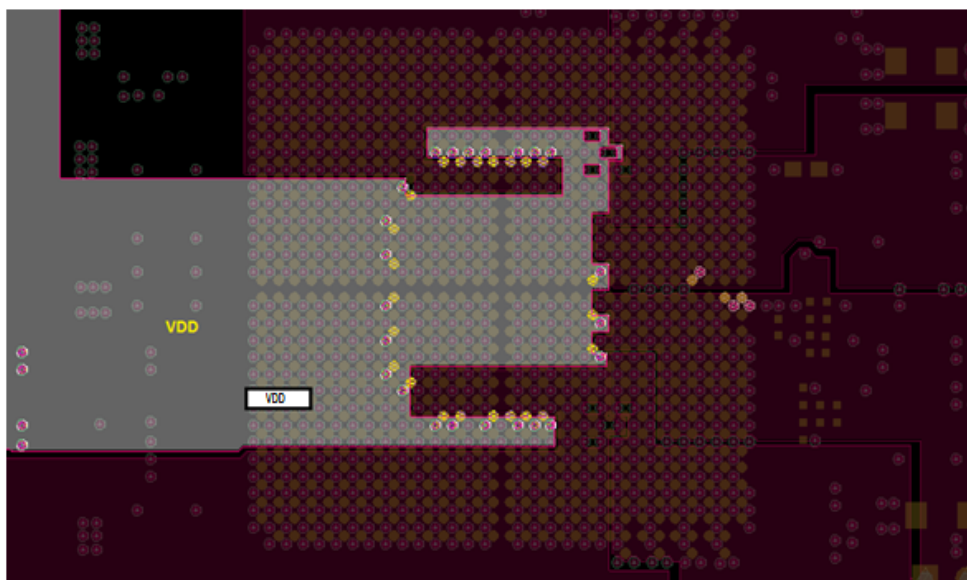
3.2.3 Simulations

The effect of the decoupling capacitors can be visualized through the power integrity simulations. The target impedance of the VDD is calculated as 40 mΩ, based on the following values:

- V_{SUPPLY} = 1.2 V
- I_{trans} = 1.5 A
- Ripple = 5%

Figure 26, page 39 shows the impedance profile of the VDD plane of the SmartFusion2 Development Kit. It shows that the capacitors used are adequate to improve the impedance profile over the bandwidth. Good coupling between the planes can be achieved by having power and ground plane in adjacent layers. Once all the capacitors (0.1 µF and 0.01 µF) are placed, the impedance of the VDD plane impedance profile improves over the frequency range. The simulation results shown in this document are done in Sigrity PowerSI tool. For more information on how to do the simulation, see the *Sigrity PowerSI Tutorial*.

Figure 26 • **Impedance Profile of VDD Plane with Respect to Frequency**

Z Amplitude (Ω)

Frequency (GHz)

———— VDD Plane with Decoupling Capacitors
———— VDD Plane without Decoupling Capacitors
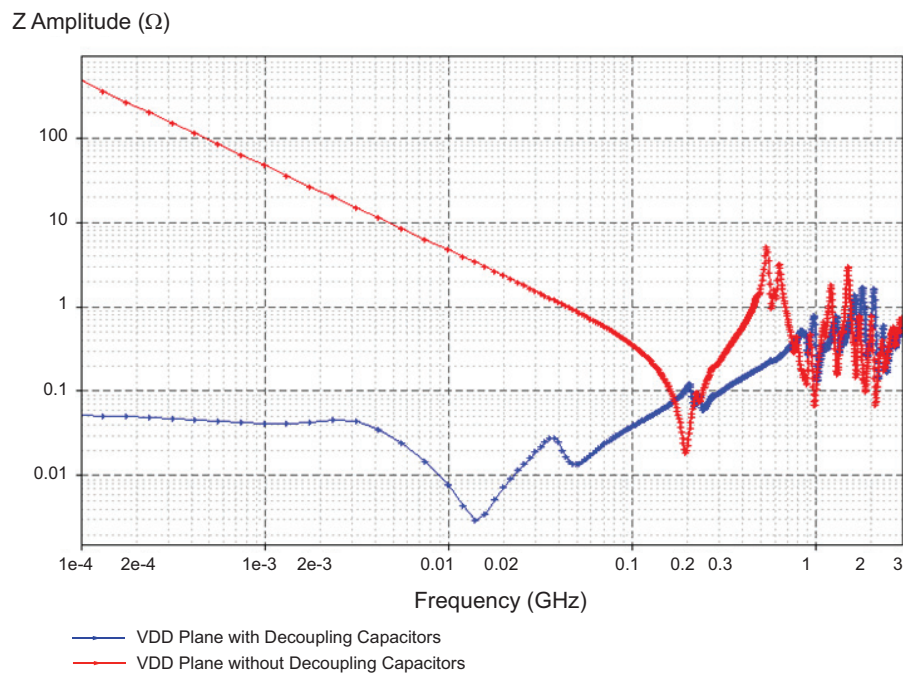
3.3 SerDes

PCB designers often overlook the requirement of isolating the noise generated by the digital components with the SerDes high-speed designs. It is necessary to provide a low-noise supply for the sensitive analog portions of the SerDes devices. Noise due to various power supply voltages can be coupled into the analog portion of the chip and may produce unwanted fluctuations in the sensitive stages of the device. The performance of SerDes highly depends on robust layout techniques. This section discusses the layout guidelines for power supply for the SerDes and the SerDes PLL.

3.3.1 Component Placement

3.3.1.1 Core Power (SERDES_x_VDD)

- All decoupling capacitors (0.1 µF and 0.01 µF) are placed on the pad adjacent to the BGA via of the corresponding pin, as shown in Figure 24, page 38. The capacitor pad to via trace should be as small as possible. At least one 0.1 µF and one 0.01 µF capacitors should be placed for each SerDes bank.
- The bypass capacitor (10 µF) should be placed at the edge of the integrated circuit (IC).

3.3.1.2 SerDes I/O Power (SERDES_x_VDDAIO)

- All decoupling capacitors (0.1 µF and 0.01 µF) are placed on the pad adjacent to the BGA via of the corresponding pin, as shown in Figure 23, page 37. At least one of the capacitors (0.1 µF and 0.01 µF) should be placed for each SerDes bank. The capacitor pad to via trace should be as small as possible.
- The bypass capacitor (10 µF) should be placed at the edge of the IC.

3.3.1.3 SerDes PLL

There are two power supply nodes required for SerDes. One is SERDES_x_VDDAPLL and another is SERDES_x_PLL_VDDA. Both of these supplies require separate filter circuits. Filter circuit for SERDES_x_VDDAPLL is shown in the following figure. A typical filter circuit for SERDES_x_PLL_VDDA is shown in the following figure.

Figure 27 • **Filter Circuit for SerDes PLL Power Supply**
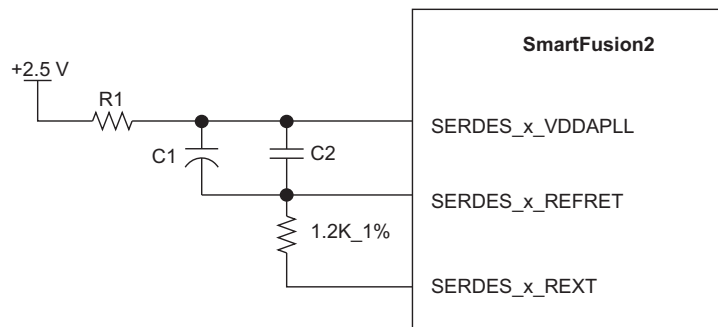
- C1 and R1 should be placed near the device.
- C2 should to be placed under the BGA via. The capacitor pad to via trace should be as small as possible.
- Apart from this, a precision resistor (1.2 K) is placed between the SERDES_x_REXT and SERDES_x_REFRET pins. This resistor should be placed near the BGA via of SERDES_x_REXT pin. Any aggressive signal traces should be kept away from this resistor to avoid unwanted noise from coupling into this critical circuit. A sample placement is shown in the following figure.

Figure 28 • **Component Between 1.2 K Resistor and K6 Pin**

For more information about R1, C1, and C2, see Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs, page 5.

3.3.2 Plane Layout

3.3.2.1 SerDes Core Power (SERDES_x_VDD)

Even though SERDES0 and SERDES1 cores share the same power supply, separate planes must be made while connecting to corresponding SerDes blocks, as shown in the following figure. This reduces the noise coupling between SERDES0 and SERDES1 blocks.

Figure 29 • **Layout for SERDES_x_VDD Plane**
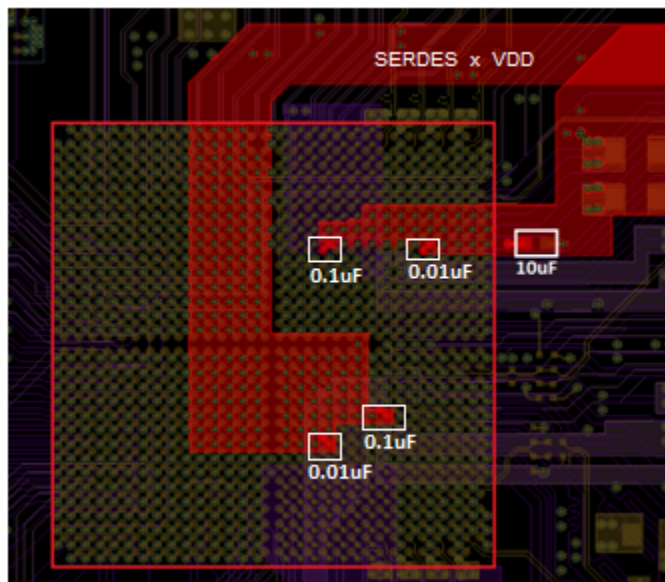
3.3.2.2 SerDes I/O Power (SERDES_x_VDDAIO)

• Even though SERDES0 and SERDES1 I/Os share the same power supply, make separate planes while connecting to the corresponding pins, as shown in the following figure. Each plane is separated as SERDES_0_L01_VDDAIO, SERDES_0_L23_VDDAIO, SERDES_1_L01_VDDAIO, and SERDES_1_L01_VDDAIO, as shown in the following figure. This reduces the noise coupling between the differential lanes.

Figure 30 • **Layout of SERDES_x_VDDAIO Plane**

3.3.2.3 SerDes PLL

- Plane routing for SERDES_1_L01_VDDAPLL and SERDES_1_L01_REFRET is shown in the following figure.
- SERDES_1_L01_VDDAPLL and SERDES_1_L01_REFRET should not be routed as traces. A small trace width causes poor noise performance due to the high inductive behavior of the trace. Even though the current requirement is low, these supply traces should be routed as small planes, as shown in the following figure.
- The connections of 1.2 kΩ resistor and SERDES_1_L01_REXT of SmartFusion2/IGLOO2 should not be routed as a thick plane. It must be routed as a signal trace in-order to meet minimum capacitance requirement of the SERDES_1_L01_REXT pin. The length of the trace should be as short as possible. The following figure shows the sample layout.
- Same layout guidelines should be followed for the remaining SerDes PLL power supplies.

Figure 31 • **Layout of SERDES_1_L01_VDDAPLL and SERDES_1_L01_REFRET**
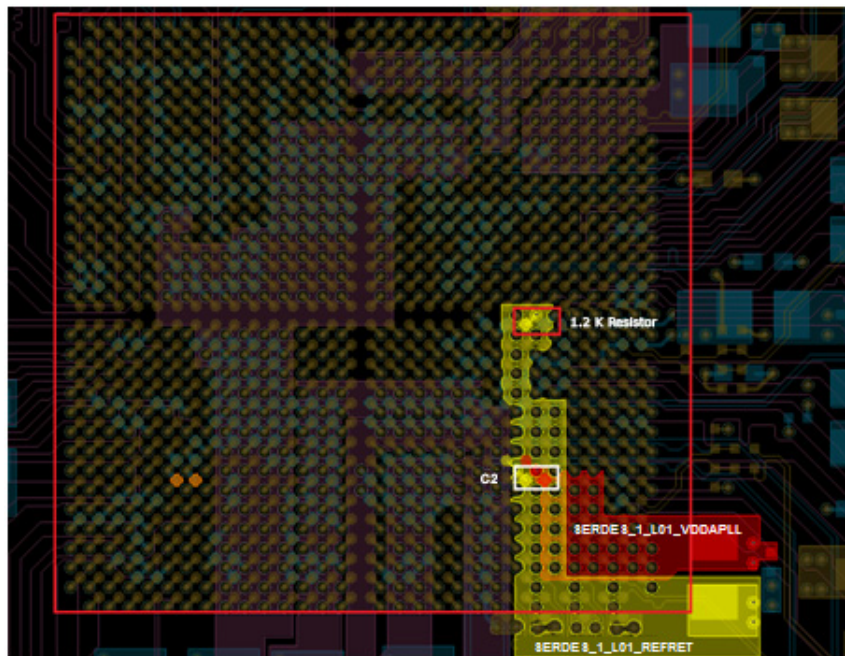
3.3.3 Simulations

3.3.3.1 SerDes Core Power (SERDES_x_VDD)

The target impedance of the SERDES_x_VDD pin is calculated as 300 mΩ, based on the following values (see Power Supply, page 36):

- V_{SUPPLY} = 1.2 V
- I_{trans} = 200 mA
- Ripple = 5%

Figure 32, page 43 shows the impedance of the plane (SERDES_x_VDD) improved by the decoupling capacitors. The impedance of the plane is kept under 0.2 Ω till 100 MHz.

Figure 32 • **Impedance Profile of SERDES_x_VDD Plane Over Frequency Range**
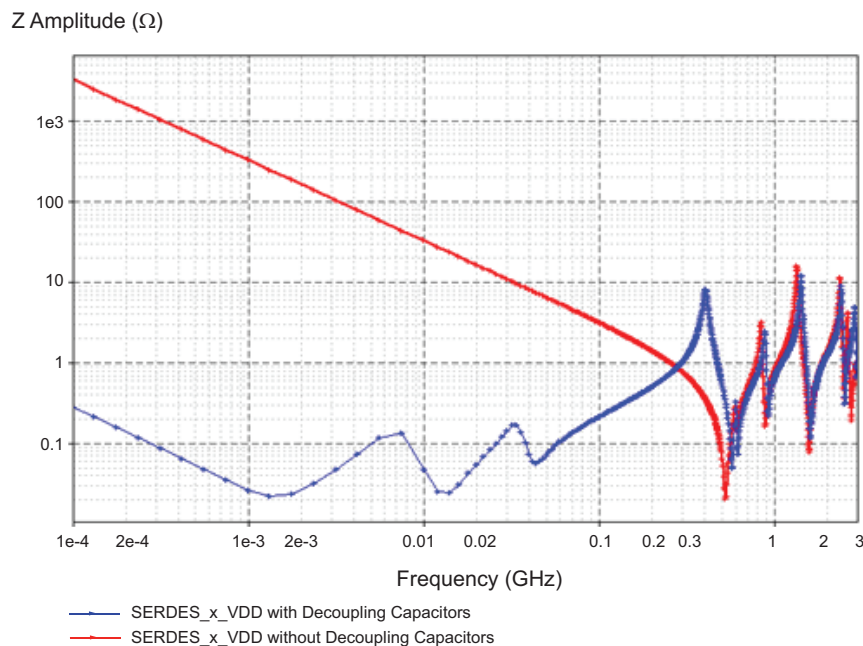
3.3.3.2 SerDes I/O Power (SERDES_x_VDDAIO)

The target impedance of the SERDES_x_VDDAIO pin is calculated as 240 mΩ, based on the following values (see Power Supply, page 36):

* V_{SUPPLY} = 1.2V
* I_{trans}= 250mA
*   Ripple = 5%

The following figure shows the impedance of the plane (SERDES_x_VDDAIO) improved by the decoupling capacitors. The impedance of the plane is kept under 0.2 Ω till 100 MHz.

Figure 33 • **Impedance Profile of SERDES_x_VDDAIO Plane Over Frequency Range**
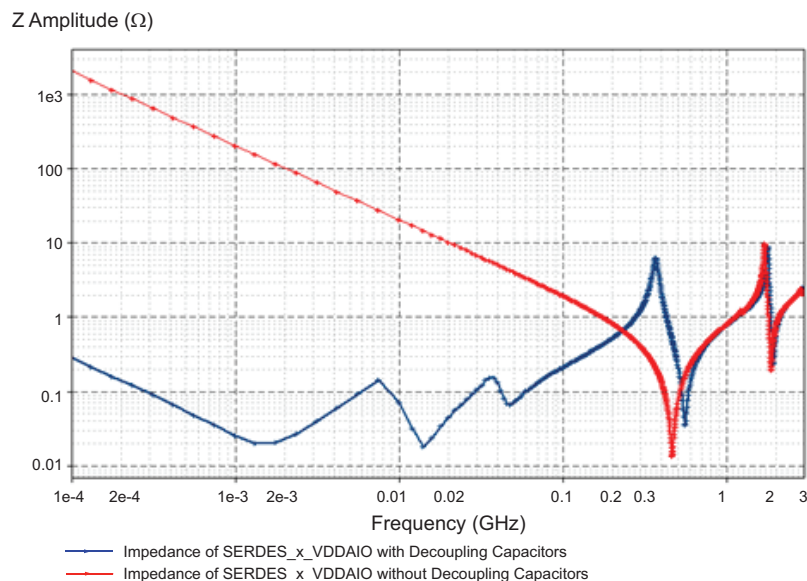
3.4　DDR

Some of the variants support the fabric DDR (FDDR) and microcontroller subsystem DDR (MDDR) and some variants support only FDDR in SmartFusion2. Refer datasheet to see on which bank DDR is supported on each particular device. The layout guidelines of the respective VDDIO should be followed. Apart from that, it requires VREF voltage for an internal reference. Noise on VREF impacts the read performance of SmartFusion2/IGLOO2 devices. VREF lines should not be routed near the aggressive nets or switching power supplies. For more information about DDR memory layout guidelines, see the *Micron DDR3 Memory Layout Guidelines*. The VDDIO guidelines should be followed for DDR bank VDDIO. This section explains the guidelines to be used for VREF.

3.4.1　Component Placement

3.4.1.1　VREF

- The bypass capacitor (10 µF) should be placed near, or at the edge of the device if possible.
- All decoupling capacitors (0.1 µF and 0.01 µF) should be 0402 or of a smaller package size as they are required to be mounted on the reverse side of the board. They should be fit between the adjacent vias of the BGA package pins. These decoupling capacitors are selected to have a low impedance over the operating frequency and temperature range.
- The capacitor pad to via trace should be as small as possible. Figure 23, page 37 shows how these capacitors are mounted. Microsemi recommends keeping the capacitor pad directly on the corresponding vias.

3.4.1.2　VDDIO

- The bypass capacitors (47 µF and 22 µF) should be placed near, or at the edge of the device if possible.
- All decoupling capacitors (0.1 µF and 0.01 µF) should be 0402 or of a smaller package size as they are required to be mounted on the reverse side of the board. They should be fit between the adjacent vias of the BGA package pins. These decoupling capacitors are selected to have a low impedance over the operating frequency and temperature range.
- The capacitor pad to via trace should be as small as possible. Figure 23, page 37 shows how these capacitors are mounted. The capacitors can also be mounted directly on the pad available on the vias.

3.4.2　Plane Layout

3.4.2.1　VREF

Noise on VREF impacts the read performance of SmartFusion2/IGLOO2 devices. The VREF lines should be routed with no aggressive net or switching power supply nearby. Even the current is low, VREF should not be routed as trace as it is very susceptible to noise.

The following figure shows the VREF5 used for MDDR.

Figure 34 • **Layout of VREF5**
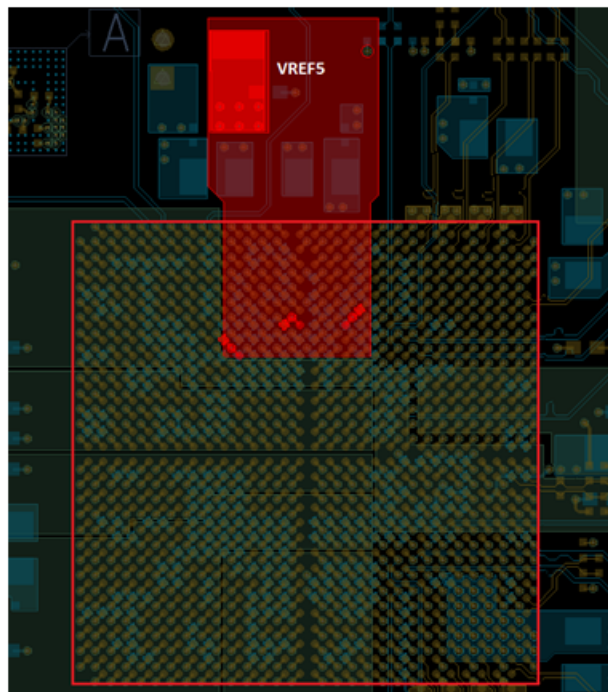
3.4.2.2 VDDIO

The shape of the plane does not have a specific requirement. The width of the plane should be sufficient to carry the required current. The following figures show the sample layout for VDDIO0 and VDDIO5 planes.

Figure 35 • **Layout of VDDIO0 Plane**
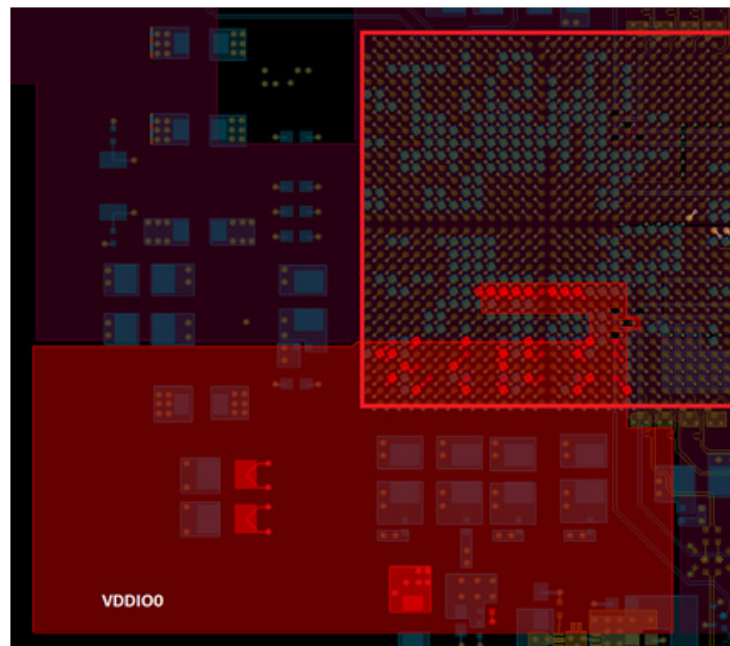
Figure 36 • **Layout of VDDIO5 Plane**
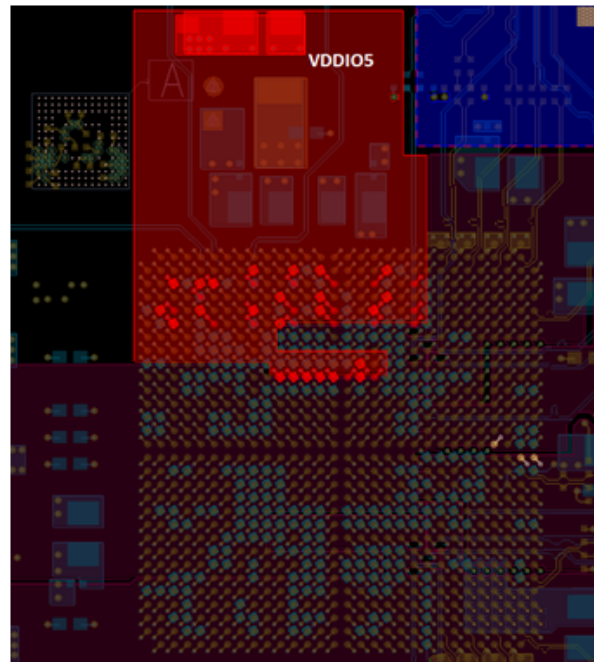
3.4.3   Simulations

The target impedance of the DDR VDDIO is calculated as 240 mΩ, based on the values (see Power Supply, page 36*)*:

- V_{SUPPLY} = 1.5V,
- I_{trans} = 250 mA
- Ripple = 5%

The impedance profile of the DDR VDDIO plane over frequency range is shown in the following figures. The impedance improves with the decoupling capacitors provided. The target impedance of 0.3 Ω has been achieved till 500 MHz.

Figure 37 • **Impedance Profile of VDDIO0 Plane Over Frequency Range**
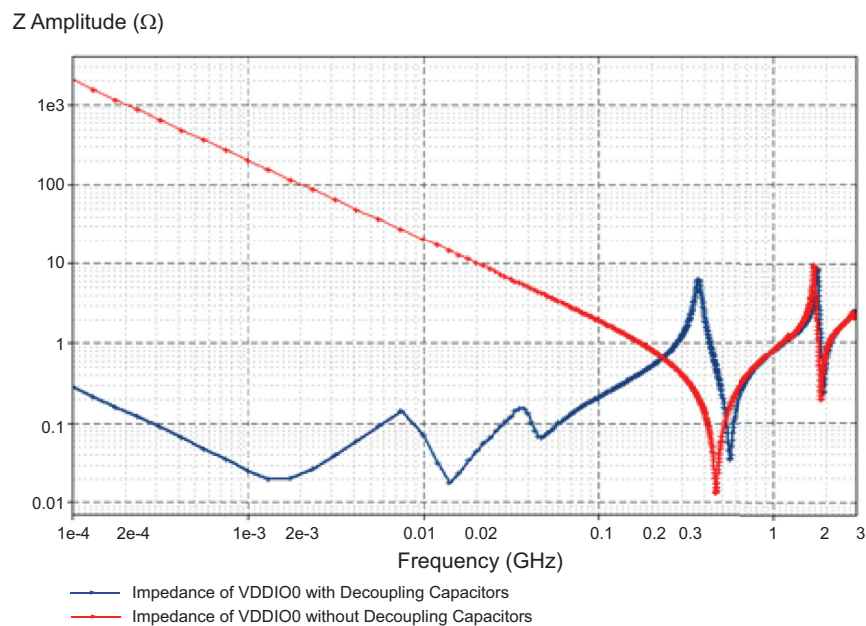
Figure 38 • **Impedance Profile of VDDIO5 Plane Over Frequency Range**
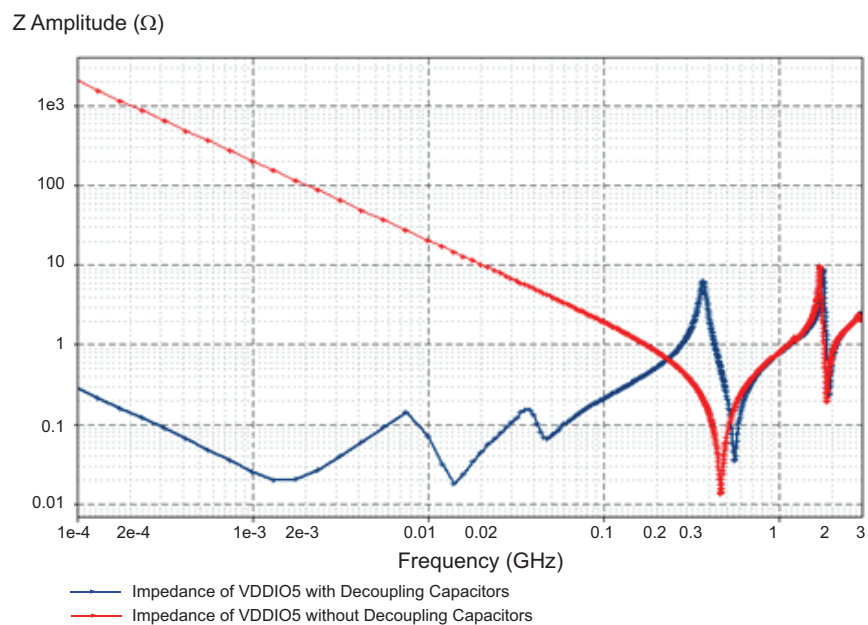
3.5 PLL

To achieve a reasonable level of long term jitter, it is vital to deliver an analog grade power supply to the PLL. An R-C or R-L-C filter is used with the C being composed of multiple devices to achieve a wide spectrum of noise absorption. Even the circuit is simple, there are specific board layout requirements. Board layout around the high-frequency capacitor and the path to the pads are critical. It is vital that the quiet ground and power are treated like analog signals. The entire VDDPLL and PLLVSSA wiring path must not be coupled with any signal aggressors – especially, any high-swing and high-slew rate signals such as TTL, CMOS, or SSTL signals used in DDR buses, and so on.

The recommended circuit for the power supply filter is shown in the following figure.

Figure 39 • **Filter Circuit for PLL**
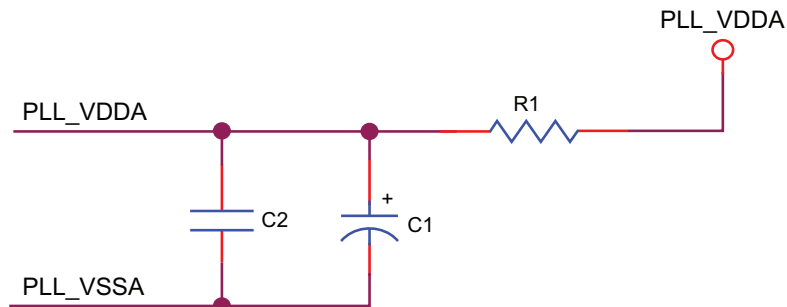
For more information about R1, C1, and C2, see Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs, page 5.

3.5.1 Component Placement

- The capacitor (C1) and series resistor (R1) should be placed near the device as close as possible to C2 device. A sample placement is shown in the following figure.
- The decoupling capacitor (C2) should be placed near the BGA via. The capacitor pad to via trace should be as small as possible. For more information about R1, C1, and C2, see Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs, page 5.

Figure 40 • **Placement of Capacitors for PLL filter Circuit**
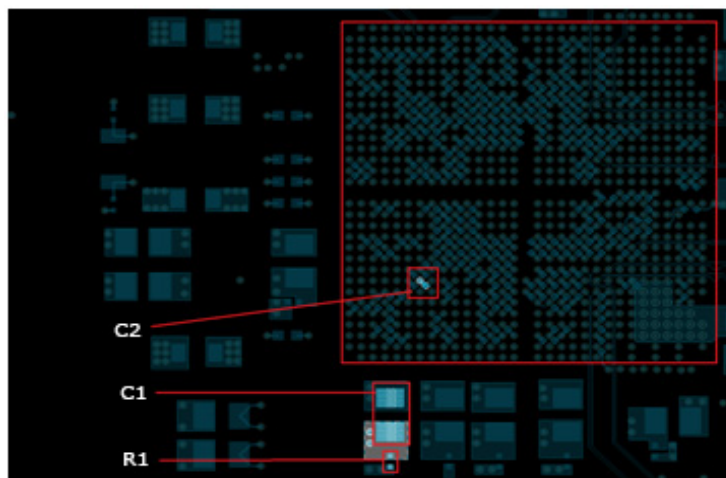
3.5.2 Plane Layout

- Plane routing for PLL0VDDA and PLL0VSSA is shown in the following figure. These are with respect to the schematic, as shown in Figure 39, page 48.
- The capacitor (22 µF) and series resistor should be placed near the device as close as possible to the 0.1 µF cap. A sample placement is shown in the following figure.

Figure 41 • **Routing for PLL Filter Circuit**
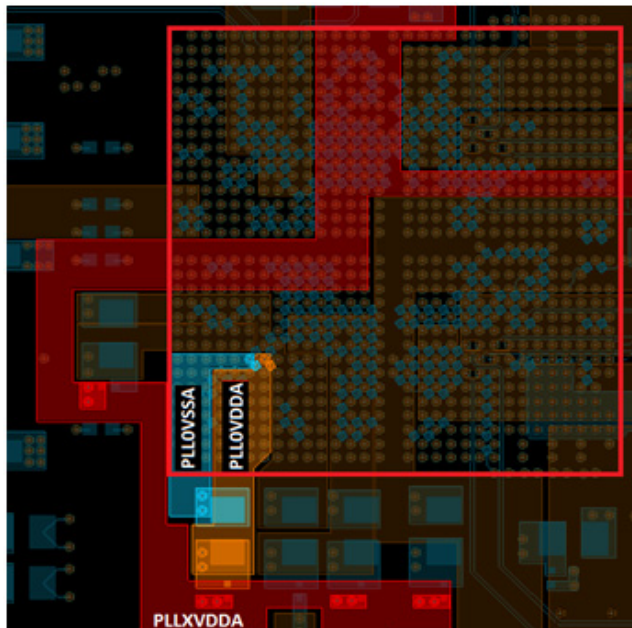
- PLL0VDDA and PLL0VSSA should not be routed with a small trace width as it increases the inductance resulting in ripples. These supply traces should be routed as plane (as shown in Figure 41, page 49), even though the current requirements are small.
- Same layout guidelines should be followed for DDR PLL power supplies. For more information about PCIe PLL guidelines, see SerDes, page 39.

3.5.3 Simulations

The target impedance of the PLL0VDDA plane is calculated as 16.5 Ω based on the values (see Power Supply, page 36):

- V_{SUPPLY} = 3.3 V
- 3.3 V, I_{trans} = 10 mA
- Ripple = 5%

The impedance of the place (Z) should be 16.5 Ω or less. For more information about ripples and its values, see *DS0128: IGLOO2 and SmartFusion2 Datasheet*. Plane impedance with and without filter circuit is shown in Figure 42, page 50.

Figure 42 • **PLL0VDDA Plane Impedance**
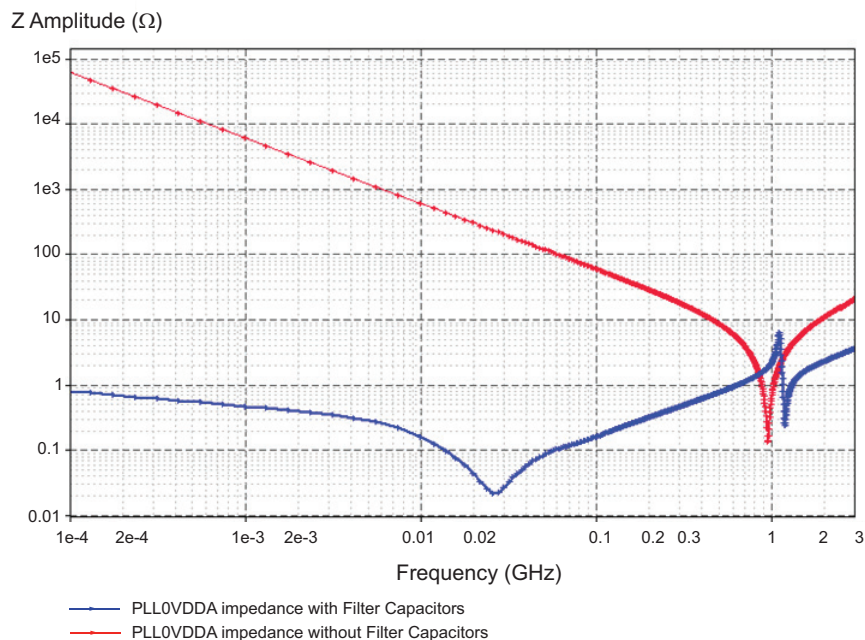
3.6 I/O Power Supply

3.6.1 Component Placement

- The bypass capacitors (47 µF and 22 µF) should be placed near, or if possible, at the edge of the device.
- All decoupling capacitors (0.1 µF and 0.01 µF) should be 0402 or of a smaller package size as they are required to be mounted under BGA package. They should be fit between the adjacent vias of BGA package pins. These decoupling capacitors are selected to have a low impedance over operating frequency and temperature range.

The capacitor pad to via trace should be as small as possible. Figure 23, page 37 shows how these capacitors are mounted. The capacitors can also be mounted directly on the pad available on the vias. The decoupling capacitors should not be shared via connections.

3.6.2 Plane Layout

The shape of the plane does not have a specific requirement. The width of the plane should be sufficient enough to carry the required current.

3.6.3 Simulations

The target impedance of the VDDIO1 plane is calculated as 330 mΩ based on the following values (see Power Supply, page 36):

- V_{SUPPLY} = 3.3 V,
- I_{trans}= 500 mA
- Ripple = 5%

The following figures show the impedance of the planes (VDDIO1 and VDDIO2). The impedance of the plane has been improved by decoupling capacitors and is kept under 0.2 Ω till 100 MHz.

Figure 43 • **Impedance Profile of VDDIO1 Plane Over Frequency Range**
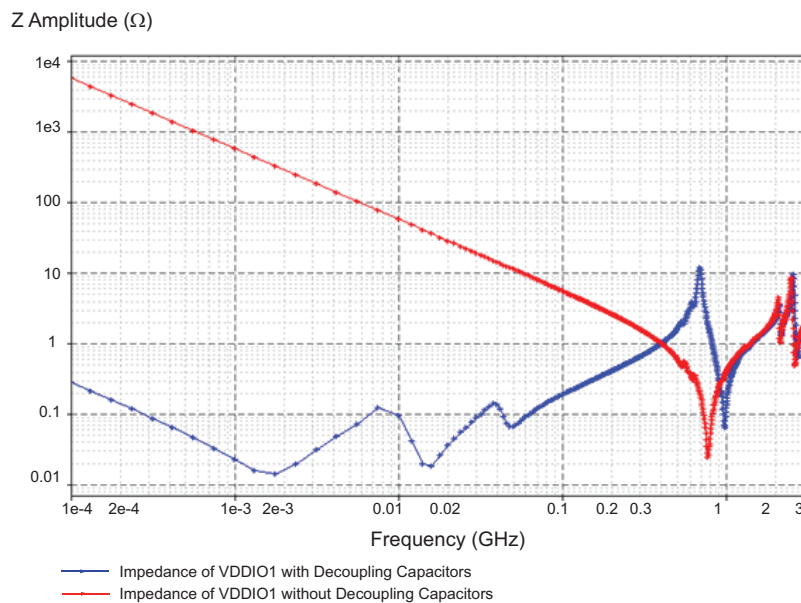
Figure 44 • **Impedance Profile of VDDIO2 Plane Over Frequency Range**
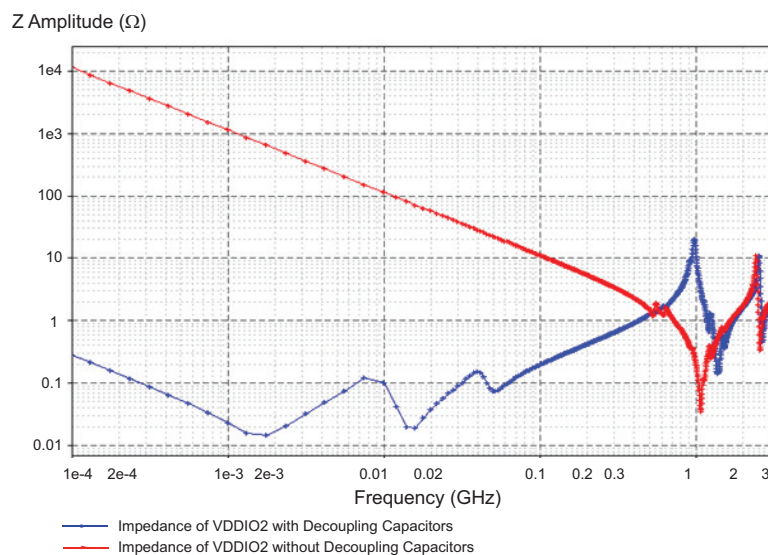
3.7 Programming Power Supply (VPP or VCCENVM)

VPP is used as an input for the internal charge pump that generates the required voltage to program flash. VCCENVM is an embedded non-volatile memory (eNVM) supply.

3.7.1 Component Placement

- The bypass capacitors (47 µF and 22 µF) should be placed near, or at the edge of the device if possible.
- All decoupling capacitors (0.1 µF and 0.01 µF) should be 0402 or of a smaller package size as they are required to be mounted on the reverse side of the board. They should be fit between the adjacent vias of BGA package pins. These decoupling capacitors are carefully selected to have low impedance over the operating frequency and temperature range.
- The capacitor pad to via trace should be as small as possible. Figure 23, page 37 shows how these capacitors are mounted. The capacitor can also be mounted directly on the pad available on the vias.

3.7.2 Plane Layout

The shape of the plane does not have a specific requirement. The width of the plane should be sufficient enough to carry the required current.

3.7.3 Simulations

The target impedance of the VPP is calculated as 3.3 Ω, based on the values (see Power Supply, page 36):

- V_{SUPPLY} = 3.3 V
- I_{trans} = 50 mA
- Ripple = 5%

The simulation result (as shown in the following figure) shows that it meets the required impedance levels.

Figure 45 • **Impedance Profile of VPP Plane Over Frequency Range**
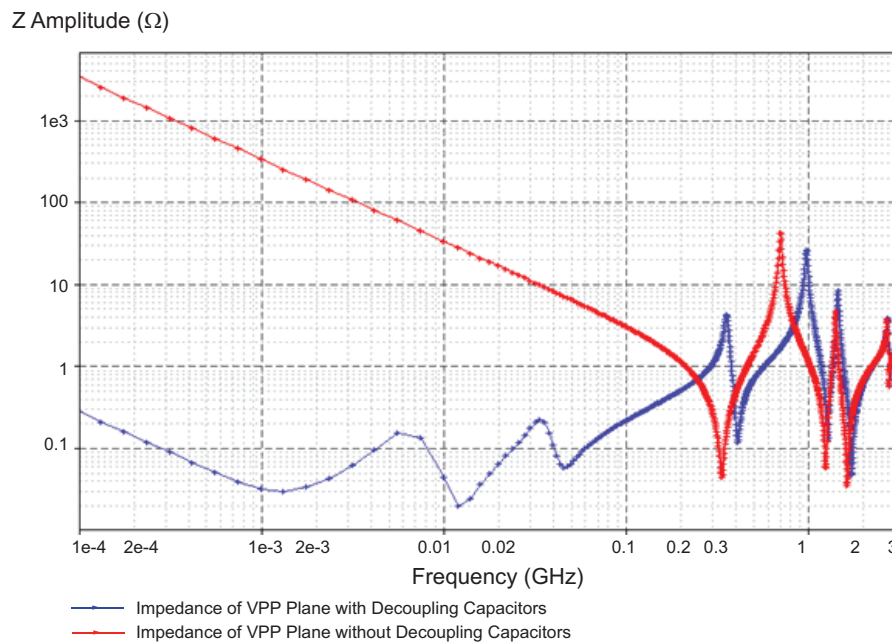
3.8 High-Speed Serial Link (SerDes)

3.8.1 Layout Considerations

3.8.1.1 Differential Traces

A well designed differential trace not must have the following qualities:

- Mismatch in impedance
- Insertion loss and return loss
- Skew within the differential traces

The following points need to be considered while routing the high-speed differential traces to meet the above qualities.

- The traces should be routed with tight length matching (skew) within the differential traces. Asymmetry in length causes conversion of differential signals in Common mode signals. The differential pair should be routed such that the skew within differential pairs is less than 5 mils. The length match should be used by matching techniques, as shown in the following figure.

Figure 46 • **Skew Matching**
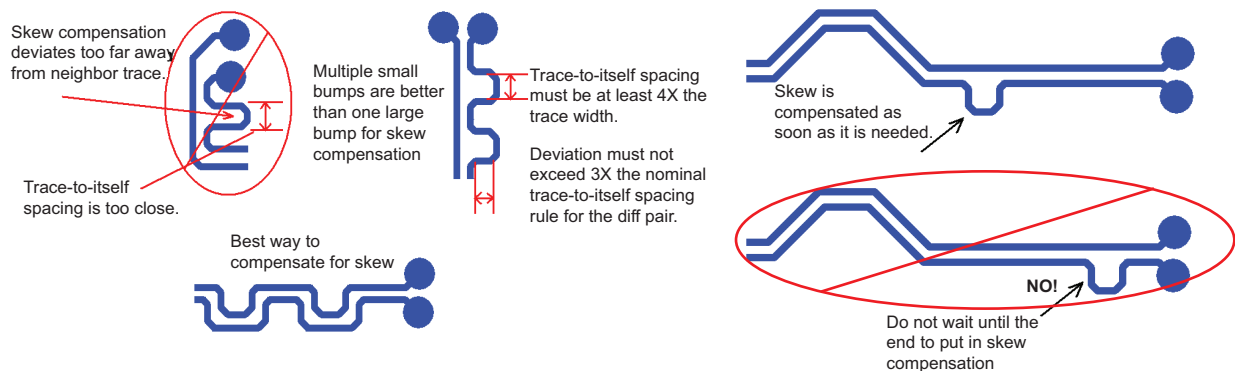
- The length of differential lanes should be matched within the TX and RX group.

This is applicable only to specific protocols like XAUI and so on.

- Route differential pairs symmetrically into and out of structures, as shown in the following figure.

Figure 47 • **Example of Asymmetric and Symmetric Differential Pairs Structure**
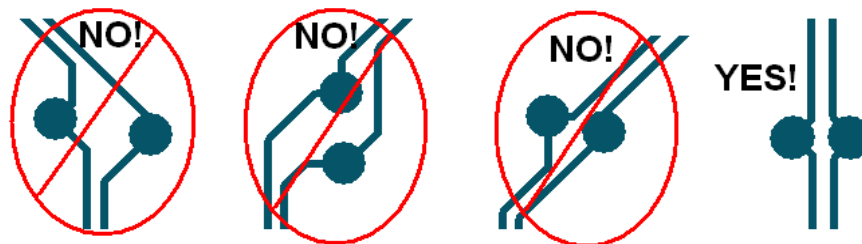
- Skin effect dominates as the speed increases. To reduce the skin effect, width of the trace has to be increased (loosely coupled differential traces). Increase in trace width causes increase in dielectric losses. To reduce the dielectric loss, use low Dissipation Factor (Df) PCB materials like Nelco 4000-13. This is approximately double the cost of FR4 PCB material, but can provide increased eye-opening performance when longer trace interconnections are required. Remember to maintain 100 Ω differential impedance. Need to consider this if the data rate is 5 Gbps and above.
- Far end cross talk is eliminated by using stripline routing. However, routing in stripline causes more dielectric loss and more variation in the impedance. Cross talk affects only when there is a high density routing. It is better to route as microstrip, if there is enough space between differential pairs (> 4 times the width of the conductor) to reduce dielectric loss. Simulations are recommended to see the best possible routing.

- 2116 or 2113 glass weaving PCB materials should be used to avoid the variations in the impedances. Zig-zag routing must be used instead of straight line routing to avoid glass weaving effect on impedance variations, as shown in the following figure. Instruct the fabrication vendor to use these PCB materials before manufacturing.

Figure 48 • **Zig-Zag Routing**
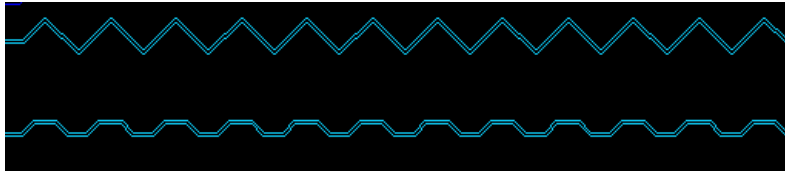
- These traces should be kept away from the aggressive nets or clock traces. For example, on M2S050T devices, the SerDes and DDR traces should not be adjacent to each other.
- Separation between the coupled differential trace pairs should be 1x. Spacing between channels should be > 3x separation. Trace stubs should be avoided. The stub length should not exceed 40 mils for 5 Gbps data rate.
- The trace lengths should be kept as small as possible.
- It is better to use low roughness, that is, smooth copper. As the speed increases insertion loss due to the copper, then roughness increases. The attenuation due to skin effect is increased proportional to the square root of frequency. The roughness courses this loss proportional to frequency. Microsemi recommends instructing the PCB fabrication house to use smooth copper, if the frequency exceeds 2 Gbps.
- Split reference planes should be avoided. Ground planes must be used for reference for all the SerDes lanes.

Figure 49 • **Ground Planes for Reference**
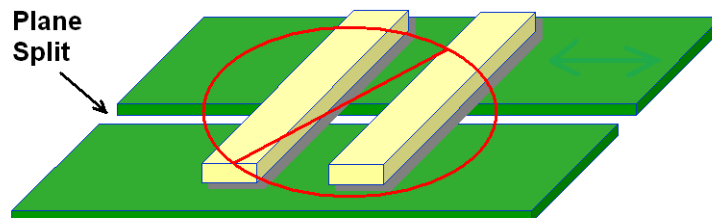
3.8.2   Via

- The target impedance of vias are designed by adjusting the pad clearance (anti-pad size). Field solver should be used to optimize the via according to the stack-up.

Figure 50 • **Via Illustration[1]**
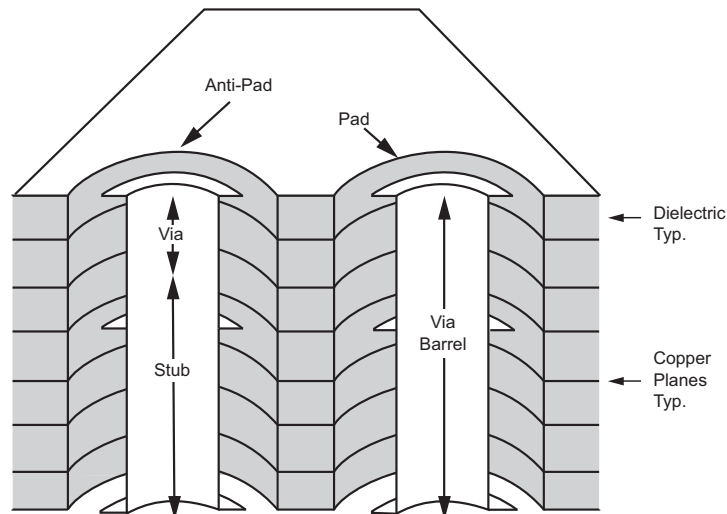
- Number of vias on different traces should be avoided or minimized. SerDes signals should be routed completely on a single layer with the exception of via transitions from component layer to the routing layer (3-via maximum).
- The length of via stub should be minimized by back drilling the vias, or by routing the signals from near top to near bottom layer, or else blind or buried vias can be used. Using blind-vias or back drilling is a good method to eliminate via stubs and reduce reflections.
- The stub length should be kept below 100 mils, if the data rate is 2.5 Gbps and 40 mils for 5 Gbps.
- If feasible, non-functional pads should be removed. Non-functional pads on via are the pads where no trace is connected. This reduces the via capacitance and stub effect of pads.

Figure 51 • **Non-Functional Pads of Via**
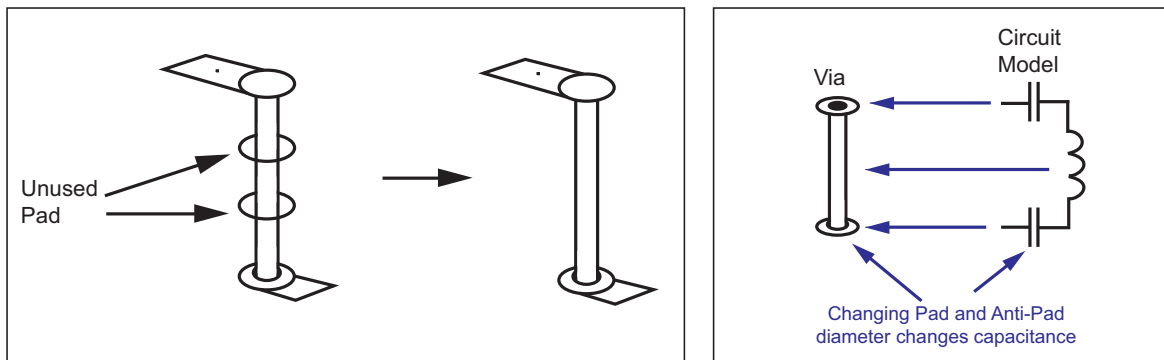
- The tight via to via pitch is practical to reduce the cross talk effect, as shown in the following figure.

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1. Simonovich, E. Bogatin, Y. Cao, Method of Modeling Differential Vias, White Paper, Jan 2011

Figure 52 • **Via-to-Via Pitch**
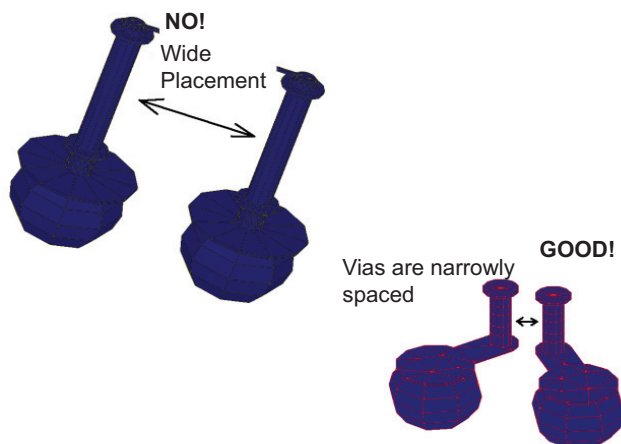
- Symmetrical ground vias (return vias) should be used to reduce discontinuity for Common mode signal component, as shown in the following figure. Common mode of part of the signal requires continuous return path RX to TX and GND. Return vias help in maintaining the continuity.

Figure 53 • **GND Via or Return Via**
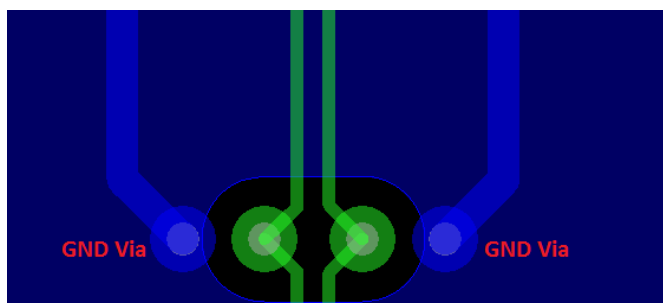
3.8.3   DC Blocking Capacitors

The plane underneath the pads of DC blocking capacitors should be removed (as shown in the following figure) to match the impedance of the pad to 50 Ω. This has to be done only on immediate reference plane, not on all planes.

Figure 54 • **Capacitor Pad Reference Plane**
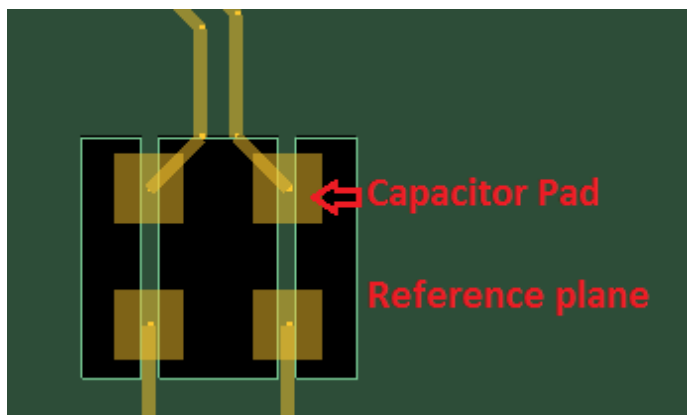
3.8.4   Connectors

The plane keep-out clearance should be optimized from the pin to get 50 Ω impedance when through hole SMAs or connectors are used. This reduces the reflection loss.

3.9 Considerations for Simulation

Microsemi recommends simulations to confirm the quality of the received signal. The following files are required to simulate the serial channel:

- IBIS: AMI files for SmartFusion2/IGLOO2 and any other devices that are connected to SerDes
- Package: files (optional). S-parameter of package improves the accuracy instead of using package parameters in the IBIS file
- Board traces model file including via models
- Connector models, if required

The following steps describe how to run the serial channel simulations:

3.9.1 Step 1: Gathering the Required Files

3.9.1.1 IBIS-AMI Models

The IBIS-AMI models of SmartFusion2/IGLOO2 and the IBIS-AMI models of IC that will be interfaced with SmartFusion2/IGLOO2 can be downloaded from the Microsemi website:

- *www.microsemi.com/soc/download/ibis/SmartFusion2.aspx*
- *www.microsemi.com/soc/download/ibis/IGLOO2.aspx*

3.9.1.2 Package Models

The package models (S-parameter models) of SmartFusion2/IGLOO2 can be downloaded from the Microsemi website:

- *www.microsemi.com/soc/download/ibis/SmartFusion2.aspx*
- *www.microsemi.com/soc/download/ibis/IGLOO2.aspx*

Accuracy of simulation improves with S-parameter model of package file instead of using package models available in the IBIS file. If S-parameter models for package are used, the package details in IBIS should be commented.

3.9.1.3 PCB Trace Models

The PCB file should be converted into a compatible format of simulator software. For example, the .HYP file format of PCB is required to be simulated in Hyperlynx, and `.SPD` file format of PCB is required to be simulated in Sigrity. Once the PCB file is loaded in the simulation tool, the stack-up that matches the PCB stack-up should be checked. The dielectric constant, Dk and dissipation factor, and Df of PCB material should be defined. The tool extracts incorrect models, if the above points are not defined properly.

The SerDes traces should be identified and ports on both the sides of the traces need to be assigned. The S-parameter models of traces should be extracted. The following tools can be used to extract S-parameter models of PCB traces:

- Agilents ADS
- Mentors Hyperlynx
- Sigritys PowerSI

It is not mandatory to use the above mentioned tools, many other tools are available in the market which can extract S-parameter models.

3.9.2 Step 2: Creating Simulation Topology

The typical topology, as shown in the following figure, shows the blocks involved in the serial link analysis. These blocks are taken from the Sigrity tool. All simulations related to SerDes are done on Sigritys SystemSI tool in this document. Topology is same in any tool. This can be done in any tool that supports the serial link analysis.

The typical topology for SLA simulation is done as following:

- AMI: AMI models of TX and RX
- TX_PRIMARY: IBIS model of TX I/O
- Pkg1 and Pkg2: Package model of TX and RX I/O

- PCB: S-parameter model of SmartFusion2 Development Kit SerDes Traces
- RX_PRIMARY: S-parameter model of either the connector or the IBIS model of the receiver IC device

Once all the model files are imported into the topology, the default configuration in the AMI model should be left to calculate the appropriate coefficients by the tool and then to run the simulations.

*Figure 55 •* **Typical Topology for SLA Simulation**
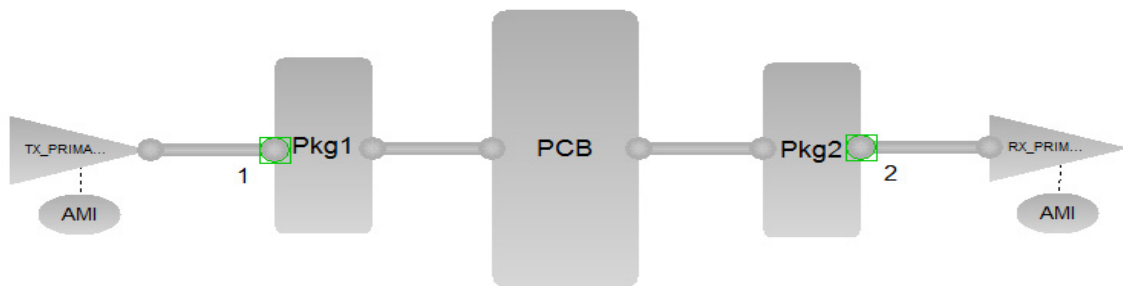
3.9.3   Step 3: Configuration of AMI Model

The following configurations on the AMI model are required before simulating the serial channel:

3.9.3.1   TX AMI Model

The following figure shows the block diagram of the 3-tap Feed Forward equalizer structure for TX. The output of the TX is given by the transfer function $t_{n-1} + t_n Z^{-1} + t_{n+1} Z^{-2}$. The TX output depends on the value of tap coefficients.

Figure 56 • **Block Diagram of the 3-tap Feed Forward Equalizer**
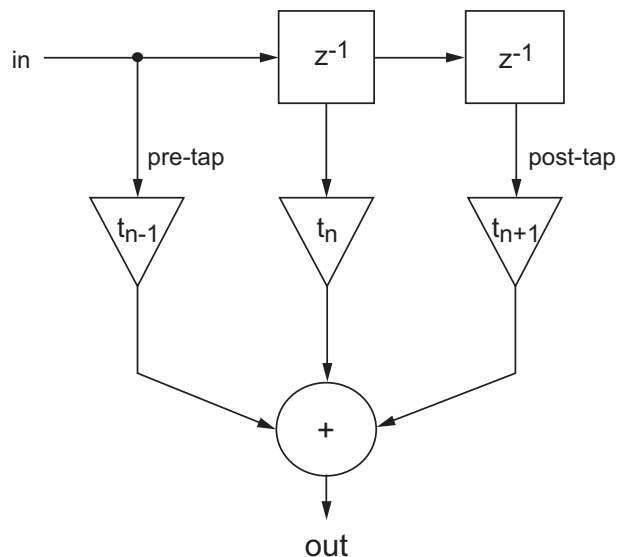
The following are the details of coefficients:

- **t0:** Pre-cursor tap setting. The range is from -0.4 to -0.01, default value is -0.01.
- **t1:** Main tap. The range is from 0.1 to 1, default value is 1.

- **t2:** Post-cursor tap. The range is from -0.5 to -0.01, default value is -0.01.
- **TapsFromFile:** Explicit feed forward equalizer (FFE) coefficients can be set through this file. If a file is used, it overrides the manual tap settings and automatic generation.
- **TapsToFile:** Output FFE tap coefficients to this file when automatic generation coefficients is used.

3.9.3.2 RX AMI Model

SerDes supports the programmable single pole continuous time linear equalization (CTLE) at the receiver. The linear equalization comprises of amplifying higher frequency components that have been more severely attenuated by the Interconnect, or attenuating the lower frequency components to a greater degree than the higher frequency components.

The low-frequency attenuation level and the low-frequency flat-band bandwidth are programmable, as shown in the following figure.

Figure 57 • **Continuous Time Linear Equalization Response**
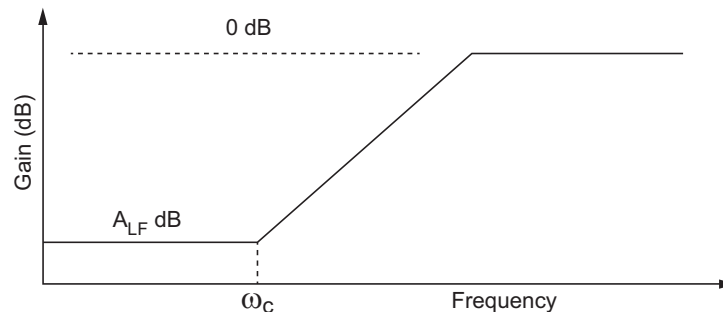
Both ALF and ω_c (f0) can be set to maximize the signal quality of the receiver for achieving the highest possible bit error rate (BER).

- Alf: Low-frequency dB loss of the filter. The range is from 0 to 50, default value is 6.
- f0: High pass cut-off frequency. The range is from $1e^6$ to $5e^{10}$, default value is $1e^9$.

3.9.4 Step 4: Results

Qualification of simulation results is done based on the eye-height, eye-width, and BER curves. Check the eye-height and eye-width at target BER of $10e^{-12}$. These results are found in the report generated by the simulation tool. For example, the Sigrity tool gives the following information at RX:

At BER of $10e^{-12}$, running at 5 Gbps bit rate

- The eye-width is 0.68 UI (Unit Interval)
- The eye-height is 213 mV

This simulation is on the SmartFusion2 Development Kit using the Sigrity tool and the waveforms are shown in the following figure. The simulation result shows that it meets the PCIe 2.0 requirements.

Figure 58 • **Expected Results from Simulations (Eye Diagram, Eye Contour, and Bath Tub Curve)**
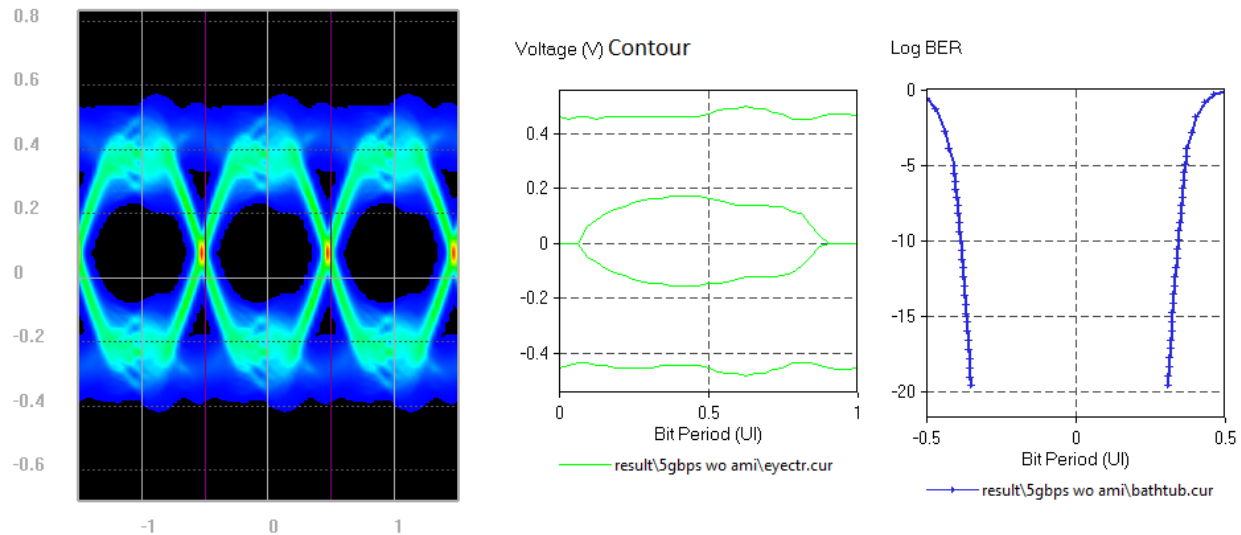
The following table lists the specifications of the received signal for PCIe.

Table 19 • **Specifications of the Received Signal for PCIe**

Bit Rate	Min Height of the Eye at RX	Min Width of the Eye at RX
2.5 Gbps	175 mV	0.6 UI
5 Gbps	120 mV	0.6 UI

For more information about PCIe 2.0 base specification, see
www.pcisig.com/members/downloads/specifications/pciexpress/PCI_Express_Base_r2_1_04Mar09.pdf

To know whether or not the system is meeting the requirements, the eye mask can be imported. Specifications of eye mask depend on the application the system is using. For example, PCIe 1.0, PCIe 2.0, XAUI, and SGMII. A typical eye mask for PCIe 2.0 is shown in the following figure.

Figure 59 • **Eye Mask for PCIe 2.0**
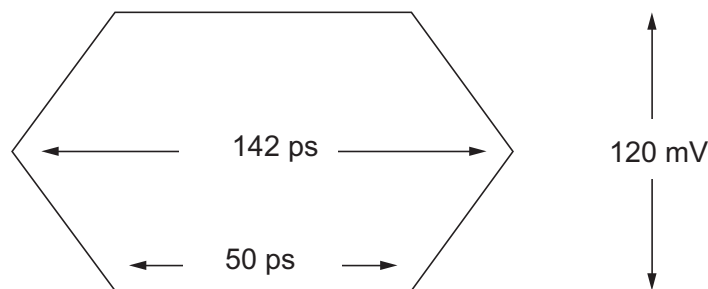
For more information about IBIS-AMI model, see *AC292- IBIS Models- Background and Usage Application Note*.

3.10 DDR3 Layout Guidelines

3.10.1 Placement

It is required to ensure that the placement for the DDR3 memories looks like *L* (shape), where, memories are at the bottom of the *L* and controllers are on the top of the *L*. This gives enough space to route the DQ signals with less number of layers. This is not mandatory to follow the suggested placement. However, the placement also depends on the board constraints. The maximum trace length of any signal in the placement should not be more than 7 inches.

Figure 60 • **DDR3 Memories**
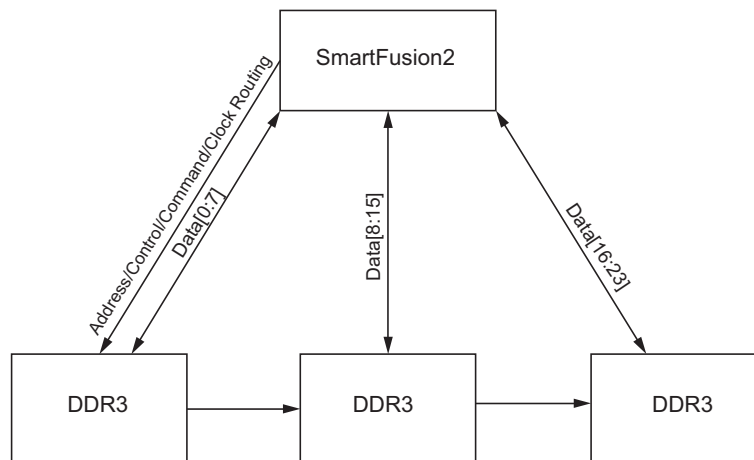
The termination resistors are not required for the DQ and DQS signals as these signals have on chip ODTs. The termination resistors are placed at the end of the address, command, control, and clock signals as these signals use fly-by topology. VTT plane/island is thick enough to handle the current required by termination resistors; at least 150 mil trace is required. The sense pin of VTT regulator should be connected at the center of the VTT island.

3.10.2 Routing

Reliability of DDR interface depends on the quality of the layout. There are many layout guidelines available from memory vendors. The following recommendations can also be used for routing the DDR3 signals. The following DDR3 signals are grouped:

- Data
- Address/Command
- Control
- Clocks
- Power

The following table lists the signals that come under a particular group:

Table 20 • **Grouping of DDR3 Signals**

Group	Signals
Data	DQ[0:7], DQ[8:15], DQ[16:23], DQ[24:31] and DQS[0:3], DM[0:3]
Address/Command	A[0:15], BA[0:2], RAS#, CAS#, and WE#
Control	CS#, CKE, and ODT
Clock	CK and CK#

3.10.2.1 Data Group Signal Routing

- The data signals should not be over the split planes.
- The reference plane for data signals should be GND plane and should be contiguous between memory and SmartFusion2/IGLOO2.
- Traces should not be routed at the edge of the reference plane and over via anti pads.
- When routing the data signals, the longest signals should be routed first, this allows to adjust the length for the short length signals, when routing data signals.
- Serpentine routing should be used to adjust the data group signals to meet this requirement.
- The DQS signal should be routed along with associated data byte lane on the same critical layer with the same via count. Using more than three vias in the connection between the FPGA controller and memory device should be avoided.
- The impedance for the data traces depends on the stack-up and the trace width. There are options to select the impedance based on the stack-up and trace width.
  - 40 Ω impedance, which requires wide traces (~7 to 8 mils). This gives the less cross talk and less spacing between the traces (~2x). Spacing between non-DDR signals and DDR signals should be ~4x.
  - 50 Ω impedance, which requires smaller trace width (~4 to 6mils). This requires more spacing between the traces (~3x). Spacing between non DDR signals and DDR signals should be ~4x.
- All data lanes should be matched to within 0.5 inch.
- Within the data lane, each trace should be matched to within ±10mils of its respective data strobe
- The DQS and DQS# need to be matched within +/- 5mils.
- Differential impedance should be between 75 to 100 Ω.
- Differential traces adjacent to noisy signals or clock chips should be avoided.
- Spacing between differential lines should be 5 to 8 mils.

3.10.2.2 Address, Control, Command, and Clock Routing

- These signals should be routed in the fly-by topology and terminated with appropriate termination resistor at the end of the signals. The resistor termination should not have a stub longer than 600 mil.
- The impedance for the trace depends on the stack-up and trace width. There are options to select the impedance based on the stack-up and trace width:
  - 40 Ω impedance, which requires wide traces (~7 to 8 mils). This gives the less cross talk and less spacing between the traces (~2x). Spacing between non DDR signals and DDR signals should be ~4x.
  - 50 Ω impedance, which requires smaller trace width (~4 to 6mils). This requires more spacing between the traces (~3x). Spacing between non DDR signals and DDR signals should be ~4w to avoid crosstalk issues.
  - Address and control signals can be referenced to a power plane if a ground plane is not available. The power plane should be related to the memory interface. However, a ground reference is preferred. Address and control signals should be kept on a different routing layer from DQ, DQS, and DM to isolate crosstalk between the signals.

3.10.2.3 Clock

- Clock signals are routed differentially, and the length matches between traces should be +/- 5 mils.
- It should be referenced to ground plane.
- The space between clock and other signals should be 25 mils.
- One clock signal is routed per rank of the DIMM, that is, one clock for single-ranked DIMM, two clock signals for the dual ranked DIMM. For non-DIMM systems, the differential terminations used by the CK/CK# pair must be located as close as possible to the memory.
- If more than one CS is used, the same clock to DQS skew should be applied to all CS.
- Address/control signals and the associated CK and CK# differential FPGA clock should be routed with trace matching ±100 mil.

**Note:** The following guidelines are applicable for DDR2, DDR3, and LPDDR:

- Short the MDDR_TMATCH_0_IN and MDDR_TMATCH_0_OUT pins under BGA using short trace.
- Short the MDDR_TMATCH_1_IN and MDDR_TMATCH_1_OUT pins under BGA using short trace.
- Short the MDDR_TMATCH_ECC_IN and MDDR_TMATCH_ECC_OUT pins under BGA using short trace.
- Short the FDDR_TMATCH_0_IN and FDDR_TMATCH_0_OUT pins under BGA using short trace.
- Short the FDDR_TMATCH_1_IN and FDDR_TMATCH_1_OUT pins under BGA using short trace.
- Short the FDDR_TMATCH_ECC_IN and FDDR_TMATCH_ECC_OUT pins under BGA using short trace.

For more information about DDR2 and LPDDR memory layout guidelines, see the *Micron Memory Layout Guidelines* in the following documents, available on the *Micron website*:

- *TN-47-20: Hardware Tips for Point-to-Point System Design from Micron*
- *TN-46-19: Hardware Tips for Point-to-Point System Design from Micron*

The following figure shows an example layout.

Figure 61 • **TMATCH Signals (Example Layout)**
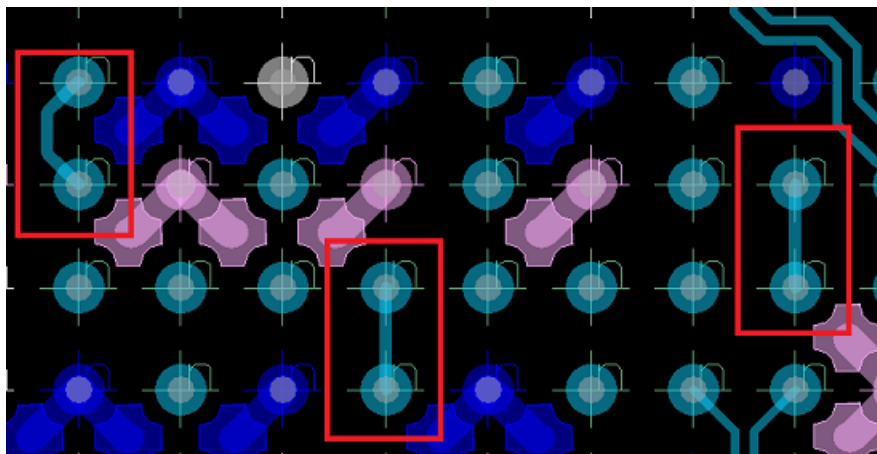
3.10.3 Simulation Considerations

Simulations ensure that the DDR and controller meet timing requirements and also ensure that the quality of the received waveform in terms of undershoot, overshoot and jitter and so on.

The following files are required for the DDR3 simulation:

- IBIS file of SmartFusion2/IGLOO2
- IBIS file of DDR3 memory
- PCB files of SmartFusion2/IGLOO2 board and DIMM, if used
- Connector models if DIMM is used

The following sections describe how to run the serial channel simulations.

3.10.3.1 Step 1: Gathering the Required Files

3.10.3.1.1 IBIS Models

To download the IBIS models of SmartFusion2/IGLOO2 and the IBIS-AMI models of DDR3 memory which is going to interface with SmartFusion2/IGLOO2, see the following web pages on the Microsemi website:

- *www.microsemi.com/soc/download/ibis/SmartFusion2.aspx*
- *www.microsemi.com/soc/download/ibis/IGLOO2.aspx*

3.10.3.1.2 PCB Trace Models

The PCB file needs to be converted into a compatible format of simulator software. For example, `.HYP` file format of PCB is required to simulate in Hyperlynx and SPD file format of PCB is required to simulate in Sigrity. Once the PCB file is loaded in the simulation tool, check the stack-up that matches the PCB stack-up and define the dielectric constant, Dk and dissipation factor, and Df of PCB material. The tool extracts wrong models, if the above points not defined properly. Some tools run the simulations on PCB file itself like Hyperlynx and some tools need S-parameter files of DDR3 traces to continue the simulations. To extract S-parameter models of PCB traces assign the ports on both sides of the traces and extract the S-parameter models of traces.

The following tools can be used to extract S-parameter models of PCB traces:

- Agilents ADS
- Mentors Hyperlynx
- Sigritys PowerSI

It is not mandatory to use above tools, there are many tools available in the market which can extract S-parameter models.

3.10.3.2 Step 2: Creating Simulation Topology

These blocks are taken from the Sigrity tool. Topology is the same in any tools. The simulation can be done in any tool, which supports DDR3 simulation.

The following figure shows the typical topology blocks involved in the DDR3 simulations.

- SmartFusion2/IGLOO2 IBIS: IBIS model of SmartFusion2/IGLOO2
- PCB: S-parameter model of PCB file, connector models and DIMM PCB models
- Connector model: Spice models of connector
- Memory IBIS: IBIS models of DDR3 memory

Figure 62 • **DDR3 Simulation Topology**
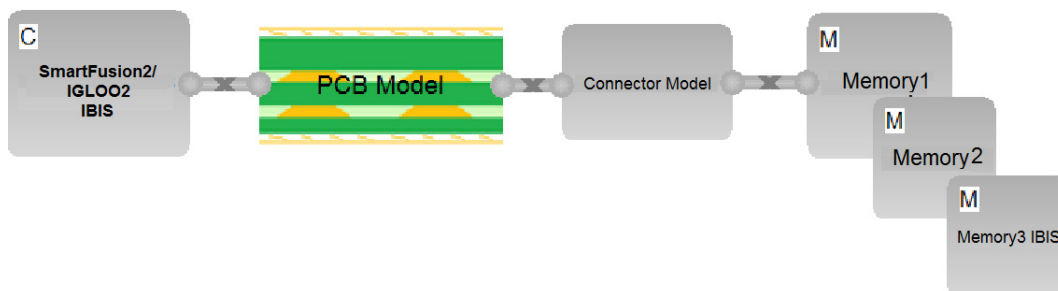
3.10.3.3 Step 3: Simulation Setup

- Assign IBIS models to SmartFusion2/IGLOO2 and memory
- Assign connector model if used
- Assign the models for on board termination resistors
- Identify the DDR3 nets and classify according to data, control and address bus
- Keep the appropriate ODT for SF2 and memory.
- Keep the 40 to 60 Ω ODT for data and 80 to 120 Ω for DQS
- Set the maximum frequency at which the system will operate. For SF2 its 333 MHz

3.10.3.4 Step 4: Results

Observe the following results:

- Setup and hold time between data signals and the respective DQS over all corners.
- Setup and hold time between Control/Command/Address signals and the clock over all corners.
- Overshoot and undershoot of all signals with respect to JEDEC specifications over all corners, and also DC threshold multi crossing that is due to the excessive ringing.

The simulation tool generates the report where all the details are available. For example, Hyperlynx generates the set of excel sheets which contain all setup and hold margin, overshoot, and undershoot information for all corners. It also generates driver and receiver waveforms for all the nets.

The following figure shows the file list where all the information regarding the simulation are stored.

Figure 63 • **List of Reports Generated by Hyperlynx**

Name	Date modified	Type	Size
DDR_report_address_allcases_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	132 KB
DDR_report_address_violations_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	11 KB
DDR_report_address_worstcases_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	11 KB
DDR_report_data_allcases_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	104 KB
DDR_report_data_violations_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	6 KB
DDR_report_data_worstcases_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	11 KB
DDR_report_SI_measurements_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	11 KB
DDR_report_skew_allcases_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	51 KB
DDR_report_skew_violations_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	6 KB
DDR_report_skew_worstcases_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	11 KB

The reports give setup and hold time for each net and also signal integrity details where overshoot and undershoots are mentioned. The following figure shows the example of report for DQ0 net. It also shows that the DQ0 has enough setup and holds time margins.

Figure 64 • **Setup and Time Margins of DQ0**

	A	O	U
1	Net Name	Setup Time Margin, tDS(margin) = tDS(min) - tDS(req), [ps]	Hold Time Margin, tDH(margin) = tDH(min) - tDH(req), [ps]
2	DDR2_DQ0	N/A	333.3
3	DDR2_DQ0	267.6	N/A
4	DDR2_DQ0	N/A	316.6

If any of the net is violating the setup and holding time margins, the length of the net should be changed accordingly. If there is any high peak overshoot or undershoot, it might be because of the high value termination resistor. It is required to adjust the value of ODT and re-iterate the simulation.

Figure 65, page 66 shows how to look at setup and hold time margins for DQ and DQS signals. Same is applicable to the margin between the Command/Control/Address and CLK signals.

Figure 65 • **Setup and Time Margins for DQ and DQS Signals**
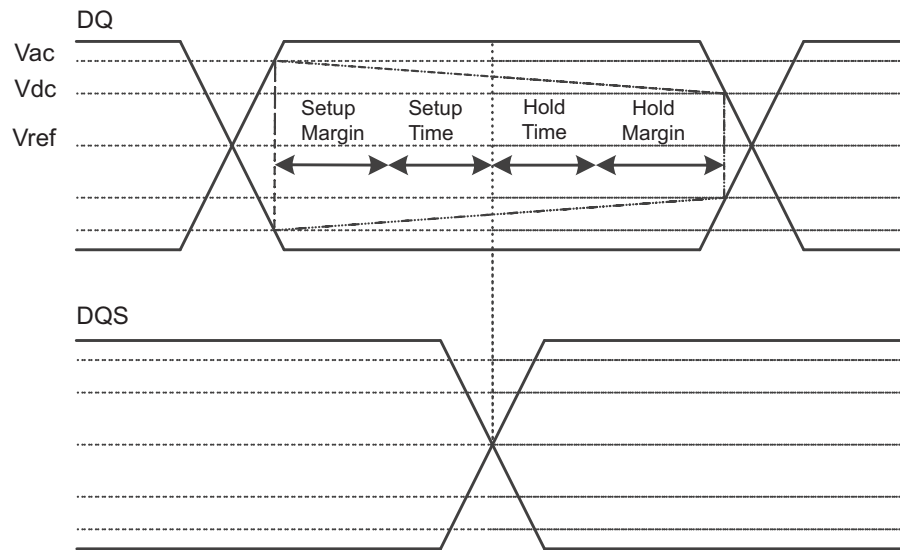
3.11 References

- Power Distribution Network (PDN) by Eric Bogatin
- Sigrity PowerSI Tutorial

4 Creating Schematic Symbols Using Cadence OrCAD Capture CIS for SmartFusion2 and IGLOO2 Designs

Creating symbols manually for application can be a time consuming task and is error prone. Cadence OrCAD Capture is a popular schematic design entry tool for system-level design.

This application note describes the recommended procedure to create schematic symbols. The schematic symbols can be created using two methods:

- Using the Microsemi published pin assignment tables (PAT) in spreadsheet format. Pin Information is imported into OrCAD Capture CIS tool. This is a two step process as explained in Creating Schematic Symbols using Pin Assignment Tables (PAT), page 67. Use this method for creating schematic symbols using Microsemi defined pins.
- Using the data export feature of Libero SoC software. Pin information can be exported to a spreadsheet and then use OrCAD Design Capture CIS tool to create symbols. This is a three step process as explained in Creating Schematic Symbols with User Defined Pin Names, page 74. Use this method for creating symbols using user defined pins for the fabric I/Os.

4.1 Creating Schematic Symbols using Pin Assignment Tables (PAT)

4.1.1 Preparing the PAT Layout File for Import into OrCAD Capture

1. Download the PAT files from the following path in the Microsemi website under Datasheets section:
   - *www.microsemi.com/products/fpga-soc/soc-fpga/smartfusion2#documents*
   - *www.microsemi.com/products/fpga-soc/fpga/igloo2-fpga#documents*
2. Open the `*Pin_Assignment_Table_Public.xlsx` file.

Figure 66 • **Example PAT Spreadsheet - Initial view**

| PKG.PIN | M2S050TS/M2S050T-FG896 Pin Name | Bank No | Direction | Total | | | Pin Parasitics (Applicable to Usable DIGITAL I/Os ONLY) | | | | | | Unused Condition |
				MSIOD (2.5V max)	MSIO (3.3V max)	DDRIO (2.5V max)	Net Length	SelfR(Ohm)	SelfL(nH)	SelfC(pF)	SelfG(uMho)	Delay(pS)	
A10	DDRIO90PB0/MDDR_DQS_ECC	0	I/O	N	N	Y	14.7524	0.69979	9.75479	1.7336	0	130.042	Libero Defined* DNC
A11	DDRIO88PB0/MDDR_DQ_ECC3	0	I/O	N	N	Y	14.1504	0.712199	9.25784	1.62799	0	122.767	Libero Defined* DNC
A12	DDRIO86PB0/MDDR_DQ0	0	I/O	N	N	Y	13.4834	0.669683	9.24447	1.57524	0	120.674	Libero Defined* DNC
A13	DDRIO84PB0/MDDR_DQS0	0	I/O	N	N	Y	13.4861	0.673458	8.70731	1.57518	0	117.114	Libero Defined* DNC
A14	DDRIO83NB0/MDDR_DQ4	0	I/O	N	N	Y	13.2354	0.675006	8.99641	1.52207	0	117.018	Libero Defined* DNC
A15	DDRIO80PB0/MDDR_DQ8	0	I/O	N	N	Y	13.3326	0.66684	9.24054	1.54588	0	119.519	Libero Defined* DNC
A16	DDRIO78PB0/GB8/CCC_NE0_CLKI3/MD	0	I/O	N	N	Y	13.4351	0.694428	8.85242	1.57645	0	118.133	Libero Defined* DNC
A17	DDRIO76PB0/GB12/CCC_NE1_CLKI12/M	0	I/O	N	N	Y	13.3008	0.664554	9.24915	1.55802	0	120.043	Libero Defined* DNC
A18	DDRIO74PB0/MDDR_DQ16	0	I/O	N	N	Y	13.292	0.675689	8.72718	1.54978	0	116.298	Libero Defined* DNC
A19	DDRIO72PB0/MDDR_DQS2	0	I/O	N	N	Y	14.1135	0.678681	9.28264	1.62298	0	122.742	Libero Defined* DNC
A2	SERDES_1_TXD0_N		O	N	N	N							DNC
A20	DDRIO71NB0/MDDR_DQ20	0	I/O	N	N	Y	14.1485	0.684028	9.43141	1.64465	0	124.545	Libero Defined* DNC
A21	DDRIO68PB0/MDDR_DQ24	0	I/O	N	N	Y	14.677	0.725941	9.61066	1.69539	0	127.647	Libero Defined* DNC
A22	DDRIO66NB0/MDDR_DQS3_N	0	I/O	N	N	Y	15.0811	0.702886	9.71092	1.74809	0	130.29	Libero Defined* DNC
A23	DDRIO64PB0/MDDR_DQ28	0	I/O	N	N	Y	15.016	0.718421	9.5998	1.72399	0	128.647	Libero Defined* DNC
A24	DDRIO60PB0/MDDR_RESET_N	0	I/O	N	N	Y	15.0875	0.704002	9.88004	1.72551	0	130.568	Libero Defined* DNC
A25	DDRIO59PB0/MDDR_CLK	0	I/O	N	N	Y	15.502	0.722614	9.44108	1.80314	0	130.475	Libero Defined* DNC
A26	DDRIO57PB0/MDDR_BA2	0	I/O	N	N	Y	15.7885	0.706085	9.86659	1.77692	0	132.409	Libero Defined* DNC
A27	DDRIO55PB0/MDDR_ADDR3	0	I/O	N	N	Y	17.2149	0.75936	10.8156	1.95462	0	145.397	Libero Defined* DNC
A28	DDRIO55NB0/MDDR_ADDR4	0	I/O	N	N	Y	17.2833	0.763441	10.7336	1.95027	0	144.684	Libero Defined* DNC
A29	VSS			N	N	N							VSS

3. Go to the sheet that has the device name that you require.
4. Retain the following columns and delete the remaining columns:
   - PGK.PIN
   - <Device> Pin Name
   - Direction
5. Insert a row at the beginning of the worksheet. See Figure 67, page 68.

Figure 67 • **Example PAT Spreadsheet - Editing Stage**

6. Add the following headings for the columns. See Figure 68, page 69:
    - Number
    - Name
    - Type
    - Pin Visibility
    - Shape
    - Pin Group
    - Position
    - Section

    For Type, Shape, Position, and Section columns, enter the information manually to avoid warnings from the OrCAD Capture tool.

7. For **Type** column, choose and type one of the following options:
    - Replace `I` with `Input`
    - Replace `O` with `Output`
    - Replace `I/O` with `Bidirectional`

    Other pin types for the remaining pins:

    - 3-State
    - Open Collector
    - Open Emitter
    - Passive (Unused pins like DNC or NC)
    - Power (Supply and ground pins)

8. Leave the **Pin Visibility** column blank. The check boxes are automatically populated in the **New Part Creation** dialog in the OrCAD Capture tool. See Figure 71, page 72.

9. In the **Shape** column, enter one of the following shapes according to the requirement:
    - Clock
    - Dot
    - Dot-Clock
    - Line
    - Short Clock

- Short Dot
- Short Dot clock
- Short
- Zero Length

The default shape for most of the FPGA symbol pins is `LINE`.

10. Leave the **Pin Group** column blank.
11. In the **Position** column, enter one of the following positions according to the requirement:
    - Bottom
    - Left
    - Right
    - Top
12. In the **Section** column, enter either a number or an alphabet based on the selection made for the Part Numbering option. OrCAD Capture supports two Part Numbering options, that is 1,2,3,4,…for Numeric option and A, B, C, D… for Alphabetical option. See Figure 71, page 72
13. **Save** the Excel file with an appropriate name.

Figure 68 • **Example PAT Spreadsheet - Final Stage**

	A	B	C	D	E	F	G	H
1	Number	Name	Type	Pin Visibility	Shape	Pin Group	Position	Section
2	A1	VSS	Power		Line		Right	L
3	A10	DDRIO75NB0/MDDR_DQ15	Bidirectional		Line		Right	A
4	A11	VSS	Power		Line		Right	L
5	A12	DDRIO83PB0/MDDR_DM_RDQS0	Bidirectional		Line		Right	A
6	A13	DDRIO83NB0/MDDR_DQ4	Bidirectional		Line		Right	A
7	A14	DDRIO82PB0/MDDR_DQ5	Bidirectional		Line		Right	A
8	A15	DDRIO84PB0/MDDR_DQS0	Bidirectional		Line		Right	A
9	A16	VSS	Power		Line		Right	L
10	A17	DDRIO88NB0/MDDR_DQ_ECC2	Bidirectional		Line		Right	A
11	A18	DDRIO88PB0/MDDR_DQ_ECC3	Bidirectional		Line		Right	A
12	A19	DDRIO90PB0/MDDR_DQS_ECC	Bidirectional		Line		Right	A
13	A2	DDRIO53NB0/MDDR_ADDR7	Bidirectional		Line		Left	A
14	A20	DDRIO92PB0/MDDR_TMATCH_ECC_OUT	Bidirectional		Line		Right	A
15	A21	VSS	Power		Line		Right	L
16	A3	DDRIO53PB0/MDDR_ODT	Bidirectional		Line		Left	A
17	A4	DDRIO57NB0/MDDR_ADDR0	Bidirectional		Line		Left	A
18	A5	DDRIO55PB0/MDDR_ADDR3	Bidirectional		Line		Left	A
19	A6	VSS	Power		Line		Right	L
20	A7	DDRIO59NB0/MDDR_CLK_N	Bidirectional		Line		Left	A
21	A8	DDRIO62PB0/MDDR_RAS_N	Bidirectional		Line		Left	A
22	A9	DDRIO62NB0/MDDR_WE_N	Bidirectional		Line		Left	A
23	AA1	VSS	Power		Line		Right	L
24	AA10	DDRIO147NB5/CCC_SW0_CLKI2	Bidirectional		Line		Right	F
25	AA11	DDRIO148NB5/PROBE_B	Bidirectional		Line		Right	F
26	AA12	VSS	Power		Line		Right	L
27	AA13	SERDES_0_TXD2_N	Output		Line		Right	J
28	AA14	VSS	Power		Line		Right	L
29	AA15	SERDES_0_RXD2_P	Input		Line		Left	J
30	AA16	VSS	Power		Line		Right	L
31	AA17	SERDES_0_TXD0_P	Output		Line		Right	J
32	AA18	VSS	Power		Line		Right	L
33	AA19	SERDES_0_RXD0_N	Input		Line		Left	J
34	AA2	MSIO2PB3/USB_STP_B	Bidirectional		Line		Right	D
35	AA20	VSS	Power		Line		Right	L
36	AA21	MSIOD145NB6/SERDES_0_REFCLK0_N	Bidirectional		Line		Right	G
37	AA3	JTAG_TMS/M3_TMS/M3_SWDIO	Input		Line		Left	E
38	AA4	XTLOSC_MAIN_XTAL	Clock		Line		Left	J
39	AA5	NC	Passive		Line		Right	L
40	AA6	DDRIO186PB5/FDDR_ODT	Bidirectional		Line		Right	F
41	AA7	DDRIO186NB5/FDDR_ADDR7	Bidirectional		Line		Right	F

Recommendations for arranging pins in the **Section** column:

- Arrange individual bank pins in separate sections
- Arrange all power supply pins in one section
- Arrange all ground pins in one section
- All passive pins can be in one section
- Arrange the remaining pins like Clock, JTAG, SERDES in one section.

4.1.2 Generating a OrCAD Capture Schematic Symbol

1. Invoke Cadence OrCAD Capture CIS.
2. Go to **File** > **New** > **Library**, then select the `*.olb` file.
3. Go to **Design** > **New Part from Spreadsheet...**
   The **New Part Creation Spreadsheet** dialog appears as shown in the following figure.
4. In the **New Part Creation Spreadsheet** dialog, specify the following:
   - Part Name
   - Number of sections
   - Part Ref Prefix - choose Alphabetic

Figure 69 • **New Part Creation Spreadsheet Dialog**

5. From the Example PAT Spreadsheet, select and copy all the cells, excluding the column headers as shown in the following figure.
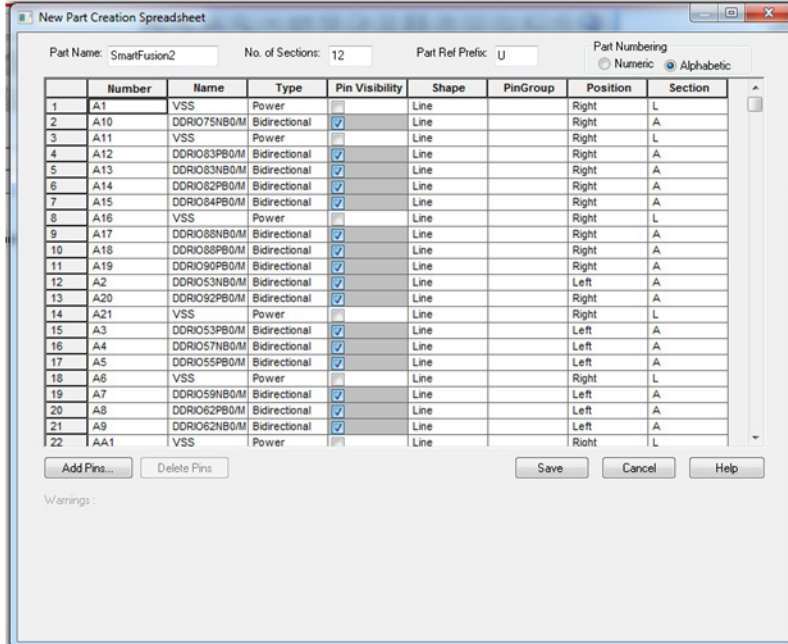
Figure 70 • **Example PAT Spreadsheet - Final Stage**

	A	B	C	D	E	F	G	H
1	Number	Name	Type	Pin Visibility	Shape	Pin Group	Position	Section
2	A1	VSS	Power		Line		Right	L
3	A10	DDRIO75NB0/MDDR_DQ15	Bidirectional		Line		Right	A
4	A11	VSS	Power		Line		Right	L
5	A12	DDRIO83PB0/MDDR_DM_RDQS0	Bidirectional		Line		Right	A
6	A13	DDRIO83NB0/MDDR_DQ4	Bidirectional		Line		Right	A
7	A14	DDRIO82PB0/MDDR_DQ5	Bidirectional		Line		Right	A
8	A15	DDRIO84PB0/MDDR_DQS0	Bidirectional		Line		Right	A
9	A16	VSS	Power		Line		Right	L
10	A17	DDRIO88NB0/MDDR_DQ_ECC2	Bidirectional		Line		Right	A
11	A18	DDRIO88PB0/MDDR_DQ_ECC3	Bidirectional		Line		Right	A
12	A19	DDRIO90PB0/MDDR_DQS_ECC	Bidirectional		Line		Right	A
13	A2	DDRIO53NB0/MDDR_ADDR7	Bidirectional		Line		Left	A
14	A20	DDRIO92PB0/MDDR_TMATCH_ECC_OUT	Bidirectional		Line		Right	A
15	A21	VSS	Power		Line		Right	L
16	A3	DDRIO53PB0/MDDR_ODT	Bidirectional		Line		Left	A
17	A4	DDRIO57NB0/MDDR_ADDR0	Bidirectional		Line		Left	A
18	A5	DDRIO55PB0/MDDR_ADDR3	Bidirectional		Line		Left	A
19	A6	VSS	Power		Line		Right	L
20	A7	DDRIO59NB0/MDDR_CLK_N	Bidirectional		Line		Left	A
21	A8	DDRIO62PB0/MDDR_RAS_N	Bidirectional		Line		Left	A
22	A9	DDRIO62NB0/MDDR_WE_N	Bidirectional		Line		Left	A
23	AA1	VSS	Power		Line		Right	L
24	AA10	DDRIO147NB5/CCC_SW0_CLKI2	Bidirectional		Line		Right	F
25	AA11	DDRIO148NB5/PROBE_B	Bidirectional		Line		Right	F
26	AA12	VSS	Power		Line		Right	L
27	AA13	SERDES_0_TXD2_N	Output		Line		Right	J
28	AA14	VSS	Power		Line		Right	L
29	AA15	SERDES_0_RXD2_P	Input		Line		Left	J
30	AA16	VSS	Power		Line		Right	L
31	AA17	SERDES_0_TXD0_P	Output		Line		Right	J
32	AA18	VSS	Power		Line		Right	L
33	AA19	SERDES_0_RXD0_N	Input		Line		Left	J
34	AA2	MSIO2PB3/USB_STP_B	Bidirectional		Line		Right	D
35	AA20	VSS	Power		Line		Right	L
36	AA21	MSIOD145NB6/SERDES_0_REFCLK0_N	Bidirectional		Line		Right	G
37	AA3	JTAG_TMS/M3_TMS/M3_SWDIO	Input		Line		Left	E
38	AA4	XTLOSC_MAIN_XTAL	Clock		Line		Left	J
39	AA5	NC	Passive		Line		Right	L
40	AA6	DDRIO186PB5/FDDR_ODT	Bidirectional		Line		Right	F
41	AA7	DDRIO186NB5/FDDR_ADDR7	Bidirectional		Line		Right	F

6. Select the top left cell of **New Part Creation Spreadsheet** dialog and paste the copied data. Check if all the columns match between the Example PAT Spreadsheet and **New part creation Spreadsheet** dialog as shown in the following figure.

Note: In the **Pin Visibility** column, select all the check boxes. Some of the check boxes for the power pins might not be selected. If you want those pins to be visible, ensure that they are selected.

Figure 71 • **New Part Creation Spreadsheet Dialog with Data**

7. Click **Save**.

Note: When you click save, the Design Rule Check (DRC) operation is triggered. If there are any errors reported during the DRC, modify the Example PAT Spreadsheet to fix those errors. If there are just warnings and if you want to ignore them, click **Continue** to proceed with generating the Part.

Figure 72 • **New Part created in the Library**

8.   Double-click the part that is created to display the first section as shown in the following figure.

Figure 73 •   **Schematic Symbol - First Section**
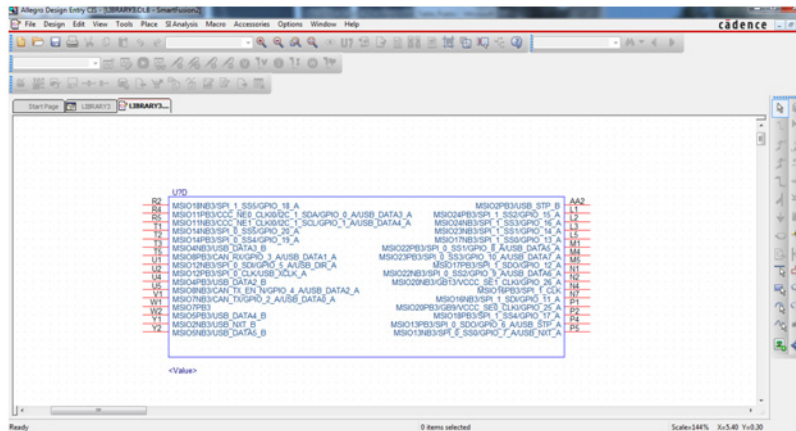
9.   You can navigate to all the sections that are created.
   •   To go to the next part, go to **View** > **Next Part** or press Ctrl + N.
   •   To go to the previous part, go to **View** > **Previous Part** or press Ctrl + B.
   •   To see all the blocks of the schematic symbol, go to **View** > **Package**.

The schematic symbol is ready to use. The following figure shows all the blocks of the schematic symbol that are generated from the Example PAT spreadsheet.

Figure 74 •   **Package View of the Schematic Symbol**
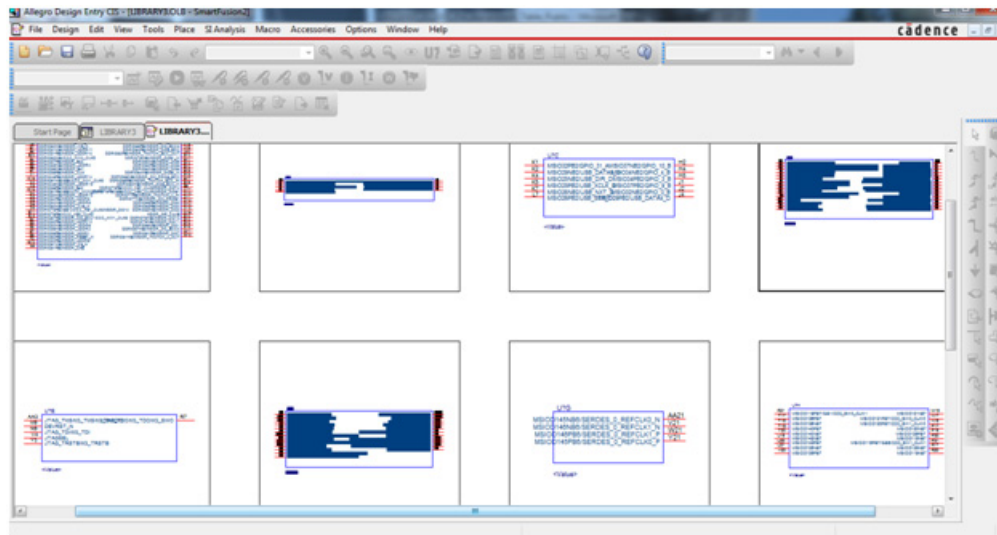
4.2 Creating Schematic Symbols with User Defined Pin Names

4.2.1 Exporting Pin Information from the Libero Design

1. Launch Libero and open project. For more information about how to use the System Builder wizard in the Libero design, see

   http://coredocs.s3.amazonaws.com/Actel/Tool/SysBuilder/sf2_system_builder_ug_1.pdf

   http://coredocs.s3.amazonaws.com/Libero/Tool/SysBuilder/igl2_system_builder_ug_1.pdf

2. Right-click port to change the name and click **Modify Port** as shown in the following figure. Change the name according to the requirement.

Figure 75 • **Modifying Port Names**
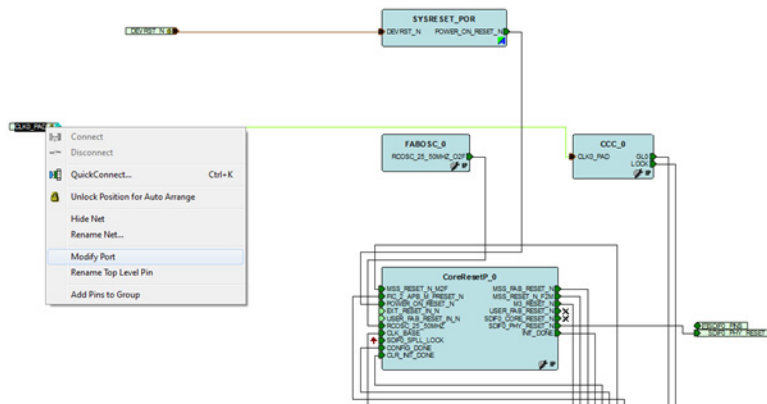
3. Check and verify all the pin names in the design. To verify the pin names, double-click **I/O Constraints** in the **Design Flow** tab as shown in the following figure.

Figure 76 • **I/O Constraints**
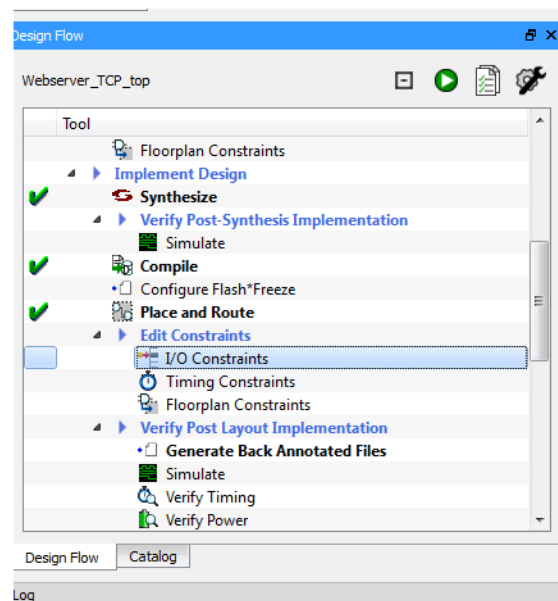
The **I/O Editor** dialog lists the port names with the updated pin names as shown in the following figure. The pin names that are not modified follow the Microsemi pin naming convention.

Note: For the **I/O Editor** dialog to open, the design must be synthesized and compiled.

Figure 77 • **I/O Editor**

Figure 78 • **Exporting pin information from Libero**
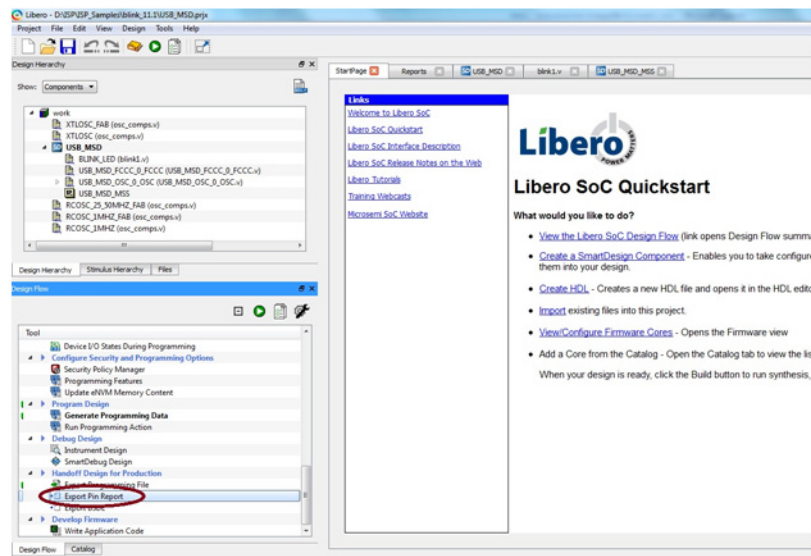
4. To export the pin names, double-click **Export Pin Report** in the **Design Flow** tab. This report has the file extension `.rpt`.

The report is stored in the project directory. The path is:

```
<Libero Project Directory>\designer\project\export\<project
Name>_top_pinrpt_number.rpt.
```

4.2.2 Preparing the Pin List for Import into OrCAD Capture CIS

1. Launch Microsoft Excel, and open the `*.rpt` file that has the exported pin information. Before you open, ensure that **All Files (*.*)** is the file type as shown in the following figure.

Figure 79 • **Importing Pin Names to the Spreadsheet**
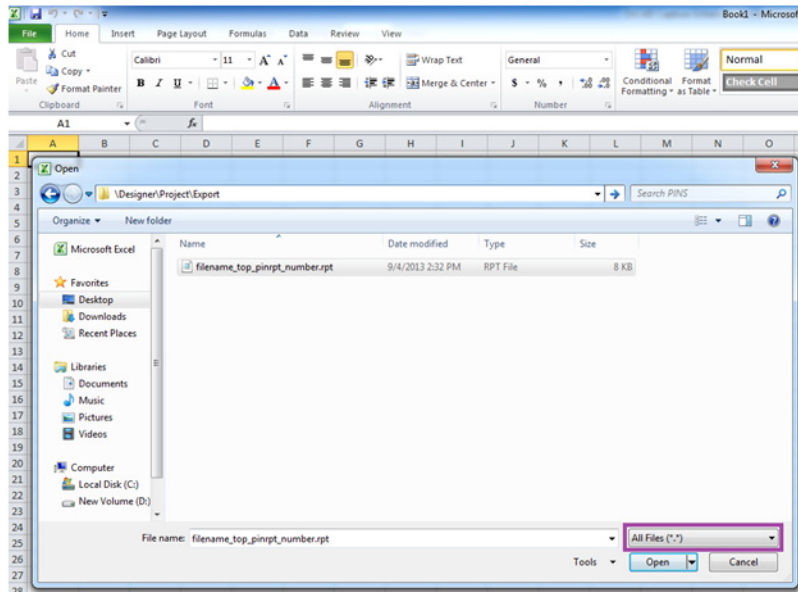
2. In the **Text Import Wizard - Step 1** dialog, select **Delimited**, start import at page 14 and click **Next**. The first 14 rows of the spreadsheet have data unrelated to the pin information.

The following figure shows the **Text Import Wizard** with the **Delimited** option selected and the **Start import at page** option having the value 14.

Figure 80 • **Importing Pin Names to the Spreadsheet—Step 1**

a **MICROCHIP** company
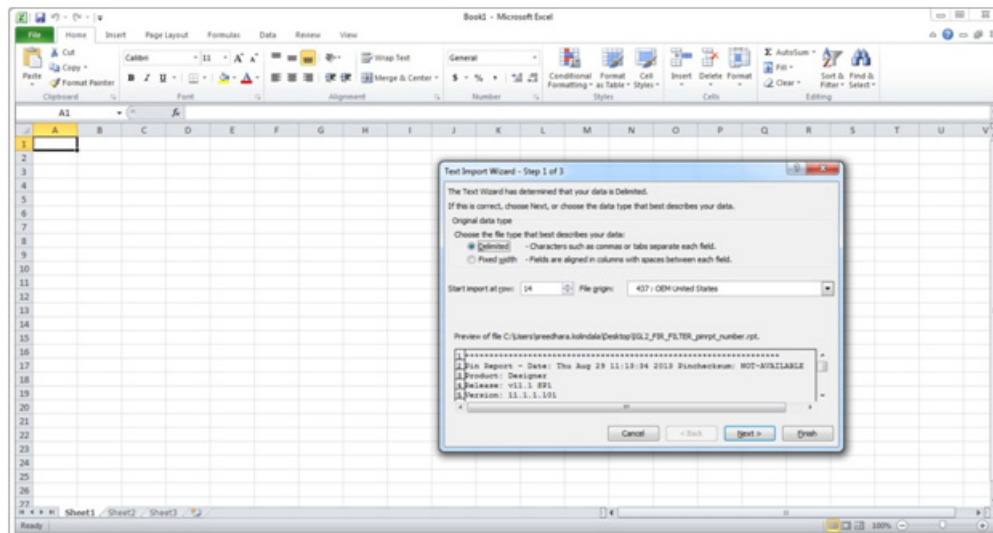
3. In the **Text Import Wizard - Step 2** dialog, select the following as Delimiters and click **Next**:
   - Tab
   - Space
   - I as other

Figure 81 • **Importing Pin Names to the Spreadsheet—Step 2**
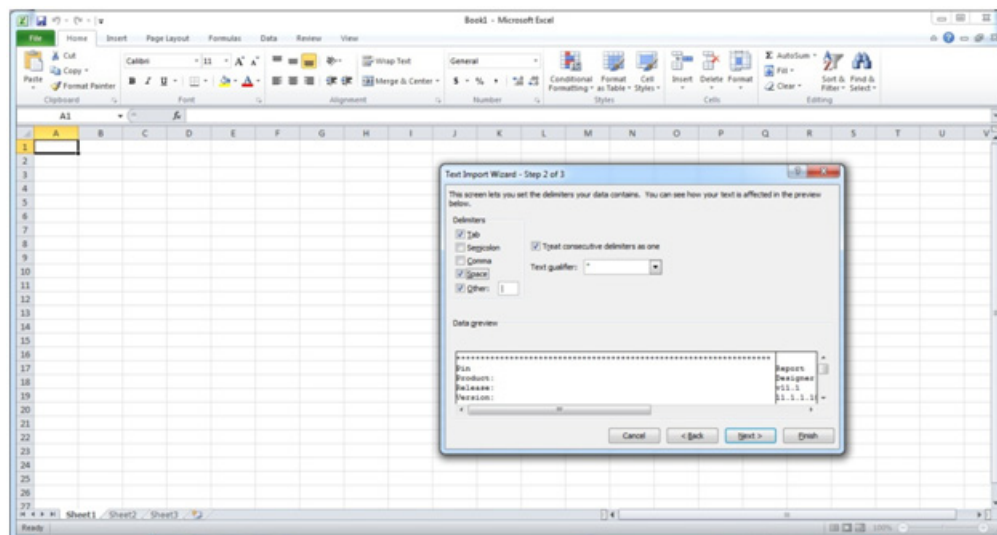
4. Click **Finish** to import the data in separate columns.

Figure 82 • **Importing Pin Names to the Spreadsheet—Final Step**

5. Retain the columns A, B, F and delete the remaining columns as they are not required for generating schematic symbols.

Figure 83 • **Spreadsheet with the Pin Names Imported**

6. Add the following headings for the columns. See Figure 84, page 79.
    - Number
    - Name
    - Type
    - Pin Visibility
    - Shape
    - Pin Group
    - Position
    - Section

By default Number, Name and Type columns are populated from the report.For Type, Shape, Position, and Section columns, add information manually to avoid warnings from the OrCAD Capture tool.

7. For **Type** column, choose and type one of the following options:
    - 3-State
    - Bidirectional
    - Input
    - Open Collector
    - Open Emitter
    - Output
    - Passive (Unused pins like DNC or NC)
    - Power (Supply and ground pins)
8. Leave the **Pin Visibility** column blank. The check boxes are automatically populated in the **New Part Creation** dialog.
9. In the **Shape** column, enter one of the following shapes according to the requirement:
    - Clock
    - Dot
    - Dot-Clock
    - Line
    - Short Clock
    - Short Dot
    - Short Dot clock
    - Short
    - Zero Length

The default shape for most of the FPGA symbol pins is the `LINE`.

10. Leave the **Pin Group** column blank.
11. In the **Position** column, enter one of the following positions according to the requirement:
    - Bottom
    - Left
    - Right
    - Top
12. In the **Section** column, enter either a number or an alphabet based on the selection made for the Part Numbering option. OrCAD Capture supports two Part Numbering options, that is, 1, 2, 3, 4,… for **Numeric** option and A, B, C, D… for **Alphabetical** option.
13. **Save** the Excel file with an appropriate name.

The following figure shows the final pin assignment spreadsheet.

Figure 84 • **Final Example Spreadsheet to be Imported into OrCAD Capture**

	Number	Name	Type	Pin Visibility	Shape	Pin Group	Position	Section
1	Number	Name	Type	Pin Visibility	Shape	Pin Group	Position	Section
2	AB13	CLK0_PAD	Input		Clock		Right	A
3	E22	HPMS_INT_M2F[4]	Output		Line		Right	A
4	F18	HPMS_INT_M2F[7]	Output		Line		Right	A
5	F19	HPMS_INT_M2F[8]	Output		Line		Right	A
6	F20	HPMS_INT_M2F[1]	Output		Line		Right	A
7	F21	COMM_BLK_INT	Output		Line		Right	A
8	G18	HPMS_INT_M2F[10]	Output		Line		Right	A
9	G19	HPMS_INT_M2F[14]	Output		Line		Right	A
10	H19	HPMS_INT_M2F[5]	Output		Line		Right	A
11	H20	HPMS_INT_M2F[6]	Output		Line		Right	A
12	J18	FIC32_0_LOCK	Output		Line		Right	A
13	K1	FIC32_0_CLK	Output		Line		Left	A
14	K15	HPMS_INT_M2F[13]	Output		Line		Left	A
15	K16	HPMS_INT_M2F[2]	Output		Line		Left	A
16	K17	HPMS_INT_M2F[3]	Output		Line		Left	A
17	K18	MSIO20PB2	Bidirectional		Line		Left	A
18	K19	VSS	Power		Short		Right	C
19	K20	HPMS_INT_M2F[15]	Output		Line		Left	A
20	K21	HPMS_INT_M2F[0]	Output		Line		Left	A
21	K22	NC	Passive		Line		Left	D
22	L6	VDDI6	Power		Short		Right	B
23	L9	VDD	Power		Short		Left	B
24	L18	HPMS_INT_M2F[9]	Output		Line		Left	A
25	L19	HPMS_FAB_RESET_N	Output		Line		Left	A

4.2.3 Generating a Capture Schematic Symbol

See Generating a OrCAD Capture Schematic Symbol, page 70".

5 Board Design and Layout Checklist

This chapter provides a set of checks for designing hardware using Microsemi SmartFusion2 and IGLOO2 FPGAs. The checklists provided in this chapter are a high-level summary to assist the design engineers in the design process.

5.1 Prerequisites

Ensure that you have gone through the following chapters before reading this chapter:

- Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs, page 5
- Layout Guidelines for SmartFusion2 and IGLOO2 Based Board Design, page 36

This checklist is intended as a guideline only. The SmartFusion2 and IGLOO2 families consists of FPGAs ranging from densities of 6 K to 100 K logic elements (LE).

5.2 Design Checklist

The following table lists the checks that design engineers must take care of while designing the system.

Table 21 • **Design Checklist**

S.No.	Checklist	Yes/No
Prerequisites		
1.	Read datasheet and pin description user guides: – *IGLOO2 and SmartFusion2 Datasheet* – *IGLOO2 Pin Descriptions* – *SmartFusion2 Pin Descriptions*	
2.	Check for available designs and development tools.	
3.	Refer to the board-level schematics of the *SmartFusion2 Security Evaluation Kit* or *SmartFusion2 Advanced Development Kit.*	
Design Specifications		
4.	Draw the high-level design with architectural block diagram including all the basic interfaces.	
5.	Specify all the I/O interfaces for all banks in the FPGA.	
6.	Create a detailed functional verification test plan.	
7.	Check for IP software that impacts the system design.	
Device Selection		
8.	Check for available device variants of the SmartFusion2 or IGLOO2 FPGA. Select a device based on the I/O pin count, transceivers, microcontroller subsystem (MSS) peripherals, phase-locked loops (PLLs), and speed grade.	
9.	Check device errata: – *SmartFusion2 Errata* – *SmartFusion2 M2S150ES/M2S090ES Errata* – *IGLOO2 Errata*	
10.	Compare the design requirements with the available interfaces and number of I/Os.	
11.	Estimate the required logic utilization, memory, number of I/O pins, and density.	

Table 21 • **Design Checklist** *(continued)*

S.No.	Checklist	Yes/No
12.	**Vertical Migration** If desiring pin compatibility within the same package, choose the largest density device for easy vertical migration without any pin conflict in case of future development. For more information, refer to the application notes available under Schematics/PCB section.	
13.	Identify the clocking requirements.	
14.	Verify that the number of differential channels is adequate.	
Design		
15.	**Power Analysis** Perform power analysis and check the results against the power budget. (Microsemi Power Calculator can be used to analyze the power consumption. Estimate the dynamic and static power consumption, and ensure that the design does not violate the power budget.)	
16.	**Noise Margin Analysis** Analyze the dynamic drive capability of output drivers to ensure that the drivers are not loaded beyond the limits (V_{OH}, V_{OL}, V_{IH}, and V_{IL}). **Loading Analysis** Analyze the dynamic drive capability of output drivers to confirm that the drivers are not loaded beyond the limits (C_L)	
17.	**Programming and Debugging Scheme** Check for the programming modes and the procedure to program the device. For programming or debugging through JTAG, add a 10-pin vertical header (2.54 mm pitch). For more information about programming, see *IGLOO2 Programming User Guide* and *SmartFusion2 Programming User Guide*.	
Power Supply		
18.	**Reference Documentation** – *IGLOO2 and SmartFusion2 Datasheet, Operating Conditions* section – *IGLOO2 Pin Descriptions / SmartFusion2 Pin Descriptions* – Figure 1, *page 6* (for more detailed connectivity)	
19.	**Voltage Rails** The design can be created with just two voltage rails. See Obtaining a Two-Rail Design for Non-SerDes Applications, page 33.	
20.	**VDD: Core Supply** VDD operates at 1.2 V.	
21.	**VPP: Programming Supply** Charge pump and eNVM can operate at 2.5 V or 3.3 V.	
22.	**VDDI Bank Supplies** Connect VDDI pins to support the I/O standards of each bank. Ensure I/O power pin compatibility with I/O standards. Check for the banks that must be powered even when unused. See Table 4, page 13 to Table 7, page 15. For recommendations on unused bank supplies, see Table 16, page 32. The recommendations vary from device to device.	

Table 21 • **Design Checklist** *(continued)*

S.No.	Checklist	Yes/No
23.	**SerDes Power Supplies** – SERDES VDD - VDD – SERDES VDDAIO - 1.2 V – SERDES VDDAPLL to REFRET through resistor-capacitor (RC) filter circuitry (2.5 V) – SERDES PLL VDDA to PLL VSSA through RC filter circuitry - 2.5 V or 3.3 V **VDDA PLL Filter** – REFRET for the SerDes serves as the local on-chip ground return path for VDDAPLL. Therefore, external board ground must not short with REFRET under any circumstances. – A high precision 1.21K_1% Ù resistor is required to connect between REXT and REFRET. For detailed information about power supplies, see Figure 1, page 6.	
24.	If SERDES transceiver is not used, the pins need to be connected as follows: – SERDES VDD - VDD – SERDES VDDAIO - 1.2 V – SERDES VDDAPLL - 1.2 V or 2.5 V – SERDES PLL VDDA - 2.5 V or 3.3 V – SERDES PLL VSSA - Ground	
25.	**V$_{REF}$ Power Supply** Design V$_{REF}$ pins to be noise free. V$_{REF}$ should be equal to half of VDDQ. See Figure 15, page 28.	
26.	**Other Supplies** CCC PLL VDDA to PLL VSSA through RC filter circuitry- 2.5 V/ 3.3 V. DDR PLL VDDA to PLL VSSA through RC filter circuitry- 2.5 V/ 3.3 V. All PLL VDDA supplies must be tied to same supply source (either 2.5 V or 3.3 V). Using the Libero SoC software, a single supply can be selected globally.	
27.	**Decoupling Capacitors** Perform power integrity (PI) analysis through the PI tool, and analyze the decoupling capacitor values and placement on the PCB.	
28.	**Unused Condition** For unused conditions of power supply pins, see the corresponding pin assignment table available on the following pages: *SmartFusion2 SoC FPGA Documentation* *IGLOO2 FGPA Documentation* Also see Figure 3, page 11.	
29.	**Brownout Detection (BOD) Circuit** Ensure that brownout detection is implemented standalone or included as part of power management circuitry. See Brownout Detection (BOD), page 34.	

Table 21 • **Design Checklist** *(continued)*

S.No.	Checklist	Yes/No
Clocks		
30.	**Crystal Oscillators (External)** − Main crystal oscillator − Auxiliary (RTC) crystal oscillator (not available in the M2S050T) **RC Oscillators (Internal)** − 1-MHz RC oscillator − 50-MHz RC oscillator IGLOO2 devices have only main crystal oscillator without auxiliary (RTC) crystal oscillator. For more information about crystal oscillators, see Table 12, page 18. **FPGA Fabric Clock Sources** The input clock frequency range for fabric clock conditioning circuits (FABCCC) depends on the usage of PLL for output clock generation: − If the PLL is used, the PLL reference clock frequency must be between 1 MHz and 200 MHz. − If the PLL is bypassed, the FABCCC input clock frequency can be up to 400 MHz. All CCC pins support external oscillators (differential or single ended).	
31.	Global buffer (GB) can be driven through dedicated global I/Os, CCC, or fabric (regular I/Os) routing. The global network is composed of GBs to distribute low-skew clock signals or high-fanout nets. Dedicated global I/Os drive the GBs directly and are the primary source for connecting external clock inputs (to minimize the delay) to the internal global clock network. For more information, see *UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide*.	
Reset		
32.	**DEVRST_N – Input** The DEVRST_N pin must have a 10 KΩ pull-up resistor. The pin must not be left floating. If a push-button switch is used to generate reset, check for switch de-bounce. For more information about DEVRST_N, see Power Supply Flow, page 10.	
JTAG		
33.	In the JTAG interface, the VDDI bank supply must be powered up for programming. The following is a list of pins available for different activities: – JTAGSEL: Low (pull-down) > ARM Cortex-M3 JTAG; High (pull-up) > FPGA fabric JTAG. – TMS: Internal weak pull-up resistor. – TCK: External pin. Should be pulled-down through 1 KΩ resistor. There is no internal pull-up resistor for this pin. – TDI: internal weak pull-up resistor. – TDO: no internal pull-up resistor. – TRSTB: internal weak pull-up resistor. An FP4 or FP5 header (10 pin – 2.54 mm pitch) can be used to connect to FlashPro4 or FlashPro5. For more information about JTAG, see Figure 10, page 22 and Table 13, page 21.	

Table 21 • **Design Checklist** *(continued)*

S.No.	Checklist	Yes/No
Programming		
34.	The device can be programmed either through JTAG interface or serial peripheral interface (SPI) interface. **FLASH_GOLDEN_N** If pulled low, it indicates that the device is to be re-programmed from an image in the external SPI flash attached through the SPI interface. If pulled high, the SPI is put in slave mode. Add a 10kΩ external pull-up resistor to VDDI. Some devices do not support the FLASH_GOLDEN_N pin. Check the *PPAT spreadsheets* available on the following Microsemi webpages: *SmartFusion2 SoC FPGA Documentation* *IGLOO2 FGPA Documentation* For more information about dedicated pins including Flash_GOLDEN_N, see Table 14, page 23.	
Configuring Pins in Open Drain Using Tri-state Buffer		
35.	To configure fabric pins in open-drain mode, the tristate buffer input pin must always be grounded, and the I/O pin of the FPGA must be connected to the active-low enable pin of the buffer. For more information, see Figure 21, page 34.	
SerDes Pins		
36.	Dedicated I/O are available for the SerDes high-speed serial interface, which supports the PCIe, SGMII, XAUI, and JESD204B protocols. **SERDES Clock:** 100 MHz to 160 MHz LVDS source. The SerDes reference clock pins have internal on-die termination (ODT) settings. These settings can be enabled through the Libero software. The reference clock source (differential clock oscillator) is selected based on many parameters such as frequency range, output voltage swing, jitter (deterministic, random, and peak-to-peak), rise and fall times, supply voltage and current, noise specification, duty cycle, duty cycle tolerance, and frequency stability. An example clock source can be the CCLD-033- LVDS clock oscillator. SerDes clock requirements for different protocols are as follows: – PCIe: 100 MHz – XAUI: 156.25 MHz – SGMII: 125 MHz – EPCS: 125 MHz – **SERDES TXD**: The transmit pair must alone have AC-coupling capacitors near the SmartFusion2/IGLOO2 device. AC-coupling capacitors of 75-200 nF are required for link detection. If the SerDes unit is unused, these pins must remain floating (DNC). – **SERDES RXD**: The receive pair must have AC-coupling capacitors near the endpoint device. If the SerDes unit unused, these pins must always be connected to ground. For more information about SerDes, see SerDes, page 39.	

Table 21 • **Design Checklist** *(continued)*

S.No.	Checklist	Yes/No
DDR Interface		
37.	**DDR Interface** Short DDR TMATCH IN to DDR TMATCH OUT. Short DDR TMATCH ECC IN to DDR TMATCH ECC OUT. VDDI bank supply should be powered as per the application: – For LPDDR - VDDI should be 1.8 V – For DDR2- VDDI should be 1.8 V – For DDR3- VDDI should be 1.5 V DDR impedance calibration pin should be pulled down with the following resistors: – For LPDDR- 150 Ω – For DDR2- 150 Ω – For DDR3- 240 Ω Though calibration is not required, it is recommended to use corresponding resistor placeholder to connect the pin to the ground with or without a resistor. All data and data strobe signals have internal ODT settings, which can be enabled through the Libero software.	
Hot-swapping and Cold-Sparing		
38.	All user I/Os have internal clamp diode control circuitry for protection. MSIO pins (except PCI 3.3 V standard) support the hot-swapping and cold-sparing operations. MSIOD and DDRIO pins do not support hot swapping and cold-sparing operations	
General Guidelines		
39.	For all MSIO, MSIOD, and DDRIO, a weak internal pull-up resistor is available. In unused condition, these pins can be left floating.	
40.	MSIOD and DDRIO support a maximum of 2.5 V. MSIO supports maximum of 3.3 V.	
41.	There is one MSI special pin (MSIO) available that can be used as input only. This pin is differentially paired with FLASH_GOLDEN_N, which is always input only. For more information, see the following documents: – *IGLOO2 Pin Descriptions* – *SmartFusion2 Pin Descriptions*	
42.	One internal signal can be allocated for probing (for example, towards the oscilloscope feature). The two live probe I/O cells are dual-purpose. They can be used for the live probe functionality or used as user I/Os (MSIO). Ensure to power up the bank where the Live Probe signals are assigned. That Bank may be different across die/package combination.	
43.	MSS peripherals (SPI, I2C, USB, and UART) are available.	
44.	Provide pull-up resistors for all open-collector or open-drain pins, even if a pin is not used.	
45.	Provide separate pull-down resistors for all used open-emitter or open-source pins.	
46.	Enable internal pull-up/pull-down resistor option for all tri-state nets through the Libero tool.	
47.	Ensure that all the critical signals on the board are terminated properly.	
48.	Terminate the unused interface signals properly to avoid metastability and electromagnetic interference (EMI)/electromagnetic compatibility (EMC) problems.	

Table 21 • **Design Checklist** *(continued)*

S.No.	Checklist	Yes/No
49.	Provide a sufficient number of ground pins for board-to-board connectors to ensure signal integrity (SI) across connectors. Dense board-to-board connectors may cause severe cross-talk problems. The severity of crosstalk depends on the frequency of the signal and the spacing between signal pins on the connectors. (The number of ground pins may be obtained after performing SI analysis.) The severity can be reduced by providing ground pins between signal pins.	
50.	Use proper voltage-level translator devices for interfacing higher-operating-voltage devices with lower-operating-voltage devices.	
51.	Perform timing analysis of all components, taking into consideration the delays introduced by buffers in the data, address, or control paths.	
52.	Perform signal integrity analysis (pre-layout and post-layout) for all critical interfaces and all types of I/Os using input/output buffer information specification (IBIS).	
53.	Analyze the design for simultaneous switching noise (SSN) problems: – Use differential I/O standards and lower-voltage standards for high switching I/Os. – Reduce the number of simultaneously switching output pins within each bank. – Reduce the number of pins that switch voltage levels at the same time. – Use lower drive strengths for high switching I/Os. The default drive strength setting might be higher than the design requirement. – Spread output pins across multiple banks if possible. – If bank usage is substantially below 100%, spread the switching I/Os evenly throughout the bank to reduce the number of aggressors in a given area to reduce SSN. – Separate simultaneously switching pins from input pins that are susceptible to SSN.	
54.	Place important clock and asynchronous control signals near ground signals and away from large switching buses.	
55.	**I/O Pin Assignment** Use a spreadsheet to capture the list of design I/Os. Microsemi provides detailed pinout information that can be downloaded from the website and customized to store the pinout information for specific designs. Pinout details for various packages with different densities are available on the following pages: *SmartFusion2 SoC FPGA Documentation* *IGLOO2 FGPA Documentation*	
56.	Check if there are any incompatible I/O standards combined in the same bank.	
57.	Check if there are two interfaces with different voltage standards in the same bank.	
58.	See the bank location diagrams in the *IGLOO2 Pin Descriptions* / *SmartFusion2 Pin Descriptions* documents to assess the preliminary placement of major components on PCB.	

## 5.3 Layout Checklist

The following table lists the layout checks.

Table 22 • **Layout Checklist**

S.No.	Description	Yes/No
Power		
1.	Are 0402 or lesser size capacitors used for all decaps (less than value?)	
2.	Are power supply filters implemented on SERDES_x_VDDAPL, and SERDES_x_PLL_VDDA as shown in the Figure 27, page 40 and Figure 39, page 48 respectively?	
3.	Is precision 1.2 K resistor between SERDES_x_REFRET and SERDES_x_REXT used?	
4.	Are placement and layout guidelines followed for 1.2 K resistor?	
5.	Is the target impedance met on all power planes?	
6.	Are VREF planes for DDRx reference supply isolated from the noisy planes?	
7.	Are enough number of decoupling capacitors used for DDRx core and VTT supply? For more information about DDRx core and VTT supply, see Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs, page 5.	
8.	Is one 0.1 µF cap for two VTT termination resistors used for DDRx?	
9.	Is enough plane width provided for VTT plane?	
DDR3		
10.	Are length match recommendations followed according to the DDR3 guidelines?	
SerDes		
11.	Are length match recommendations followed according to the SerDes guidelines?	
12.	Are the DC blocking capacitors used for SerDes TX and if required on RX lines?	
13.	Is tight controlled impedance maintained along the SerDes traces?	
14.	Are differential vias well designed to match SerDes trace impedance?	
15.	Are DC blocking capacitor pads designed to match SerDes trace impedance?	
Dielectric Material		
16.	Is proper PCB material selected for critical layers?	

6 Appendix: Special Layout Guidelines - Crystal Oscillator

The placement of the crystal needs to be close to the SmartFusion2 or IGLOO2 device. Two capacitors are to be placed symmetrically around the crystal so that the lengths from the crystal pad to capacitor are equal, as shown in the following figure. Two traces from crystal to SmartFusion2/IGLOO2 should have equal lengths.

Figure 85 • **Layout of the Crystal Oscillator**
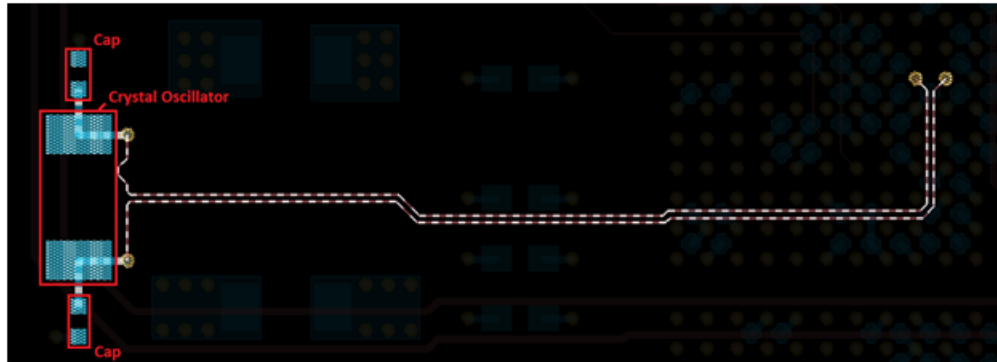
Figure 86 • **Schematics of Crystal Oscillator**
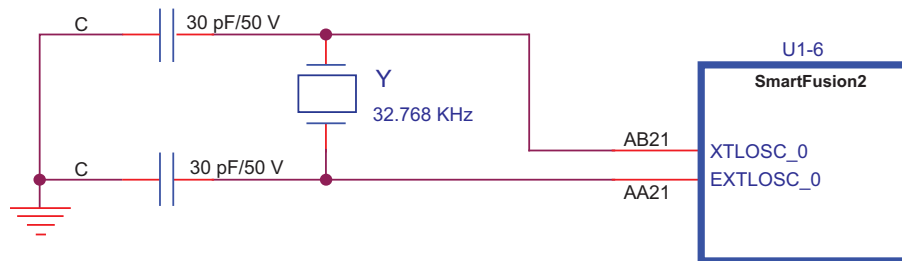
7 Appendix: Stack-Up

A good stack-up leads towards better performance. The number of layers in the stack-up is dependent on many factors such as form factor of the board, number of signals to be routed, and power requirements. Therefore, the designer chooses how many layers the board requires. The SmartFusion2 Development Kit/IGLOO2 Evaluation Kit has 16-layer stack-up, as shown in

Note: All the guidelines in this document are with respect to 16-layer board stack-up.

Utilizing upper power layers should be used for high priority supplies. High-switching current supplies should be placed vertically closer to the devices to decrease the distance the currents need to travel through vias. Ground planes are placed adjacent to the high transient current power planes to reduce inductance and couple the high-frequency noise.

It is good to have power and ground layers on side-by-side layer. The benefits of this inter-plane capacitance provide better decoupling at high frequencies. The effect of via on power pins is reduced by having a power plane near the device.

Signal integrity depends on how well the traces have controlled impedance, so it is always recommended to have controlled impedance.

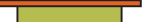Microsemi recommends that all critical high-speed signals like DDR and PCIe signals need to have ground reference. All signal layers should be separated from each other by ground or power planes. This minimizes crosstalk and provides balanced and clean transmission lines with properly controlled characteristic impedance between devices and other board components.

Best performance is obtained when using dedicated ground plane layers that are continuous across the entire board area. Power planes can provide adequate reference, however, the power planes should be related to the signals they serve to reference.

Note: Refrain from using unrelated power planes as a signal reference.

Slots should not interrupt the planes, or else they can possibly force current to find an alternate return path. This undesired return path could cause a localized bounce on the power or ground plane that can possibly be capacitive coupled to all signals adjacent to the planes.

Figure 87 • **Stack-up Used in Development Board**

Lamination Stack-up: L#/Type: Description:			Thickness and Tolerance: Cu+: Lamination/PrePreg:			Base Material Requirements: Type: Description:
1 Mix 2 Pin		Core 0.0040 Q/H	.00035 .00060	.0040		NP 4000-13EP
		Pre-Preg (1 x 2113)		.0034		NP 4000-13EP
3 Mix 4 Pin		Core 0.0035 H/H	.00060 .00060	.0035		NP 4000-13EP
		Pre-Preg (1 x 2113)		.0034	+/- 0.0003	NP 4000-13EP
5 Mix 6 Pin		Core 0.0035 H/H	.00060 .00060	.0035		NP 4000-13EP
		Pre-Preg (1 x 1080)		.0022	+/- 0.0002	NP 4000-13EP
7 Mix 8 Pin		Core 0.0030 1/H	.00120 .00060	.0030		NP 4000-13EP
		Pre-Preg (1 x 1080)		.0026	+/- 0.0003	NP 4000-13EP
9 Mix 10 Pin		Core 0.0030 H/1	.00060 .00120	.0030		NP 4000-13EP
		Pre-Preg (1 x 1080)		.0023	+/- 0.0002	NP 4000-13EP
11 Mix 12 Pin		Core 0.0035 H/H	.00060 .00060	.0035		NP 4000-13EP
		Pre-Preg (1 x 2113)		.0034	+/- 0.0003	NP 4000-13EP
13 Mix 14 Pin		Core 0.0035 H/H	.00060 .00060	.0035		NP 4000-13EP
		Pre-Preg (1 x 2113)		.0034	+/- 0.0003	NP 4000-13EP
15 Mix 16 Pin		Core 0.0040 H/Q	.00060 .00035	.0040		NP 4000-13EP

| **Target Post-Lam Thickness: 0.0600 +/- 0.0030**	**Stack-up Notes:**
Copper Oz Legend: H = 1/2 Oz T = 3/8 Oz Q = 1/4 Oz S = 1/16 Oz	0.004 Q/H CORES MUST BE MADE OF (1 x 2116 PREG) 0.0035 H/H CORES MUST BE MADE OF (1 x 2113 PREG) 0.003 1/H CORES MUST BE MADE OF (1 x 1080 PREG)

8 Appendix: Dielectric Material

The impedance of the traces depends on the geometry of the traces and the dielectric material used. The skew of the signal depends on the dielectric constant and loss of signal strength depends on the loss tangent of the material. The SmartFusion2 Development Kit board uses Nelco 4000-13 dielectric material. However, selection of the material is made based on the speed and length of the high-speed traces. Simulations are recommended on high-speed serial links to converge on the type of the material used.

If the total trace length is less than 20 inches with a speed at or below 3.125 Gbps, FR-4 may be acceptable. Another design option is to use low-loss dielectric PCB material, such as Rogers 4350, GETEK, or ARLON. It can provide increased eye-opening performance when longer trace interconnections are required. If longer traces or faster speed are required, consider using a high-speed material such as ROGERS 3450.

While designing for gigabit serial links, the weaving structure of PCB dielectric material should be taken into consideration. A PCB dielectric substrate is constructed from woven fiberglass fabrics strengthened and bound together with epoxy resin.

A typical weaving is shown in the following figure.

Figure 88 • **Fiberglass Weaving**[2]
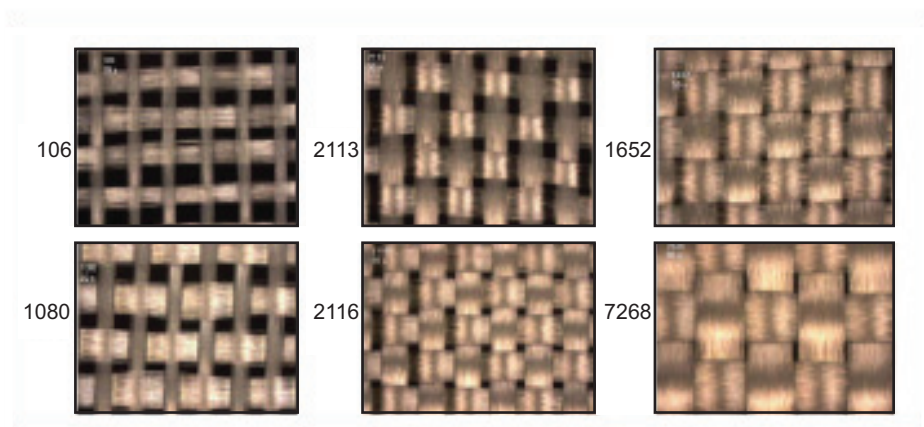
Depending on the density of weaving, the PCB materials are numbered as 106, 1080, 2113, 2116, 1652, and 7268. Trace routed on the PCB is non-homogeneity in dielectric constant due to weaving. This causes discontinuities in the trace impedance, which results in improper eye-opening at the receiving end. For further reading, refer to the *Solving PCB Fiber Weave Issues*.

2. *signal-integrity.tm.agilent.com/2011/pcb-fiber-weave*

9 Appendix: Power Integrity Simulation Topology

The following figure shows the topology that is considered for simulating the power plane for power integrity analysis.

Figure 89 • **Power Integrity Simulation Topology**
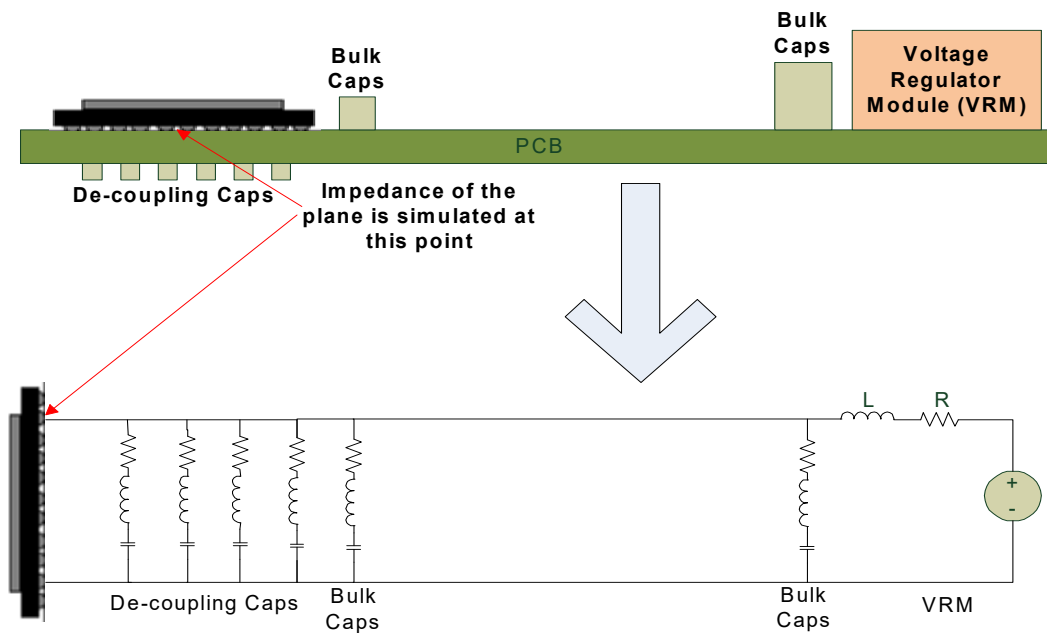
Note: Package parameters of SmartFusion2 are not considered for simulations.