

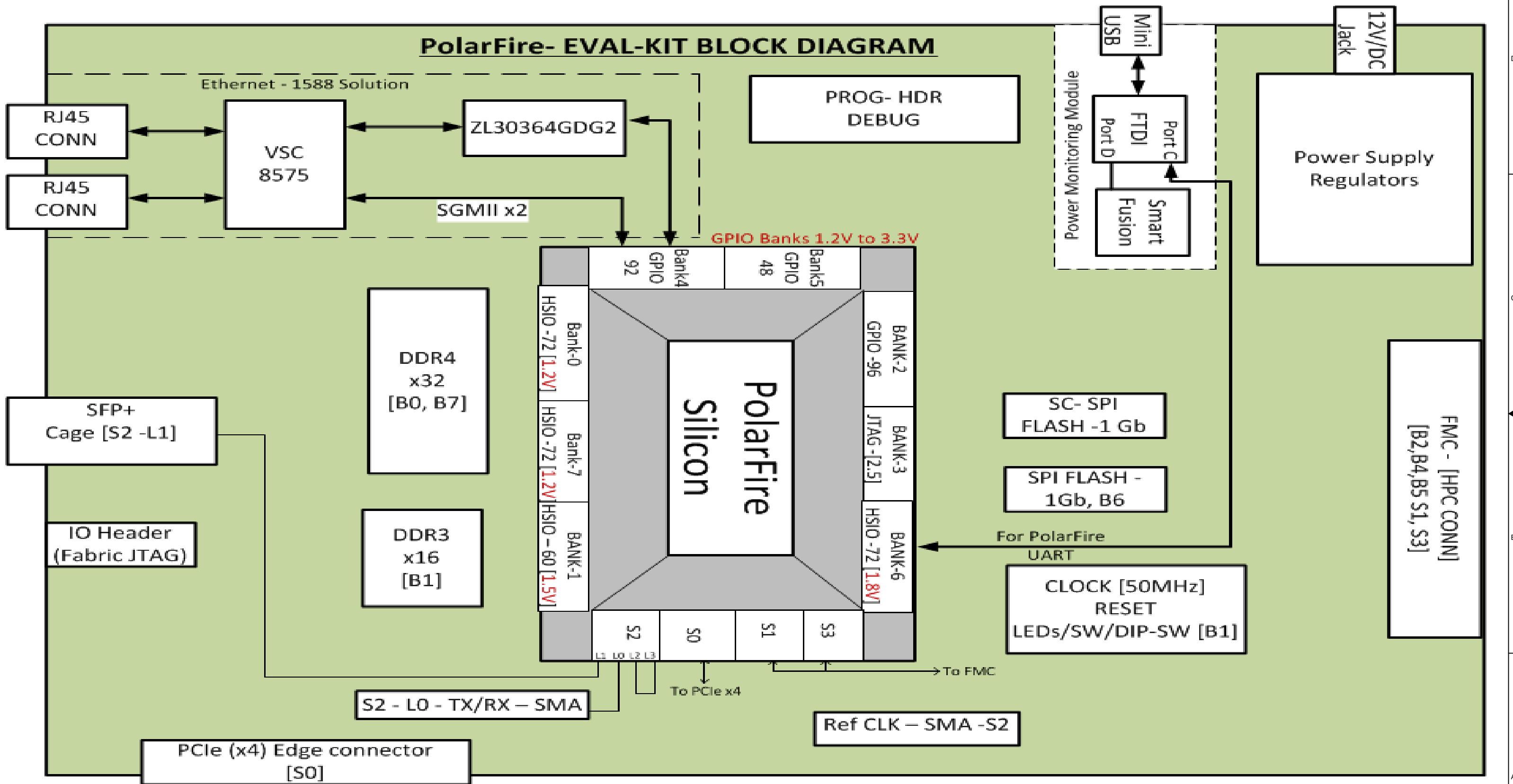
POLARFIRE EVAL KIT

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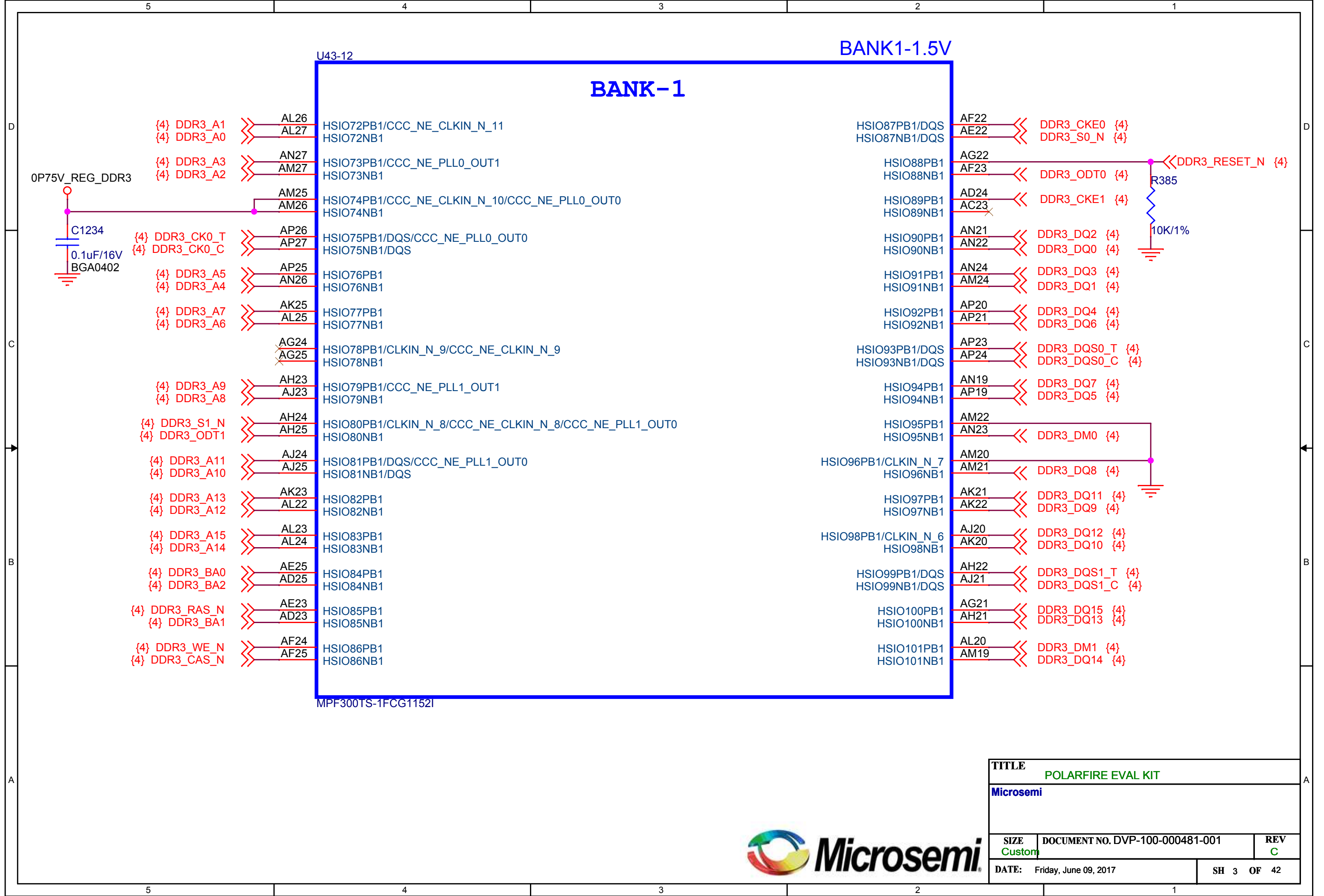


Project Name:		
POLARFIRE EVAL KIT		
Rev	Part Number:	
C	MICROSEMI DVP-100-000481-001	PACTRON: 305-PD-17-0215
Originator:		
GHURU KUMARAVELU		
Size	Date:	
B	Friday, June 09, 2017	
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BLOCK DIAGRAM



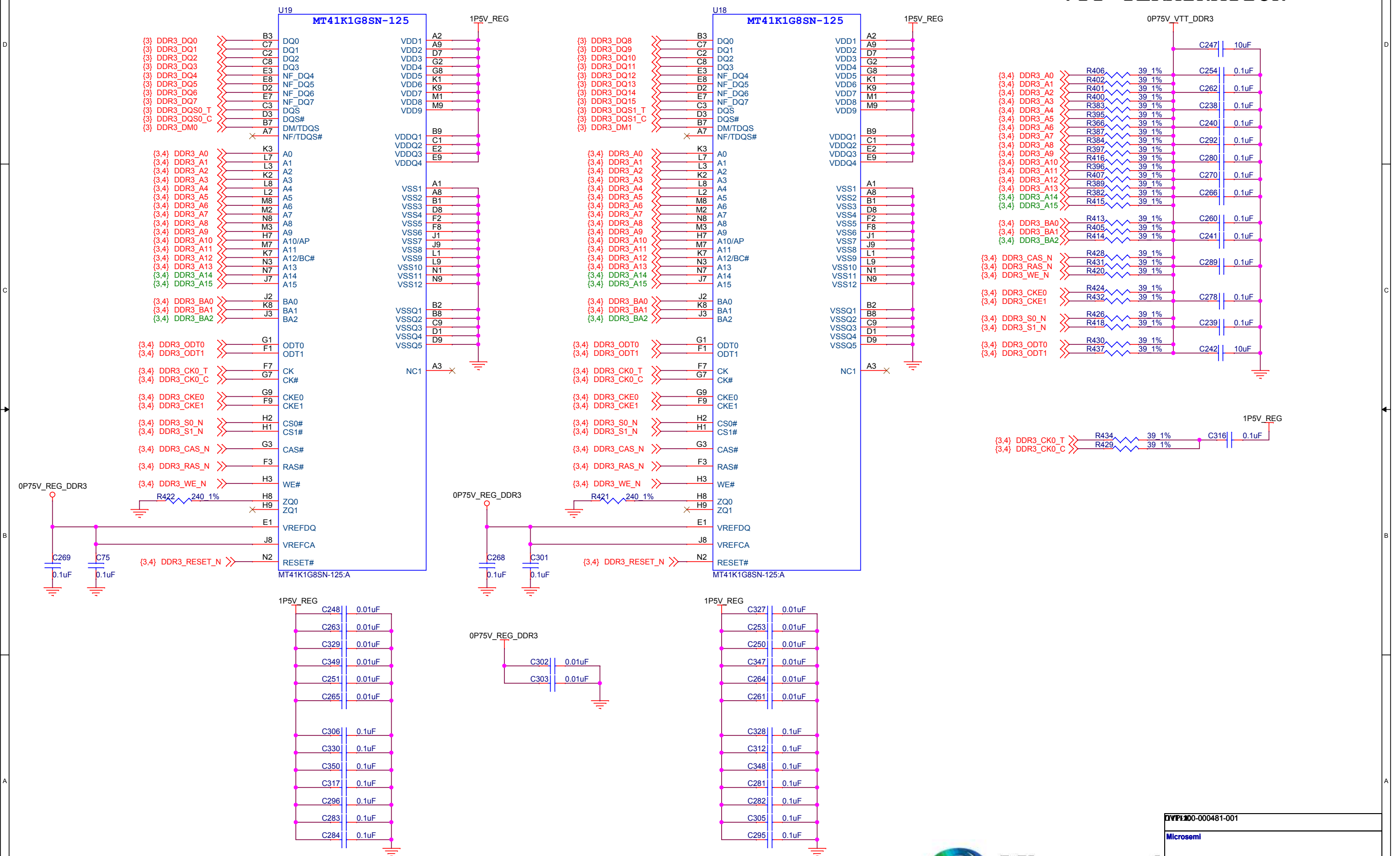
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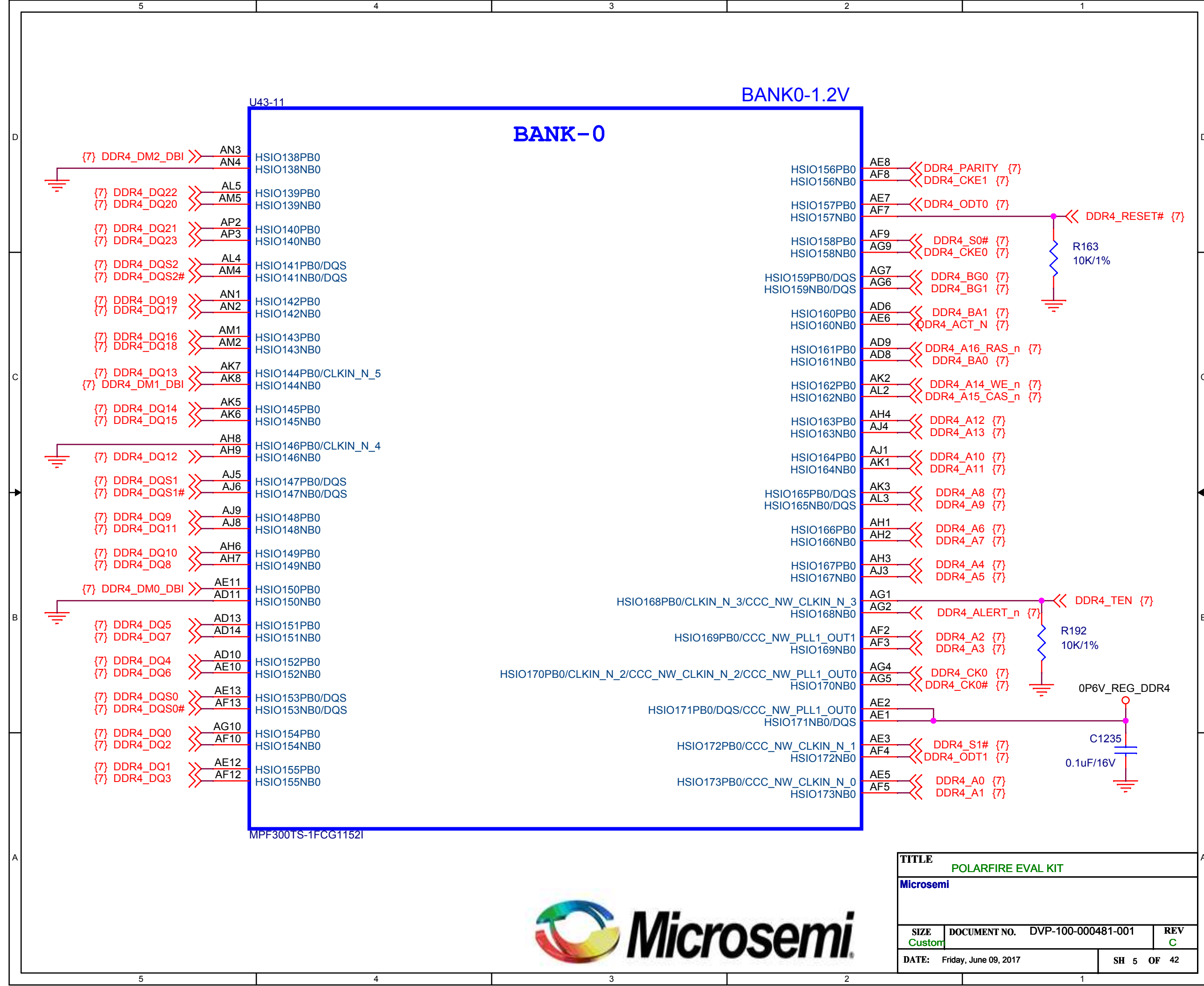
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DDR3 MEMORY-BANK1

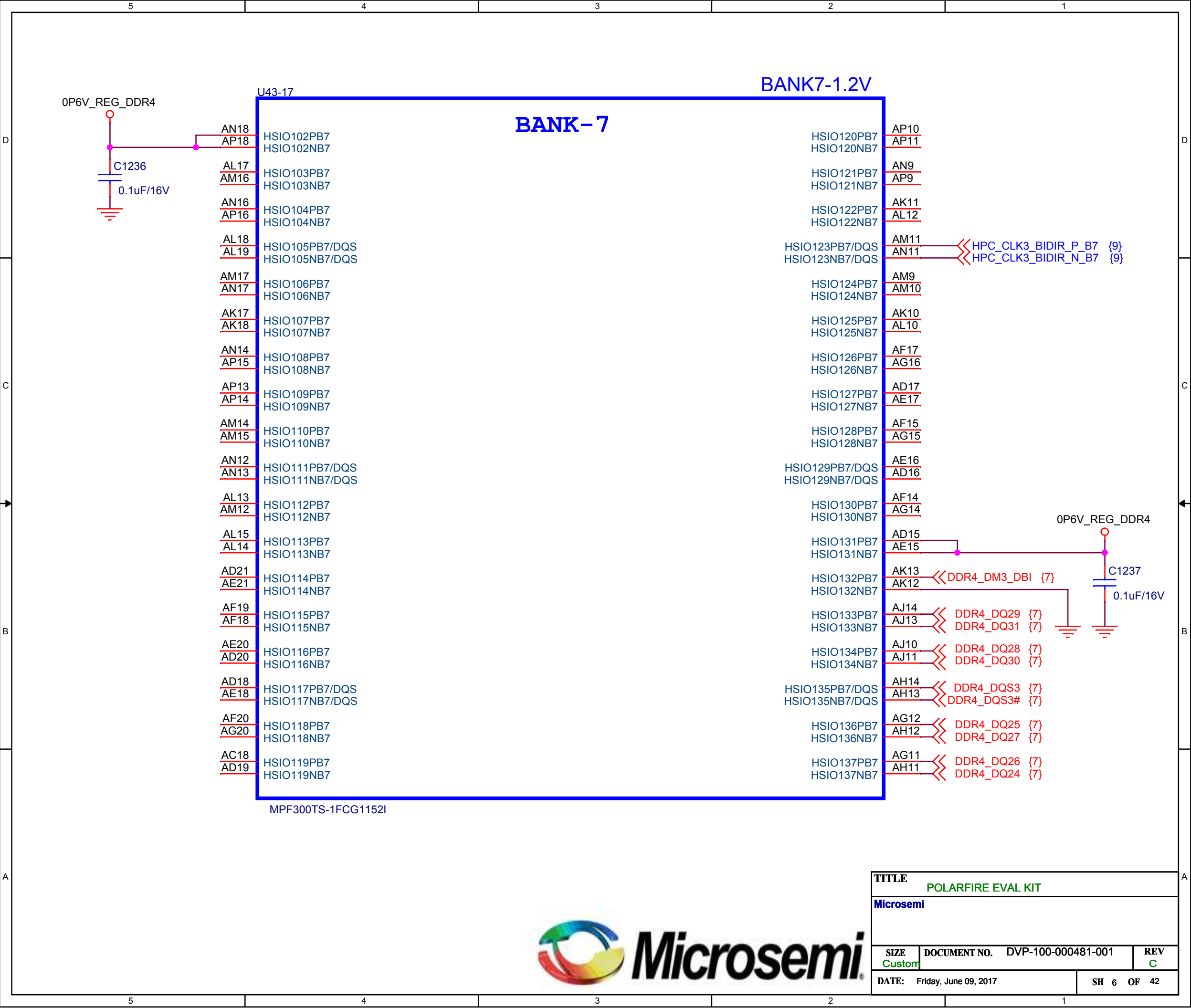
VTT TERMINATION



DVP100-000481-001			
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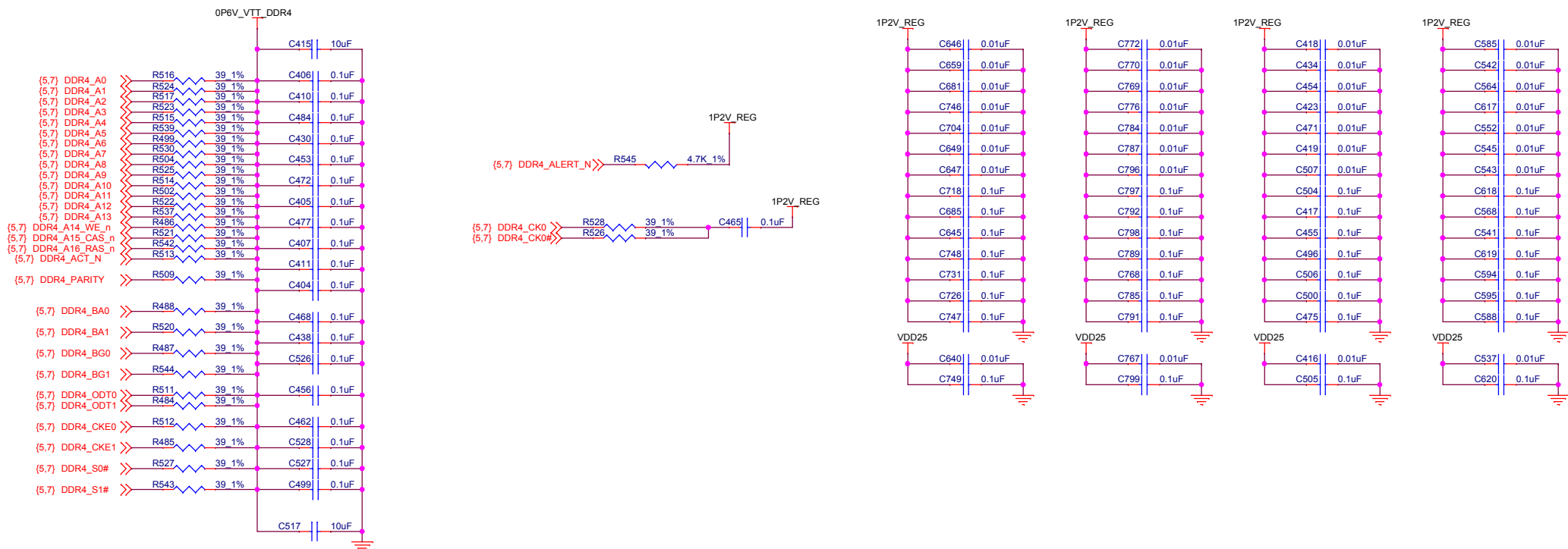
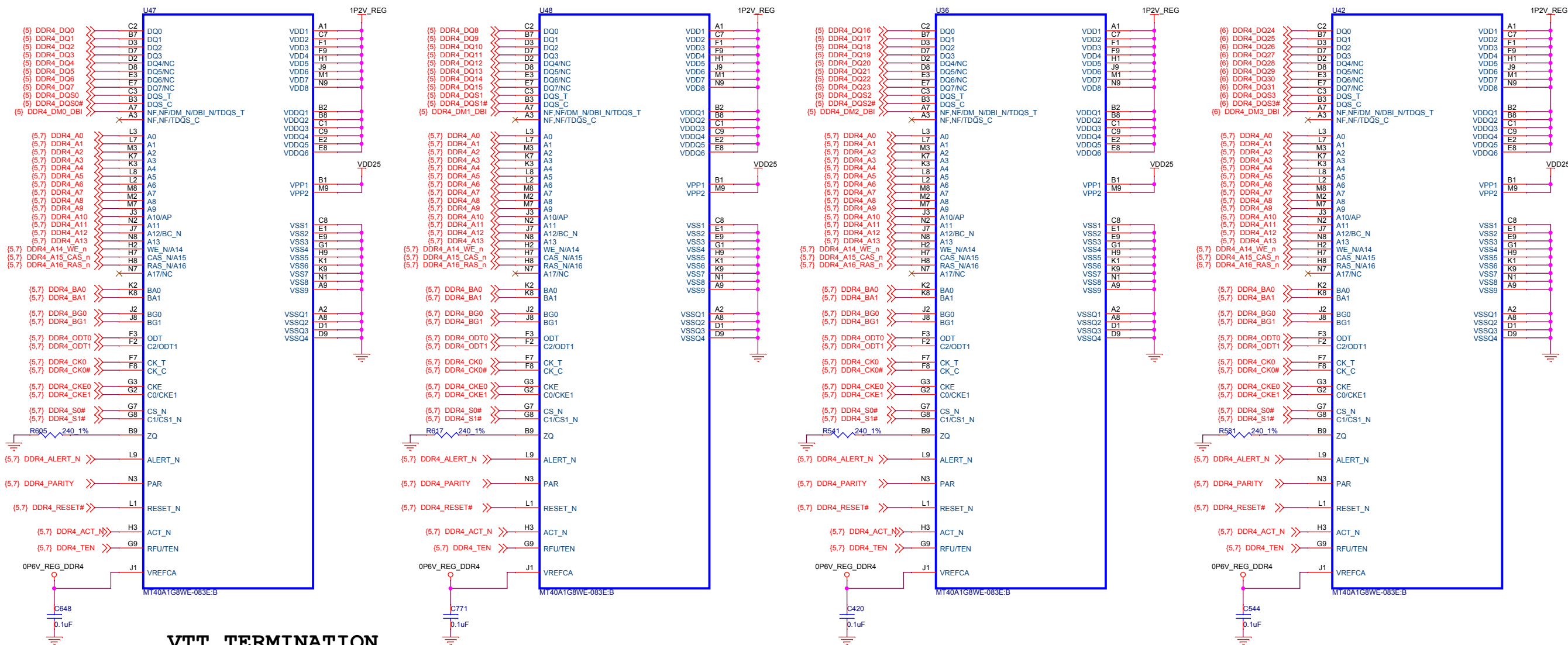


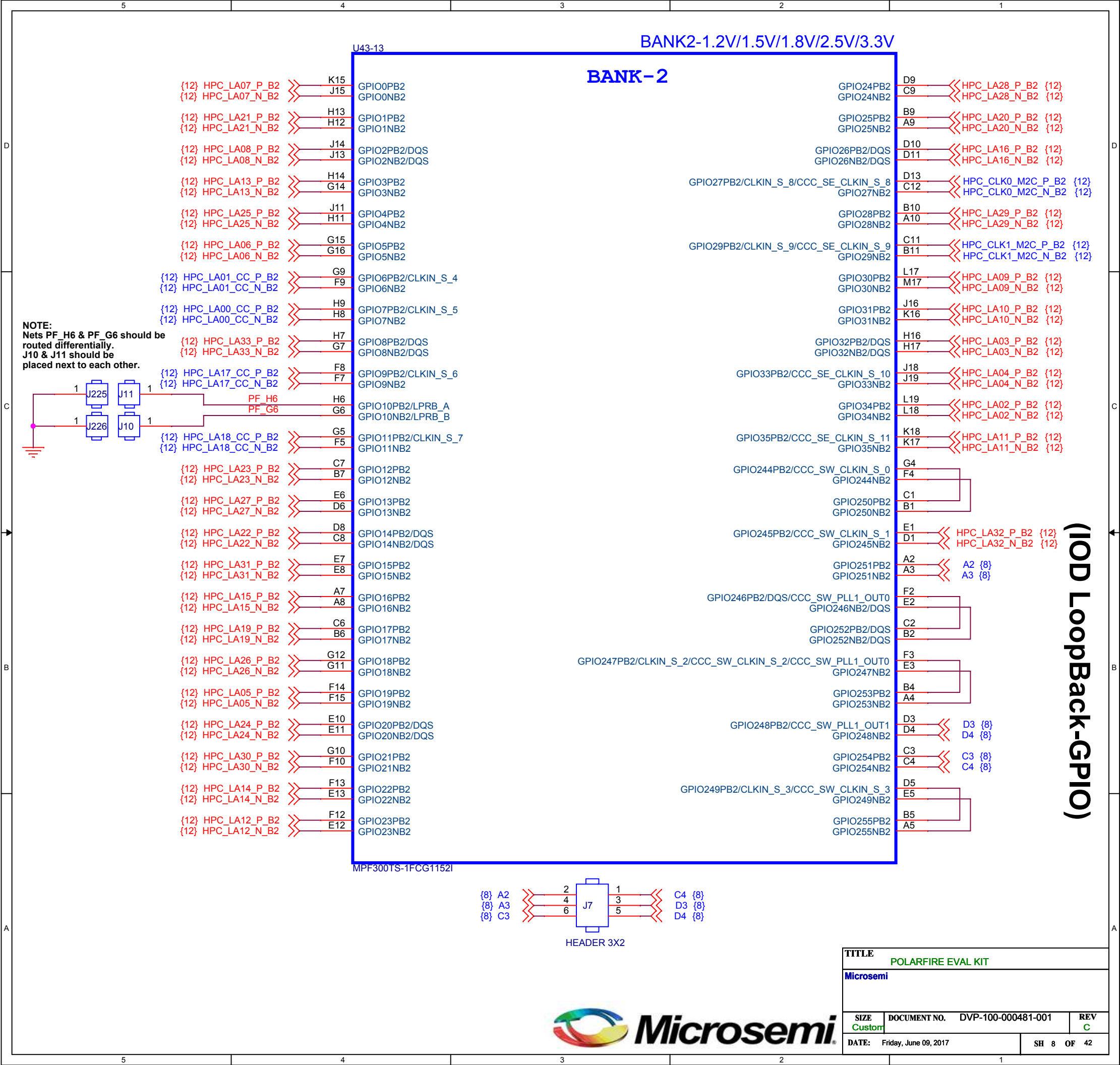
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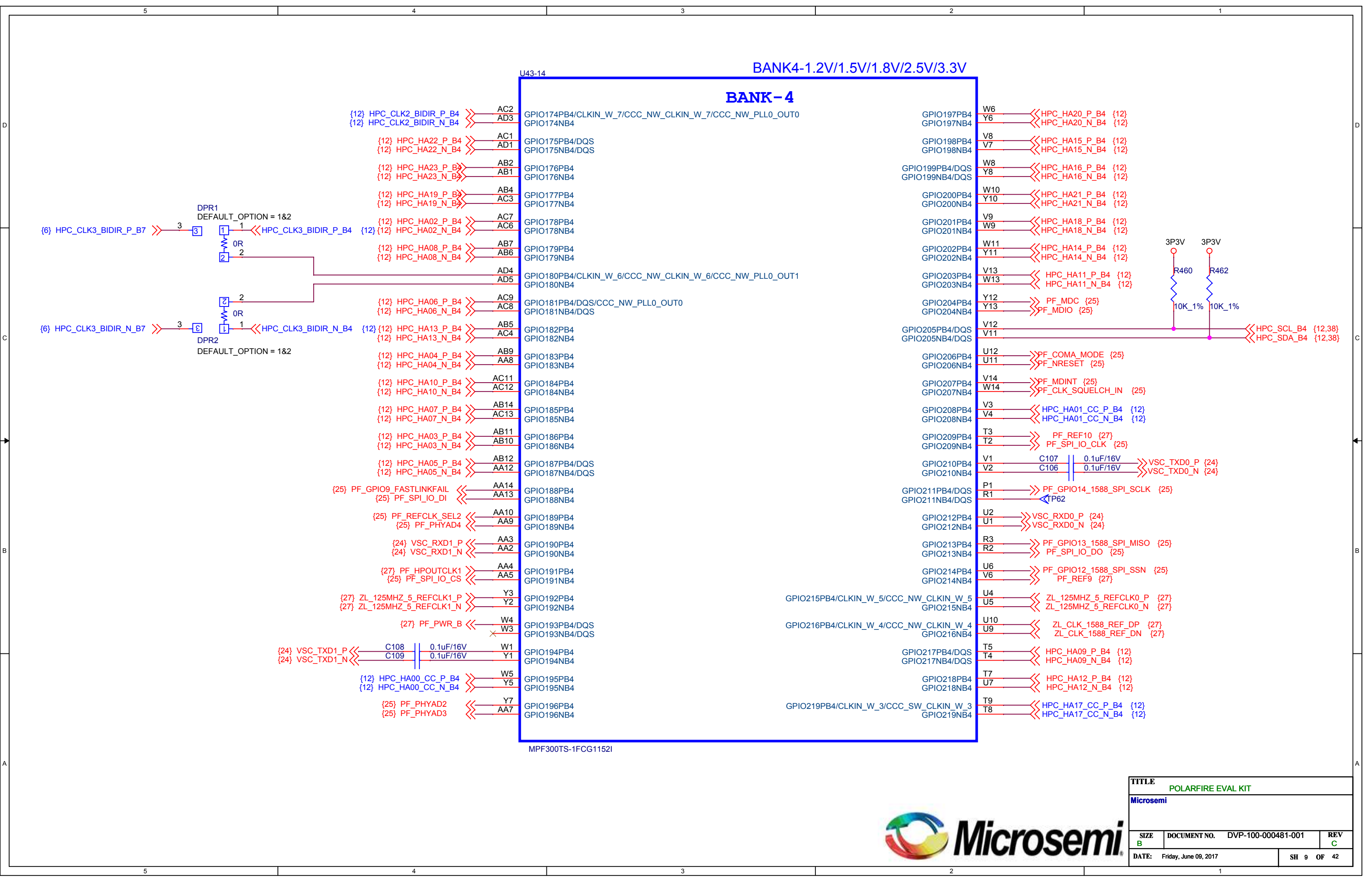
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DDR4 MEMORY-BANK0&7





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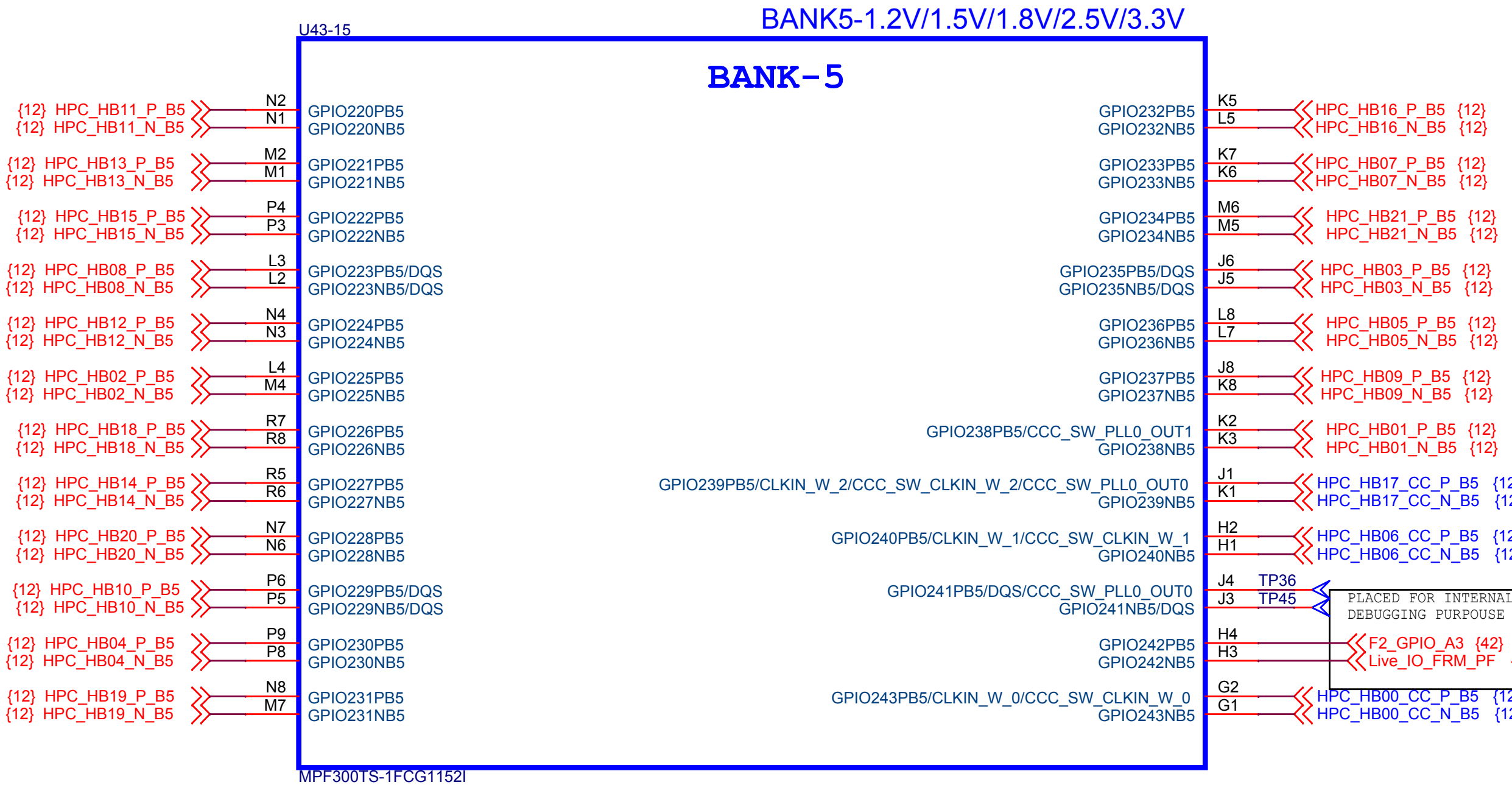
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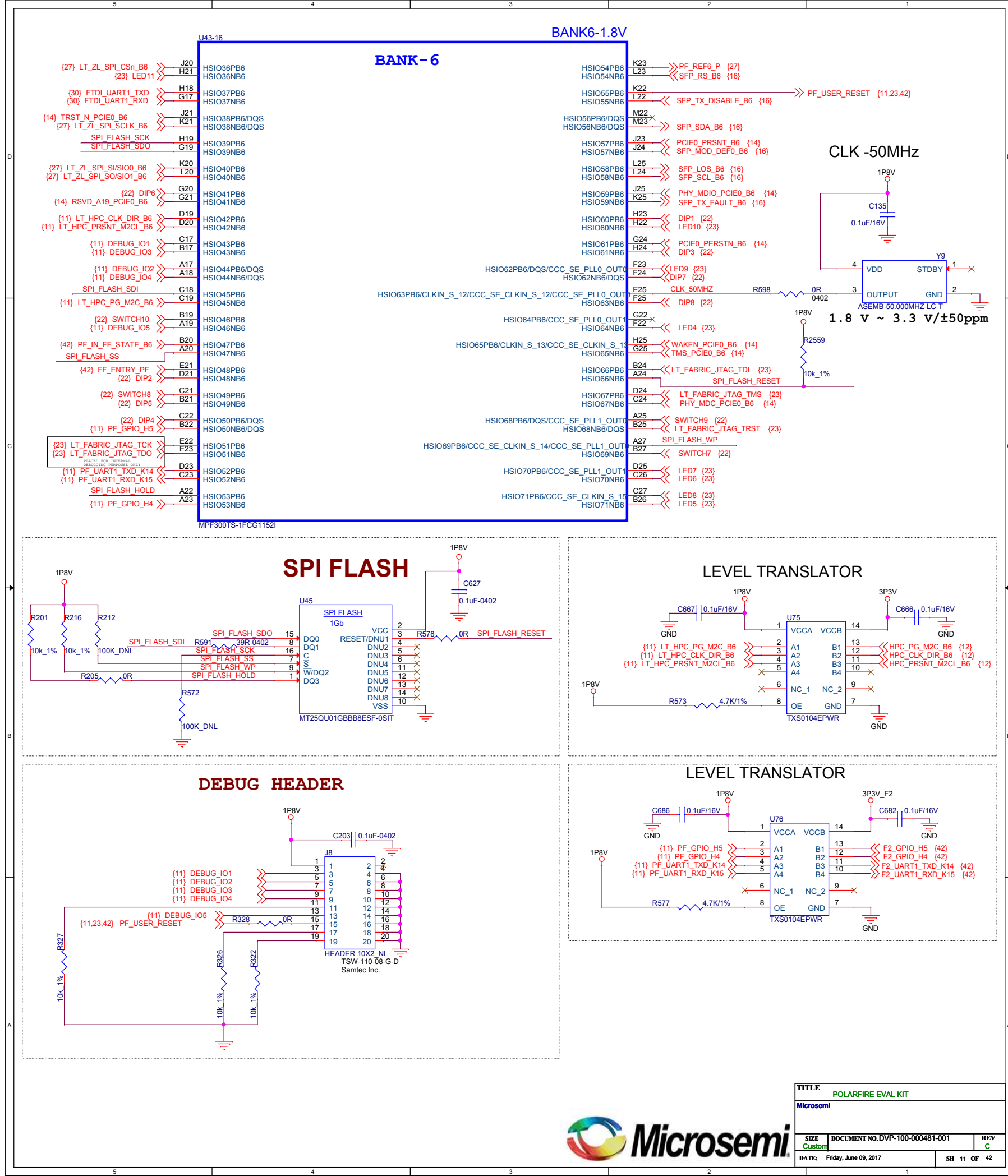
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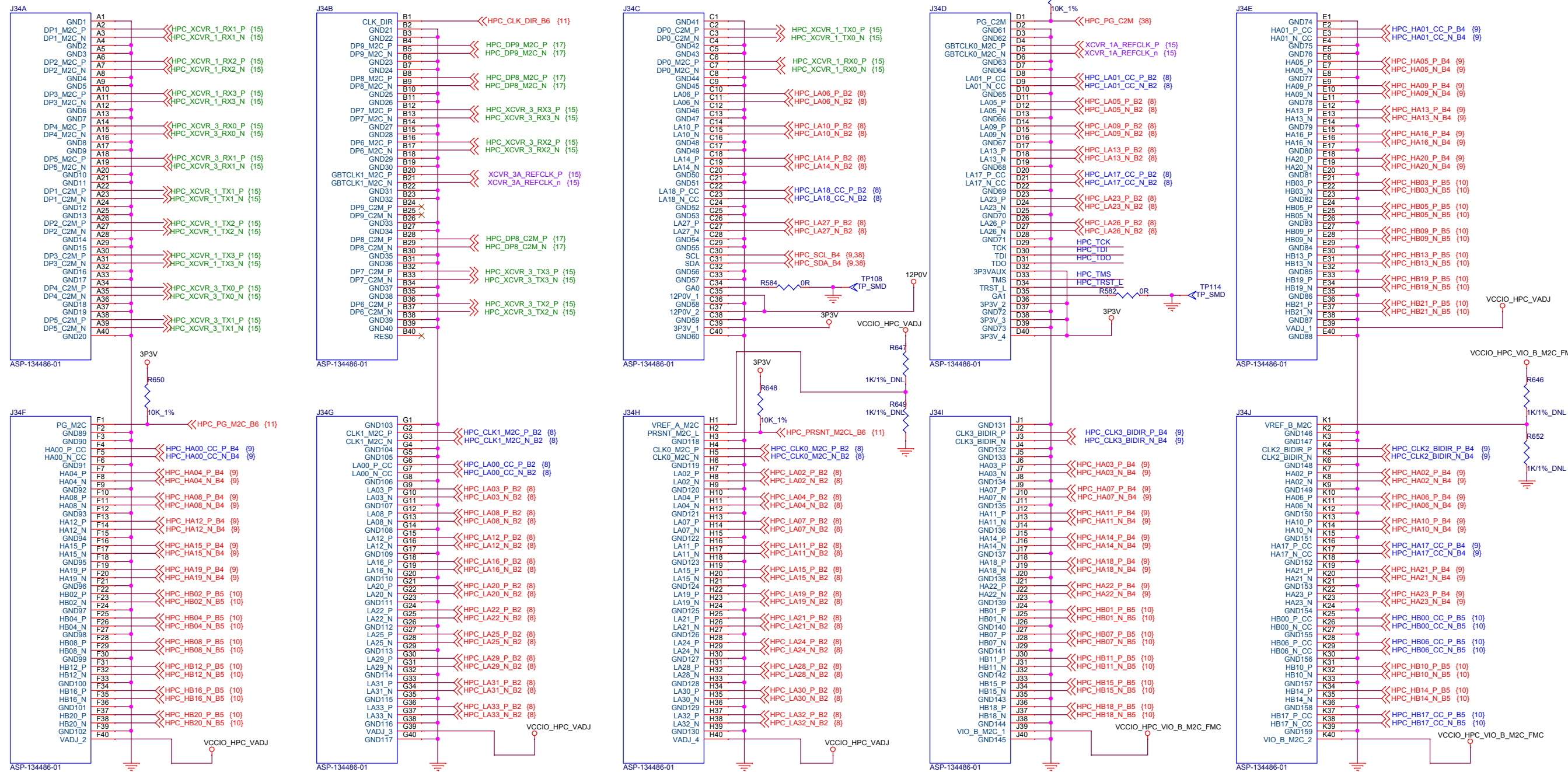
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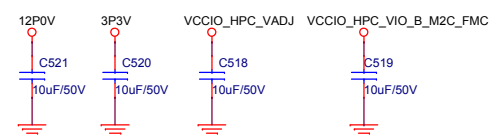
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FMC CONNECTOR(HPC)

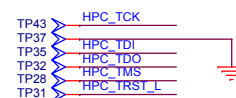


DECOUPLING CAPACITORS



NOTE:

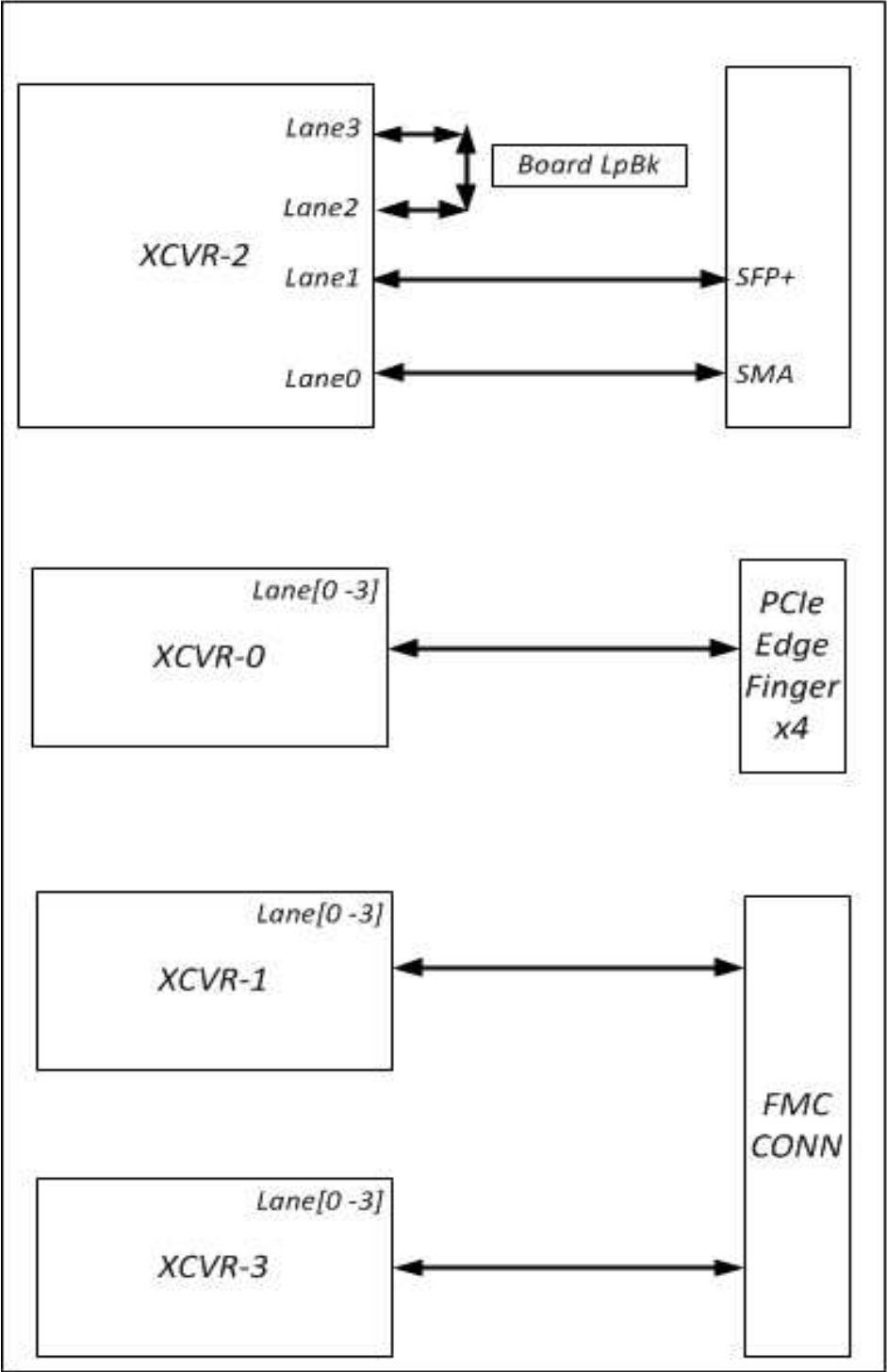
- 1.FMC HPC LA ,HA and HB bank IO's support maximum of 3.3V.
- 2.The Supporting Voltages of FMC HPC(VCCIO_HPC_VADJ) are 1.2V,1.5V,1.8V, 2.5V and 3.3V.



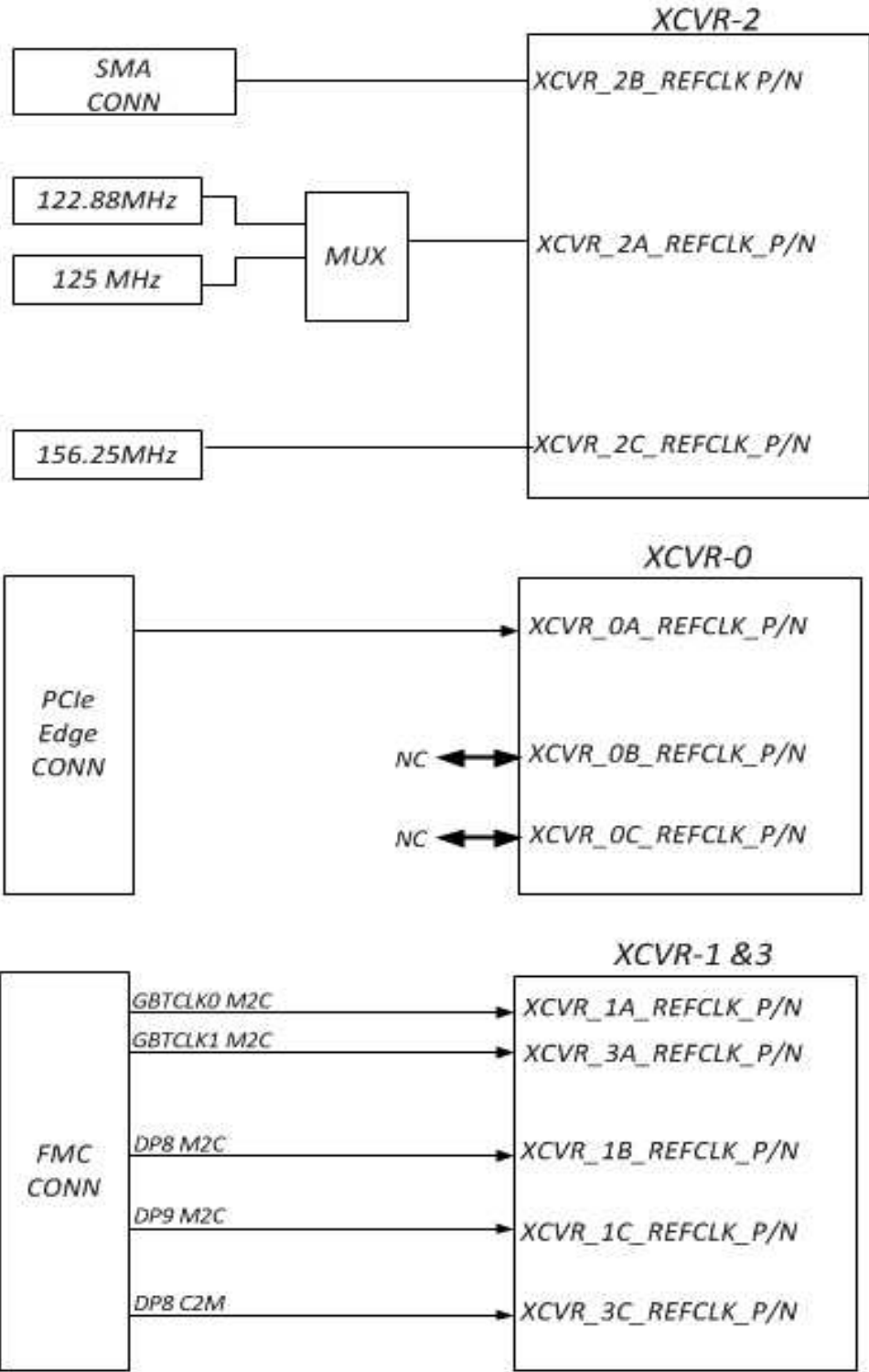
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TRANSCEIVER BLOCK DIAGRAM

Transceiver Block Allocations

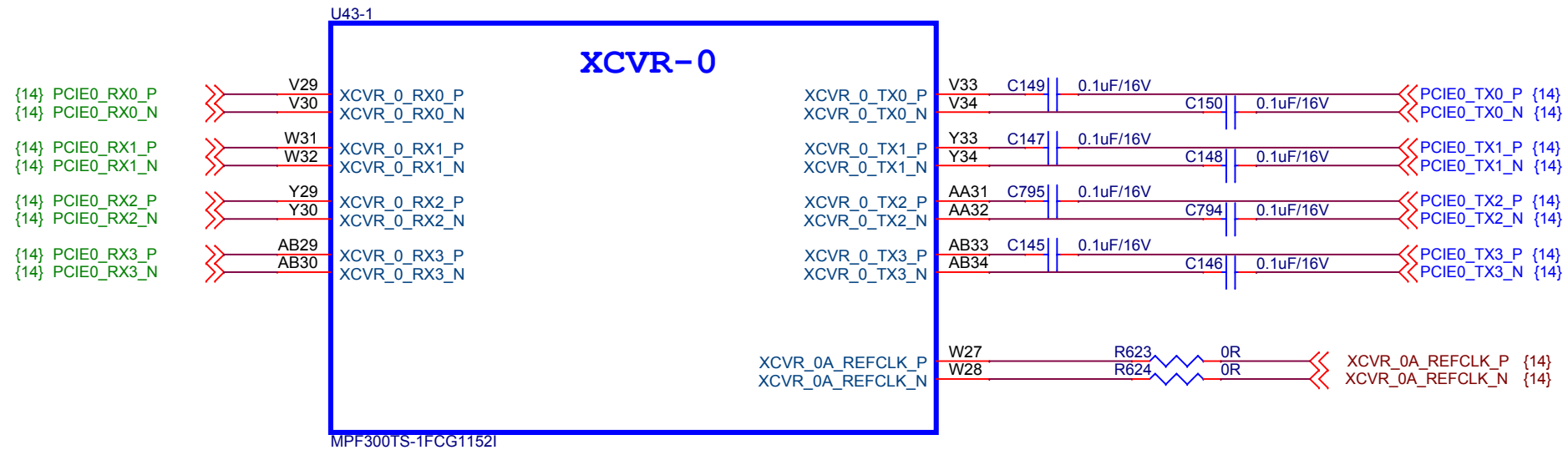


Transceiver Blocks clock scheme

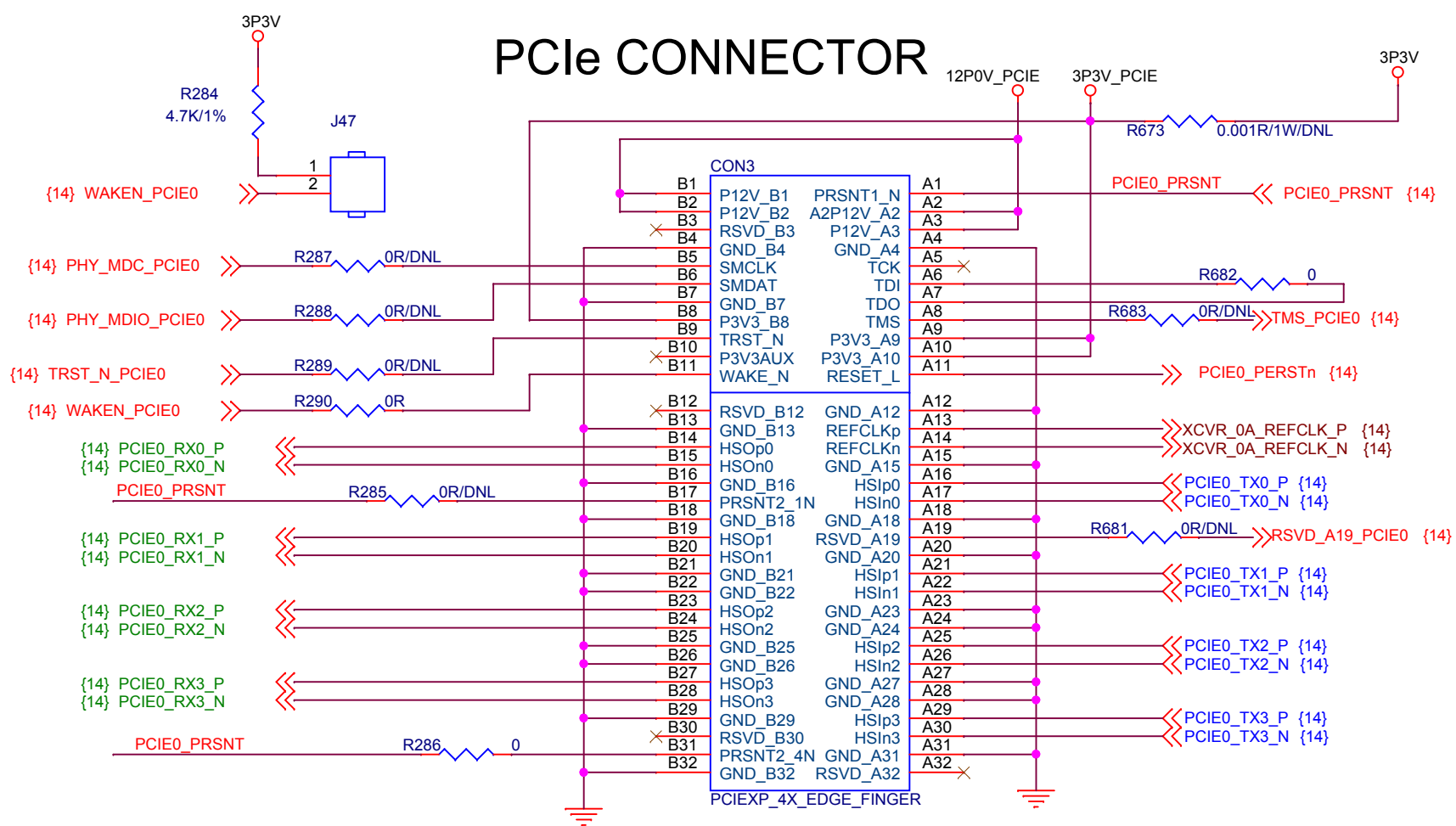


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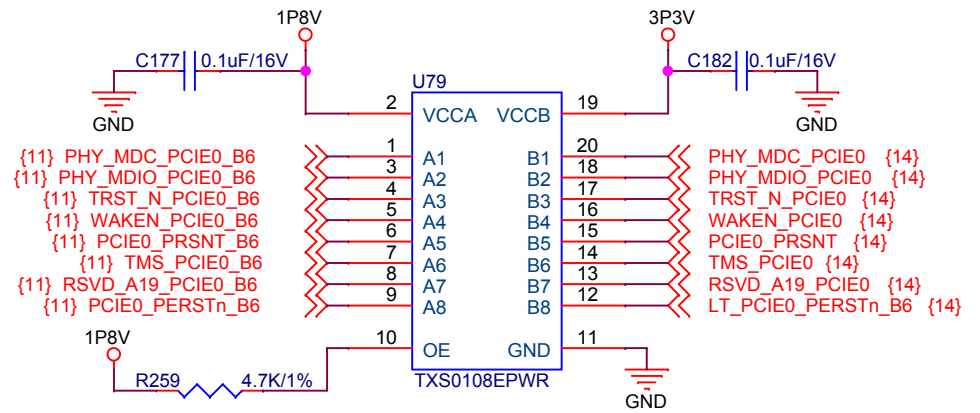
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PCIe CONNECTOR

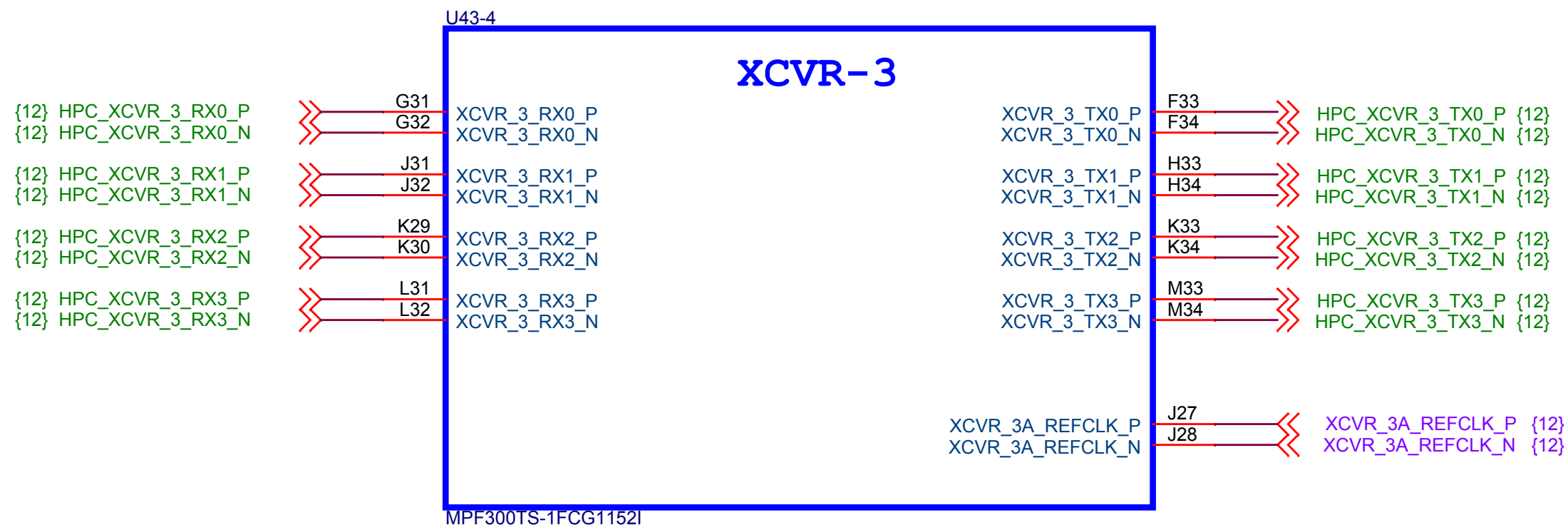
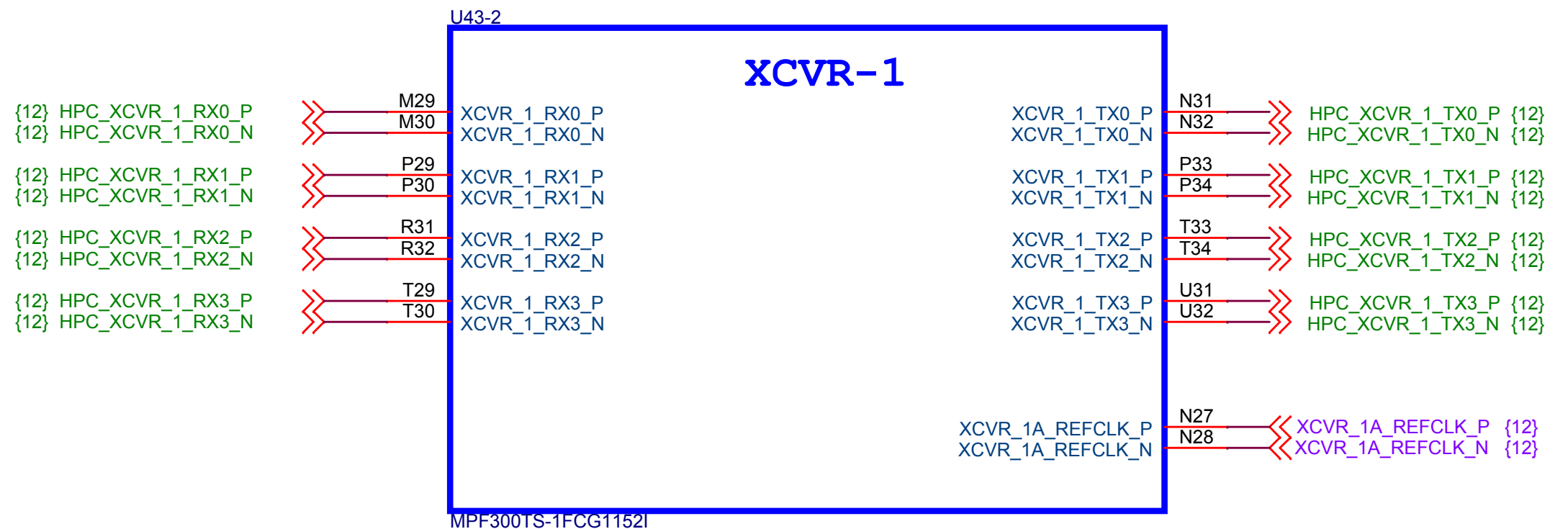


LEVEL TRANSLATOR



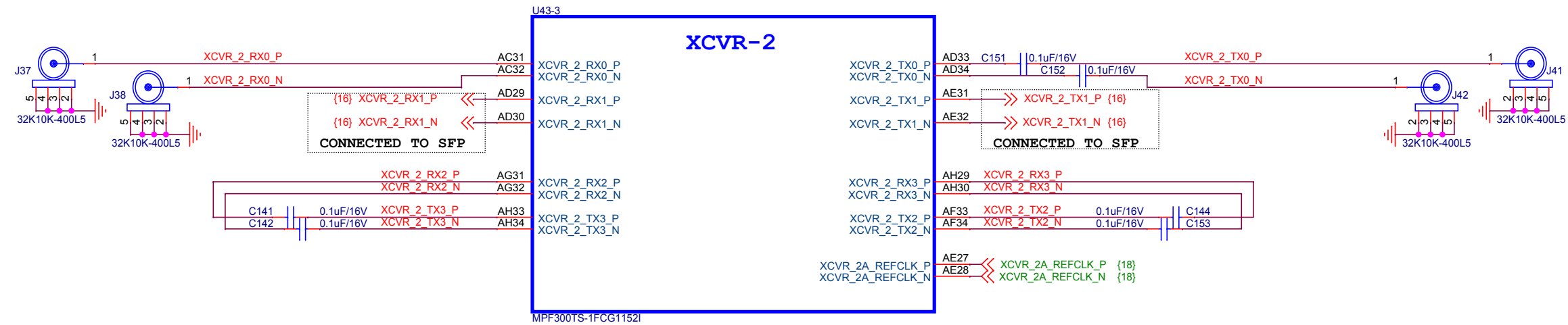
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TRANSCEIVER-1 & TRANSCEIVER-3

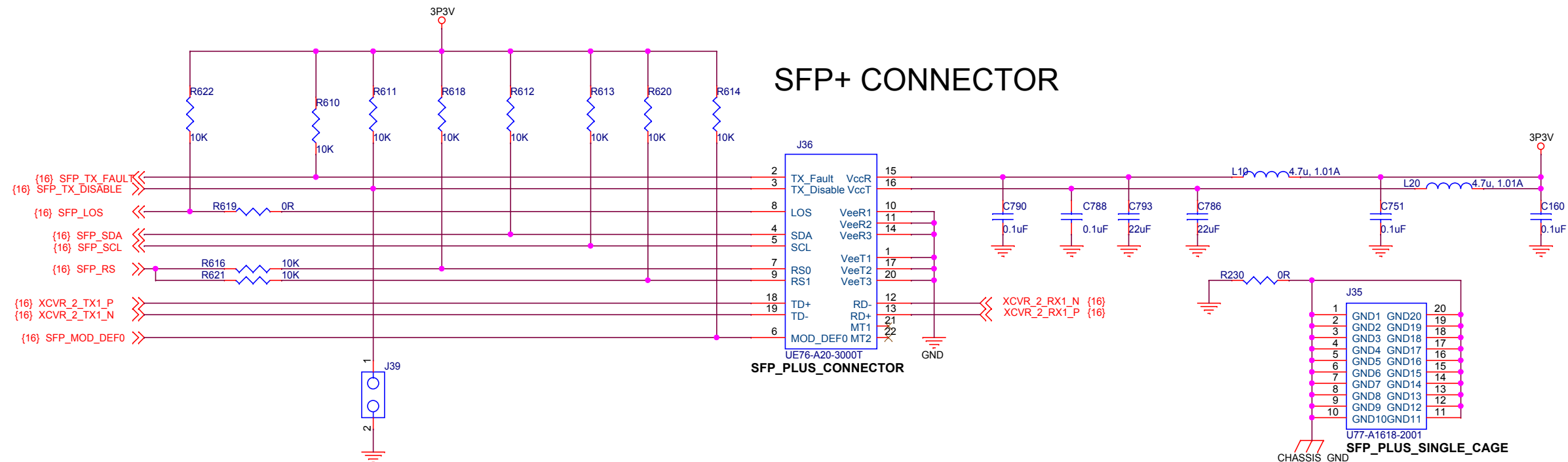


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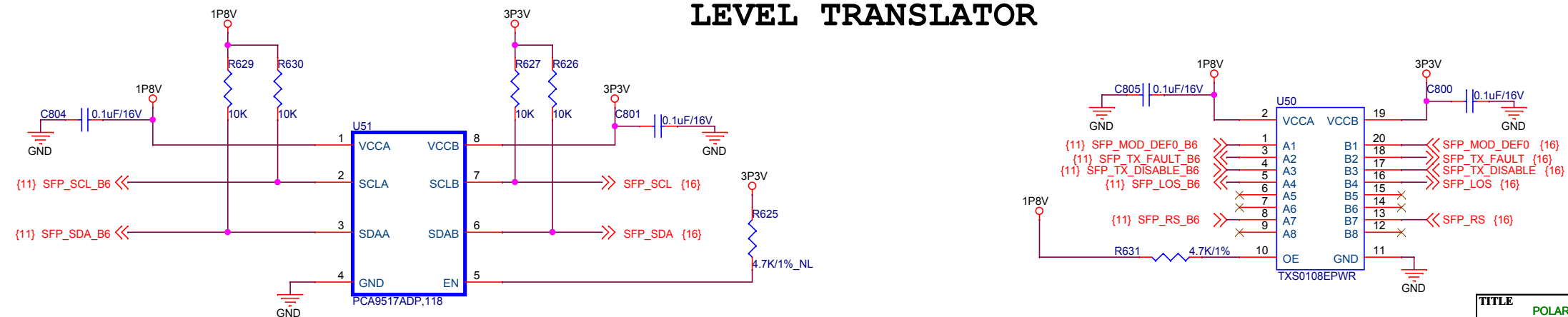
TRANSCEIVER 2



SFP+ CONNECTOR



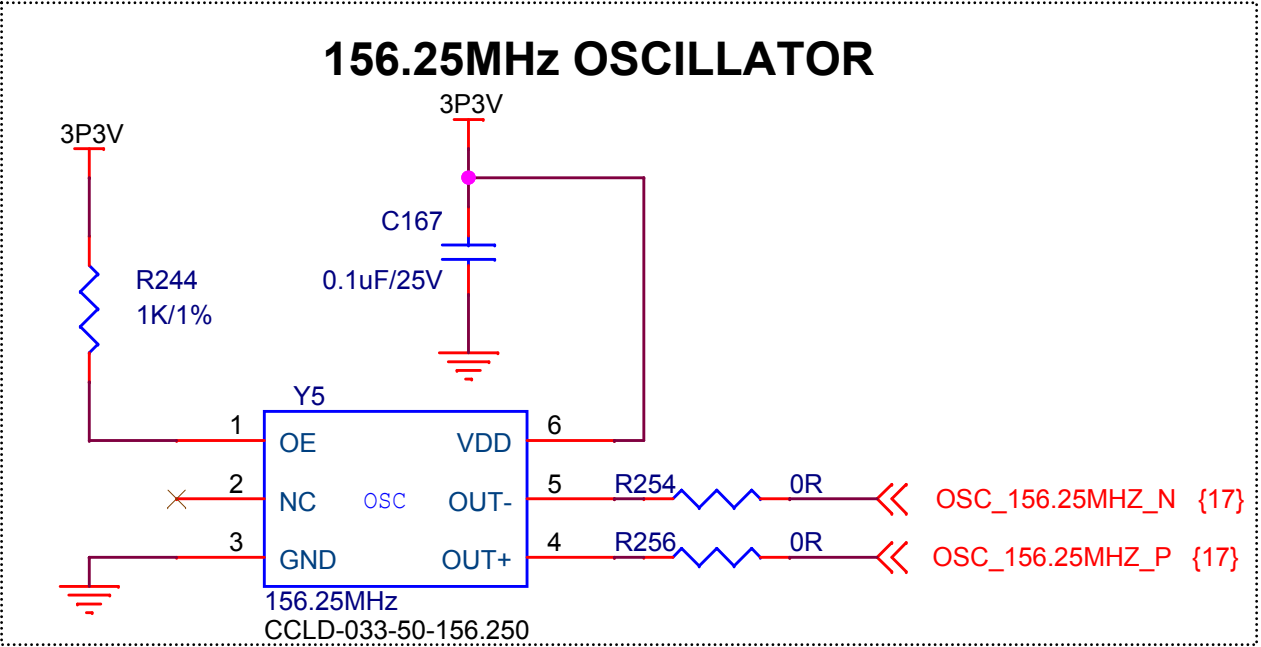
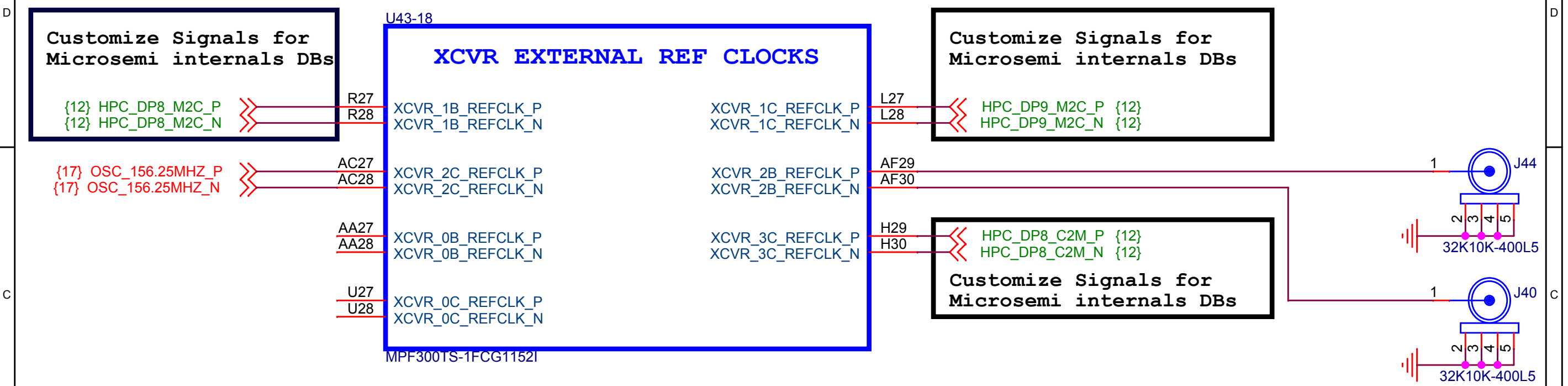
LEVEL TRANSLATOR



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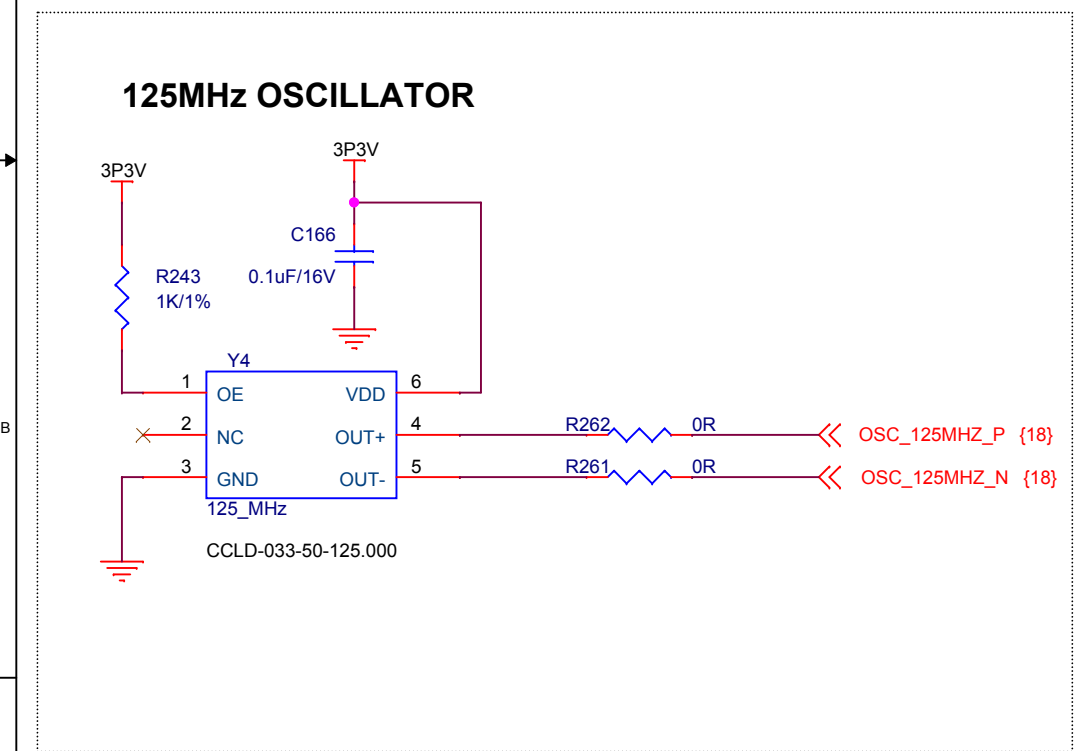
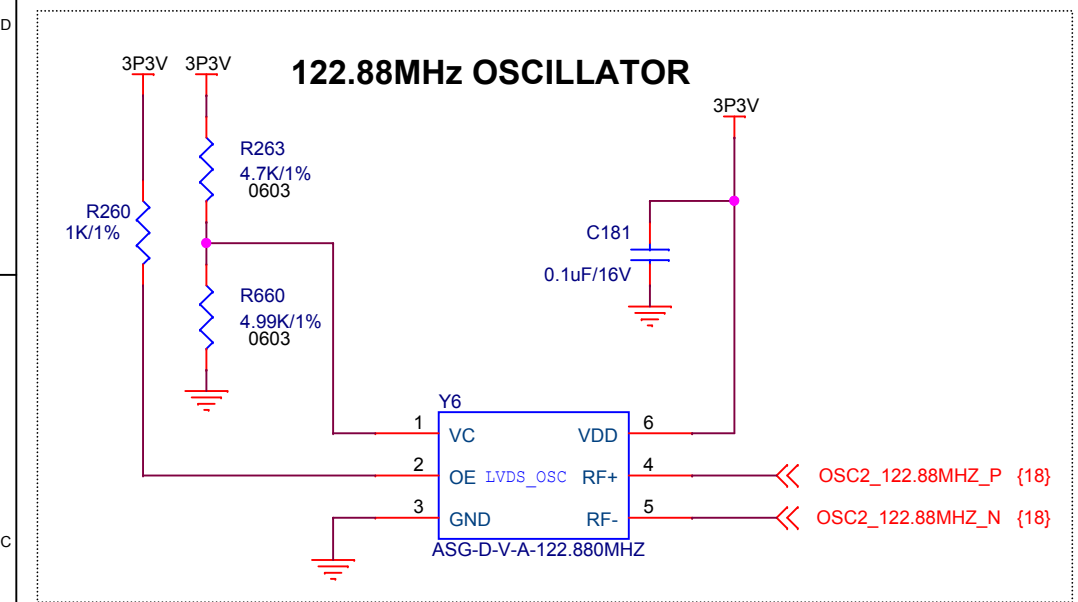


TRANSCEIVER EXTERNAL REF CLOCKS

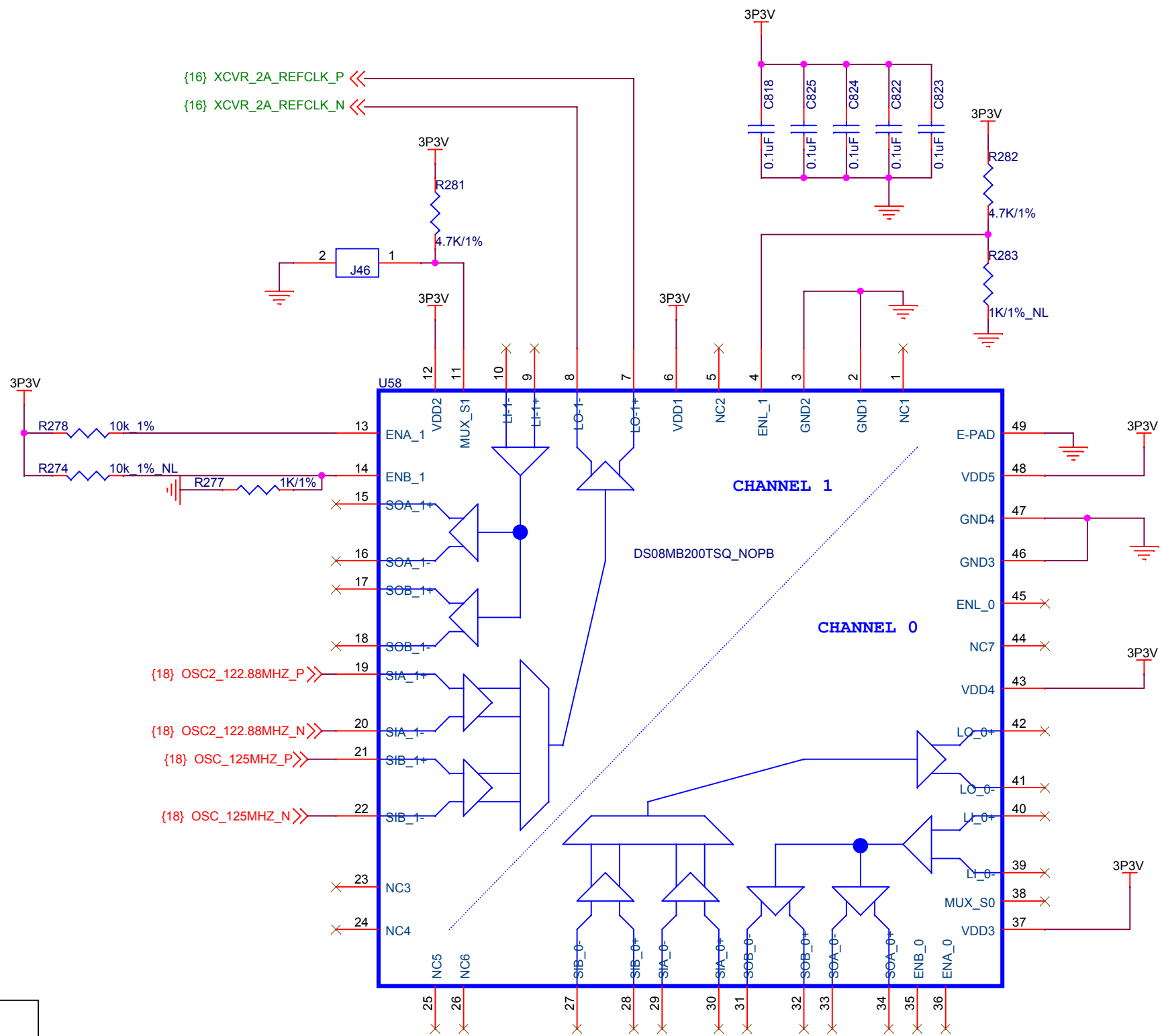


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TRANSCEIVER REF CLOCKS

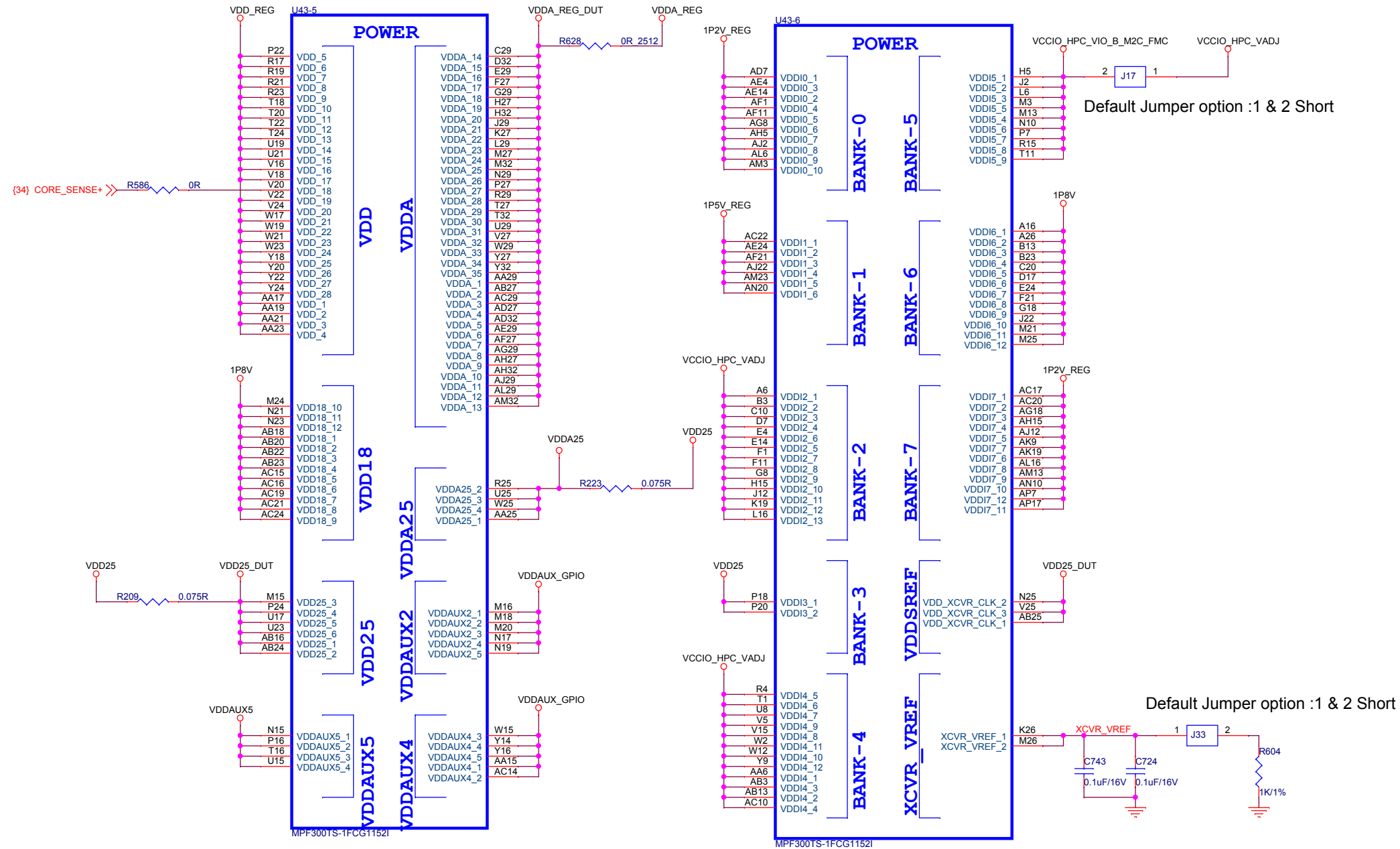


CHANNEL1		
ENL1	MUX S1-J46	XCVR_2A_INT_REFCLK
L	X	X
H	L	Osc-125MHz
H	H	Osc2-122.88MHz

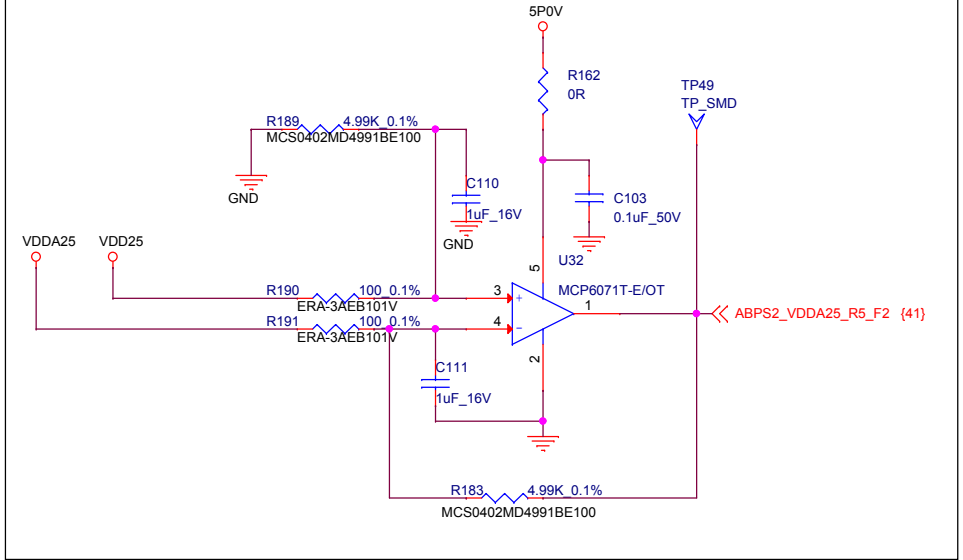


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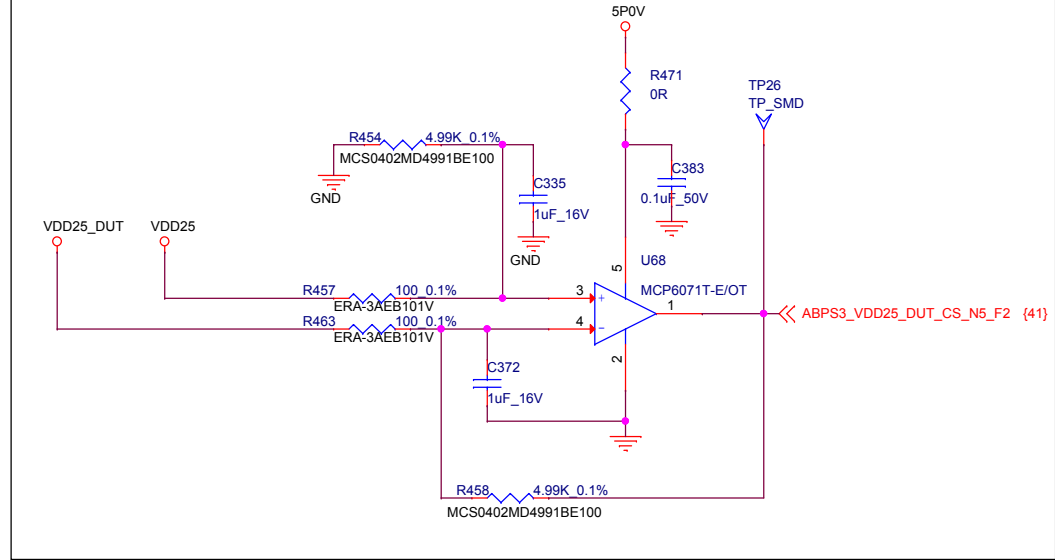
POWER CONNECTIONS



VDDA25 CURRENT SENSE CIRCUIT

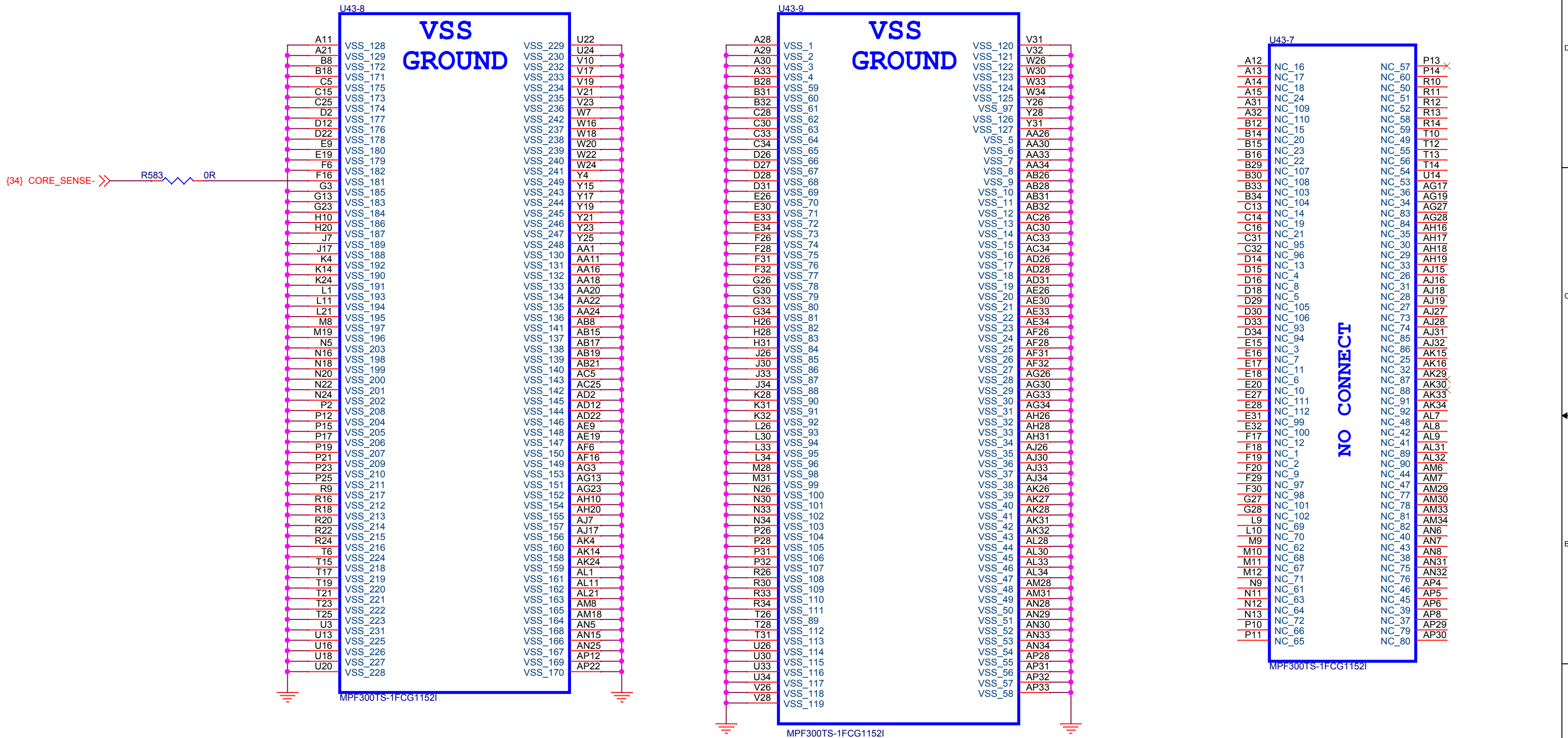


VDD25 CURRENT SENSE CIRCUIT



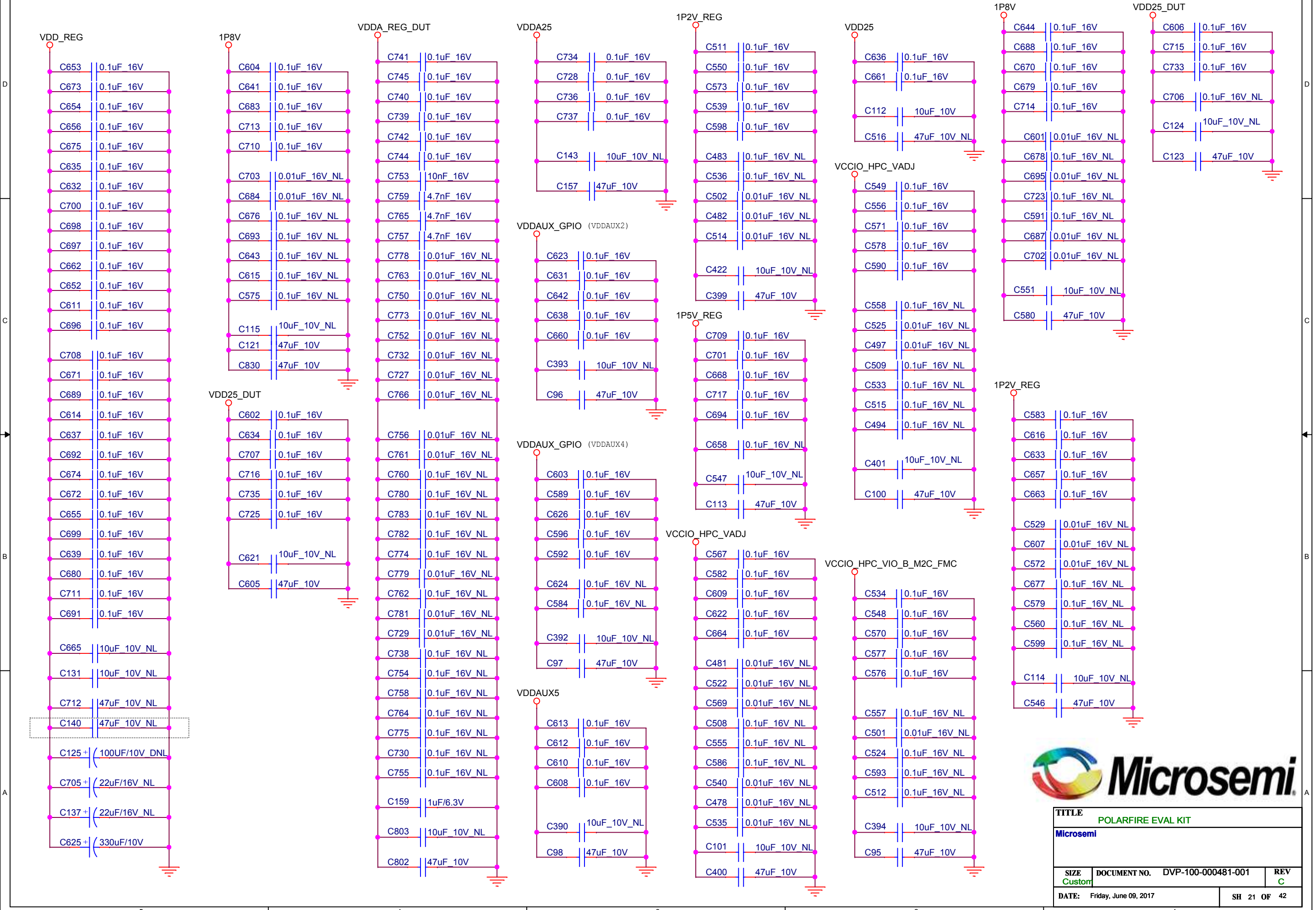
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GROUND & NC CONNECTION



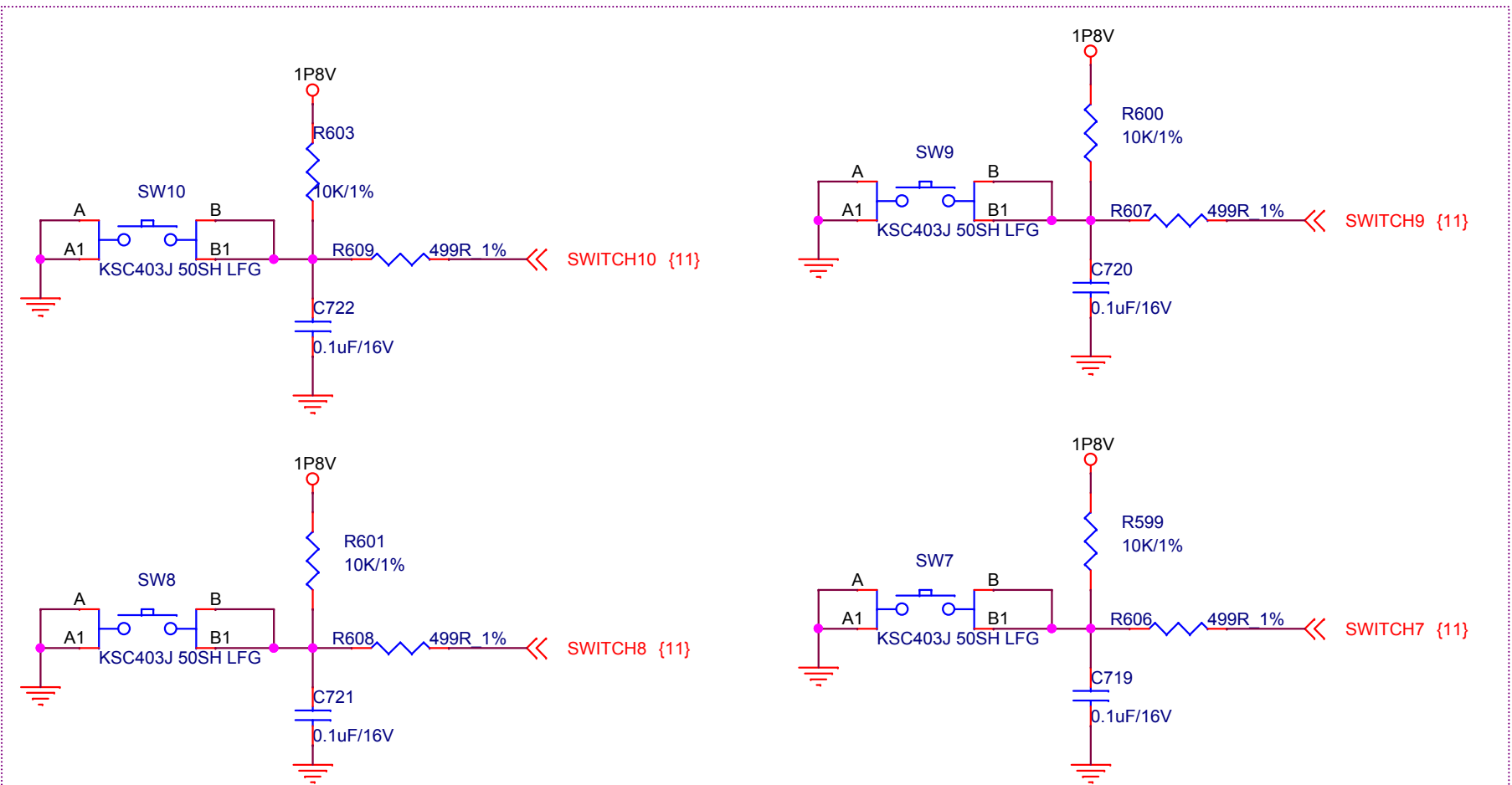
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DECOUPLING CAPACITORS



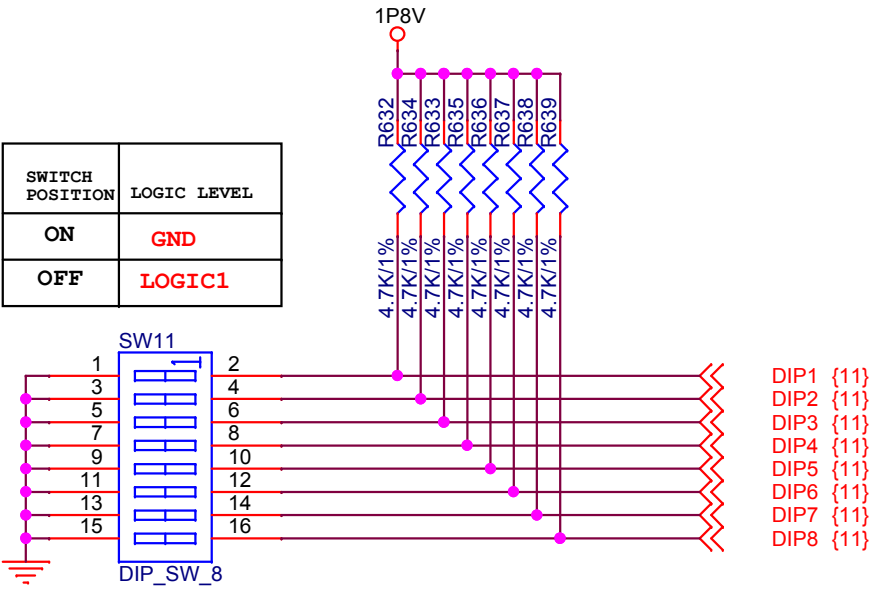
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DEBUG CIRCUITRY



PUSH BUTTON SWITCH CONNECTION TABLE

NET NAME	FPGA PIN NO	FPGA PIN NAME	BANK
SWITCH10	B19	HSIO46PB6	BANK-6
SWITCH8	C21	HSIO49PB6	BANK-6
SWITCH9	A25	HSIO68PB6/DQS/CCC_SE_PLL1_OUT0	BANK-6
SWITCH7	B27	HSIO69NB6	BANK-6

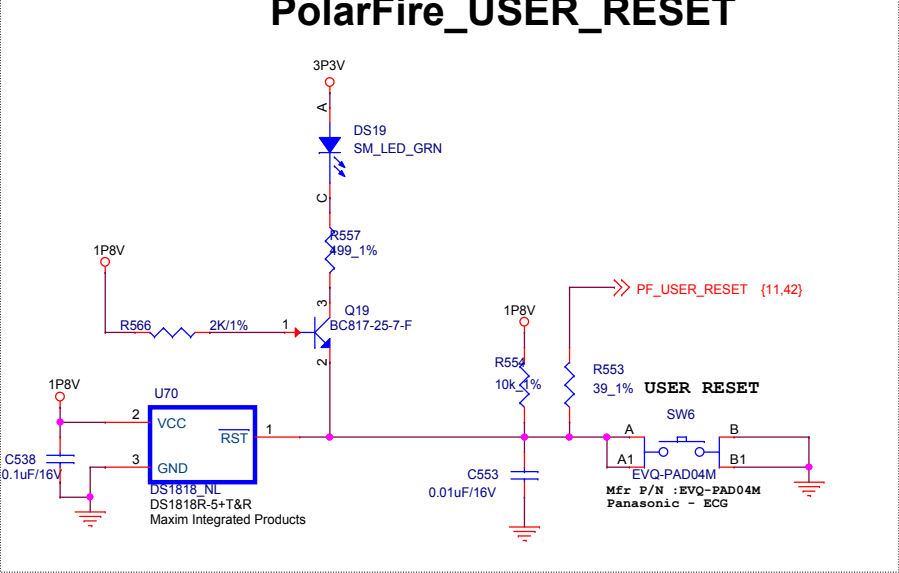
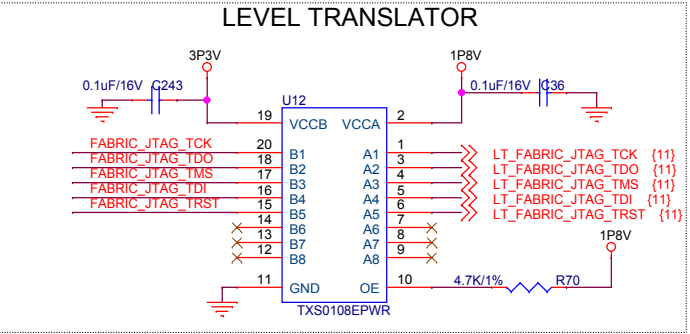
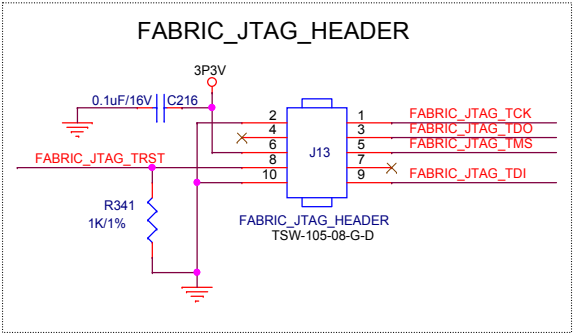
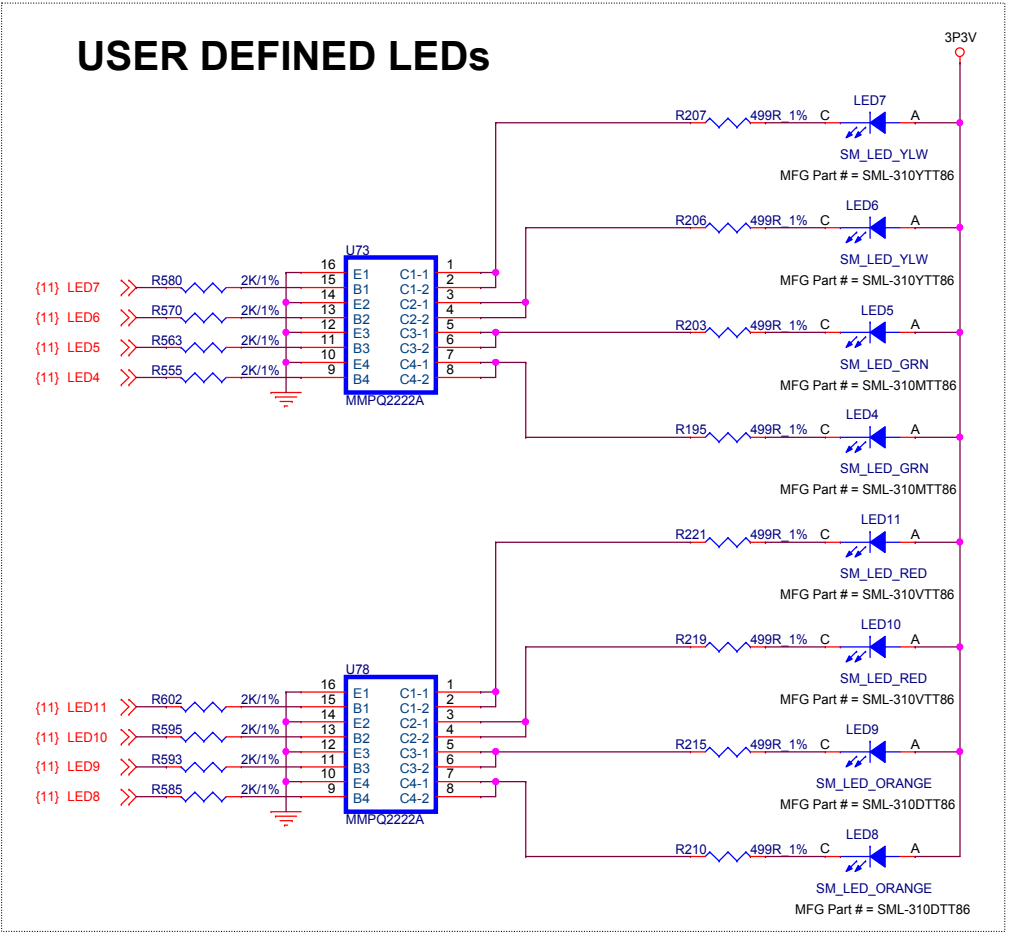
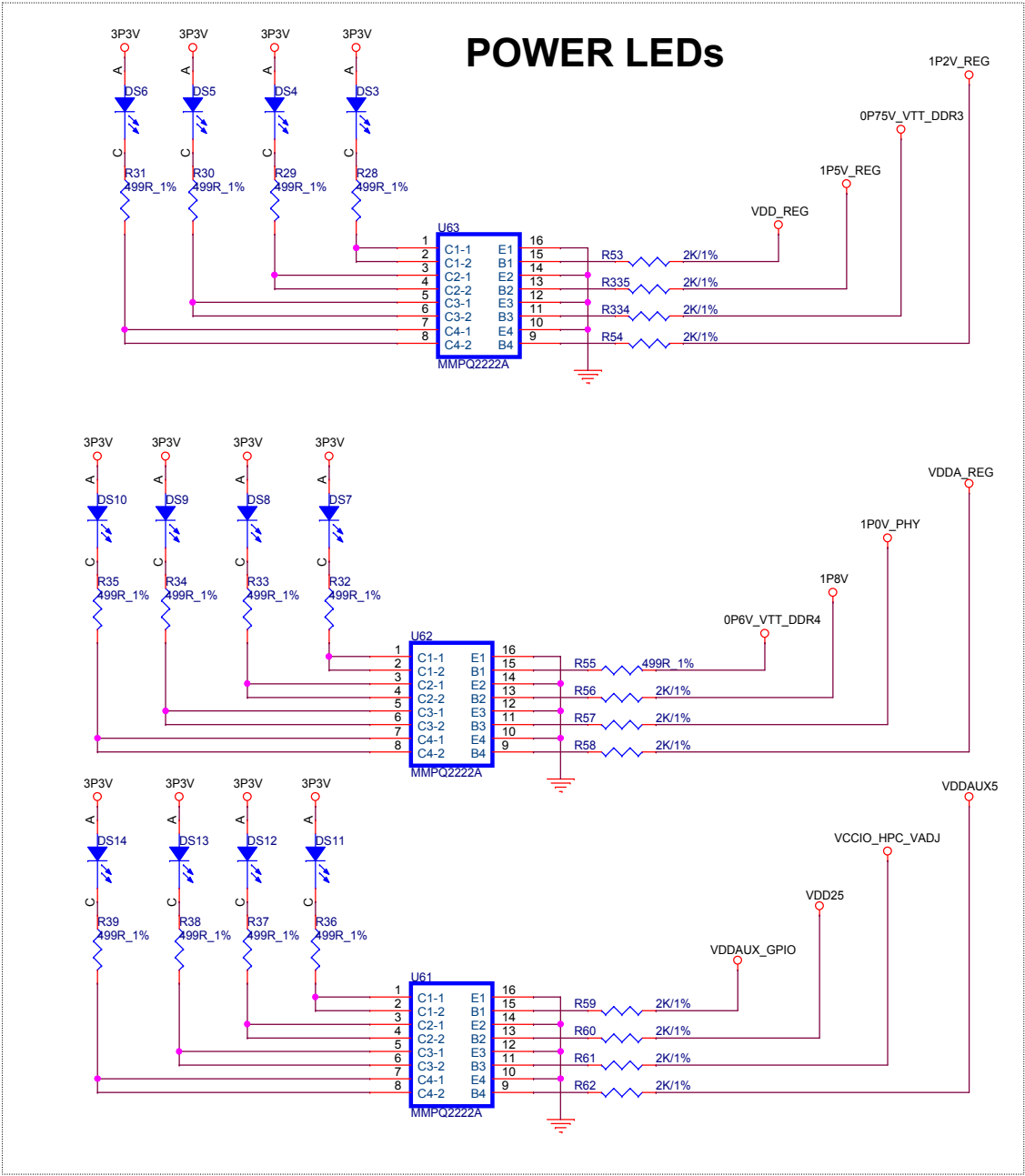


DIP SWITCH CONNECTION TABLE

NET NAME	FPGA PIN NO	FPGA PIN NAME	BANK
DIP1	H23	HSIO60PB6	BANK-6
DIP2	D21	HSIO48NB6	BANK-6
DIP3	H24	HSIO61NB6	BANK-6
DIP4	C22	HSIO50PB6/DQS	BANK-6
DIP5	B21	HSIO49NB6	BANK-6
DIP6	G20	HSIO41PB6	BANK-6
DIP7	F24	HSIO62NB6/DQS	BANK-6
DIP8	F25	HSIO63NB6	BANK-6

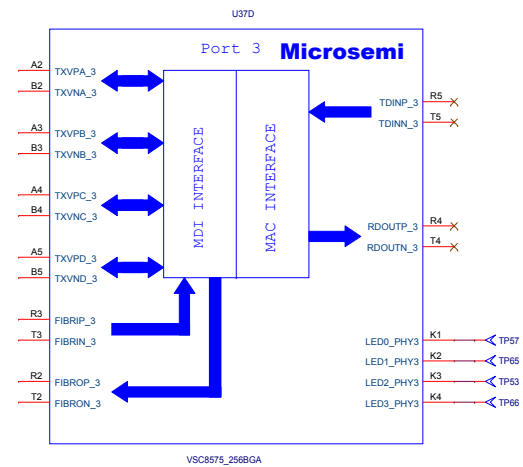
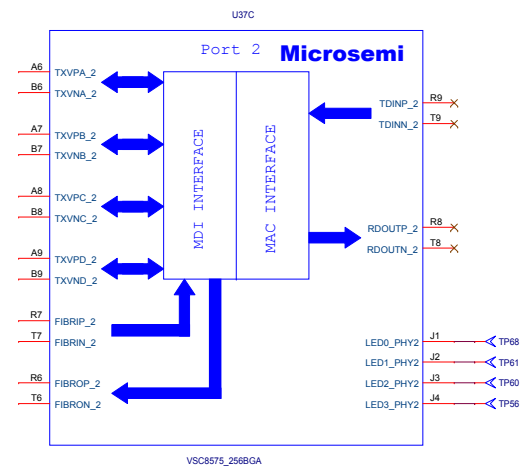
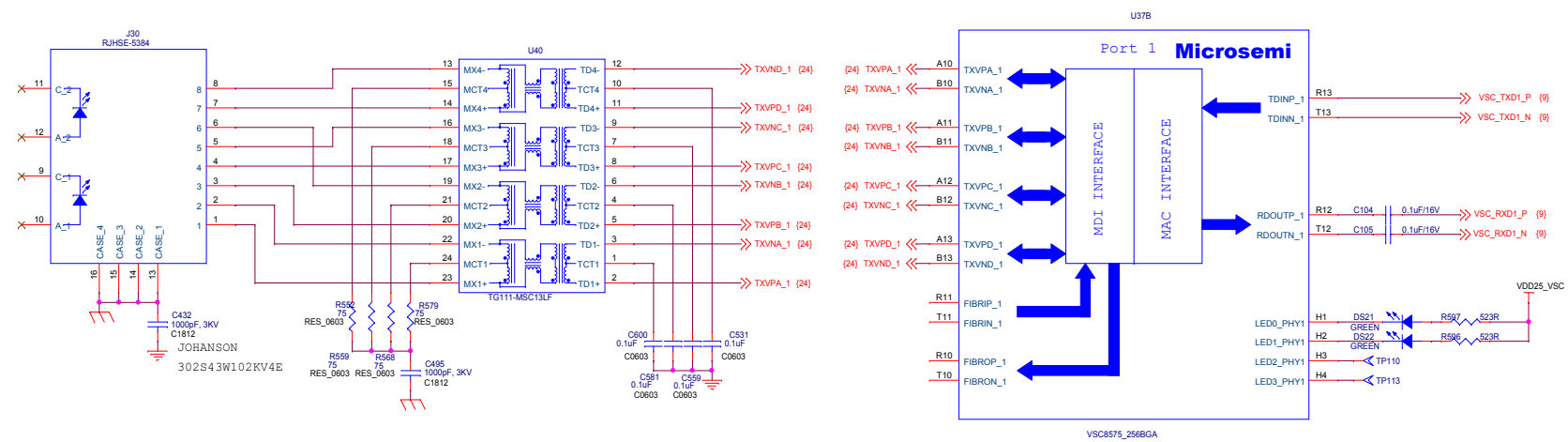
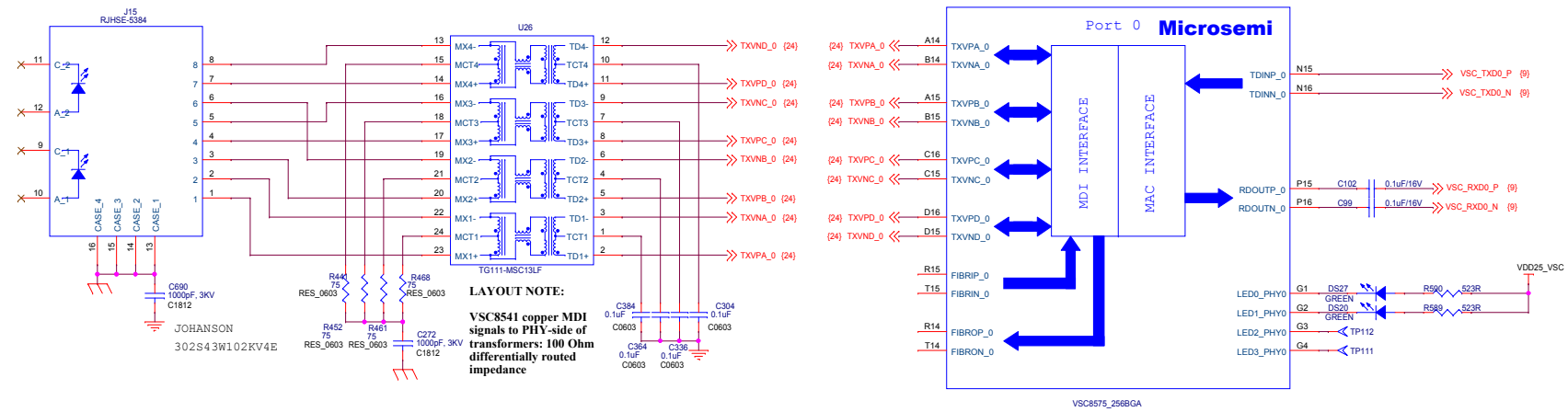


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1588 Solution - VSC8575-MAC INTERFACE

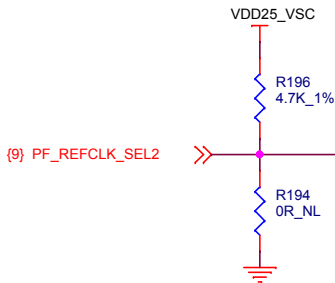


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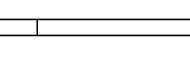
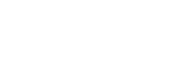
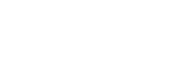
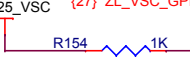
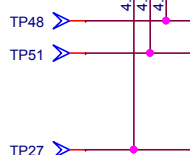
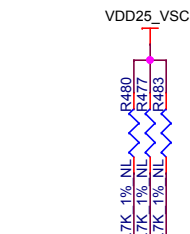
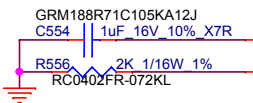
1588 Solution - VSC8575 CONNECTIONS

LAYOUT NOTE FOR RC CIRCUIT R556 & C554:

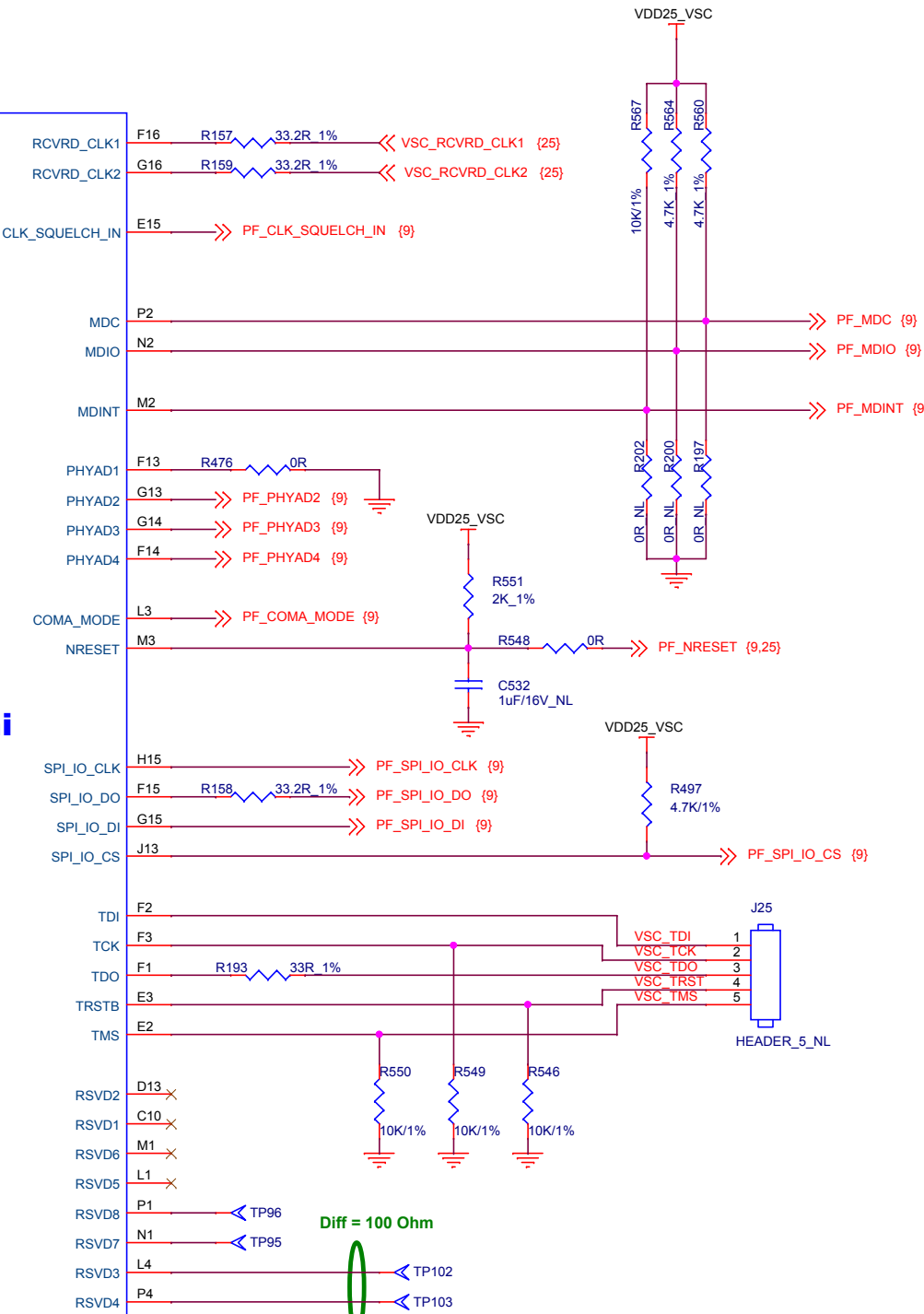
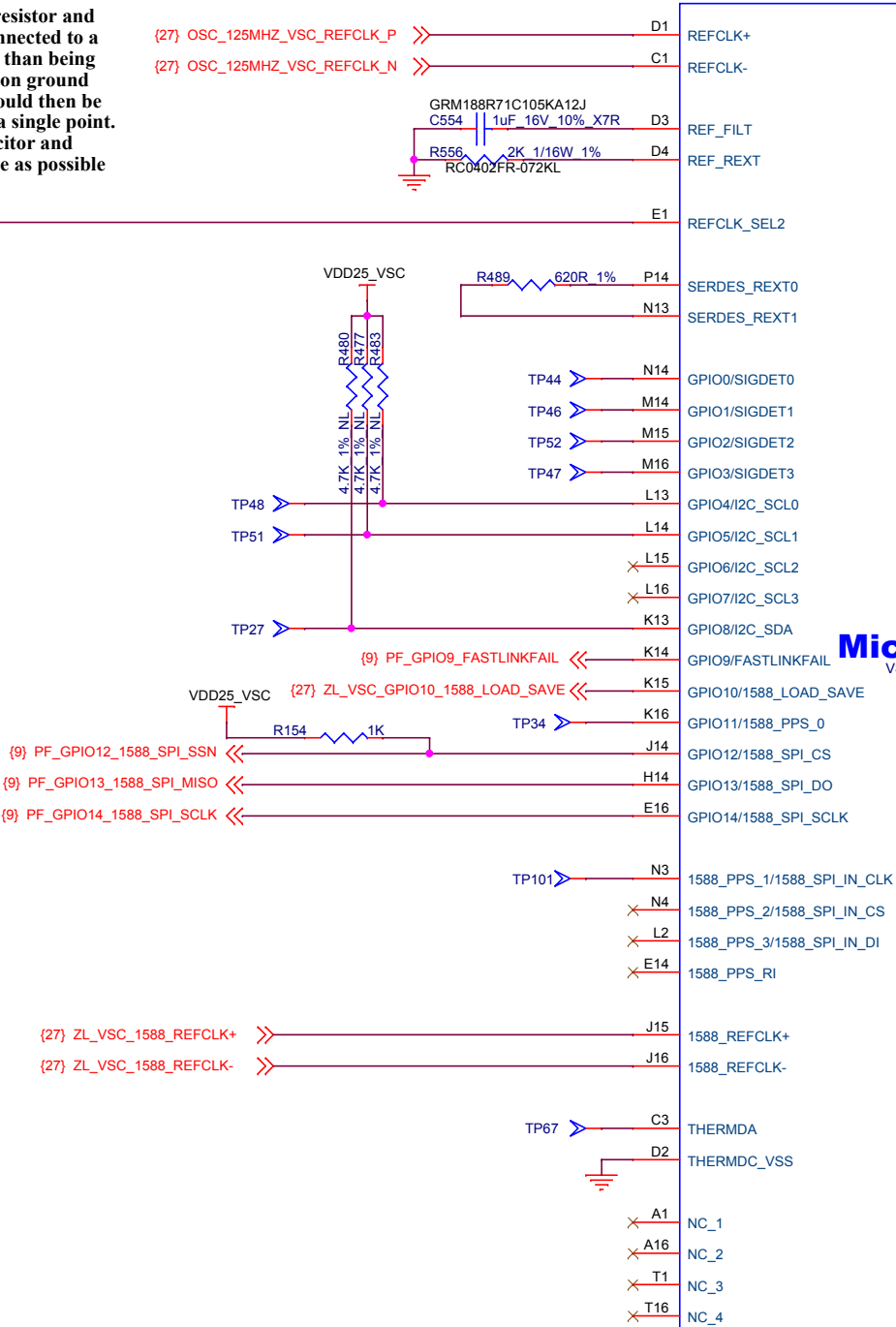
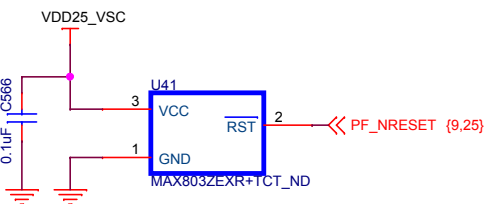
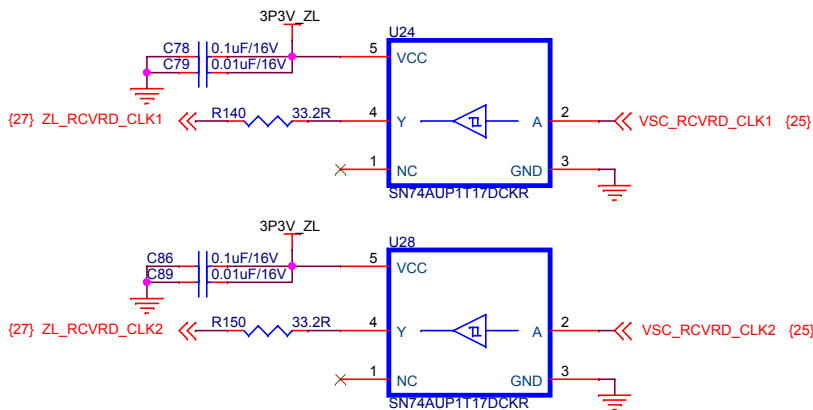
The ground connections of the resistor and the capacitor should each be connected to a shared PCB signal trace, rather than being connected individually to common ground plane. This PCB signal trace should then be connected to a ground plane at a single point. In addition, the reference capacitor and resistor should be placed as close as possible to the VSC8575



{27} OSC_125MHZ_VSC_REFCLK_P
{27} OSC_125MHZ_VSC_REFCLK_N

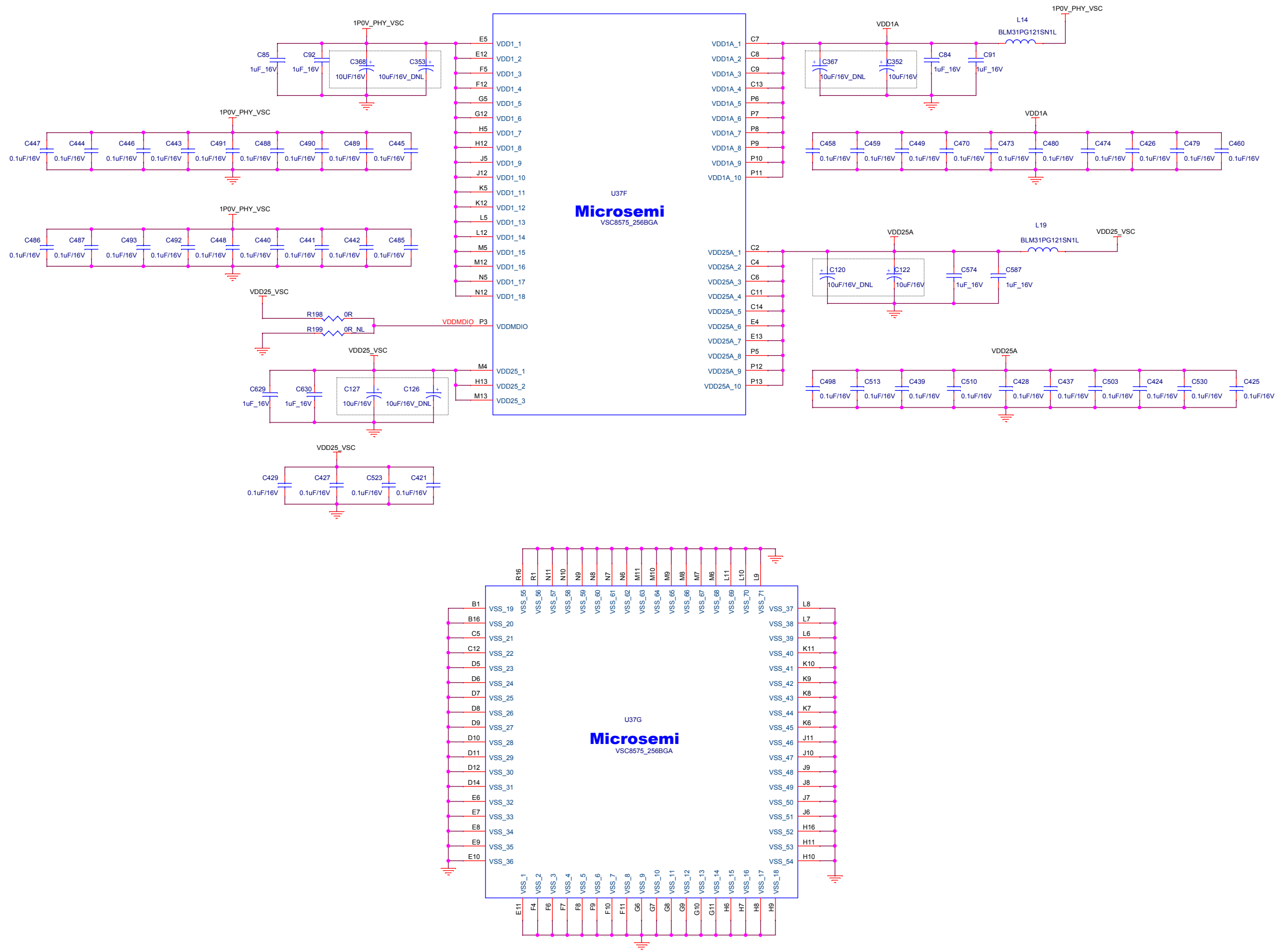


BUFFER CIRCUIT CONNECTION



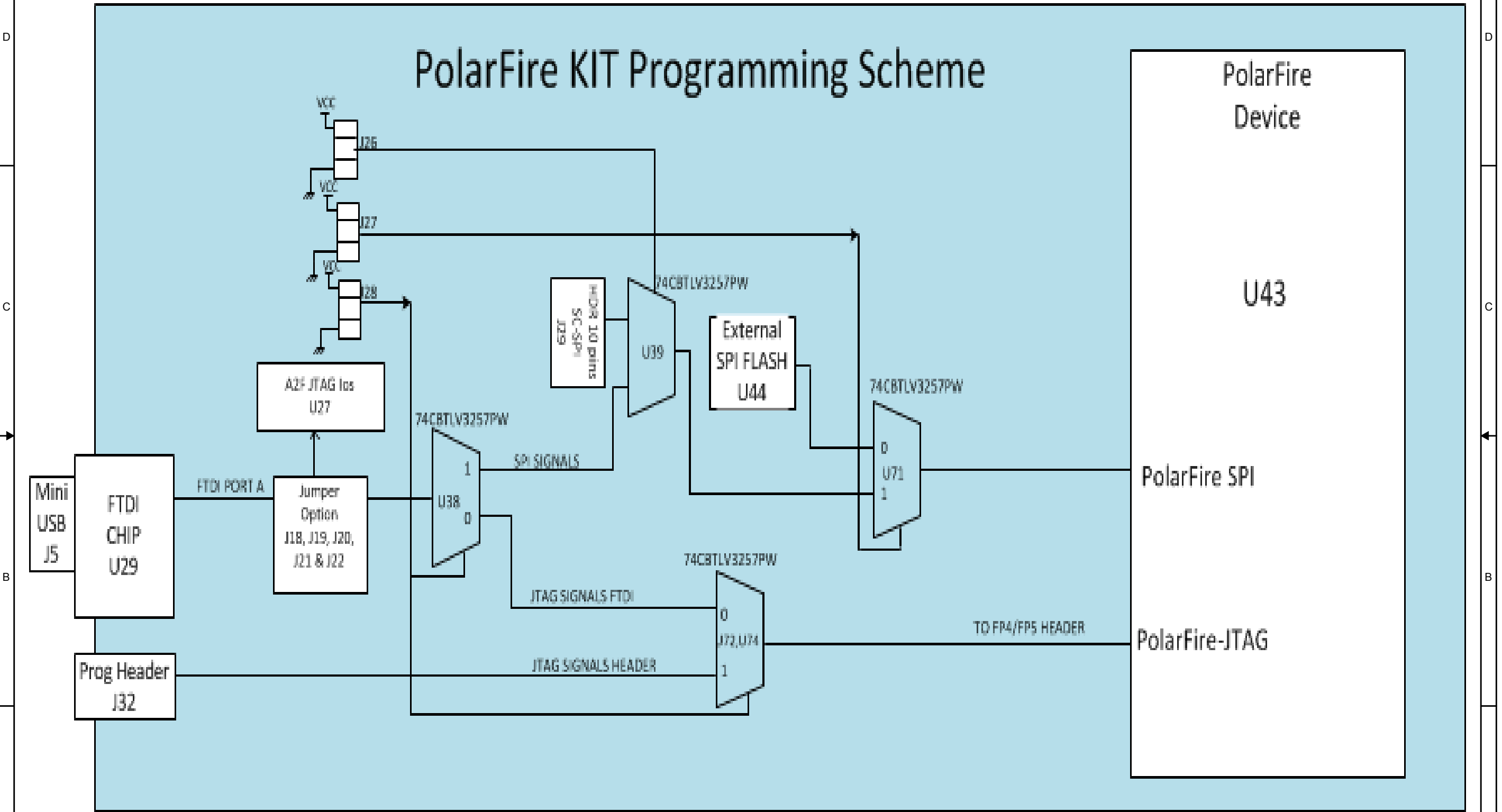
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1588 Solution - VSC8575-POWER & GROUND



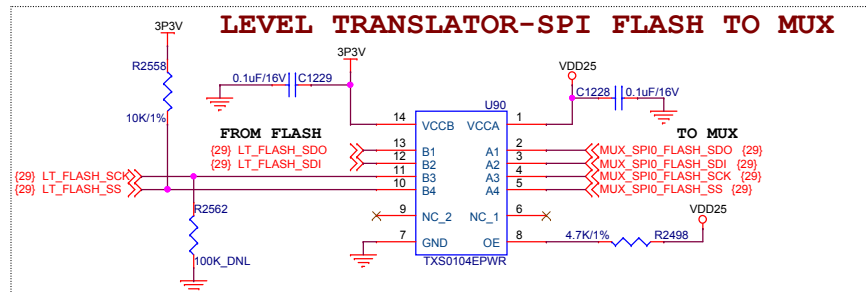
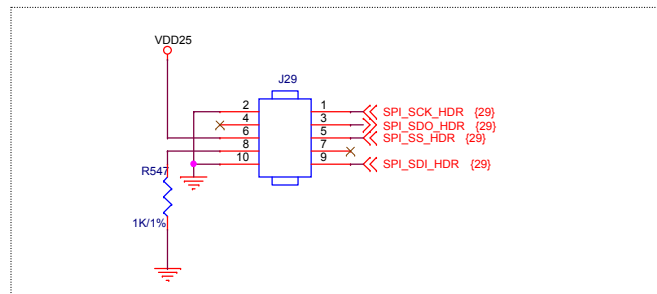
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PROGRAMMING SCHEME BLOCK DIAGRAM

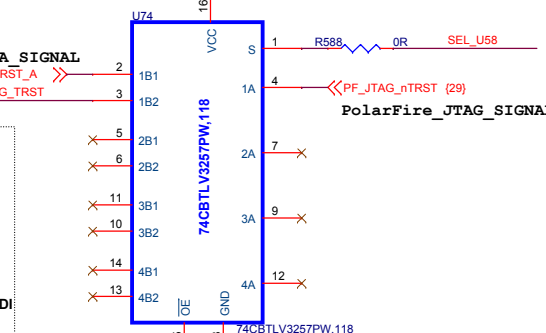
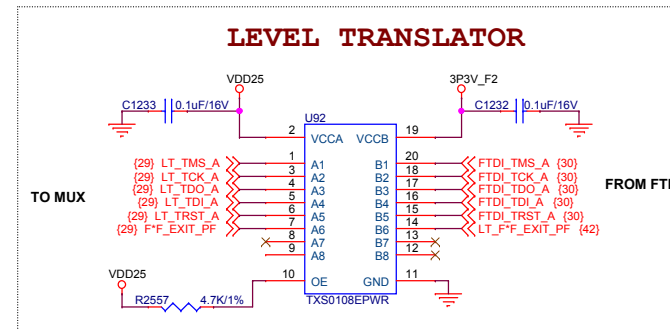
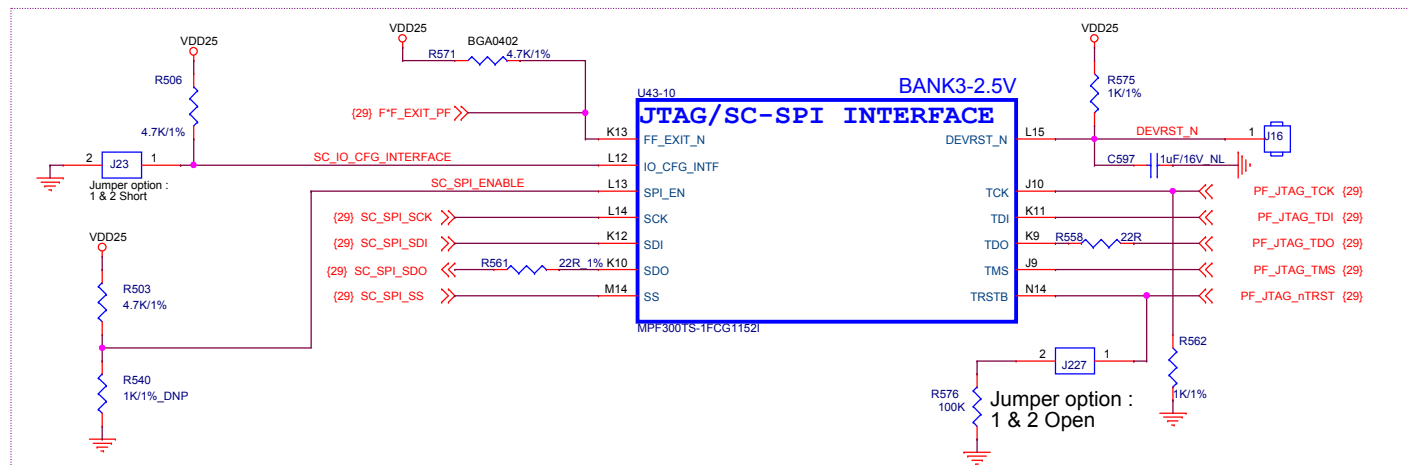
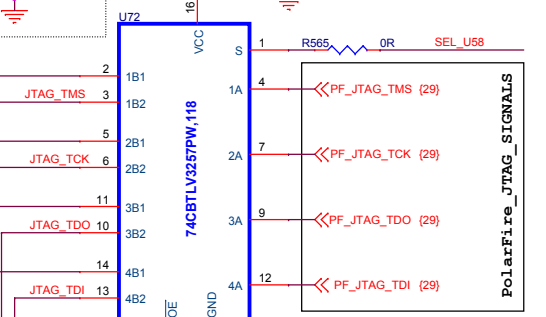
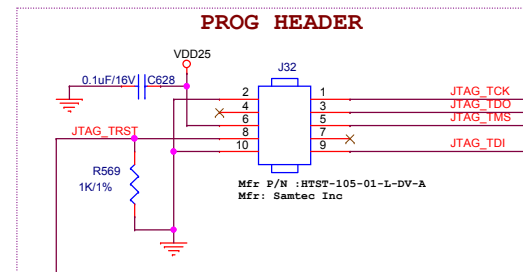
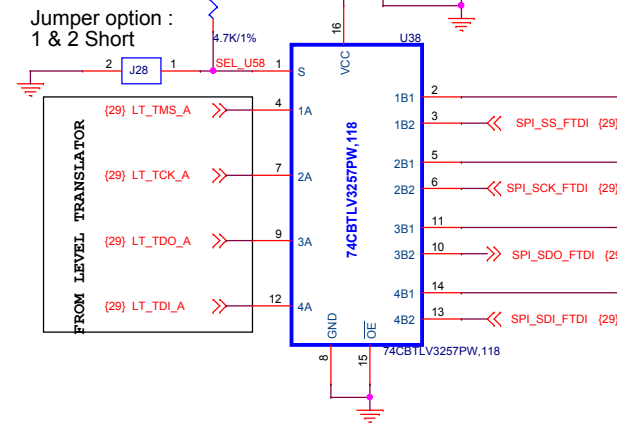
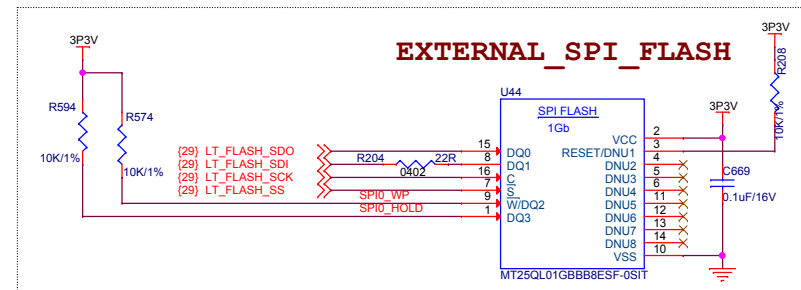
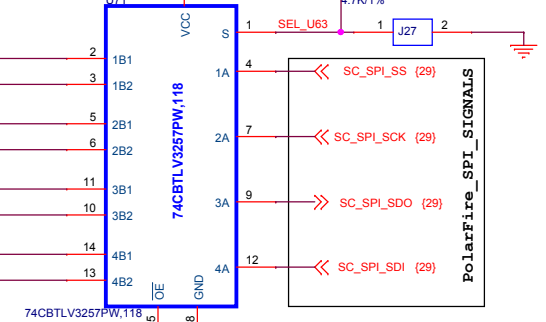
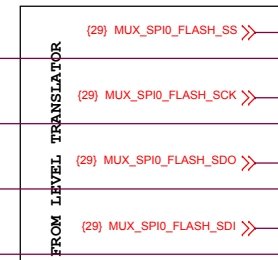
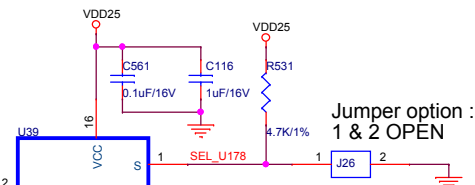
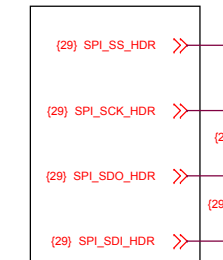


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POLARFIRE EVAL KIT			
Microsemi			
SIZE	DOCUMENT NO.	REV	
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PROGRAMMING SCHEME

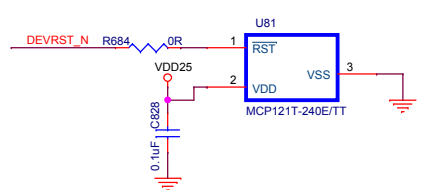


EXTERNAL_SPI_SIGNALS



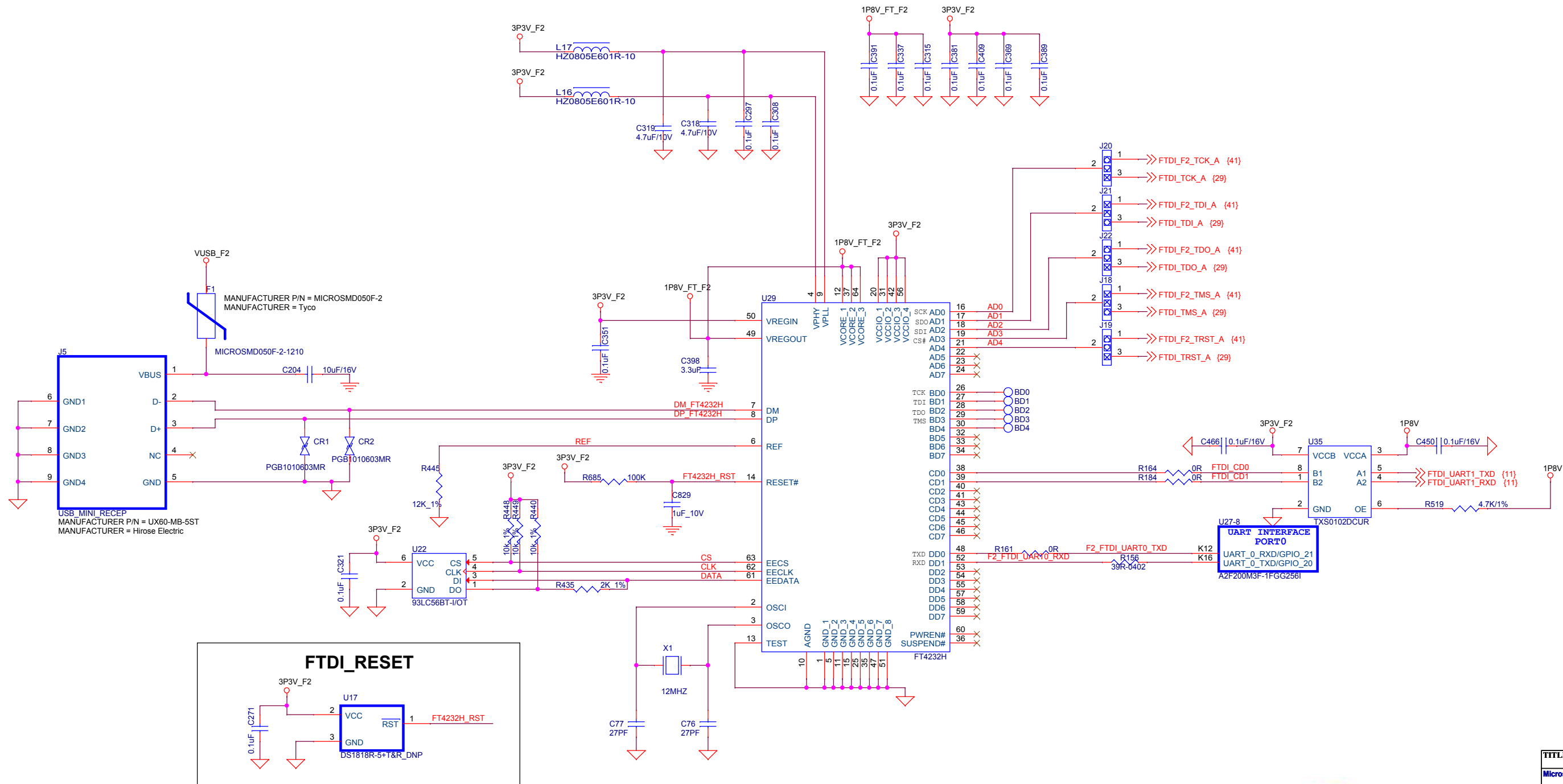
SR No	PROG MODE	Jumper		
		J28	J27	J26
1	JTAG Programming using Prog Header	OPEN	X	X
2	JTAG Programming using embedded FP5	SHORT 1-2	X	X
3	SPI Slave programming using embedded FP5	OPEN	OPEN	OPEN
4	IAP programming	X	SHORT 1-2	X
5	Programming External SPI Flash using Prog Header	OPEN	SHORT 1-2	X
6	Programming External SPI Flash using Embedded JTAG	SHORT 1-2	SHORT 1-2	X

DEVICE_RESET



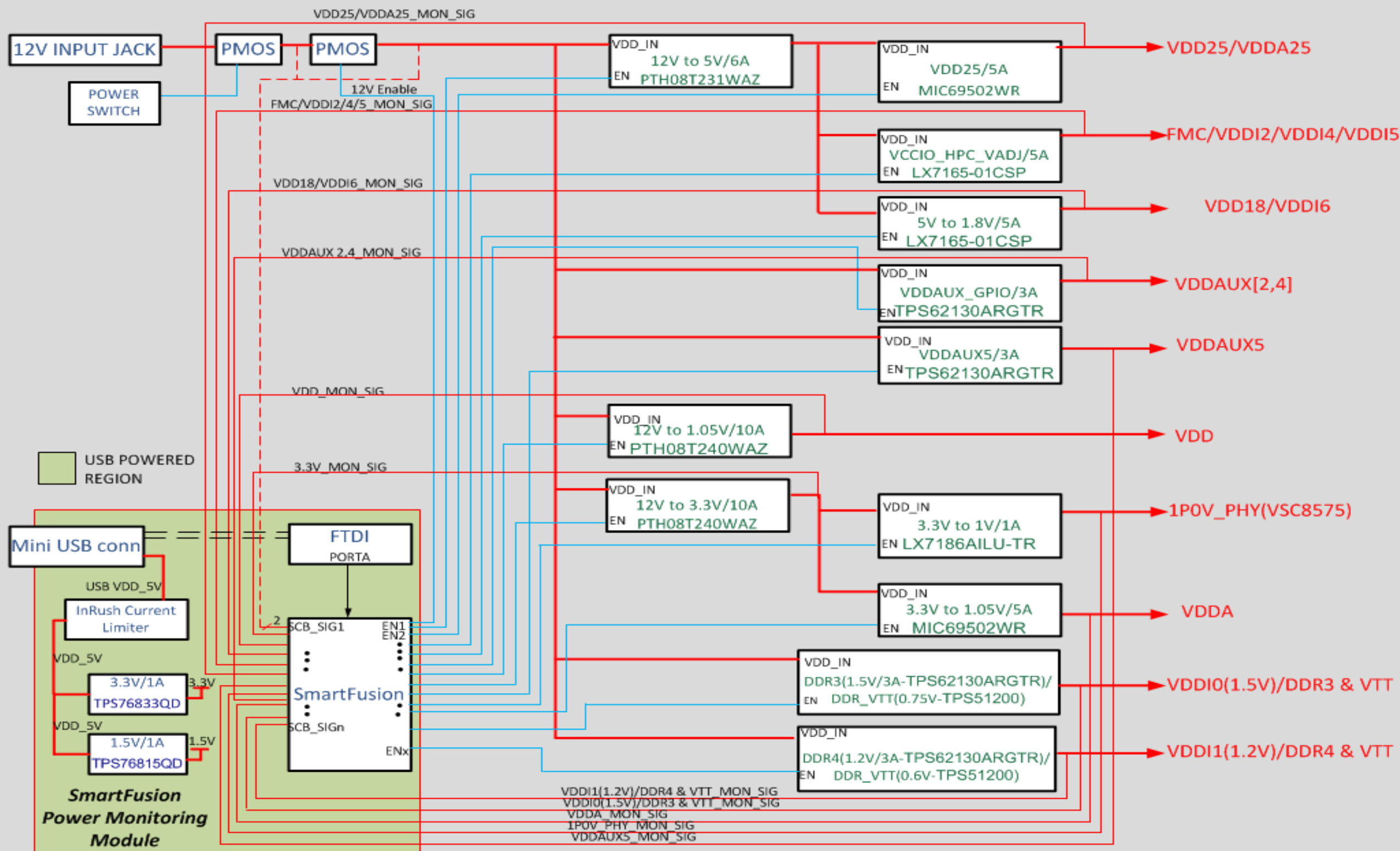
TITLE POLARFIRE EVAL KIT		
Microsemi		
SIZE Custom	DOCUMENT NO. DVP-100-000481-001	REV C
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FT4232H INTERFACE



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Microsemi							
SIZE		DOCUMENT NO.				REV	
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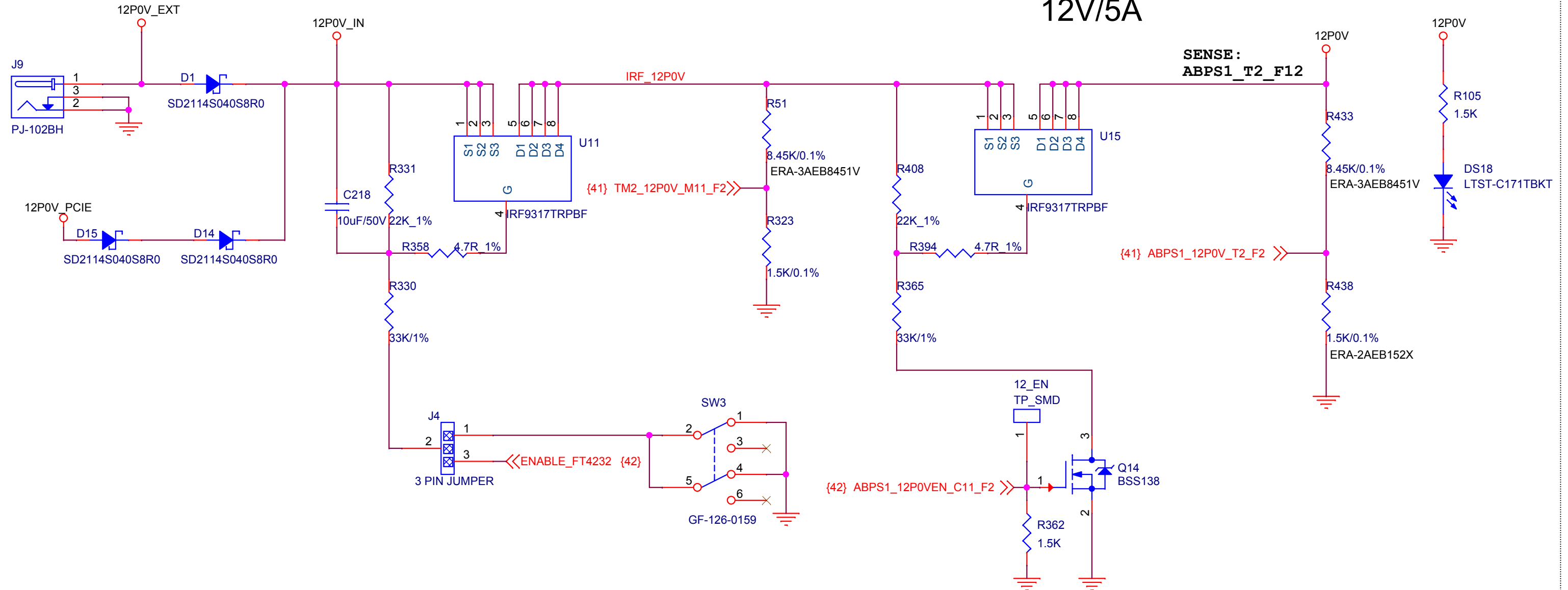
Polarfire Power Management Scheme



TITLE POLARFIRE EVAL KIT			
Microsemi			
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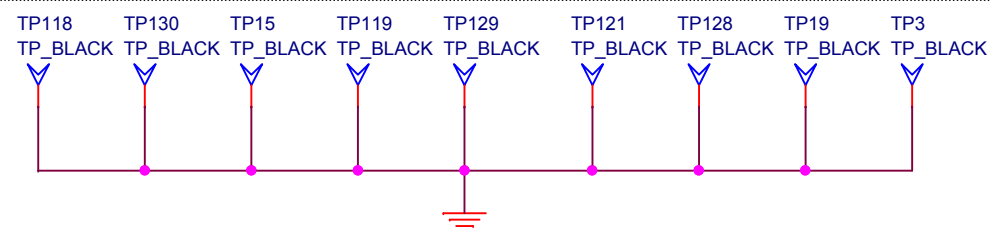
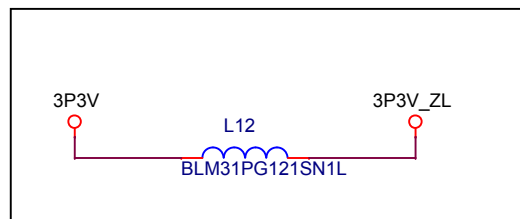
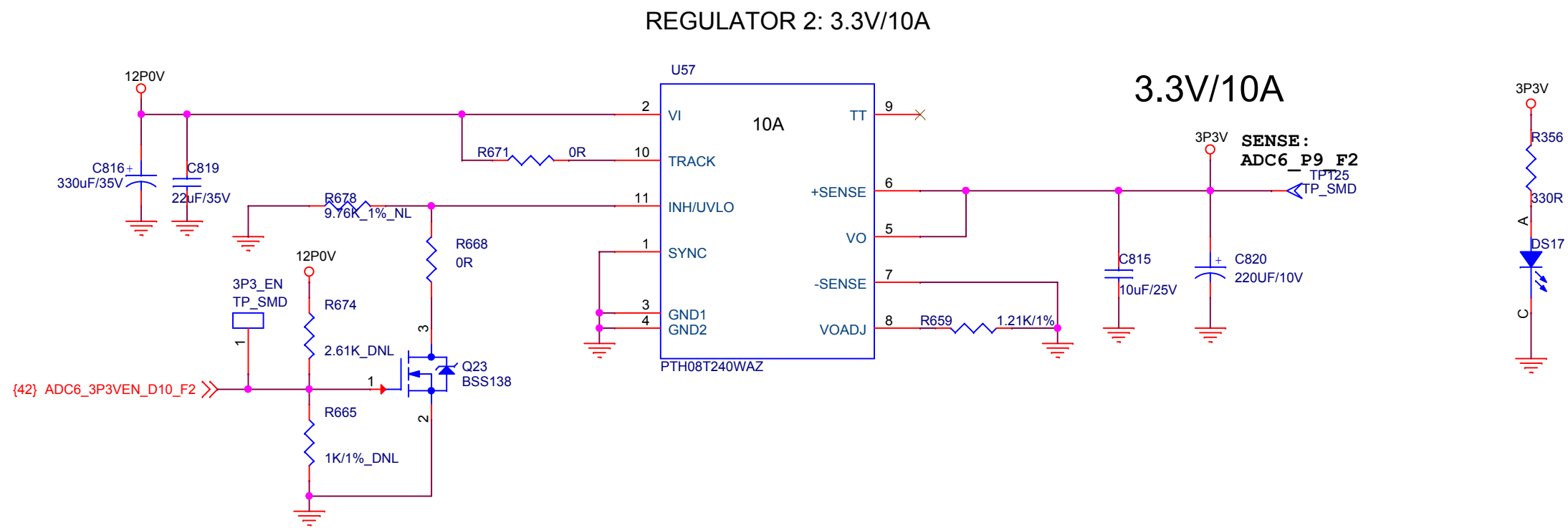
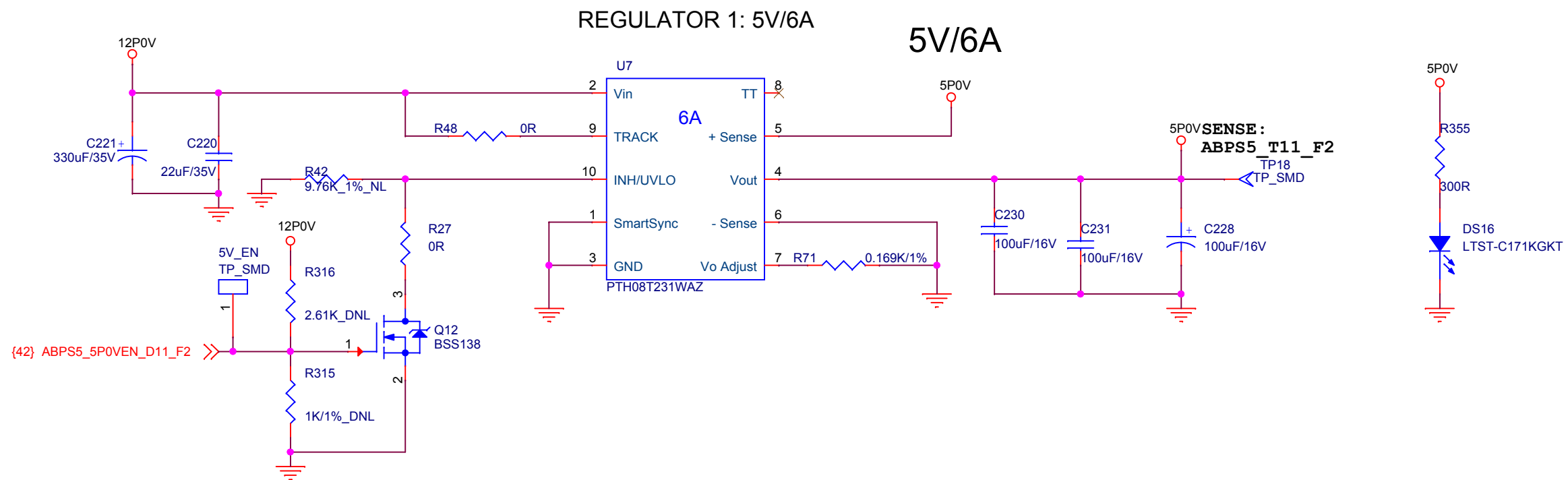
12V EXTERNAL SUPPLY

12V/5A



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"POWER SUPPLIES1" - "3.3V" & "5V"

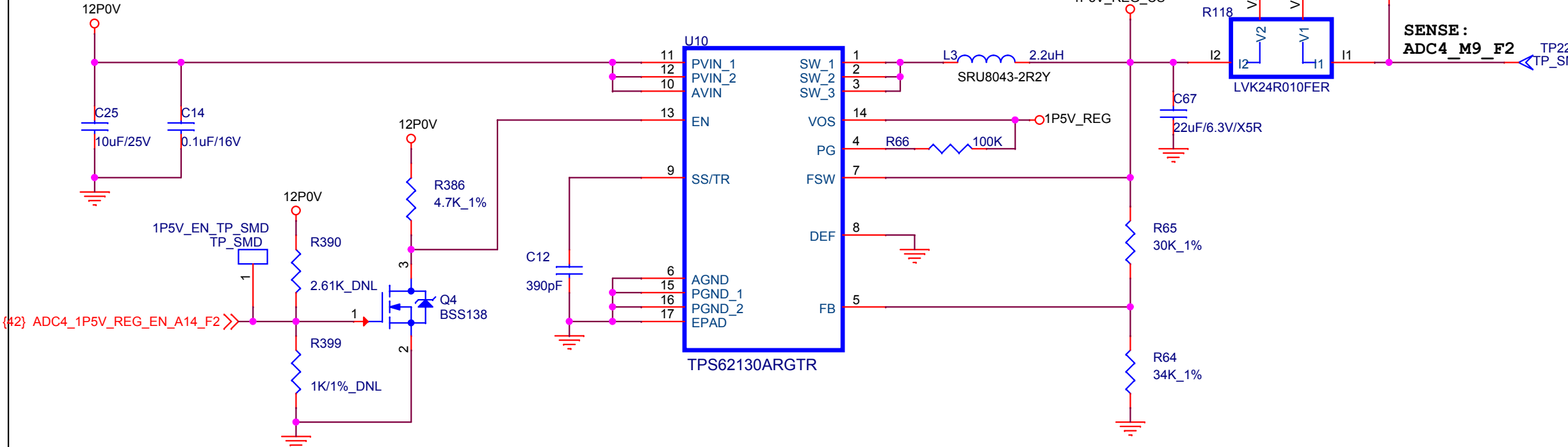


TITLE			
POLARFIRE EVAL KIT			
Microsemi			
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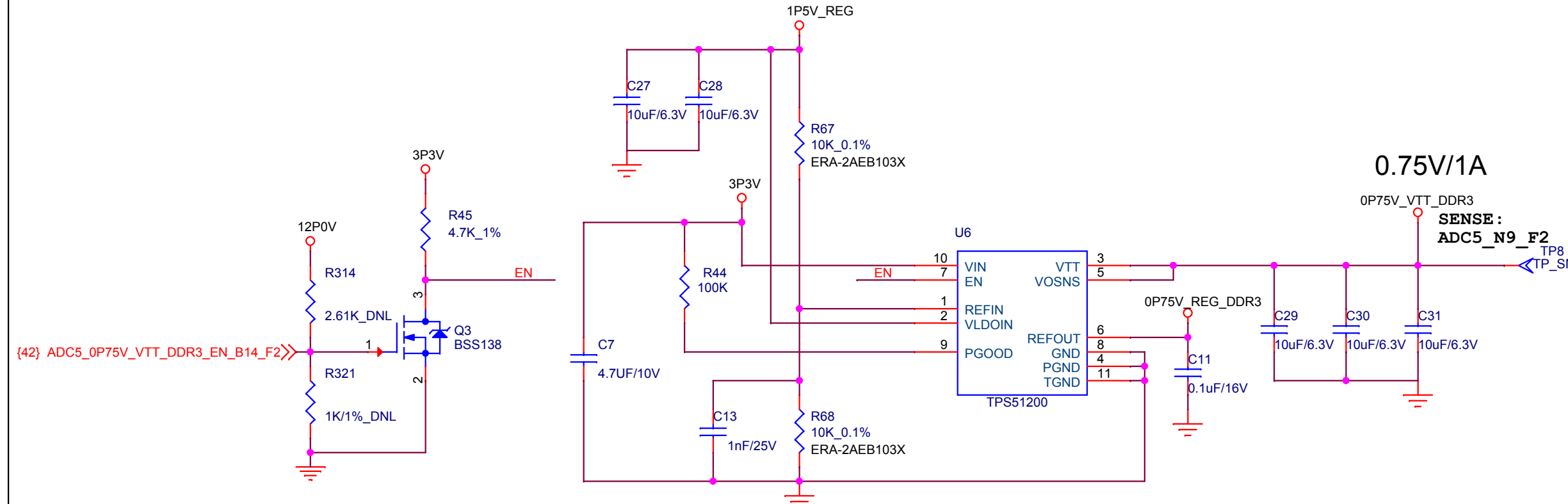
[illegible][illegible][illegible]

"POWER SUPPLIES3" - "0.75V" & "1.5V"

REGULATOR 4 : 12V to 1.5V/3A

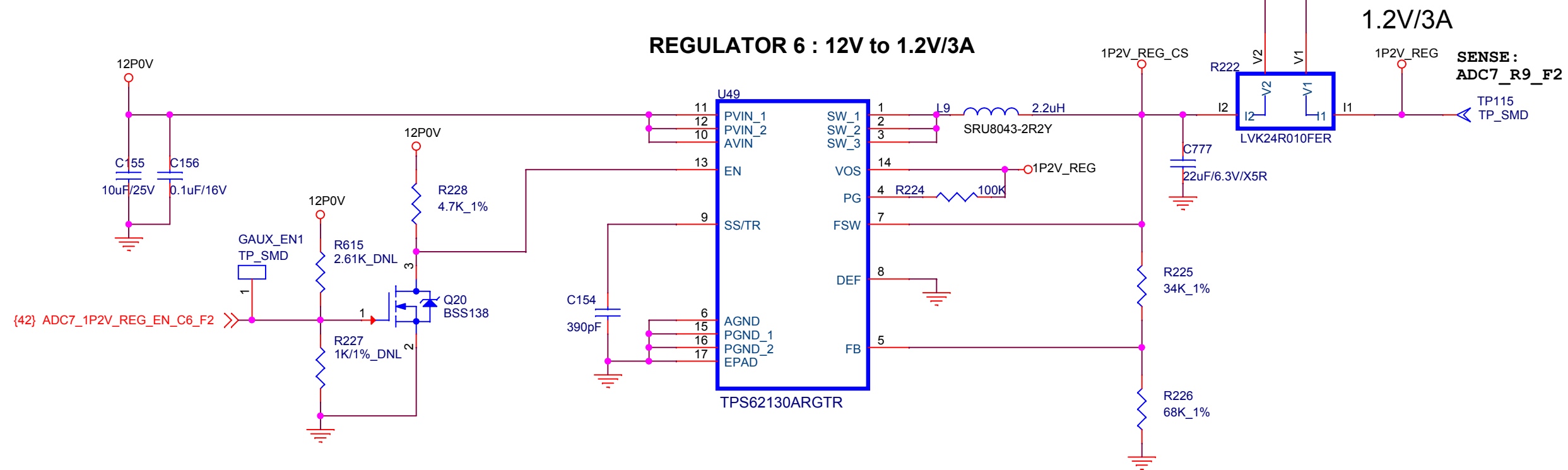


REGULATOR 5: 0.75V FOR DDR3 -VTT SUPPLY

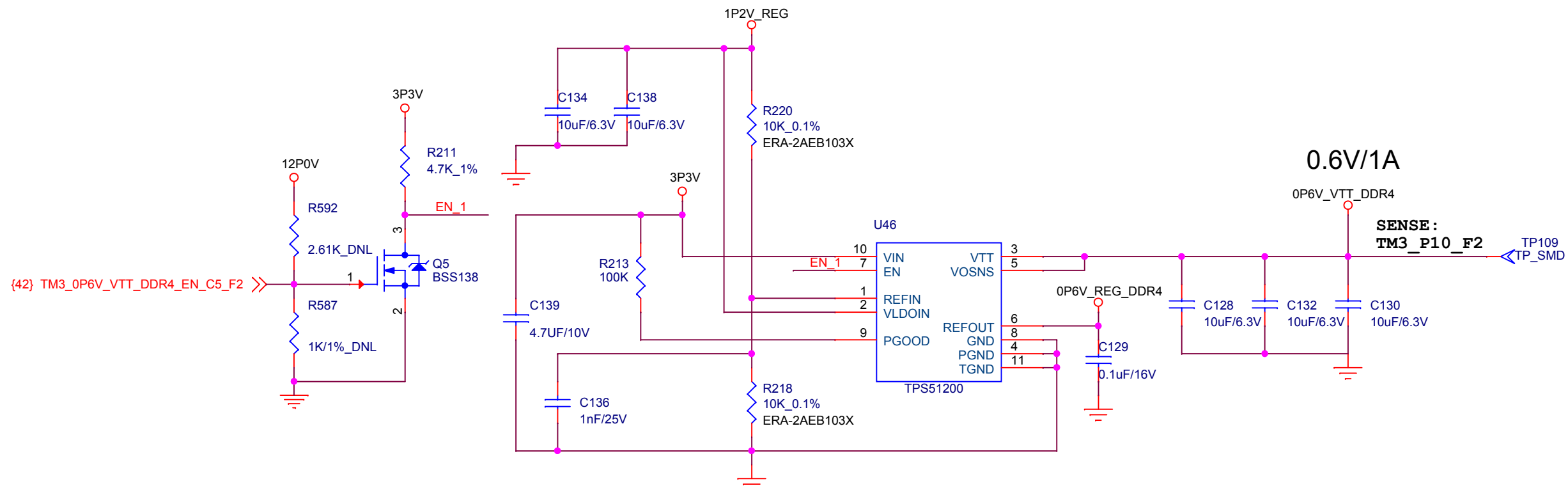


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"POWER SUPPLIES4" - "0.6V" & "1.2V"



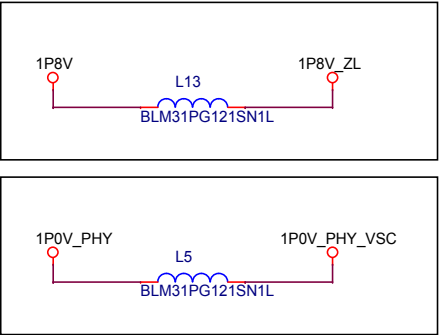
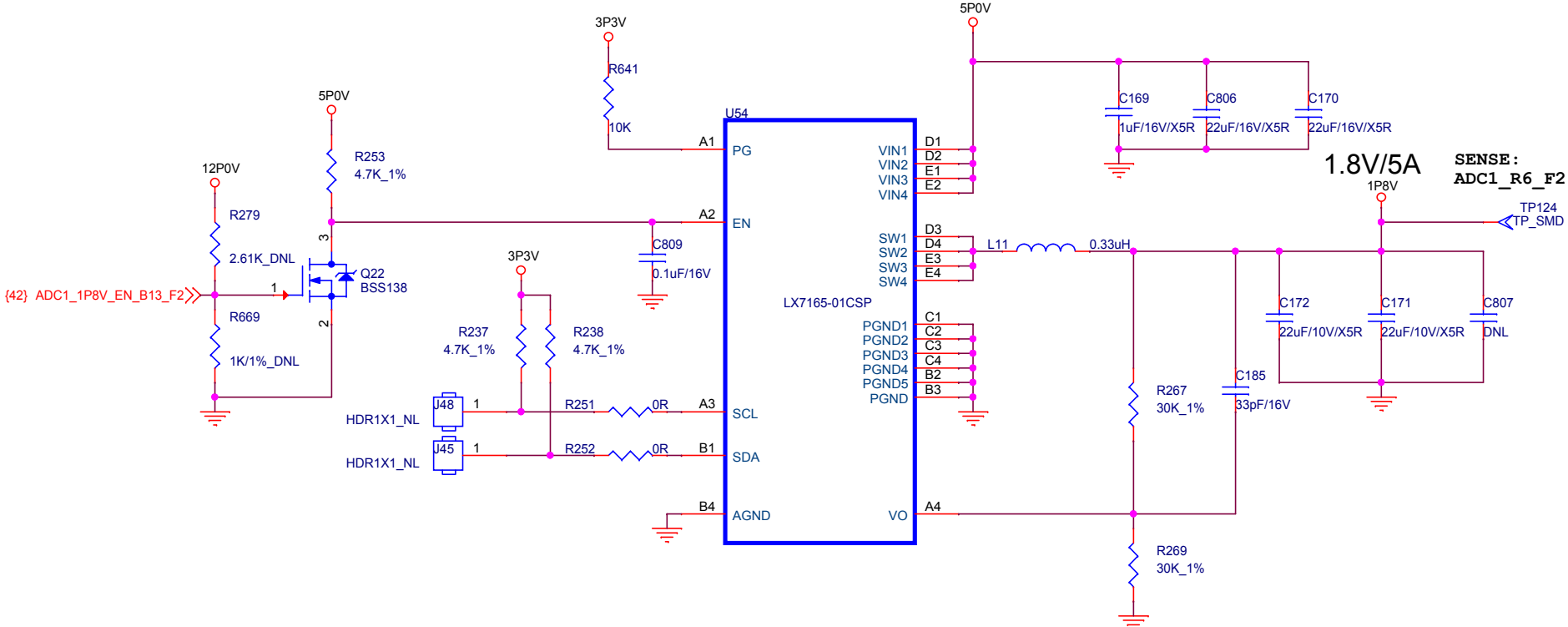
REGULATOR 7: 0.6V FOR DDR4 -VTT SUPPLY



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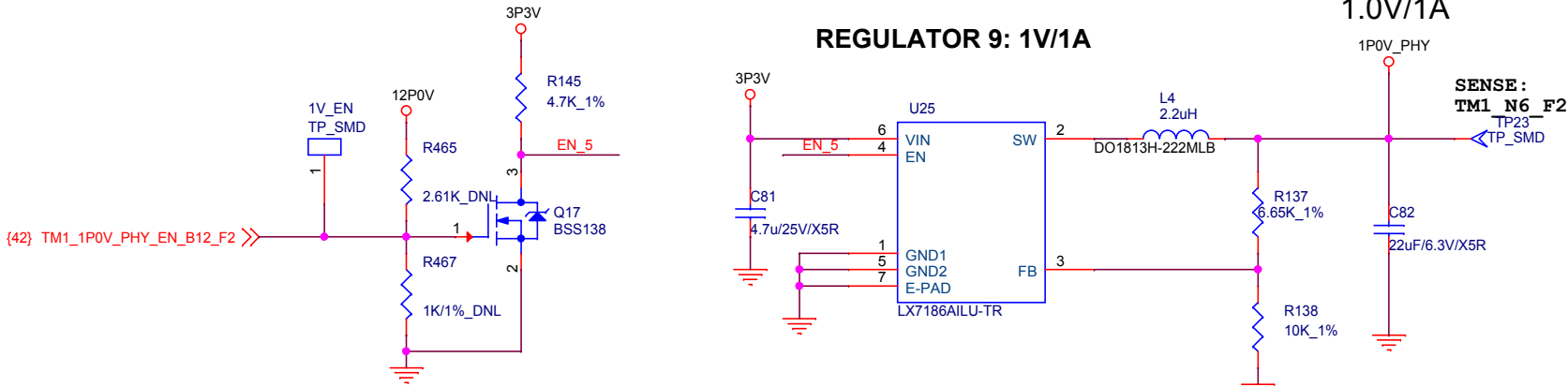
"POWER SUPPLIES5" - "1.05V", "1V" & "1.8V"

REGULATOR 8: 1.8V/5A FOR VPP AND VAUX-HSIO BANK

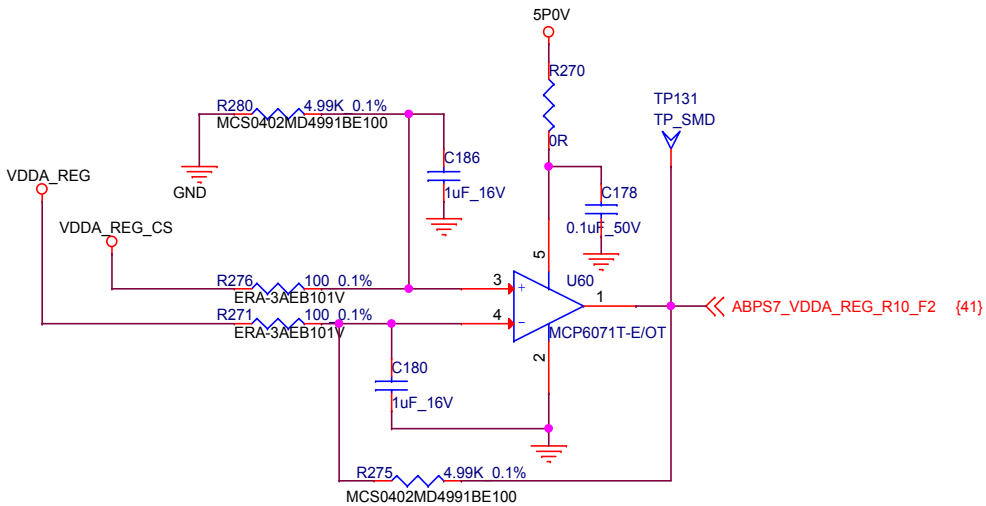


REGULATOR 9: 1V/1A

1.0V/1A

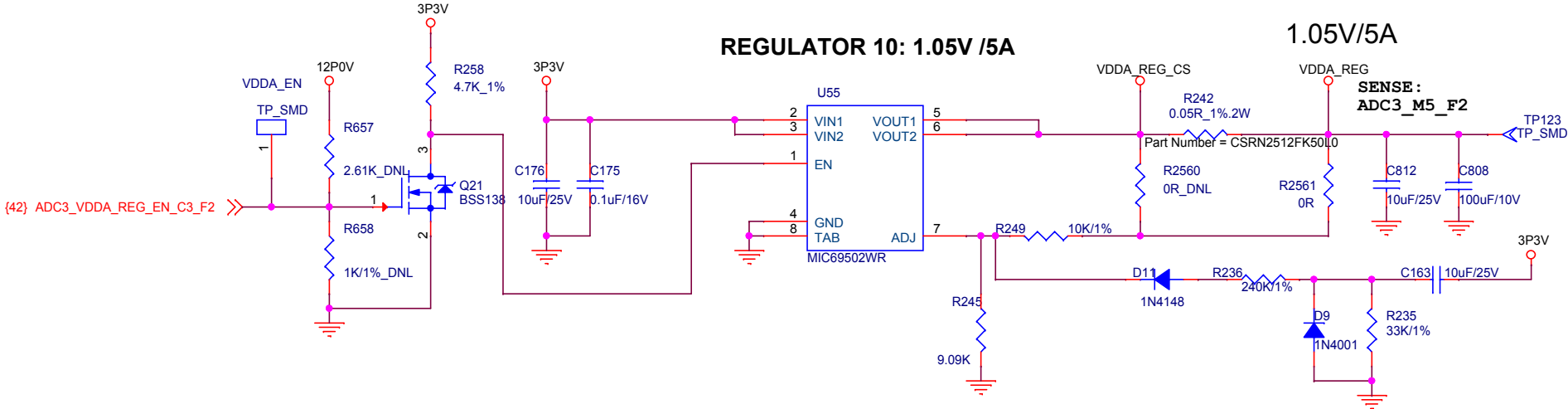


TRANSCEIVER CORE CURRENT SENSE CIRCUIT



REGULATOR 10: 1.05V /5A

1.05V/5A



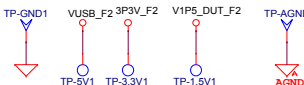
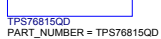
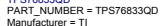
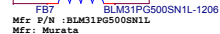
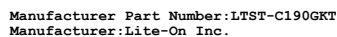
TITLE			
POLARFIRE EVAL KIT			
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POWER MONITORING SOLUTION USING SmartFusion



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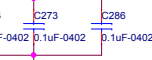
USB ACTIVE IN RUSH LIMITER



SmartFusion ANALOG BLOCK



NOTE: PLACE ALL CAPS NEAR DUT BALLS



SmartFusion POWER SUPPLY



The schematic diagram shows the MSS BLOCK circuit. The block is labeled "MSS BLOCK" and contains pins K3, K6, N2, K5, J11, J15, L11, M14, and F16. It is connected to a 3P3V_F2 input, a V1F5_OUT_F2 output, and a VCC_OSC input. The VCC_OSC input is connected to a 33nH-0603 inductor and a 0.1uF-0402 capacitor. The block is also connected to a VCCRCOSC input and a VCCENVM input. The block is labeled with the part number A2F200MSJ-1FGG256I.

DIGITAL GND

A1 GND1
 A5 GND2
 A9 GND3
 A12 GND3
 A16 GND4
 B5 GND5
 B15 GND6
 C7 GND7
 C13 GND8
 D3 GND9
 E6 GND10
 E8 GND11
 F2 GND12
 F7 GND13
 F9 GND14
 F11 GND15
 F15 GND16
 G6 GND17
 G8 GND18
 G8 GND19
 G10 GND20
 H1 GND21
 H7 GND22
 H9 GND23
 H11 GND24
 H16 GND25
 J6 GND26
 J8 GND27
 J10 GND28
 K7 GND29
 K9 GND30
 K11 GND31
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 L1 GND33
 L6 GND34
 L8 GND35
 L10 GND36
 L16 GND37
 M4 GND39
 N15 GND40

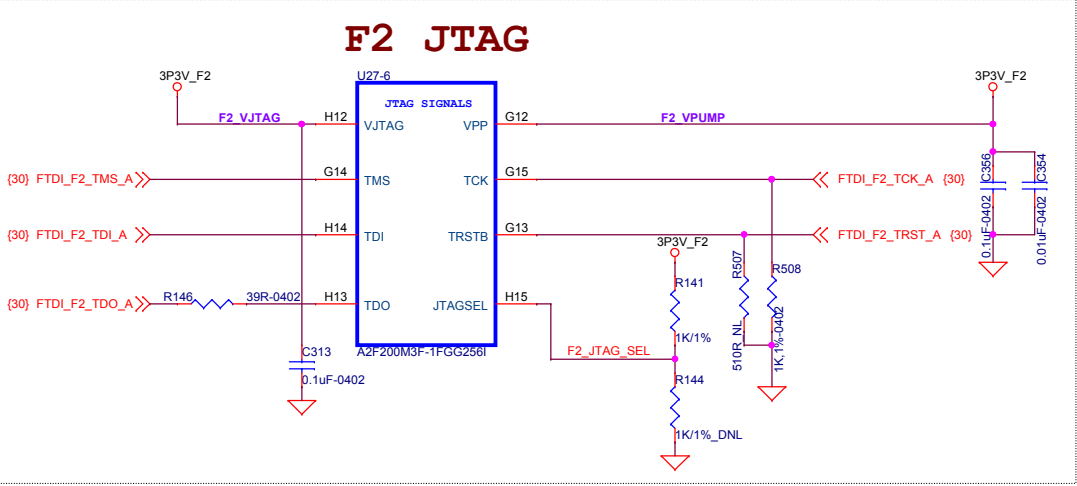
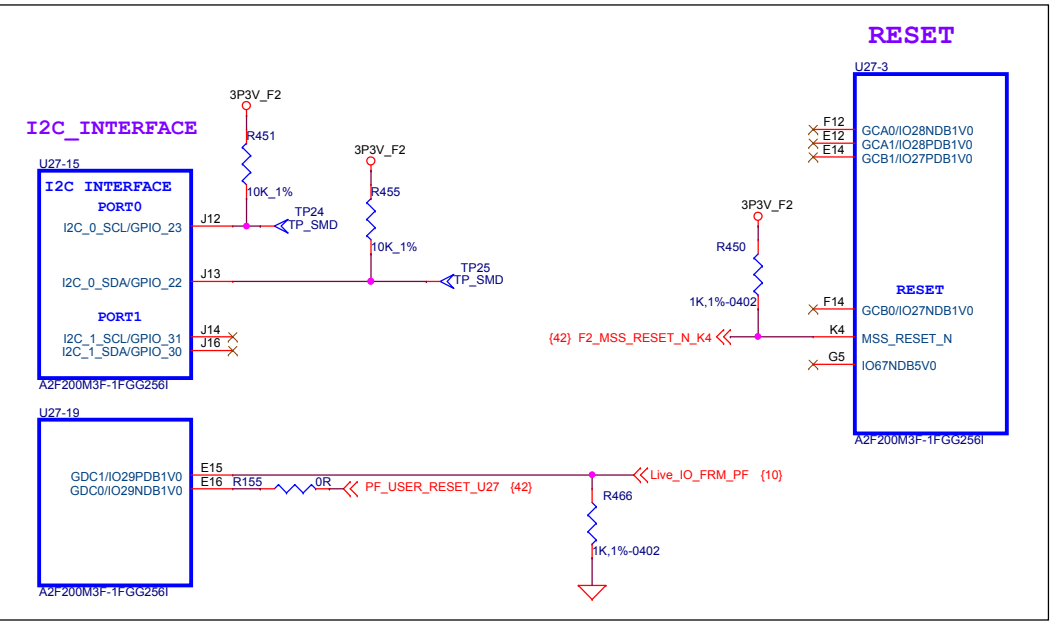
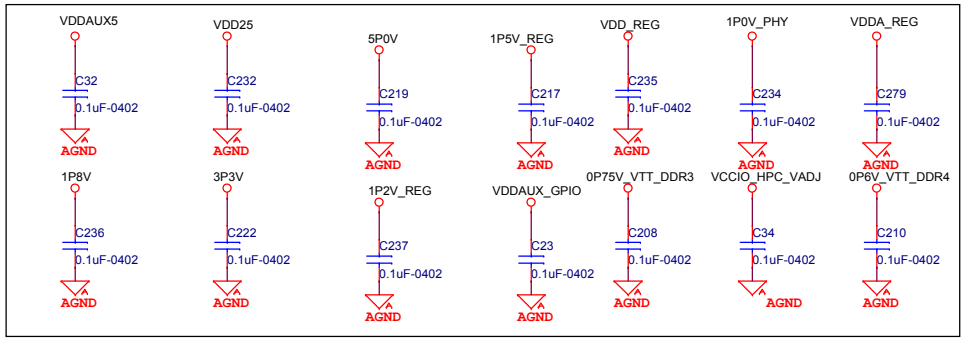
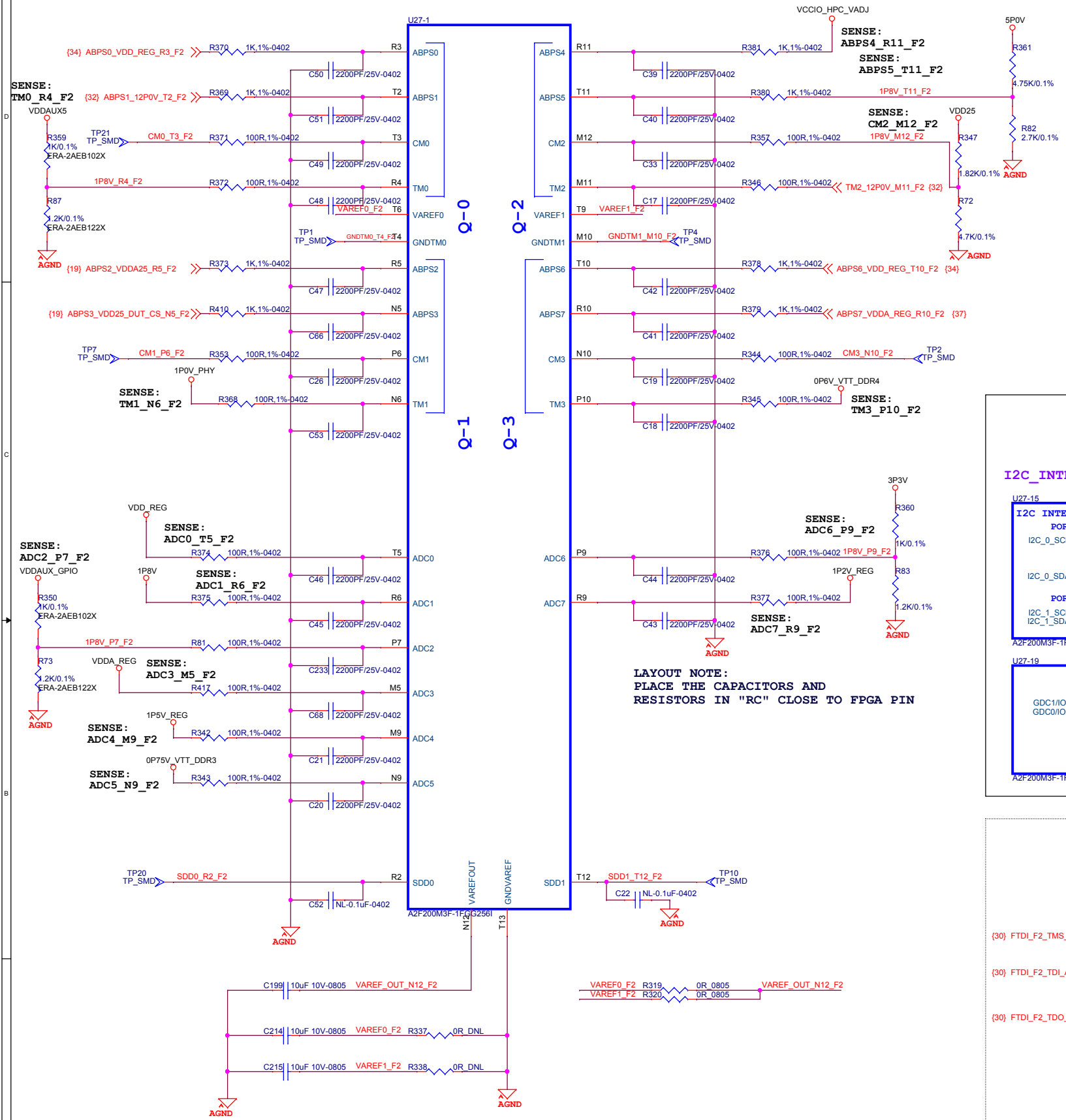
B16 GNDQ1
 D4 GNDQ2
 D12 GNDQ3
 E5 GNDQ4
 F13 GNDQ5
 J5 GNDQ6

GNDRCOSC
 GNDENVLM

J4
 G16

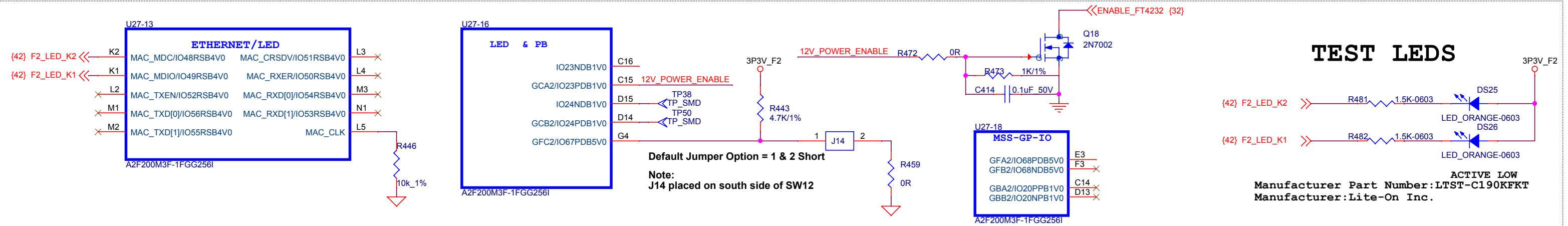
A2F-200M3F-1FGC2560

ANALOG SIGNAL INTERFACE

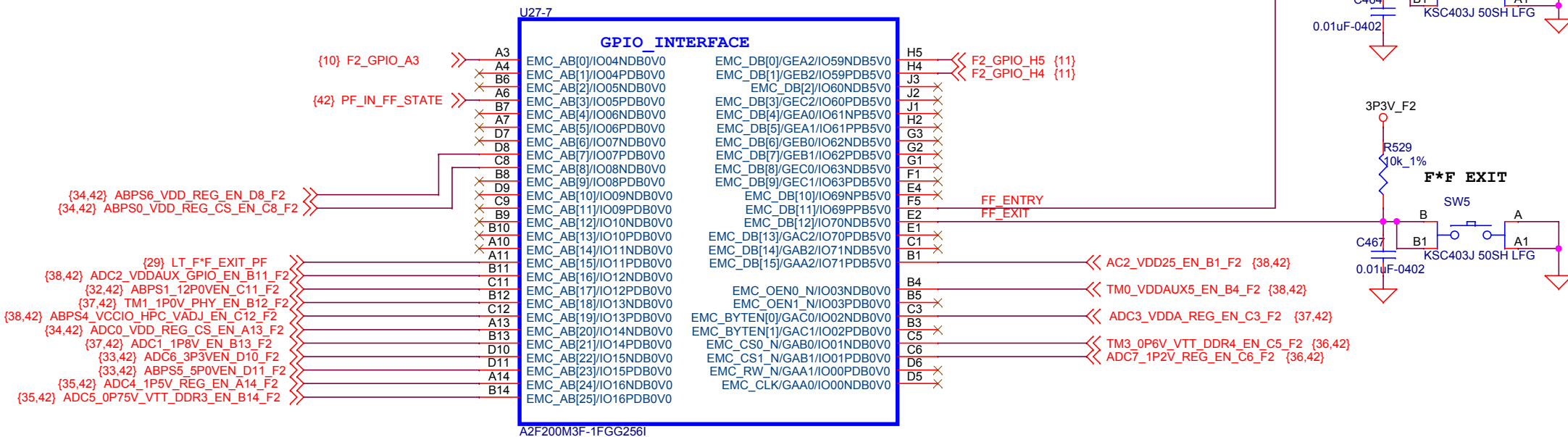


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Microsemi			
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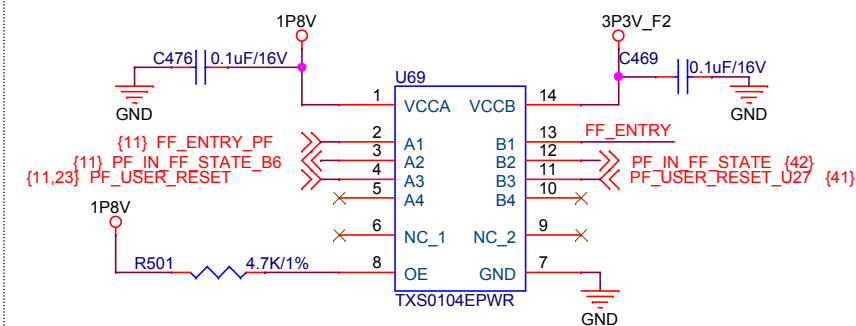
USER DEBUG LOGIC



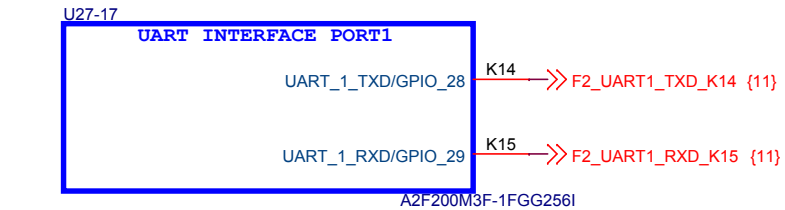
GPIO INTERFACE



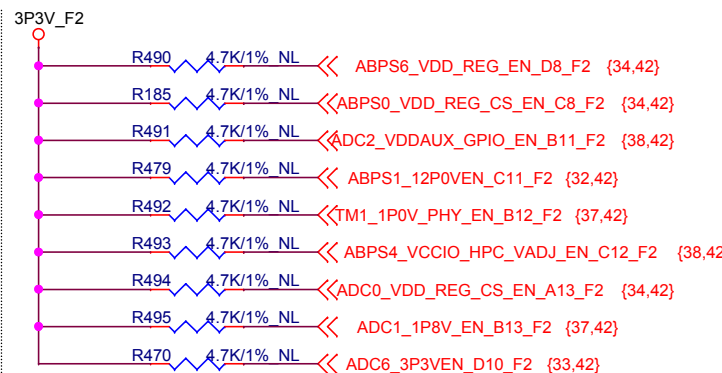
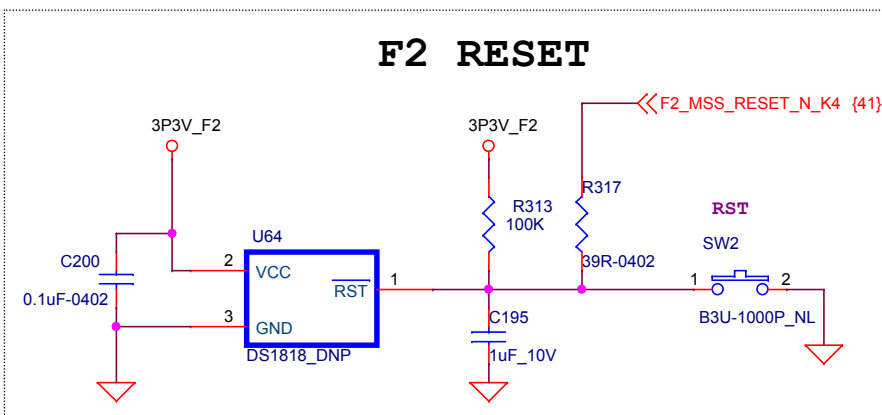
LEVEL TRANSLATOR



UART INTERFACE



F2 RESET



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