

DG0637
Demo Guide
SmartFusion2 SoC FPGA CoreTSE_AHB 1000 Base-T
Loopback Demo - Libero SoC v11.7 SP2

Superseded



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Contents

1	Revision History	1
1.1	Revision 2.0	1
1.2	Revision 1.0	1
2	SmartFusion2 SoC FPGA CoreTSE_AHB 1000 Base-T Loopback Demo	2
2.1	Design Requirements	2
2.2	Demo Design	3
2.2.1	Demo Design Features	4
2.2.2	Demo Design Description	5
2.3	Simulating the Design	6
2.3.1	Simulation	6
2.4	Setting up the Demo Design	8
2.4.1	Programming the Demo Design	9
2.4.2	Connecting SmartFusion2 Security Evaluation Kit Board to Host PC	11
2.4.3	Running the Demo Design with Cat Karat and Wireshark on the Hardware	12
3	Appendix: Running the Demo Design Using Spirent Test Center	15

Figures

Figure 1	Demo Design Files Top-Level Structure	3
Figure 2	SmartFusion2 CoreTSE_AHB 1000 Base-T Loop back Demo	4
Figure 3	Libero SmartDesign	5
Figure 4	SmartDesign for Simulation	7
Figure 5	Libero SmartDesign Top Module	8
Figure 6	FlashPro New Project	9
Figure 7	FlashPro Project Configuration	10
Figure 8	FlashPro Programming Passed	11
Figure 9	SmartFusion2 Security Evaluation Kit Setup	12
Figure 10	Wireshark Network Analyzer	13
Figure 11	Cat Karat Packet Generate Window	13
Figure 12	Packet Flow Control	14
Figure 13	Wireshark Software Window	14
Figure 14	Spirent Test Center Stream Block – General Tab	15
Figure 15	Spirent Test Center	16
Figure 16	Spirent Test Center Stream Block – Frame Tab	16

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Tables

Table 1	Design Requirements	2
Table 2	SmartFusion2 Security FPGA Evaluation Kit Jumper Settings	8

Superseded

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Libero SoC, FlashPro, and SoftConsole design requirements were updated. For more information, see [Design Requirements](#), page 2.
- Throughout the document, the names of SoftConsole projects used in the demo design and all the associated figures were updated.

1.2 Revision 1.0

Revision 1.0 was the first publication of this document.

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2 SmartFusion2 SoC FPGA CoreTSE_AHB 1000 Base-T Loopback Demo

Microsemi Triple-Speed Ethernet MAC, CoreTSE_AHB is a configurable soft intellectual property (IP) core that complies with the IEEE 802.3 standard.

This demo design provides an Ethernet solution for the SmartFusion2 SoC FPGA and implements a CoreTSE_AHB-based 1000 Base-T loopback design on the SmartFusion2 Security Evaluation Kit. CoreTSE_AHB enables system designers to implement a broad range of Ethernet designs, from low-cost 10/100 Ethernet to higher-performance 1 gigabit ports. CoreTSE_AHB suits networking equipments such as switches, routers, and data acquisition systems. CoreTSE is also available in a version that works with IGLOO®2 FPGA family.

CoreTSE_AHB has the following interfaces:

- 10/100/1000 Mbps Ethernet MAC with a gigabit media independent interface (GMII) and ten bit interface (TBI) to support serial gigabit media independent interface (SGMII), 1000BASE-T, and 1000BASE-X
- GMII or TBI physical layer interface connects to Ethernet PHY
- MAC data path interface
- Advanced peripheral bus (APB) slave interface for MAC configuration registers and status counter access

CoreTSE_AHB can be configured as GMII or TBI for Ethernet network at 10/100/1000 Mbps data transfer rates (line speeds).

The CoreTSE IP is available in two different versions:

- CoreTSE_AHB: Uses AHB interface for both the transmit and receive paths. This IP works for SmartFusion2 SoC FPGA.
- CoreTSE (Non-AMBA): Uses direct access to the MAC with a streaming packet interface. This IP works for IGLOO2 FPGA and SmartFusion2 SoC FPGA.

CoreTSE and CoreTSE_AHB are identical to MSS hard Ethernet MAC in SmartFusion2 with respect to the supported features, register configuration, and register addresses. Multiple CoreTSE IPs can be used in SmartFusion2 to achieve Ethernet solutions. CoreTSE_AHB can be used in SmartFusion2 devices along with MSS Ethernet MAC to support multiple Ethernet interfaces. For more information about CoreTSE_AHB, see to the [CoreTSE_AHB Handbook](#).

For more information about Ethernet applications, see the [AC423: SmartFusion2/IGLOO2 Ethernet Application Note](#).

Note: CoreTSE_AHB requires license for using in Libero® system-on-chip design. For license request, send an email to soc_marketing@microsemi.com.

2.1 Design Requirements

The following table lists the design requirements for running the demo.

Table 1 • Design Requirements

Hardware Requirements	Description
SmartFusion2 Security Evaluation Kit:	Rev D or later
• 12 V adapter • FlashPro4 programmer	
Host PC or Laptop (12 GB RAM)	Windows 64-bit Operating System
Spirent Test Center (Optional)	

Table 1 • Design Requirements (continued)

Software Requirements	
Libero SoC	11.7 SP2
FlashPro Programming Software	11.7 SP2
SoftConsole	v4.0
Cat Karat Packet Generator Software	Provided with design files
Wireshark Software	Provided with design files
IP Requirements	
CoreTSE_AHB	License provided on request. Send an email to soc_marketing@microsemi.com .

2.2 Demo Design

The demo design files are available for download from the following path:

http://soc.microsemi.com/download/rsc/?f=m2s_dg0637_liberov11p7sp2_df

The demo design files include:

- Libero project
- Programming files
- Source files
- Readme.txt file

See the `Readme.txt` file for the complete directory structure.

The following figure shows the top-level structure of the design files.

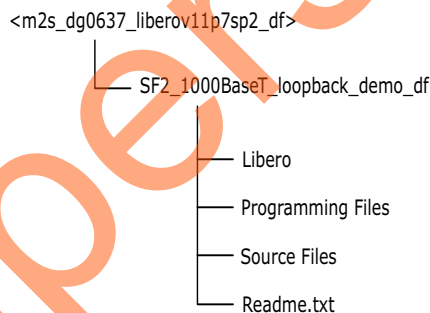
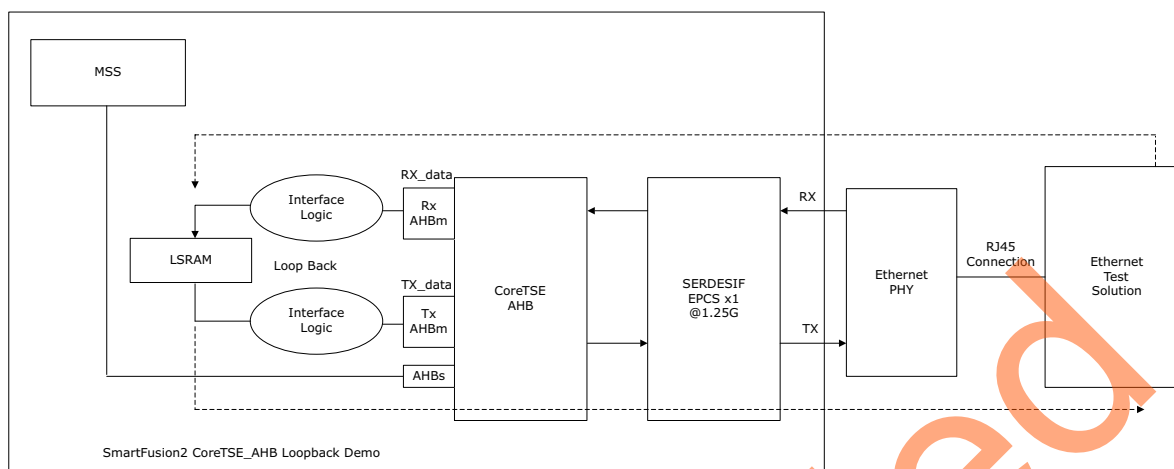
Figure 1 • Demo Design Files Top-Level Structure

Figure 2, page 4 shows the demo design block diagram.

Figure 2 • SmartFusion2 CoreTSE_AHB 1000 Base-T Loop back Demo

In this demo design CoreTSE_AHB is instantiated in the FPGA fabric and connected to the on-board Ethernet PHY using high-speed serial interface (SERDES_IF).

In the previous figure, the dotted arrow in red shows the transfer of Ethernet packet from the host PC to the internal LSRAM and the dotted arrow in blue shows the retransmission of packet from LSRAM to the host.

2.2.1 Demo Design Features

The demo design performs Ethernet loopback using CoreTSE_AHB in TBI 1000 Base-T on hardware and also in simulation.

Following are the demo design features:

- Simulation model for CoreTSE_AHB loopback design.
- CoreTSE_AHB loopback design on SmartFusion2 Security Evaluation Kit.

The following section explains the initialization and configuration of CoreTSE_AHB, SERDES_IF, and the loopback mechanism.

2.2.1.1 High-Speed Serial Interface Configuration

During the design process, CoreTSE_AHB was configured to present a Ten Bit Interface (TBI) to the SERDESIF block, which is configured for External Physical Coding SubLayer (EPCS) operation using lane 3 to create an SGMII link to the external physical-layer (PHY) device.

2.2.1.2 CoreTSE_AHB IP MAC Initialization

At power-up, firmware running on the Cortex-M3 processor will initialize control registers in CoreTSE_AHB and the external PHY device to place them in 1000 Base-T mode.

2.2.1.3 Ethernet Packet Loopback Mechanism

The following Ethernet loopback mechanism is used in this demo:

2.2.1.3.1 Ethernet Packet Reception

CoreTSE_AHB receives the Ethernet packet from the on-board Ethernet PHY through highspeed SERDES_IF.

CoreTSE_AHB receive (RX) path is connected to LSRAM through the AHB interface. The Cortex-M3 processor moves the Ethernet packet data to the LSRAM memory using DMA.

2.2.1.3.2 Ethernet Packet Transmission

To loop back the Ethernet packet, the Cortex-M3 processor reads the Ethernet packet data from LSRAM memory through AHB interface and forwards it to it on the CoreTSE_AHB transmit (TX) path.

CoreTSE_AHB transmits the Ethernet packet to the on-board Ethernet PHY through highspeed SERDES.

2.2.1.4 Ethernet Test Solution

There are many ways to evaluate the CoreTSE_AHB 1000 Base-T loopback demo on the SmartFusion2 Security Evaluation board.

2.2.1.4.1 Solution 1

- The Cat Karat packet generator software installed on the host PC is used to transmit the Ethernet packet through RJ45 Ethernet copper cable.
- The Wireshark packet receiver software installed on the host PC captures the Ethernet packet (loopback) through RJ45 Ethernet copper cable.

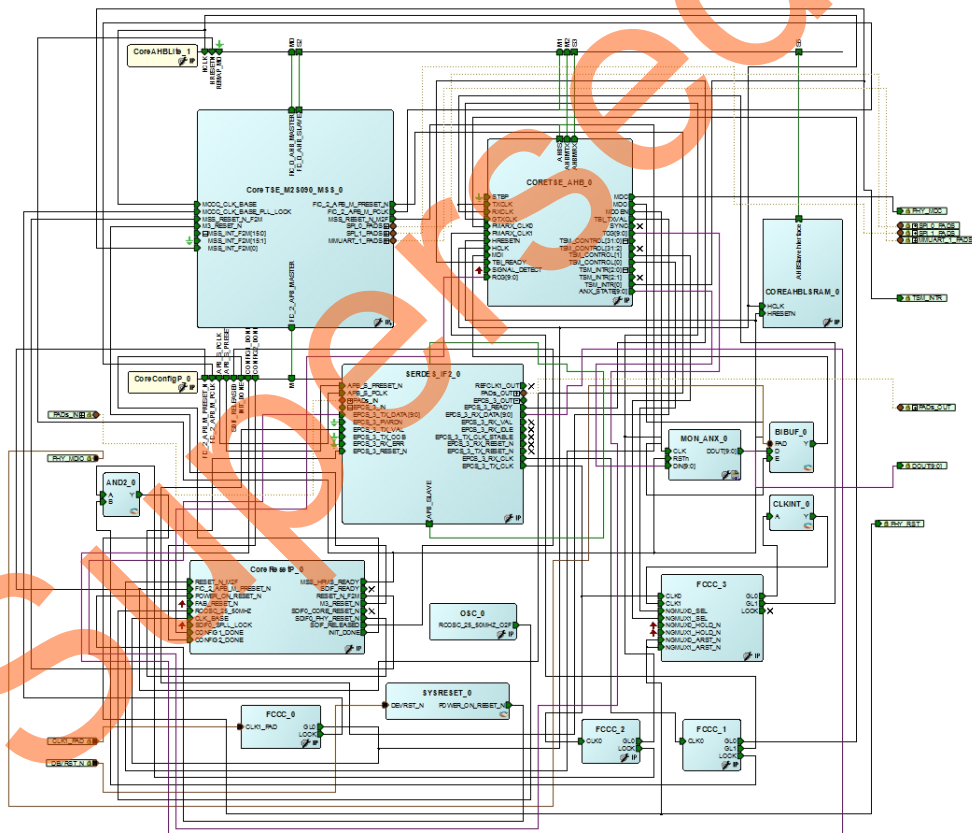
2.2.1.4.2 Solution 2

Spirent test center or an equivalent solution can be used to test the CoreTSE_AHB loopback demo. For more information, see [Appendix: Running the Demo Design Using Spirent Test Center](#), page 15.

2.2.2 Demo Design Description

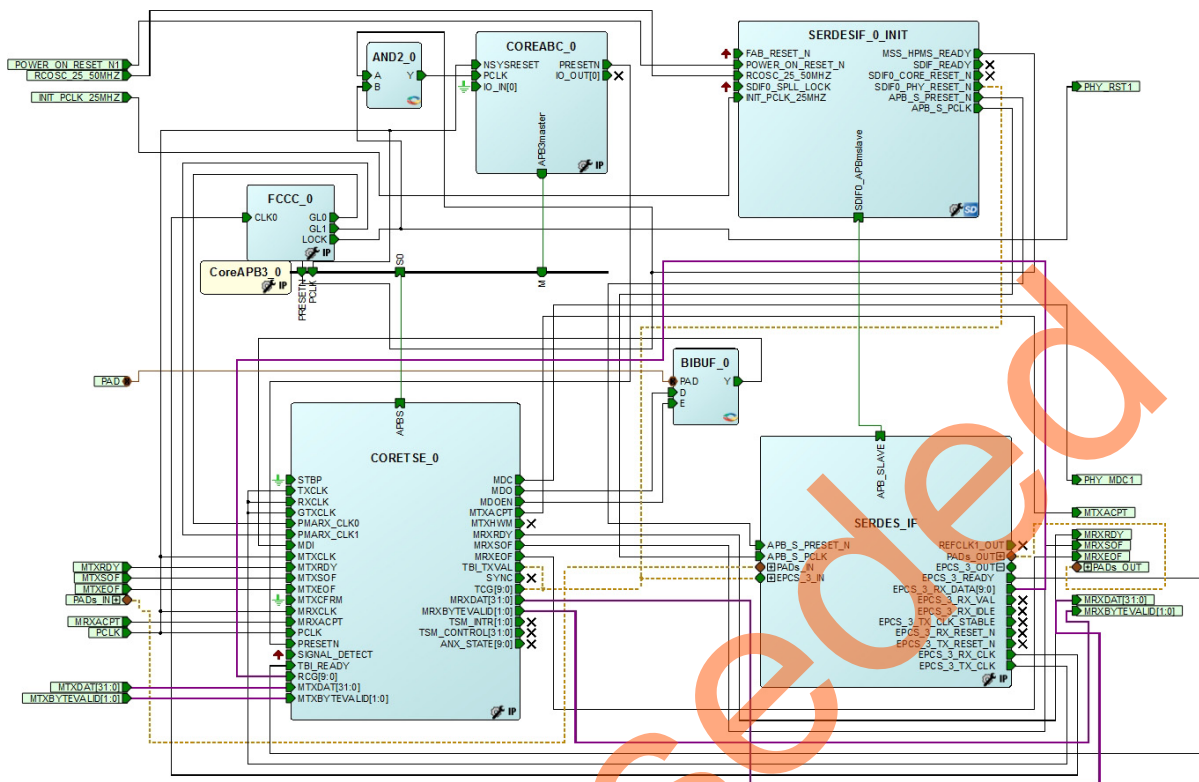
This demo design is implemented by configuring the CoreTSE_AHB for the TBI mode. The following figure shows the Libero SoC hardware implementation for this demo design.

Figure 3 • Libero SmartDesign

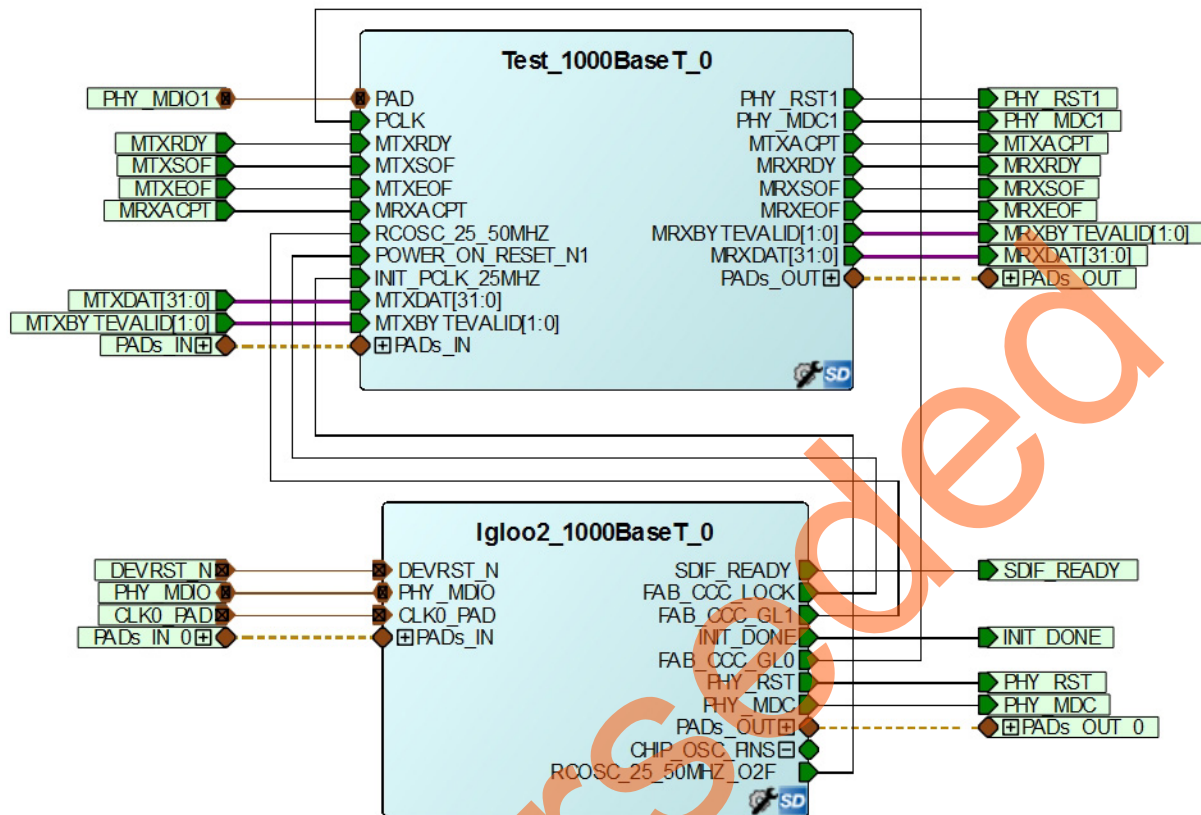


Libero hardware project uses the following resources:

- CoreTSE_AHB
- Cortex M3 (microcontroller sub system) to configure CoreTSE_AHB and on-board Ethernet PHY
- High-speed serial interface (SERDES_IF) configured for EPCS lane 3 mode
- SoftConsole - application for initializing the CoreTSE_AHB and for transferring the Ethernet packet data to/from LSRAM
- Dedicated input pad 0 as the clock source

Figure 4 • SmartDesign for Simulation


The Libero SmartDesign top module contains the CoreTSE_AHB loopback design and the testbench module.

Figure 5 • Libero SmartDesign Top Module

2.4 Setting up the Demo Design

The following steps describe how to setup the demo:

1. Connect the **FlashPro4 Programmer** to the J5 connector on the SmartFusion2 FPGA Security Evaluation Kit board.
2. Connect the jumpers to the SmartFusion2 FPGA Security Evaluation Kit board as shown in the following table.

Table 2 • SmartFusion2 Security FPGA Evaluation Kit Jumper Settings

Jumper	Pin (from)	Pin (to)	Comments
J22	1	2	Default
J23	1	2	Default
J24	1	2	Default
J8	1	2	Default
J3	1	2	Default

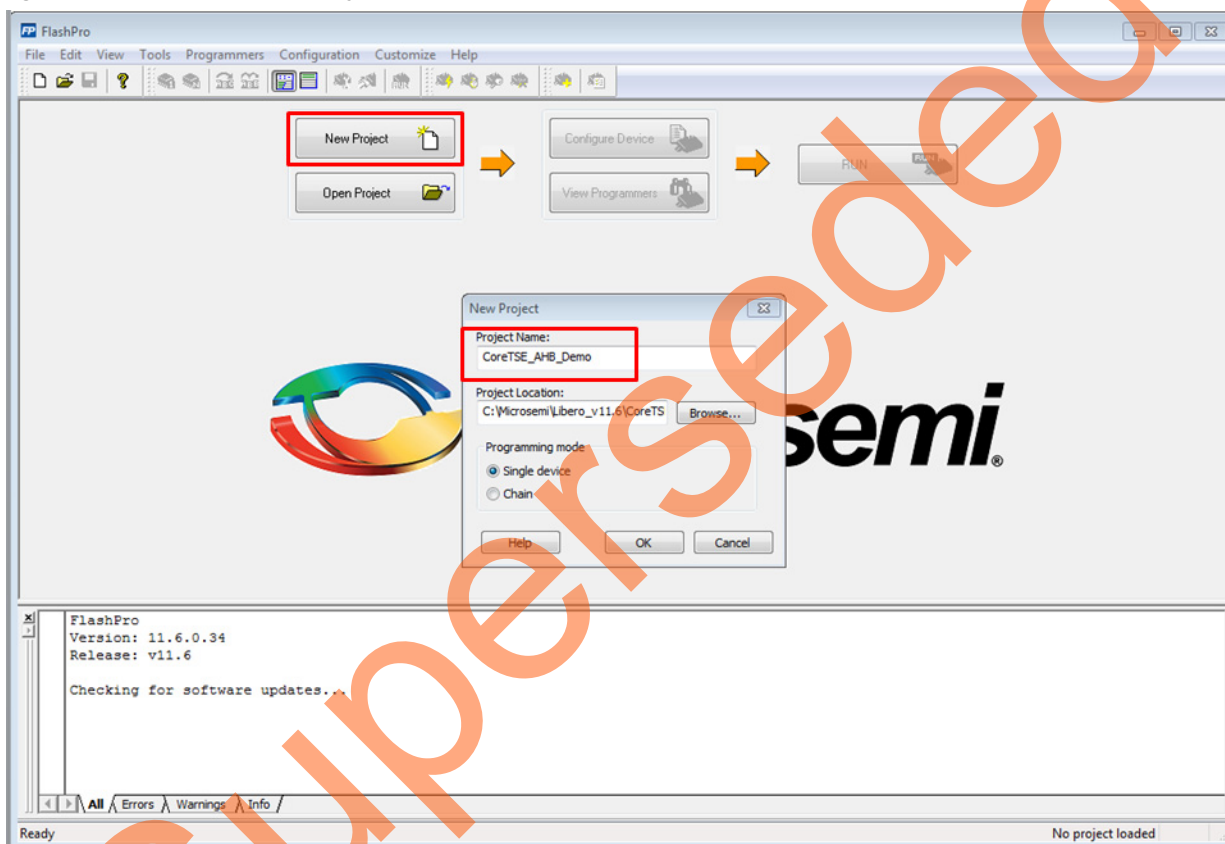
3. Connect the power supply to the J6 connector.

2.4.1 Programming the Demo Design

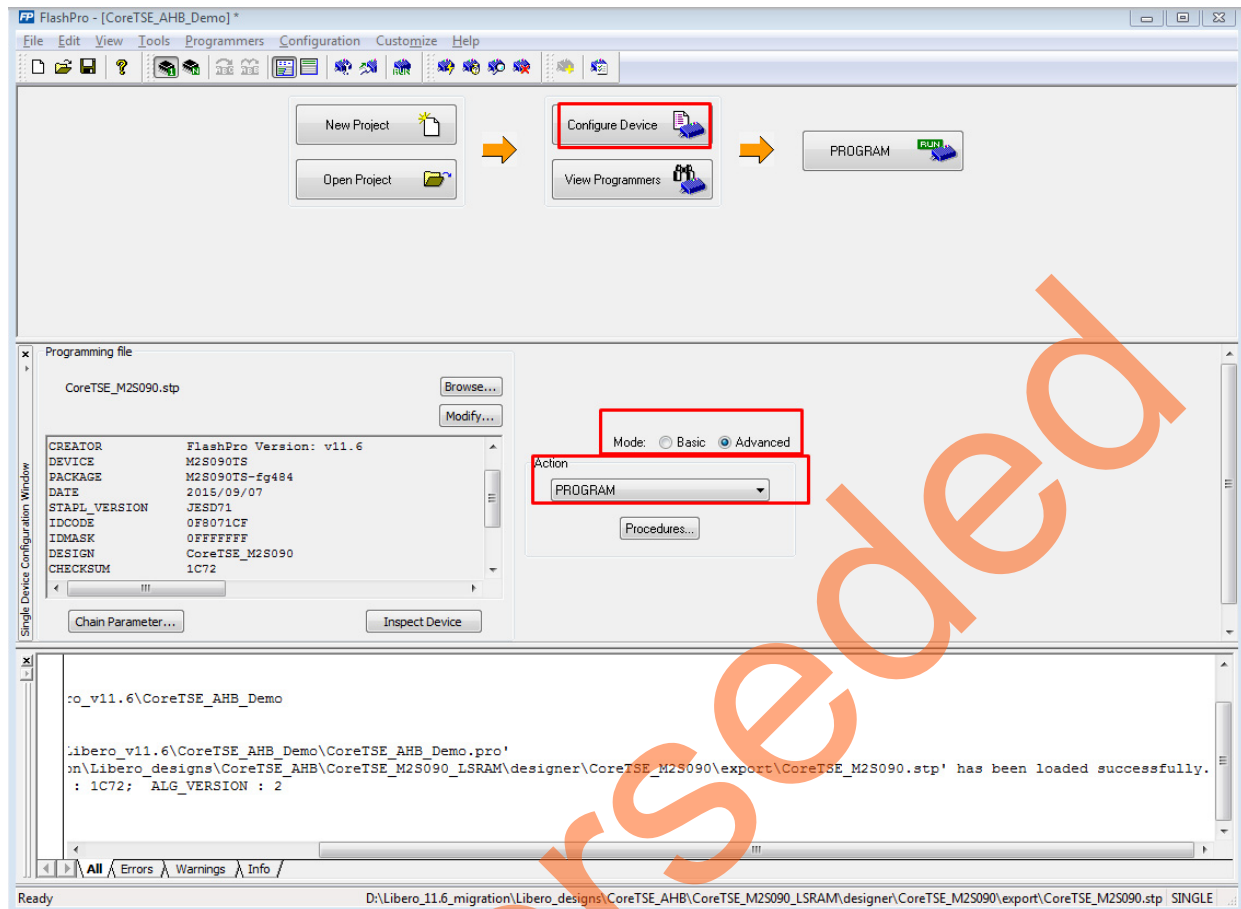
The following steps describe how to program the demo design:

1. Download the demo design from the following path:
http://soc.microsemi.com/download/rsc/?f=m2s_dg0637_liberov11p7sp2_df
2. Switch ON the power supply switch, **SW7**.
3. Launch the **FlashPro** software.
4. Click **New Project**.
5. In the **New Project** window, enter the project name as **CoreTSE_AHB_Demo**.
6. Click **Browse** and navigate to the location to save the project.
7. Select **Single Device** as Programming mode.
8. Click **OK** to save the project.

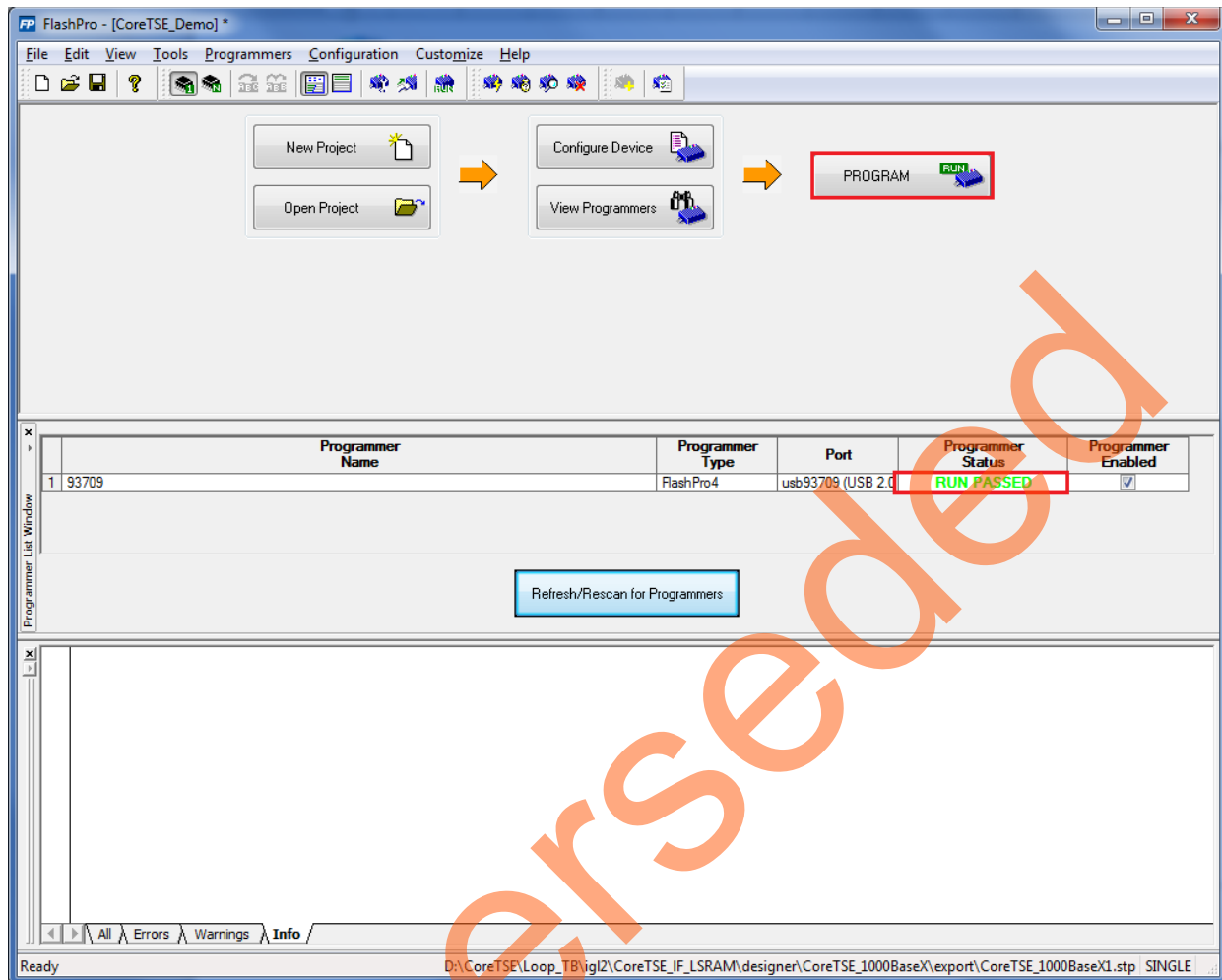
Figure 6 • FlashPro New Project



9. Click **Configure Device**.

Figure 7 • FlashPro Project Configuration

10. Click **Browse** and navigate to the location where the SF2_1000BaseT_Demo.stp file is located and select the file. The default location is:
<download_folder>\SF2_1000BaseT_loopback_demo_df\ProgrammingFile\
11. Select **Advanced** as Mode and **PROGRAM** as Action.
12. Click **PROGRAM** to start programming the device. Wait until the programmer status is changed to **RUN PASSED**.

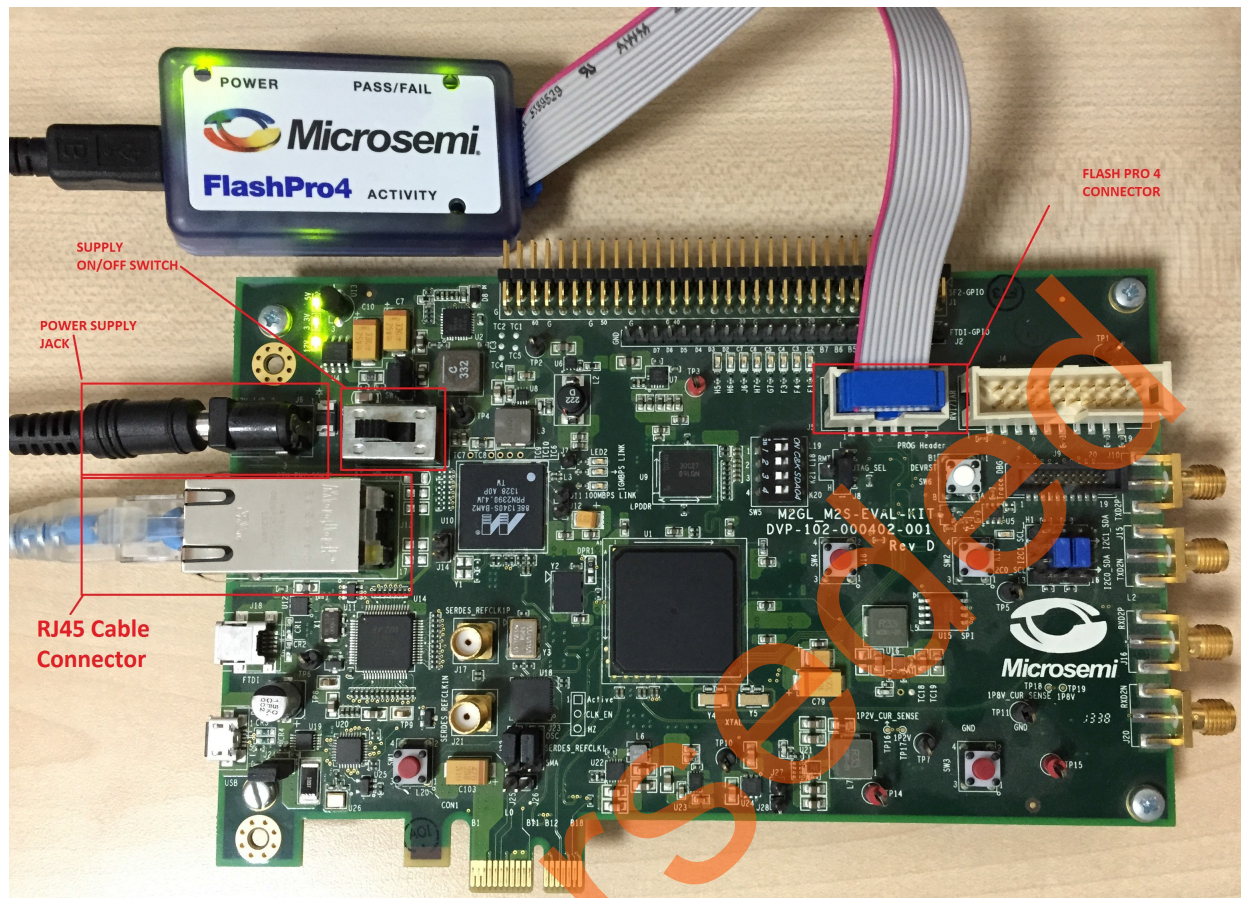
Figure 8 • FlashPro Programming Passed

2.4.2 Connecting SmartFusion2 Security Evaluation Kit Board to Host PC

The following steps describe how to connect the SmartFusion2 Security Evaluation Kit board to the host PC:

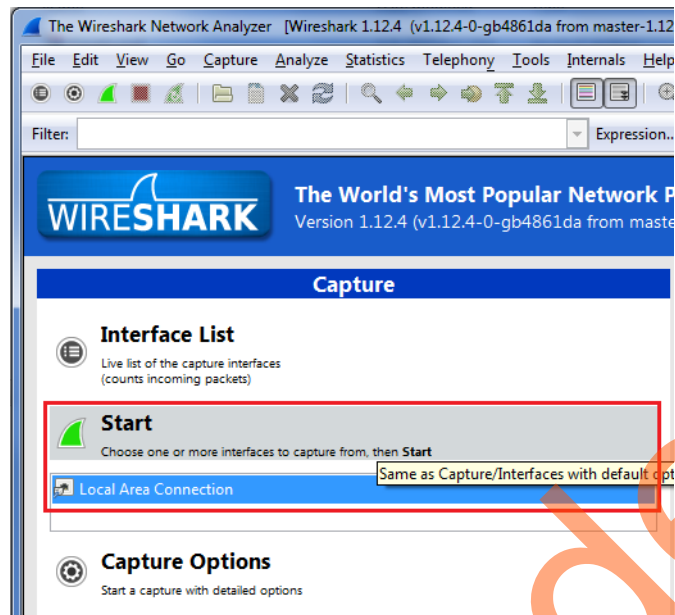
1. After successful programming, switch OFF the SmartFusion2 Security Evaluation Kit board.
2. Connect the host PC to the J13 connector on the SmartFusion2 Security Evaluation Kit using the RJ45 cable.

Figure 9, page 12 shows the SmartFusion2 Security Evaluation Kit board setup.

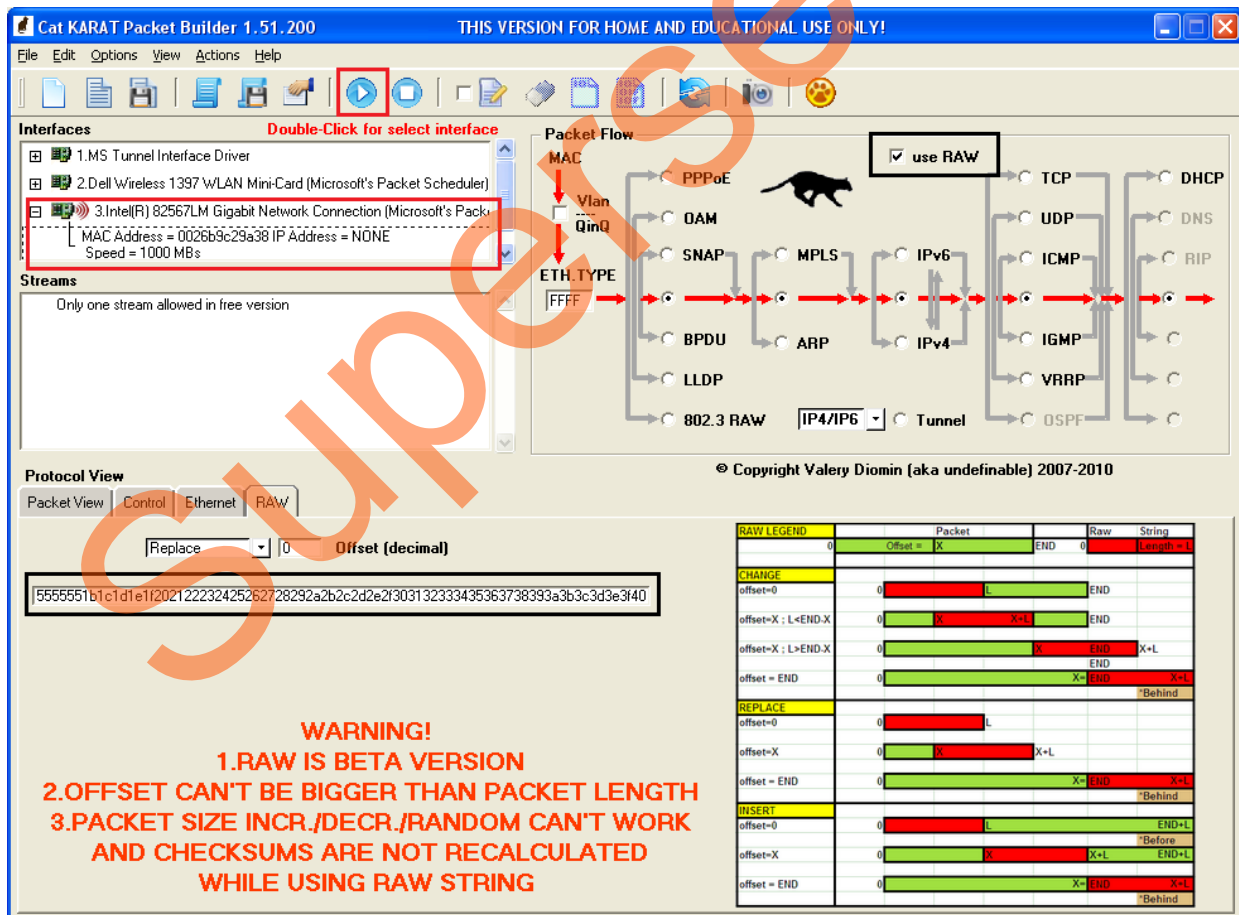
Figure 9 • SmartFusion2 Security Evaluation Kit Setup


2.4.3 Running the Demo Design with Cat Karat and Wireshark on the Hardware

1. Switch ON the power supply switch, SW7.
2. Install the Cat Karat packet software and Wireshark software on the host PC from the source files. (<download folder>\SF2_1000BaseT_loopback_demo_df\Source Files\)
3. On the host PC, open the Wireshark network analyzer. Select **Start** as shown in Figure 10, page 13.

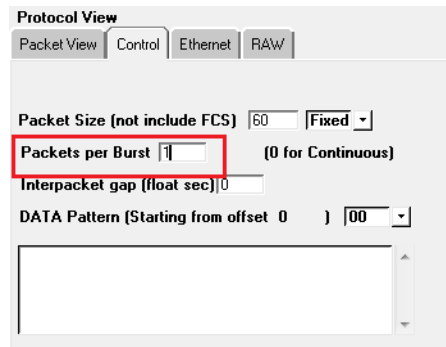
Figure 10 • Wireshark Network Analyzer

4. On the host PC, open the Cat Karat software, as shown in the following figure.

Figure 11 • Cat Karat Packet Generate Window

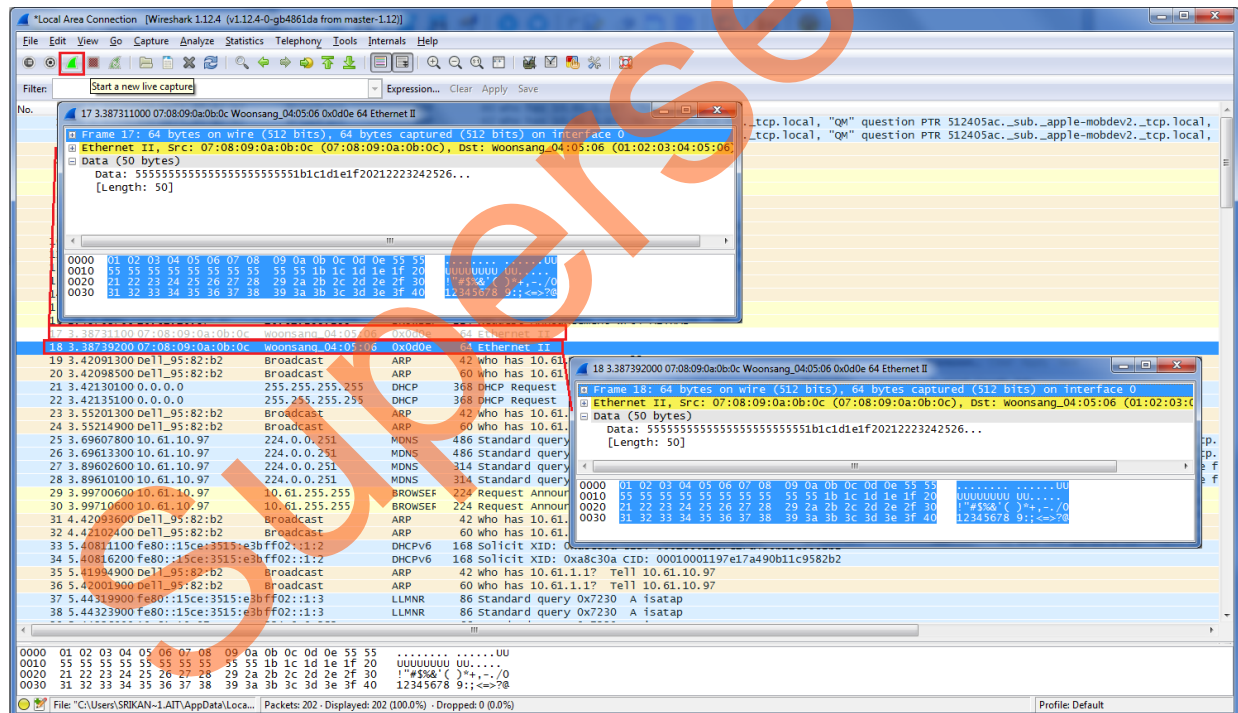
- Under **Protocol View**, select the **Control** tab and enter the value 1 for Packets per Burst, as shown in the following figure.

Figure 12 • Packet Flow Control



- Under **Packet Flow**, select use **RAW**, as shown in Figure 11, page 13.
- Under **Protocol View**, select the **RAW** tab and copy the Ethernet net packet from the source files (<download folder> SF2_1000BaseT_loopback_demo_df\Source Files\Raw_packet.txt), as shown in Figure 11, page 13.
- Under **Interfaces**, select the Ethernet connection to the SmartFusion2 Evaluation board.
- Select **Start Transmit** from the menu, as shown in Figure 11, page 13, to transmit the packet.
- In the Wireshark software window, double-click Ethernet-II, as shown in the following figure. The transmitted and received Ethernet packets are displayed.

Figure 13 • Wireshark Software Window

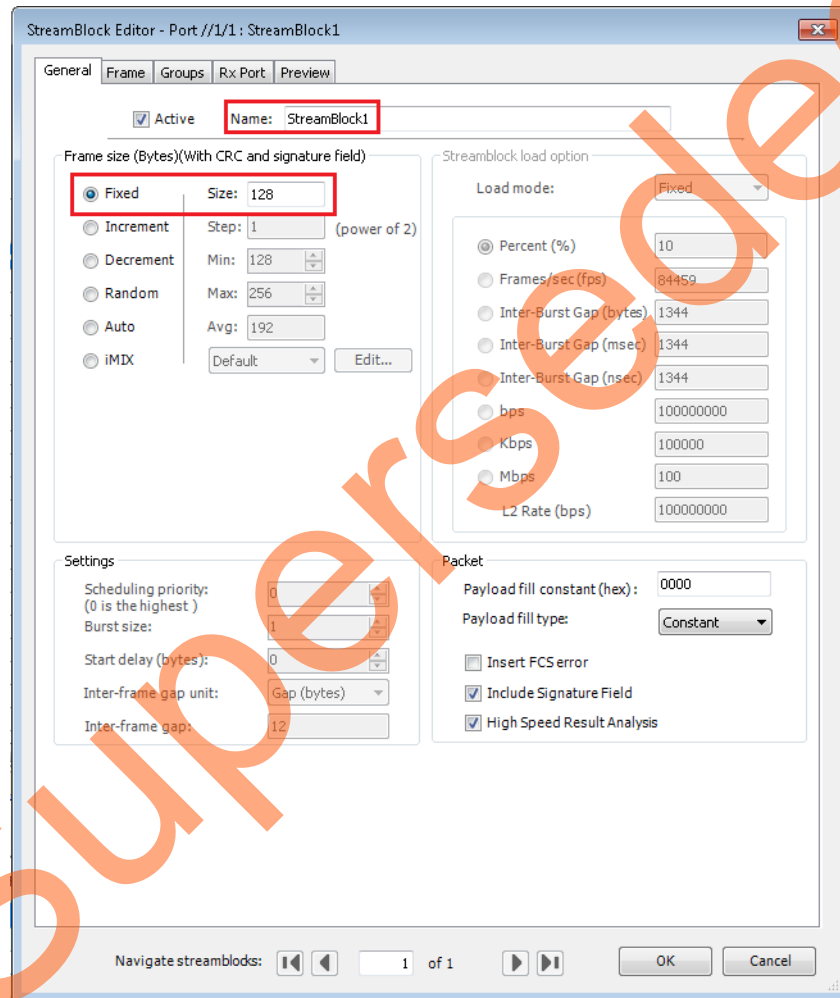


3 Appendix: Running the Demo Design Using Spirent Test Center

The following steps describe how to run the CoreTSE_AHB loopback demo using Spirent test center:

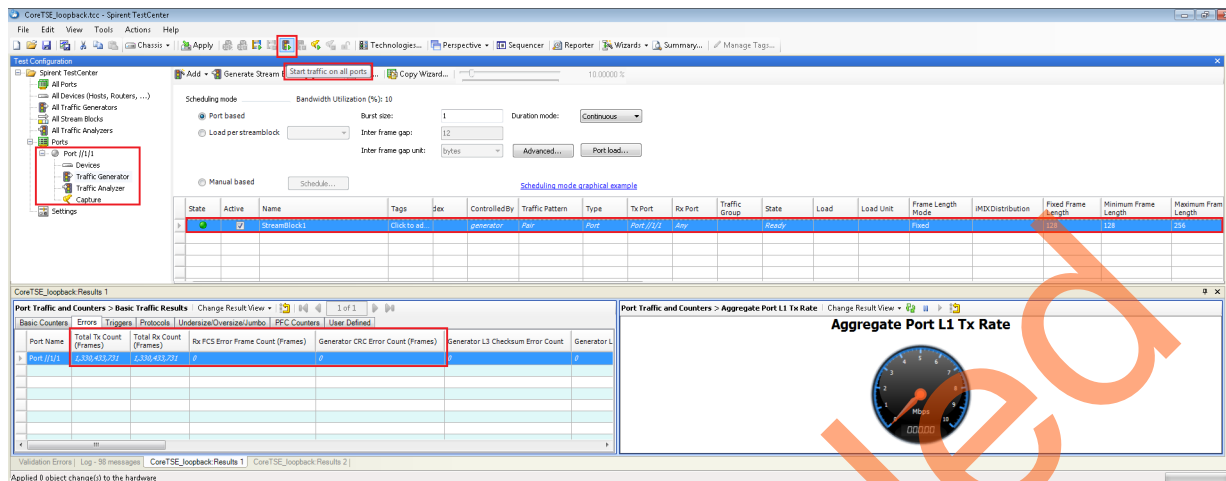
1. Connect the SmartFusion2 Security Evaluation Kit to the slot 1 Ethernet port on the Spirent test equipment using the RJ45 cable.
2. In the host PC, open the Spirent test center configurator.
3. Add port (Ethernet) in Spirent test center, as shown in the following figure.

Figure 14 • Spirent Test Center Stream Block – General Tab



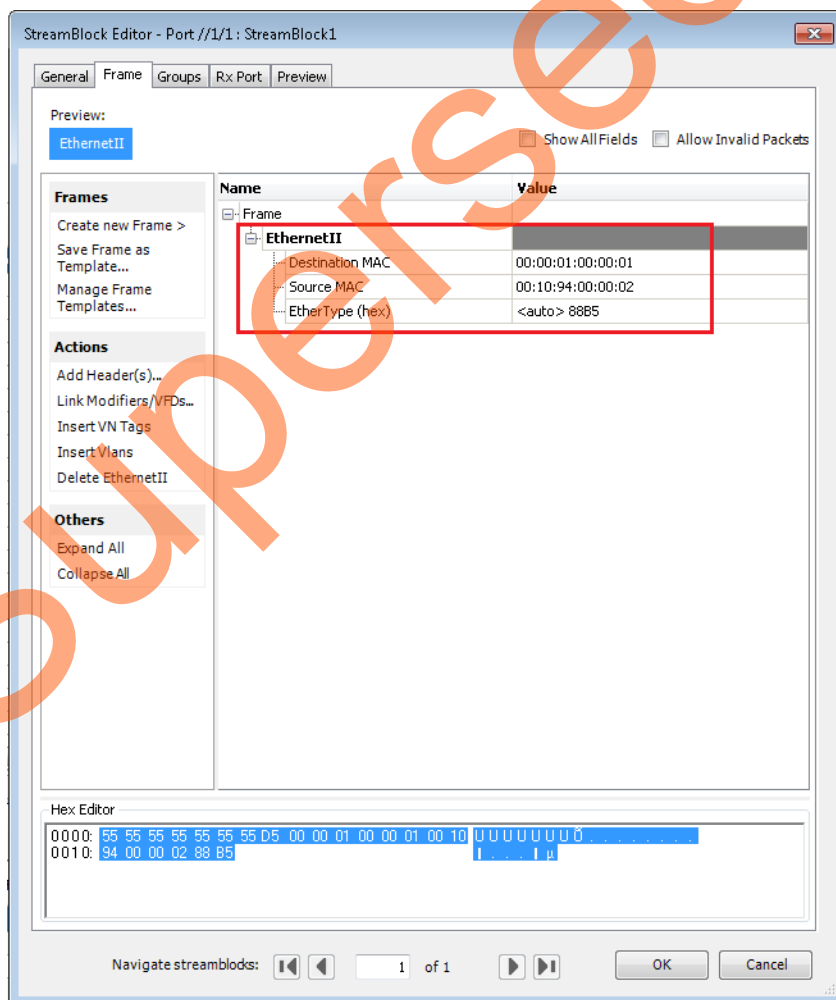
4. Select **Traffic generator** under **Port**, add packet information in stream block editor, and click **OK**, as shown in the following figure.

Figure 15 • Spirent Test Center



5. Click **Start traffic on all ports**, as shown in the following figure. Ethernet packets are transmitted and received on port 1 through the RJ45 cable.

Figure 16 • Spirent Test Center Stream Block – Frame Tab



6. Observe the total TX, RX, RX FCS, and CRC error counts.
[Figure 16](#), page 16 shows the total TX, RX, RX FCS, and CRC error count information in Spirent test center. 0 indicates no loss in the packet transmission and reception.

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