Power Matters™

Libero® SoC Design Suite

Microsemi
Power Matters.™

Introduction to Libero SoC Design Suite

The Libero® SoC Design Suite enables high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools for designing with Microsemi's power–efficient flash SmartFusion®2, IGLOO®2, and RTG4™ FPGAs. The suite integrates industry –standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation tools with best-in-class constraints management, debug capabilities, and secure production programming support.

Comprehensive

Design Entry	—	create full designs, sub-systems, testbenches, or use IPs with VHDL, Verilog, SystemVerilog or SmartDesign
Simulation	—	functional, gate-level, and timing verification using Mentor Graphics ModelSim
Synthesis	—	design optimization for power and performance using Synopsys Synplify Pro
Place and Route	—	optimize design for timing and performance. Reduce runtime with advanced, incremental, and multi-pass layout options
Power Analysis	—	in-depth visualization of power consumption for each individual design element using SmartPower
Timing Analysis	—	support for multiple constraint scenarios to optimize timing using SmartTime
Programming	—	complete solution with industry's first Secure Production Programming Solution (SPPS)
Debug	—	best-in-class debug solution with SmartDebug and Synopsys Identify

Easy-to-Learn

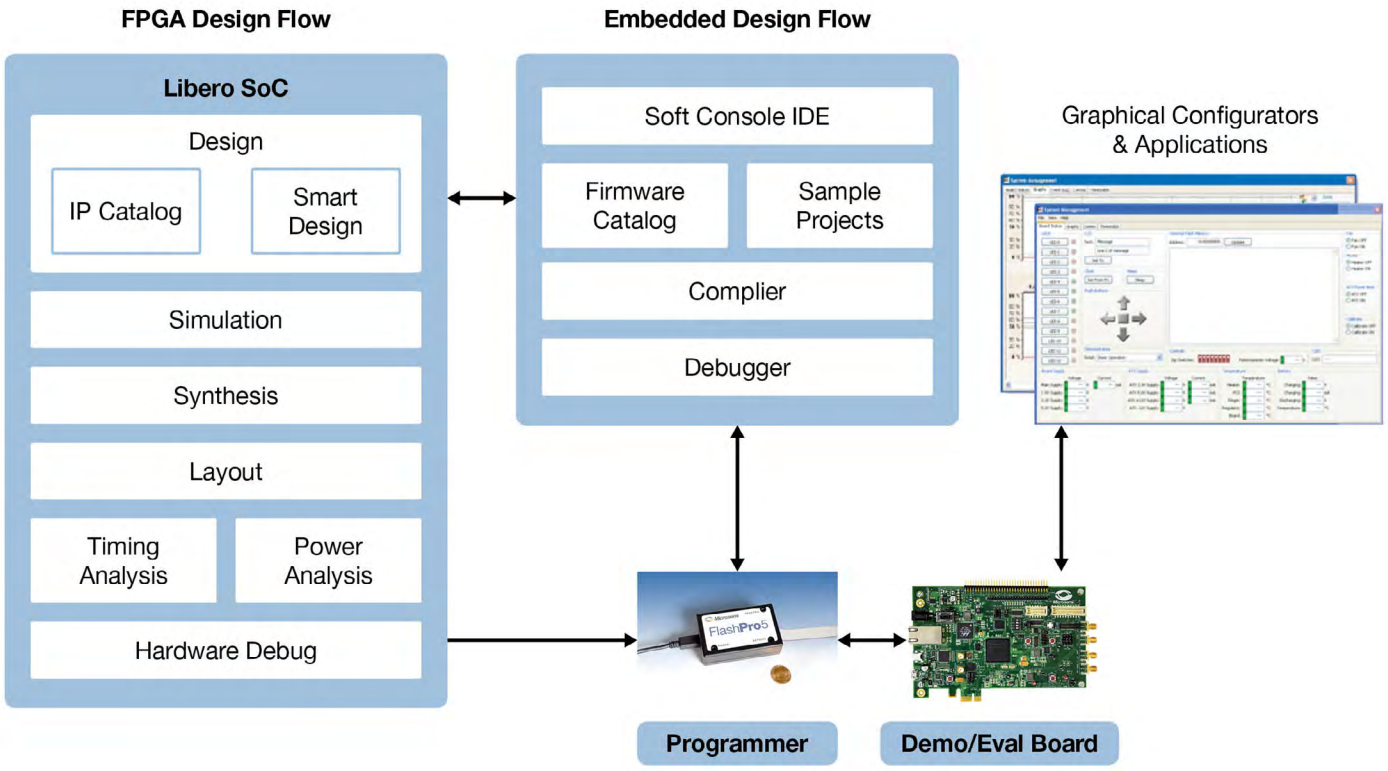
- Intuitive design flow
- GUI wizards to guide through the design process

Easy-to-Adopt

- Single-click flow from synthesis to programming
- Integrates industry-standard third-party tools
- Rich IP library of DirectCores and CompanionCores
- Complete reference designs and development kits available

Libero Design Flow

Libero SoC Design suite provides a comprehensive design flow including traditional FPGA Design flow, Embedded design flow and graphical configurators. FPGA design flow is the standard VLSI design flow starting from design entry till programing and debug. The embedded design flow enables development of embedded processing solutions for high performance and high reliability applications using low-power SoC FPGAs and FPGAs. It provides comprehensive development environment to build embedded solutions using hard core and soft core processors. Graphical configurators provide a user friendly design entry approach for various peripherals, applications and solutions.



Path to Design Acceleration

- Dedicated probe points allow debug without recompilation and minimal resource utilization
- Best-in-class power, performance, and area optimization options for synthesis, place, and route
- Centralized GUI to apply, edit and manage constraints through Constraints Manager flow
- Provide better timing results by enabling cross-probing between SmartTime and ChipPlanner
- Prevent overbuilding and cloning with SPPS

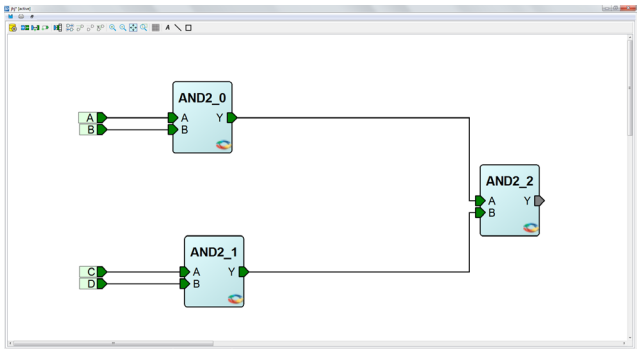
Differentiated Features

The Libero SoC design suite comes with following differentiated features that increase security, usability, and efficiency of FPGA designs, enabling faster time-to-market.

Block–Based Design Using SmartDesign

A block diagram approach for visualization, instantiation, and connection of the design. Provides a simple and intuitive tool, enabling you to work at the abstraction level at which you are most comfortable. Can be used to implement an entire FPGA design, part of a larger design, or a user–created IP that can be stored and used multiple times.

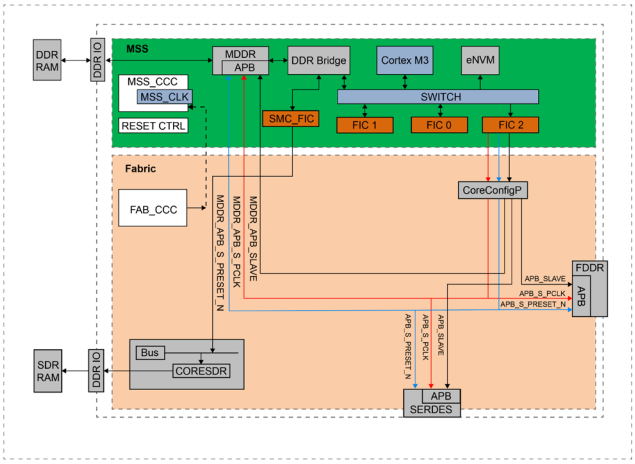
- Easy–to–build design using IP cores, HDL modules, and more.
- Enables creation of parameterized blocks from HDL modules and instantiating/configuring them into SmartDesigns.



System Builder for Easy Processor Configuration

The System Builder design tool for SmartFusion2 ARM-based SoC designs now offers an improved graphical interface with a broader range of integrated blocks and IPs. This enables fast and reliable automated system configuration and assembly. It is an easy-to-use design tool that walks you through a set of high-level questions, enabling you to define your intended system.

- Allows creation of system-level embedded designs using ARM Cortex-M3 processor and fabric peripherals
- Single-click flow to configure Microcontroller Subsystem (MSS)
- The built-in design rule check feature prevents the creation of a design containing mistakes or conflicts
- Rich library of integrated blocks and IPs



Constraint Management Flow

Microsemi's Constraints Manager Flow enables management of timing, input/output (I/O) attribute, floor planning, and netlist attribute constraints to ensure that they can be created, imported, edited, and organized in a single view. These constraints are file-based and human–readable, so that is what you see is what you get.

- Ability to verify constraints before place and route
- Flexibility to apply constraints at any stage of the design
- Derives clock constraints automatically for known sources (CCCs, OSC, SerDes, and MSS)
- Generates automatic constraints for synthesis
- Enables cross probing between SmartTime and ChipPlanner

Differentiated Features

SmartTime Static Timing Analysis Tool

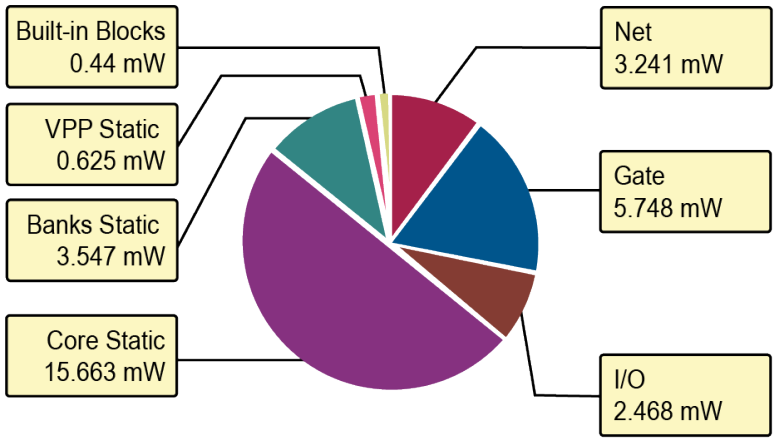
SmartTime is the Libero SoC static timing analysis tool. With SmartTime, you can perform a complete timing analysis of your design to ensure that all timing constraints are met, and that the design operates at the desired speed and amount of margin across all operating conditions.

- Supports a wide range of timing constraints to provide useful analysis
- Option to create multiple scenarios for the design

SmartPower for Detailed Power Analysis and Power Scenario Testing

Enables in-depth visualization of actual and potential power consumption of your design. This will help you to make adjustments, to reduce power, when possible. It also generates detailed hierarchical power consumption reports for easy evaluation.

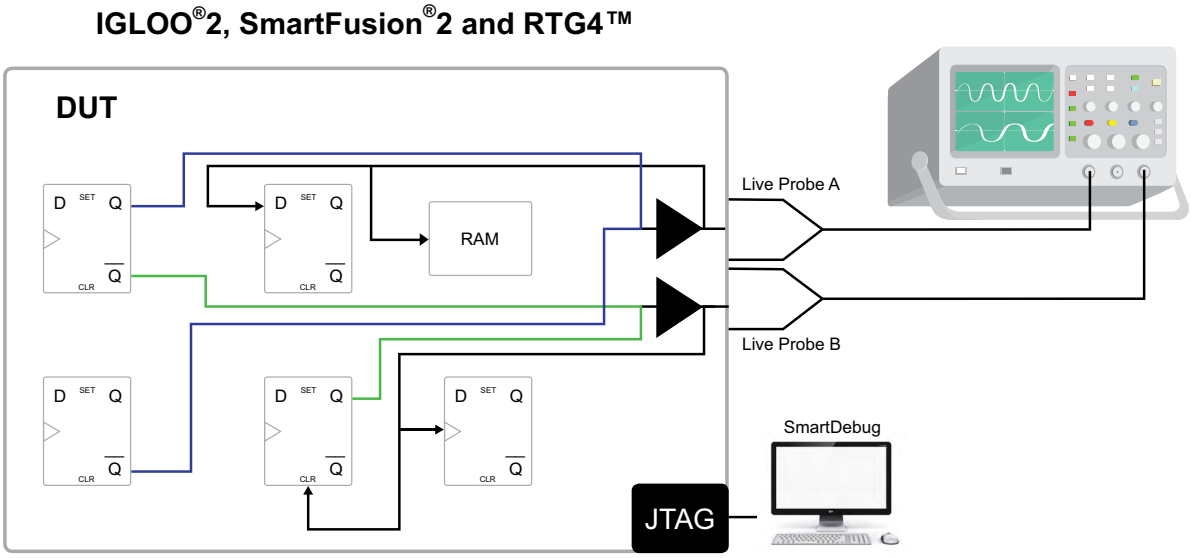
- The only tool to allow creation of test scenario profiles
- Displays static and dynamic power values of the design
- Analyzes power at every power cycle
- Details power consumption in the design by nets, gates, I/O, memory, and so on
- Allows setting of the battery capacity and generation of battery life reports
- Provides option to import user VCD from timing level simulation for accurate activity



SmartDebug

The SmartDebug tool is a new approach to debug the Microsemi FPGAs and SerDes without using an integrated logic analyzer (ILA). SmartDebug utilizes the dedicated and specialized probe points built into the FPGA fabric, significantly accelerating and simplyfing debugging. It also provides the ability to select different probe points without additional overhead and saves significant recompile time. The enhanced debug features implemented in these SmartFusion2, IGLOO2 and RTG4 FPGAs give access to any logic element and enable designers to check the state of flip-flop in real time, without any need for re-design.

- Uses minimal FPGA resources for debug
- Active probes support static and pseudo static signals
- Live probe supports dynamic signals
- Requires no recompilation or re-programming
- Has observability and controllability features
- Allows for on-the-fly changing of probe points



FPGA Hardware Breakpoint Auto Instantiation

The FPGA Hardware Breakpoint (FHB) Auto Instantiation feature automatically instantiates an FHB per clock domain using gated clocks. The FHB instances gate the clock domain they are instantiated on. These instances can be used to force halt the design or halt the design through a live probe signal. Once a selected clock domain or all clock domains are halted, you can play or step on the clock domains, either selectively or all at once. The FHB controls in the Smart Debug UI allow you to control the debugging cycle.

FHB comes with two clock domain options - Operate on All Clock Domains and Operate on Selected Clock Domain

The Trigger Signal updates when a live probe is assigned. Clicking on the Arm Trigger, makes the design halts on the next positive edge that occurs on the signal connected to Live Probe.

When a certain number of clock cycles are required before halting the clock domain after triggering, a value between 0 and 255 must be entered for Delay Cycles Before Halt. This sets the FHBs to trigger after the specified delay from the rising edge trigger.

Provision to save the waveform view of the selected active probes using Export Waveform by specifying the number of clock cycles to capture. The waveform is saved to a .vcd file.

Highly Differentiated Features

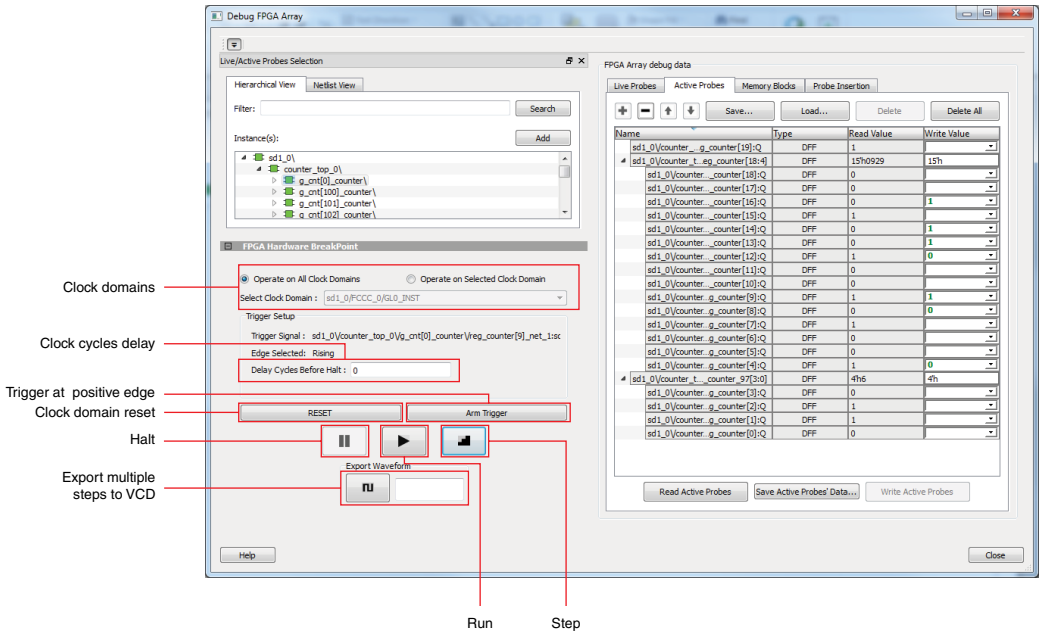
Halt operation will force halt a selected clock domain or all clock domains based on mode selection

Run operation will run a selected clock domain from halt state (live probe halt or force halt)

Step operation will run a selected clock domain for one clock cycle

Export Waveform will capture and save the waveform view (.vcd) for the selected active probes for the specified number of clock cycles

Reset will reset a selected clock domain or all clock domains

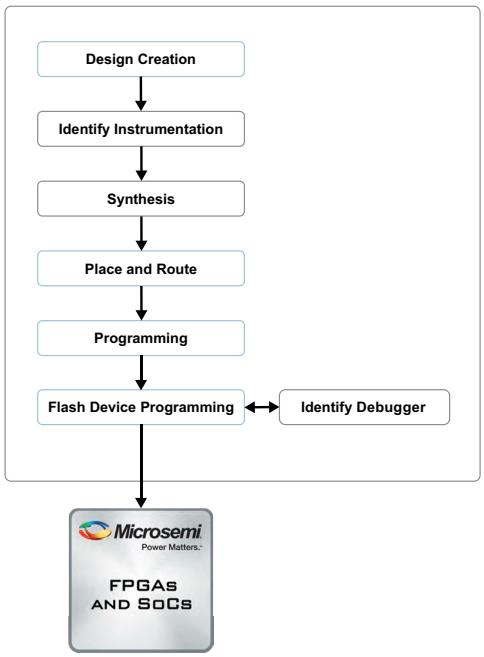


Identify ME

Libero SoC utilizes the Synopsys Identify ME debugger tool. The Identify RTL tool probe and debug your FPGA design directly with in the source RTL. Use Identify software when the design's behavior after programming does not match the simulation results. Identify ME supports all flash FPGA families.

- Adds probe points inside pre-synthesized design
- Monitors dynamic signals with a recompile option
- Debugs internal signals and external I/Os
- Provides options for advanced triggering
- Debug results can be overlayed on top of HDL design

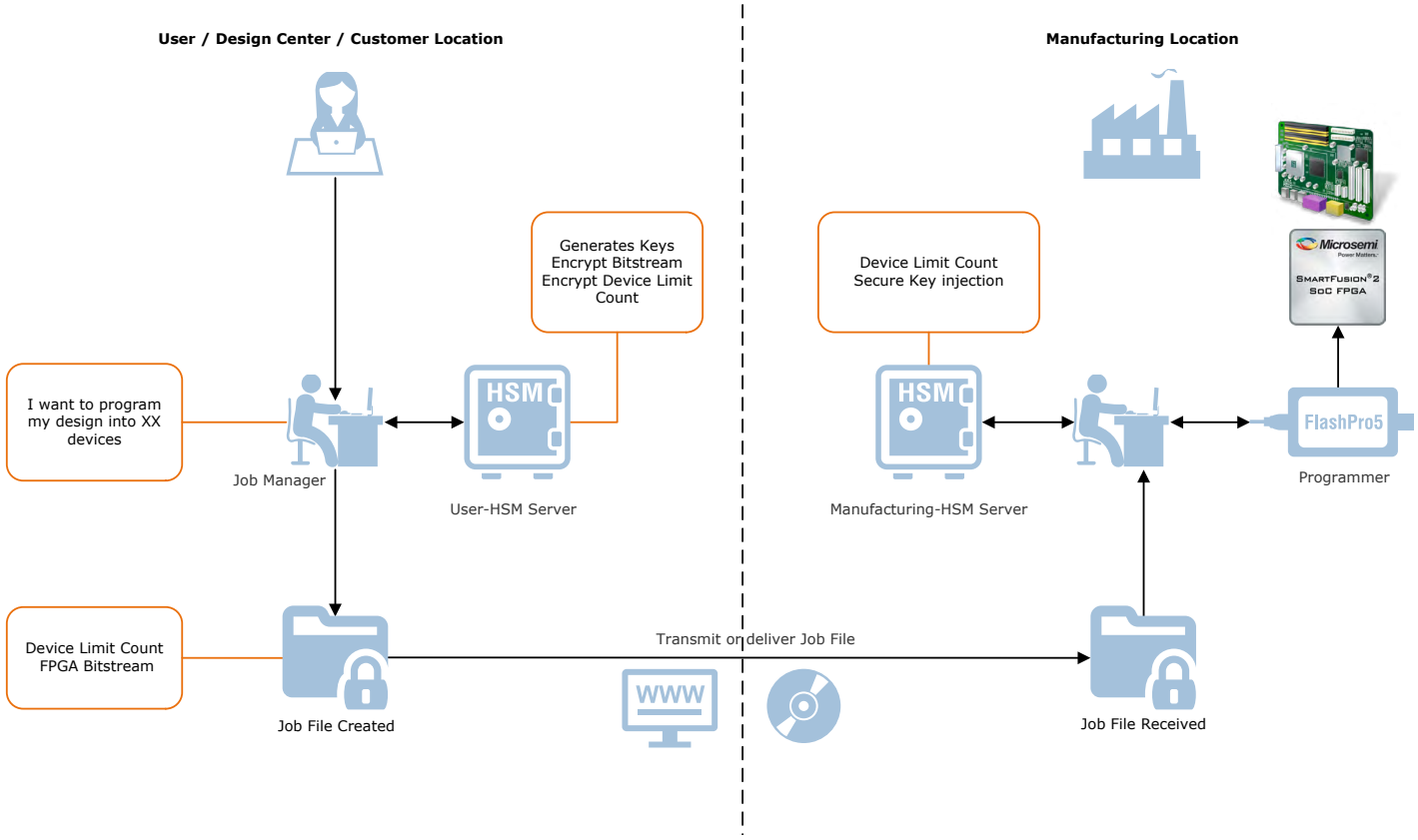
Identify Flow



Highly Differentiated Features

Secured Production Programming Solution (SPPS) Prevents Overbuilding and Cloning

SPPS enables secured production programing of Microsemi FPGAs and SoCs by generating and injecting cryptographic keys and configuration bitstreams. This prevents cloning, reverse engineering, malware insertion, IP leaks, overbuilding, and other security threats. It is the ideal solution for eliminating the risk of overbuilding customer systems. It builds upon existing hardware security modules (HSMs), custom firmware, and state-of-the-art security protocols built into Microsemi SmartFusion2 SoC FPGA and IGLOO2 FPGA families to automatically prevent overbuilding.



- Supports multiple programming file formats
- Single- and chain-programming support using SPI and JTAG programming modes
- Auto-update and programming recovery modes
- Interfaces software and hardware security modules
- Allows initial key loading in unstructured environment
- Leverages underlying SmartFusion2 and IGLOO2 security protocols
- Validates Microsemi devices that can be programmed
- Controls the exact number of devices to be programmed

Libero Licensing Information

Supported Devices

Product Family	Device	Software		License Type			
		Libero IDE	Libero SoC	Eval (Free)	Silver (Free)	Gold	Platinum/ Standalone
RTG4	RT4G150		✓	✓			✓
SmartFusion2, IGLOO2	M2S005, M2S010, M2S025 (T devices included) M2GL005, M2GL010, M2GL025 (T devices included)		✓	✓	✓	✓	✓
	All SmartFusion2 and IGLOO2 devices (S devices included)		✓	✓		✓	✓
SmartFusion, IGLOO, ProASIC3, Fusion	All devices		✓	✓	✓	✓	✓
ProASIC and ProASIC^{PLUS}	All devices	✓				✓	✓
RTAX-S	RTAX250S, RTAX1000S	✓				✓	✓
	RTAX2000S, RTAX4000S	✓					✓
RTAX-DSP	RTAX2000D, RTAX4000D	✓					✓
RT ProASIC3	RT3PE600L		✓	✓		✓	✓
	RT3PE3000L		✓	✓			✓
RTSX-SU	All devices	✓				✓	✓
Axcelerator	AX125, AX250, AX500, AX1000	✓				✓	✓
	AX2000	✓					✓
SX-A, eX, MX	All devices	✓				✓	✓

License Types

	Evaluation	Silver	Gold	Platinum	Platinum Archival	Standalone Archive	Standalone (1 Year)
Validity	60 days	1 Year	1 Year	1 Year	20 Years (No Upgrades)	Permanent (No Upgrades)	1 Year
Licensing Requirements per Device	See Supported Devices table above			All	All	All	All
IP DirectCores	Libero IP bundle obfuscated and selected RTL IPs		RTL for Libero IP bundle cores				
SoftConsole		✓	✓	✓	✓	✓	✓
Simulation	Mixed language	Single language	Mixed language	Mixed language	Mixed language		
Synthesis (Synplify Pro)	✓	✓	✓	✓	✓		
Programming		✓	✓	✓	✓	✓	✓
Debug		Identify and SmartDebug*	Identify and SmartDebug*	Identify and SmartDebug*	Identify and SmartDebug*	SmartDebug*	SmartDebug*
Price / Renewal	$0 (Node Locked, and Floating)	$0 (Node Locked, and Floating)	$995 / $695 (Node Locked and Floating)	$2995 / $2495 (Node Locked) $3495 / $2995 (Floating)	$6995 (USB Node Locked)	$6995 (Floating)	$1995 /$1495 (Node Locked and Floating)

Note: Evaluation and Silver licenses are supported from Libero SoC v11.8 and later releases only.

*SmartDebug is supported for SmartFusion2, IGLOO2 and RTG4 only

Additional Resources

- The latest version of Libero SoC: http://www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-soc#downloads
- Documentation: http://www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-soc#documents
- Libero SoC videos: http://www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-soc
- Programming and debug tools : http://www.microsemi.com/products/fpga-soc/design-resources/programming-debug-tools
- Power calculators: http://www.microsemi.com/products/fpga-soc/design-resources/power-calculator
- DirectCores: http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores#directcores
- CompanionCores: http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores#companioncores
- IP core design examples: http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores#design-examples
- FPGA and SoC catalog: http://www.microsemi.com/document-portal/doc_download/131351-fpga-and-soc-productcatalog
- SynplifyPro ME tool: https://www.microsemi.com/products/fpga-soc/design-resources/design-software/synplify-pro-me
- ModelSim ME tool: https://www.microsemi.com/products/fpga-soc/design-resources/design-software/modelsim
- Synphony Model Compiler tool: https://www.microsemi.com/products/fpga-soc/design-resources/design-software/synphony
- SoftConsole tool: https://www.microsemi.com/products/fpga-soc/design-resources/design-software/softconsole
- Libero Licensing: https://www.microsemi.com/products/fpga-soc/design-resources/licensing
- Programming and Debug: https://www.microsemi.com/products/fpga-soc/design-resources/programming-debug-tools

For more information on Libero SoC, visit: http://www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-soc#overview

Notes

Microsemi is continually adding new products to its industry-leading portfolio.

For the most recent updates to our product line and for detailed information and specifications, please call, email, or visit our website.

Toll-free: 800-713-4113

sales.support@microsemi.com

www.microsemi.com

Microsemi
Power Matters.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo, CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

Libero-Brochure. 1.0. 04/17