Enhanced Low Dose Rate Sensitivity (ELDRS) Radiation Testing of the Microsemi LX7730 Telemetry Controller (50krad(Si) exposure)

Test information

Location: Survivability, Vulnerability Assessment Directorate (SVAD), White Sands Missile Range, NM 88002
Radiation Source: Co-60
Test Completion Date: 18th January 2017
Lot #: Die1: T71899 - Die2: E27915
Date Code: 1612
Quantity tested: 9; Serial Numbers: 112, 116, 136, 185, 187, 196, 218, 233 and 237
Test Method: MIL-STD-883J, Test Method 1019.9, Condition D (Dose rate 0.01rad(Si)/s)
Irradiation Temperature: Room
Irradiation Bias (VCC/VDD): Static at 15V/3.3V
Pre and Post Test facility: Microsemi - San Jose

Summary

The LX7730 performance after 50krad(Si) ELDRS exposure is overall very stable and comparable to pre-radiation.
A few shifts that could push some parameters outside the pre-radiation specification were observed:

- Programmable current source
  - Full scale decreases by about 2-2.5% (same behavior observed during TID)
- Instrumentation amplifier
  - Offset variation of up to 8mV at gain=0.4, 5mV at gain=2 and 4mV at gain=10 were observed (same behavior observed during TID)
- Adjustable threshold Bi-level MUX and DAC
  - The threshold might shift by up to 25mV and the hysteresis is halved when the comparator input is biased between 0 and 5V (similar behavior, but slightly less pronounced, observed during TID)
  - The threshold might shift by up to 0.2V and the hysteresis is halved when the comparator input is biased at a negative voltage (similar behavior, but slightly less pronounced, observed during TID)
- Fixed Threshold Bi-Level Inputs
  - The threshold might shift by up to 20mV and the hysteresis is reduced by up to 20mV (same behavior observed during TID)
  - The propagation delays increase by up to 65% (similar behavior, but slightly less pronounced, observed during TID)

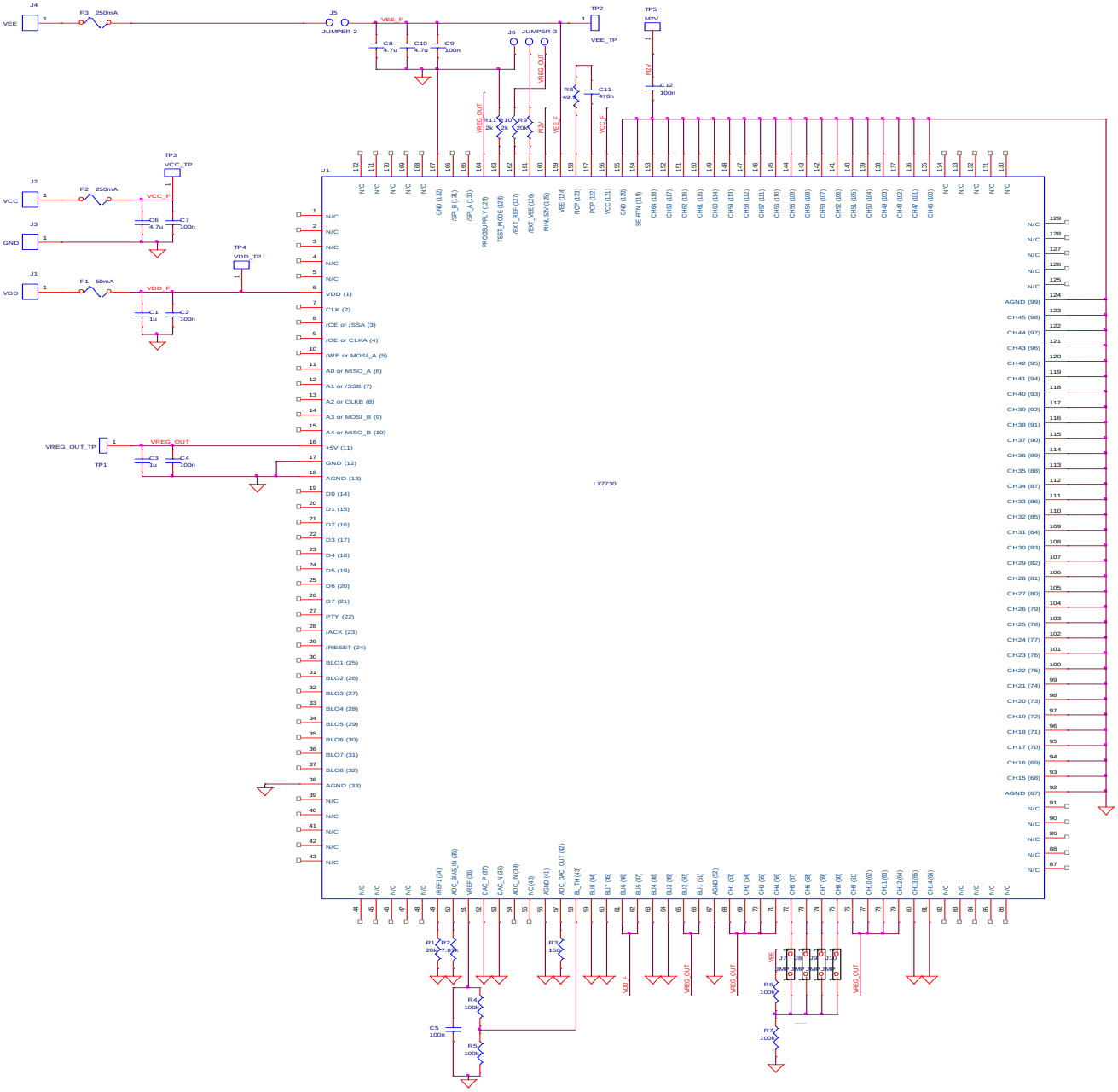
Conclusions

The test results indicate that after 50kRad ELDRS exposure, the performance of the LX7730 is consistent with the pre-radiation results. ELDRS results are consistent with TID results.

The few observed performance degradations can be mitigated at the system level as follows:

- Programmable current source full scale shift
  - Providing a method to calibrate the variation in programmable current using a precision current sense resistor on a dedicated calibration channel
- Instrumentation amplifier offset shift
  - The offset voltage can be assessed using a 100mV reference from a VREF voltage divider on a dedicated channel.
- Adjustable threshold Bi-level MUX and DAC shift
  - The threshold shift can be minimized by ensuring the comparator input is not biased with a negative voltage.

Bias circuit



Detailed Results

The pre Radiation specifications apply over the operating ambient temperature of -55C ≤ T_A ≤ 125C except where otherwise noted with the following test conditions: VCC = 15V, VDD = 3.3V; R_{IREF} = 20kΩ; $R_{ADC\_BIAS\_IN}$ = 7.87kΩ; $R_{ADC\_DAC\_OUT}$ = 158Ω; / EXT_VEE open, /EXT_REF open. CH1 and CH2 selected and CH2 grounded. CLK = 500kHz. Reg 7 =001010xx. Typical parameter refers to T_J = 25°C. Positive currents flow into the pin.

Pre and Post Irradiation measurements taken at 25C.

Parameters	Pre Radiation Specification				Post 25k ELDRS	Post 50k ELDRS	Comment	Comparison to 100k TID
	Min	Typ	Max	Units				
Operating Current								
VCC Normal Current	38	73	84	mA	All Units Pass pre rad spec	All Units Pass pre rad spec	Slight decrease	TID units decrease less
VCC Standby Current	2.0	4.0	7.0	mA	All Units Pass pre rad spec	All Units Pass pre rad spec	Stable	TID units have slight increase
VEE Current	-6.0	-5.0	-2.5	mA	All Units Pass pre rad spec	All Units Pass pre rad spec	Slight increase	TID units increase less
Under Voltage Detection								
VCC UVLO	9.5	10	10.5	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
VCC UVLO Hyst	150	200	400	mV	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
VEE UVLO	-7.5	-8.00	-8.20	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Slight Decrease	Same behavior
VEE UVLO Hyst	150	200	400	mV	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
+5V UVLO	3.9	4.15	4.40	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
+5V UVLO Hyst	0	200	400	mV	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Internally Regulated Voltages and Currents								
VCC to VEE voltage drop	1.5	2.5	3.0	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Slight Decrease	Same behavior
+5V voltage	4.75	5.00	5.25	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
VREF voltage	4.95	5.00	5.05	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
IREF pin voltage	1.568	1.60	1.632	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Analog MUX								
Differential Range	0		5	V	Pass	Pass		
Common Mode Range	-5		5	V	Pass	Pass		
Voltage Clamp power applied	15	16	17	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
	-23	-17	-15	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Voltage Clamp (VCC=VEE=0)	15	20	23	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
	-23	-20	-15	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Settling Time			10	us	All Units Pass pre rad spec	All Units Pass pre rad spec	50% increase at 50krad	50% increase at 100krad
Bias Current	-200	0	200	nA	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Leakage Current	-200	0	200	nA	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Programmable Current Source								

Parameters	Pre Radiation Specification				Post 25k ELDRS	Post 50k ELDRS	Comment	Comparison to 100k TID
	Min	Typ	Max	Units				
Full scale current (doubWt OFF)	1.880	1.940	2.000	mA	All Units Pass pre rad spec	All Units Pass pre rad spec	~2-2.5% Decrease at 50k	Same behavior (~4-5% Decrease at 100k)
Integral nonlinearity	-7.5	0	7.5	µA	All Units Pass pre rad spec	All Units Pass pre rad spec	Stable	Stable
Differential nonlinearity	-5.0	0	5.0	µA	All Units Pass pre rad spec	All Units Pass pre rad spec	Stable	Stable
Full scale current (doubWt ON)	3710	3840	3950	µA	All Units Pass pre rad spec	All Units Pass pre rad spec	~2-2.5% Decrease at 50k	Same behavior (~4-5% Decrease at 100k)
Integral nonlinearity	-15		15	µA	All Units Pass pre rad spec	All Units Pass pre rad spec	Stable	Stable
Differential nonlinearity	-15		15	µA	All Units Pass pre rad spec	All Units Pass pre rad spec	Stable	Stable
At DAC=31	290	300	310	uA	All Units Pass pre rad spec	Some Units Fail pre rad spec	~2-2.5% Decrease at 50k	Same behavior (~5-6% Decrease at 100k)
Integral nonlinearity	-2.0		2.0	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Stable	Some increase
Differential nonlinearity	-2.0		2.0	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Stable	Stable
Instrumentation Amplifier								
Offset Voltage, Gain = 0.4	-2		25	mV	All Units Pass pre rad spec	Some Units Fail pre rad spec	Up to 5mV increase at 50k	Up to 7mV increase at 100k
Offset Voltage, Gain = 2	-3		3	mV	All Units Pass pre rad spec	Some Units Fail pre rad spec	Up to 5mV change at 50k	Up to 4mV change
Offset Voltage, Gain = 10	-3		3	mV	All Units Pass pre rad spec	Some Units Fail pre rad spec	Up to 4mV change at 50k	Up to 3mV change
Gain Accuracy, Gain = 0.4	0.398	0.400	0.402	-	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Gain Accuracy, Gain = 2	1.992	2.000	2.004	-	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Gain Accuracy, Gain = 10	9.965	9.995	10.025	-	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
400Hz 1st Pole Frequency	360	600	1000	Hz	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
2kHz 1st Pole Frequency	1.4	2.8	3.8	kHz	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
10kHz 1st Pole Frequency	8.8	13.5	18.2	kHz	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
400Hz 2nd Pole Frequency	360	600	1000	Hz	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
2kHz 2^{nd} Pole Frequency	1.4	2.8	3.8	kHz	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
10kHz 2^{nd} Pole Frequency	8.8	13.5	18.2	kHz	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Output Step Rise Time, G=0.4	120	210	333	us	All Units Pass pre rad spec	All Units Pass pre rad spec	~15% Increase after 50k	TID units increase less (~15-17% Increase after 100k)
Output Step Rise Time, G=2	31	52	87	us	All Units Pass pre rad spec	All Units Pass pre rad spec	~10% Increase after 50k	TID units increase less (~8-10% Increase after 100k)
Output Step Rise Time, G=10	31	52	87	us	All Units Pass pre rad spec	All Units Pass pre rad spec	~10% Increase after 50k	TID units increase less (~8-10% Increase after 100k)
Analog-to-Digital Converter (input at ADC_IN)								
Linear Range	0		2.0	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Full scale error	-2.5	0	2.5	%	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Offset Error	-10		10	mV	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Integral nonlinearity	-6		6	LSB	All Units Pass pre	All Units Pass pre	Very stable	Very stable

Parameters	Pre Radiation Specification				Post 25k ELDRS	Post 50k ELDRS	Comment	Comparison to 100k TID
	Min	Typ	Max	Units				
					rad spec	rad spec		
Differential nonlinearity	-1		3	LSB	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Leakage current	-0.2	0	0.2	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Adjustable threshold Bi-level MUX and DAC								
Threshold DAC Max Output (If input is >=0V during TID)	4.95	5	5.05	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Up to 25mV increase at 50k	Same behavior (Up to 50mV increase at 100k)
Hysteresis DAC Max Output (If input is >=0V during TID)	0.075	0.112	0.150	V	All Units Pass pre rad spec	All Units Fail pre rad spec	~50% decrease at 50k	TID units decrease less (~25% decrease at 100k)
Threshold DAC Max Output (If input is VEE/2 during TID)	4.95	5	5.05	V	All Units Fail pre rad spec	All Units Fail pre rad spec	~4% decrease at 50k	TID units decrease more (~10% decrease)
Hysteresis DAC Max Output (If input is VEE/2 during TID)	0.075	0.112	0.150	V	All Units Pass pre rad spec	Some Units Fail pre rad spec	~40% decrease at 50k	TID units decrease less (~20% decrease at 100k)
10 Bit Current DAC								
Full Scale	-2.06	-2.00	-1.94	mA	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Integral nonlinearity	-5		5	LSB	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Differential nonlinearity	-0.5		0.5	LSB	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
DAC Settling Time			1	us	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Fixed Threshold Bi-Level Inputs								
Threshold – Internal ref (Rising Voltage)	2.45	2.50	2.55	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Up to 20mV increase at 50k	Same behavior (Up to 35mV increase at 100k)
Threshold Hysteresis – Internal reference	60	120	180	mV	All Units Pass pre rad spec	All Units Pass pre rad spec	Up to 20mV decrease at 50k	TID units decrease less (up to 10mV decrease at 100k)
Threshold – External 2.5V (Rising Voltage)	2.45	2.50	2.55	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Up to 20mV increase at 50k	Same behavior (Up to 40mV increase at 100k)
Threshold Hysteresis – External 2.5V	60	120	180	mV	All Units Pass pre rad spec	All Units Pass pre rad spec	Up to 20mV decrease at 50k	TID units decrease less (up to 10mV decrease at 100k)
Voltage Clamp (power applied) – 1mA into the pin	15	20	23	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Voltage Clamp (power applied) – 1mA out of the pin	-23	-20	-15	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Voltage Clamp (power remove) – 1mA into the pin	15	20	23	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Voltage Clamp (power removed) – 1mA out of the pin	-23	-20	-15	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Bias Current at 5V	-0.2	0	1.5	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Bias Current at 0V	-0.2	0	1.5	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Leakage Current at 5V (power off)	-0.2	0	1.5	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Leakage Current at 0V (power off)	-0.2	0	1.5	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Propagation Delay - High to	0.3	0.8	1.3	us	All Units Pass pre rad spec	Some Units Fail pre rad spec	~30-65% increase after 50k	TID units increase less (~40-60% increase after

Parameters	Pre Radiation Specification				Post 25k ELDRS	Post 50k ELDRS	Comment	Comparison to 100k TID
	Min	Typ	Max	Units				
Low transition								100k)
Propagation Delay - Low to High transition	0.8	2.1	3.4	us	All Units Pass pre rad spec	Some Units Fail pre rad spec	~25-50% increase after 50k	TID units increase less (~25-40% increase after 100k)
Threshold Pin Leakage at 5V	-0.2	0	2.0	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Threshold Pin Leakage at 0V	-0.2	0	2.0	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Logic Levels for FPGA Interface I/Os								
Input Logic Threshold at 3.3V	1.155	1.65	2.145	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Stable	Stable
Program pins Threshold	2.0	2.5	3.0	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Stable	Stable
Logic Output VOH at 100uA at 3.3V	3.0		3.3	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Logic Output VOL at 100uA at 3.3V	0		0.3	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
IIH SPI_A, SPI_B (3.3V)	-2	0	2	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
IIL SPI_A, SPI_B (0V)	-10	-4	-1.5	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
IIH Pins 2,6,8-10,14-21, 22: I/O as input (3.3V)	1.5	4	10	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
IIL Pins 2,6,8-10,14-21, 22: I/O as input (0V)	-2	0	2	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
IIH Pins 3-5, 7 I/O as input (3.3V)	-2	0	2	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
IIL Pins 3-5, 7: I/O as input (0V)	-10	-4	-1.5	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
IIH /EXT_VREF or /EXT_VEE = 5V	-2	0	2	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
IIL /EXT_VREF or /EXT_VEE = 0V	-12	-6	-1.5	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
IIH /RESET (5V)	-1.5	4	10	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
IIL /RESET (0V)	-150	-66	-33	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable

Parameters tested but not specified

Parameters	Pre Radiation Test Limits				Post 25k ELDRS	Post 50k ELDRS	Comment	Comparison to 100k TID
	Min	Typ	Max	Units				
Instrumentation Amplifier								
Offset Voltage, Gain = 0.4 16V/3.3V	-2		32	mV	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Up to 7mV increase at 50k	Same behavior (Up to 8mV increase at 100k)
Offset Voltage, Gain = 0.4 11.4V/3.3V	-2		32	mV	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Up to 8mV increase at 50k	Same behavior (Up to 11mV increase at 100k)
Offset Voltage, Gain = 2 16V/3.3V	-3.5		4.5	mV	All Units Pass pre rad test limits	Some Units Fail pre rad test limits	Up to 5mV change at 50k	Same behavior (Up to 3mV change at 100k)

Parameters	Pre Radiation Test Limits				Post 25k ELDRS	Post 50k ELDRS	Comment	Comparison to 100k TID
	Min	Typ	Max	Units				
Offset Voltage, Gain = 2 11.4V/3.3V	-3.5		4.5	mV	All Units Pass pre rad test limits	Some Units Fail pre rad test limits	Up to 5mV change at 50k	Same behavior (Up to 8mV increase at 100k)
Offset Voltage, Gain = 10 16V/3.3V	-3.5		3.5	mV	All Units Pass pre rad test limits	Some Units Fail pre rad test limits	Up to 4mV change at 50k	Same behavior (Up to 3mV change at 100k)
Offset Voltage, Gain = 10 11.4V/3.3V	-3.5		3.5	mV	All Units Pass pre rad test limits	Some Units Fail pre rad test limits	Up to 4mV change at 50k	Same behavior (Up to 6mV change at 100k)
Gain Accuracy, Gain = 0.4 15V/3.3V at CM=5V	0.398		0.402	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 0.4 15V/3.3V at CM=-5V	0.398		0.402	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 0.4 11.4V/3.3V at CM=5V	0.397		0.403	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 0.4 11.4V/3.3V at CM=0V	0.398		0.402	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 0.4 11.4V/3.3V at CM=-5V	0.397		0.403	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 0.4 16V/3.3V at CM=5V	0.398		0.402	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 0.4 16V/3.3V at CM=0V	0.398		0.402	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 0.4 16V/3.3V at CM=-5V	0.398		0.402	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 2 15V/3.3V at CM=5V	1.992		2.004	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 2 15V/3.3V at CM=-5V	1.992		2.004	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 2 11.4V/3.3V at CM=-5V	1.990		2.010	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 2 11.4V/3.3V at CM=0V	1.992		2.004	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 2 11.4V/3.3V at CM=5V	1.990		2.010	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 2 16V/3.3V at CM=5V	1.992		2.004	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 2 16V/3.3V at CM=0V	1.992		2.004	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 2 16V/3.3V at CM=-5V	1.992		2.004	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 10 15V/3.3V at CM=5V	9.965		10.025	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 10 15V/3.3V at CM=-5V	9.965		10.025	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 10 11.4V/3.3V at CM=-5V	9.965		10.025	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 10 11.4V/3.3V at CM=0V	9.965		10.025	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 10 11.4V/3.3V at CM=5V	9.965		10.025	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 10 16V/3.3V at CM=5V	9.965		10.025	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable

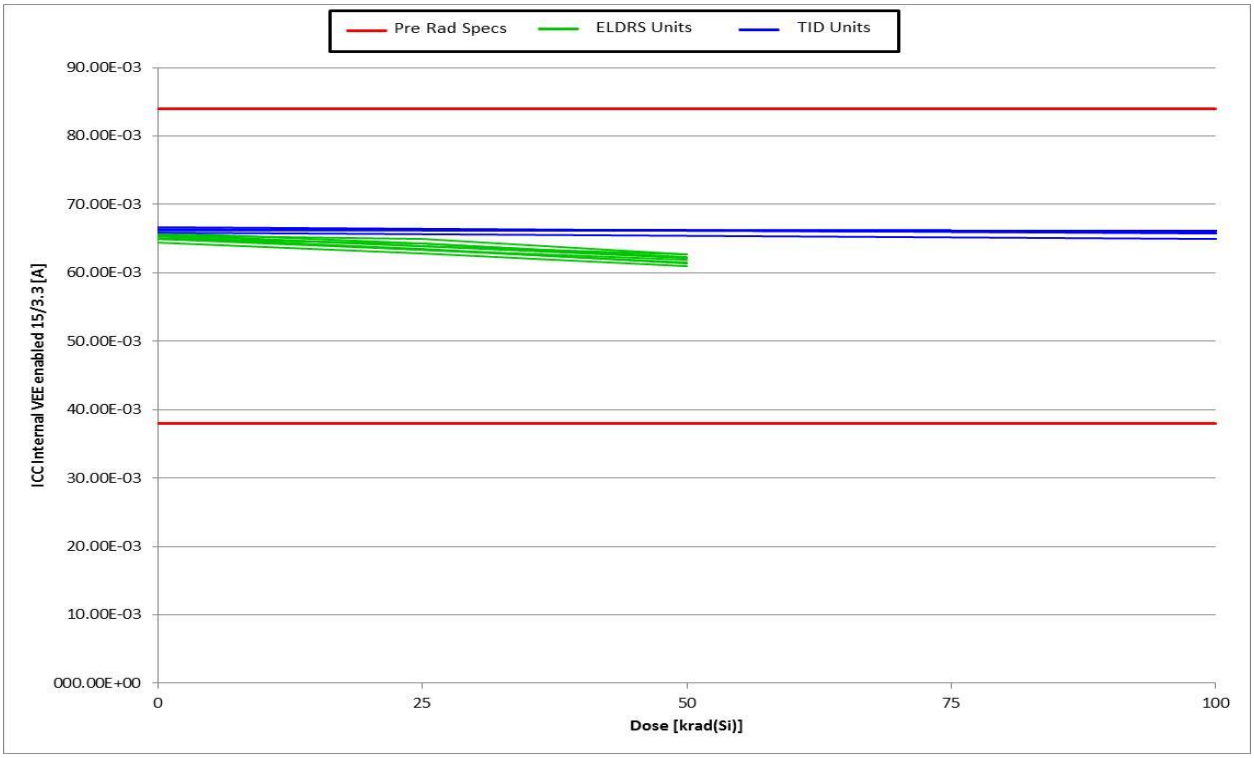
Parameters	Pre Radiation Test Limits				Post 25k ELDRS	Post 50k ELDRS	Comment	Comparison to 100k TID
	Min	Typ	Max	Units				
Gain Accuracy, Gain = 10 16V/3.3V at CM=0V	9.965		10.025	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Gain Accuracy, Gain = 10 16V/3.3V at CM=-5V	9.965		10.025	-	All Units Pass pre rad test limits	All Units Pass pre rad test limits	Very stable	Very stable
Logic Levels for FPGA Interface I/Os								
Input Logic Threshold at VDD=2.25V	0.7875	1.125	1.463	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Input Logic Threshold at VDD=5.5V	1.925	2.725	3.575	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Logic Output VOH at 100uA at VDD=2.25V	1.95		2.25	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Logic Output VOL at 100uA at VDD=2.25V	0		0.3	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Logic Output VOH at 100uA at VDD=5.5V	5.2		5.5	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Logic Output VOL at 100uA at VDD=5.5V	0		0.3	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Very stable	Very stable
Programmable Current Source								
Full scale current (doubWt OFF) at VCC=11.4V	1.880	1.940	2.000	mA	All Units Pass pre rad spec	All Units Pass pre rad spec	~2-2.5% Decrease at 50k	Same behavior (~4-5% Decrease at 100k)
Integral nonlinearity at VCC=11.4V	-7.5	0	7.5	µA	All Units Pass pre rad spec	All Units Pass pre rad spec	Stable	Stable
Differential nonlinearity at VCC=11.4V	-5.0	0	5.0	µA	All Units Pass pre rad spec	All Units Pass pre rad spec	Stable	Stable
Full scale current (doubWt ON) at VCC=11.4V	3710	3840	3950	µA	All Units Pass pre rad spec	All Units Pass pre rad spec	~2-2.5% Decrease at 50k	Same behavior (~4-5% Decrease at 100k)
Integral nonlinearity at VCC=11.4V	-15		15	µA	All Units Pass pre rad spec	All Units Pass pre rad spec	Stable	Stable
Differential nonlinearity at VCC=11.4V	-15		15	µA	All Units Pass pre rad spec	All Units Pass pre rad spec	Stable	Stable
At DAC=31 at VCC=11.4V	290	300	310	uA	All Units Pass pre rad spec	Some Units Fail pre rad spec	~2-2.5% Decrease at 50k	Same behavior (~5-6% Decrease at 100k)
Integral nonlinearity at VCC=11.4V	-2.0		2.0	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Stable	Some increase
Differential nonlinearity at VCC=11.4V	-2.0		2.0	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Stable	Stable
Full scale current (doubWt OFF) at VCC=16V	1.880	1.940	2.000	mA	All Units Pass pre rad spec	All Units Pass pre rad spec	~2-2.5% Decrease at 50k	Same behavior (~4-5% Decrease at 100k)
Integral nonlinearity at VCC=16V	-7.5	0	7.5	µA	All Units Pass pre rad spec	All Units Pass pre rad spec	Stable	Stable
Differential nonlinearity at VCC=16V	-5.0	0	5.0	µA	All Units Pass pre rad spec	All Units Pass pre rad spec	Stable	Stable
Full scale current (doubWt ON) at VCC=16V	3710	3840	3950	µA	All Units Pass pre rad spec	All Units Pass pre rad spec	~2-2.5% Decrease at 50k	Same behavior (~4-5% Decrease at 100k)
Integral nonlinearity at VCC=16V	-15		15	µA	All Units Pass pre rad spec	All Units Pass pre rad spec	Stable	Stable
Differential nonlinearity at VCC=16V	-15		15	µA	All Units Pass pre rad spec	All Units Pass pre rad spec	Stable	Stable
At DAC=31 at VCC=16V	290	300	310	uA	All Units Pass pre rad spec	Some Units Fail pre rad spec	~2-2.5% Decrease at 50k	Same behavior (~5-6% Decrease at 100k)
Integral nonlinearity at	-2.0		2.0	uA	All Units Pass pre	All Units Pass pre	Stable	Some increase

Parameters	Pre Radiation Test Limits				Post 25k ELDRS	Post 50k ELDRS	Comment	Comparison to 100k TID
	Min	Typ	Max	Units				
VCC=16V					rad spec	rad spec		
Differential nonlinearity at VCC=16V	-2.0		2.0	uA	All Units Pass pre rad spec	All Units Pass pre rad spec	Stable	Stable
Fixed Threshold Bi-Level Inputs								
Threshold – External 0.1V (Rising Voltage) at VCC=15V	0.0	0.1	0.2	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Up to 25mV increase at 50k	Same behavior (Up to 40mV increase at 100k)
Threshold Hysteresis – External 0.1V at VCC=15V	60	120	180	mV	All Units Pass pre rad spec	All Units Pass pre rad spec	Up to 20mV decrease at 50k	TID units decrease less (up to 10mV decrease at 100k)
Threshold – External 4.9V (Rising Voltage) at VCC=15V	4.8	4.9	5.0	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Up to 25mV increase at 50k	Same behavior (Up to 40mV increase at 100k)
Threshold Hysteresis – External 4.9V at VCC=15V	60	120	180	mV	All Units Pass pre rad spec	All Units Pass pre rad spec	Up to 20mV decrease at 50k	TID units decrease less (up to 10mV decrease at 100k)
Threshold – Internal ref (Rising Voltage) at VCC=11.4V	2.45	2.50	2.55	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Up to 20mV increase at 50k	Same behavior (Up to 40mV increase at 100k)
Threshold Hysteresis – Internal reference at VCC=11.4V	60	120	180	mV	All Units Pass pre rad spec	All Units Pass pre rad spec	Up to 25mV decrease at 50k	TID units decrease less (up to 16mV decrease at 100k)
Threshold – External 4.9V (Rising Voltage) at VCC=11.4V	4.8	4.9	5.0	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Up to 20mV increase at 50k	Same behavior (Up to 40mV increase at 100k)
Threshold Hysteresis – External 4.9V at VCC=11.4V	60	120	180	mV	All Units Pass pre rad spec	All Units Pass pre rad spec	Up to 25mV decrease at 50k	TID units decrease less (up to 10mV decrease at 100k)
Adjustable threshold Bi-level MUX and DAC								
Threshold DAC Max Output (If input is >=0V during TID) at VCC=11.4V	4.95	5	5.05	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Up to 25mV increase at 50k	Same behavior (Up to 50mV increase at 100k)
Hysteresis DAC Max Output (If input is >=0V during TID) at VCC=11.4V	0.075	0.112	0.150	V	All Units Pass pre rad spec	All Units Fail pre rad spec	~50% decrease at 50k	TID units decrease less (~25% decrease at 100k)
Threshold DAC Max Output (If input is VEE/2 during TID) at VCC=11.4V	4.95	5	5.05	V	All Units Fail pre rad spec	All Units Fail pre rad spec	~4% decrease at 50k	TID units decrease more (~10% decrease)
Hysteresis DAC Max Output (If input is VEE/2 during TID) at VCC=11.4V	0.075	0.112	0.150	V	All Units Pass pre rad spec	Some Units Fail pre rad spec	~40% decrease at 50k	TID units decrease less (~20% decrease at 100k)
Threshold DAC=0 Output (If input is >=0V during TID) at VCC=15V	-0.05	0	0.05	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Up to 25mV increase at 50k	Same behavior (Up to 25mV increase at 100k)
Hysteresis DAC=0 Output (If input is >=0V during TID) at VCC=15V	0.075	0.112	0.150	V	All Units Pass pre rad spec	Some Units Fail pre rad spec	~50% decrease at 50k	TID units decrease less (~25% decrease at 100k)
Threshold DAC=0 Output (If input is VEE/2 during TID) at VCC=15V	-0.05	0	0.05	V	All Units Fail pre rad spec	All Units Fail pre rad spec	~0.15-0.2V decrease at 50k	TID units decrease more (~0.45-0.5V decrease)
Hysteresis DAC=0 Output (If input is VEE/2 during TID) at VCC=15V	0.075	0.112	0.150	V	All Units Pass pre rad spec	Some Units Fail pre rad spec	~40% decrease at 50k	TID units decrease less (~15mV decrease at 100k)
Threshold DAC=0 Output (If input is >=0V during TID) at VCC=11.4V	-0.05	0	0.05	V	All Units Pass pre rad spec	All Units Pass pre rad spec	Up to 25mV increase at 50k	Same behavior (Up to 40mV increase at 100k)

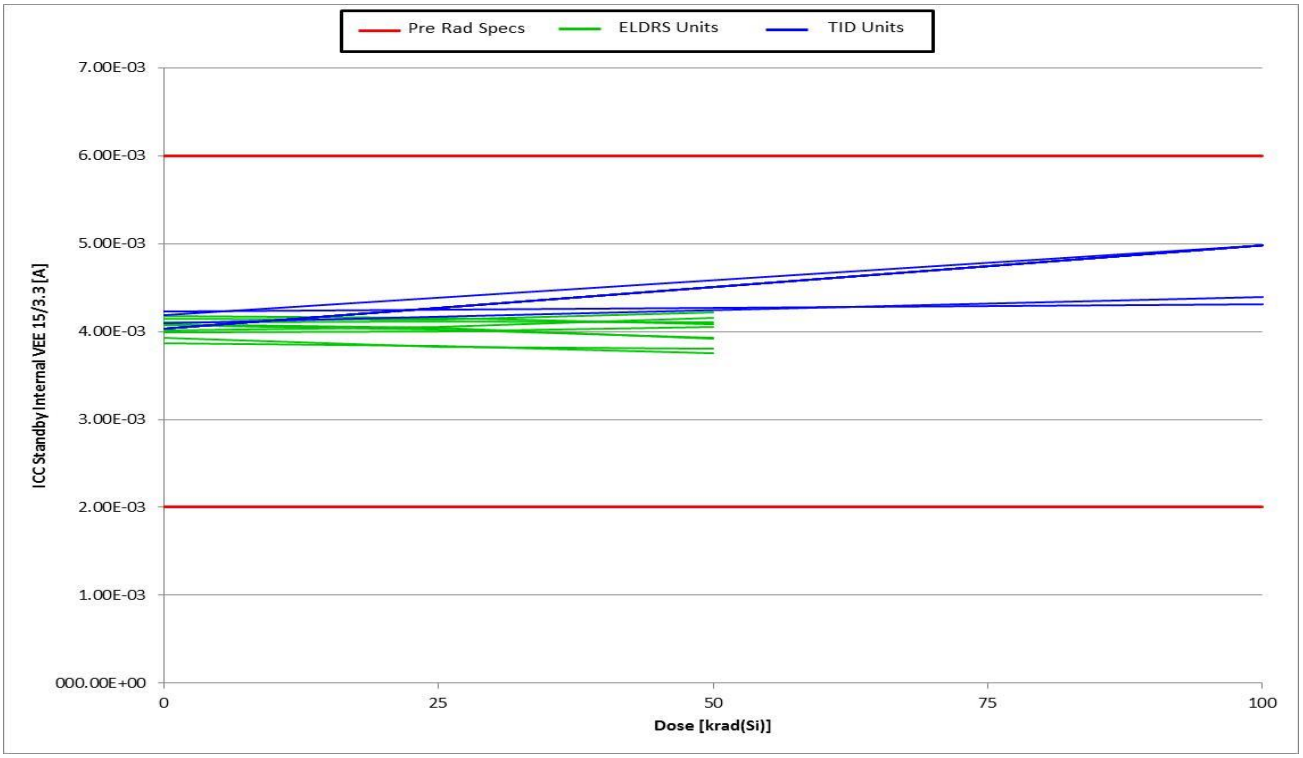
Parameters	Pre Radiation Test Limits				Post 25k ELDRS	Post 50k ELDRS	Comment	Comparison to 100k TID
	Min	Typ	Max	Units				
Hysteresis DAC=0 Output (If input is >=0V during TID) at VCC=11.4V	0.075	0.112	0.150	V	All Units Pass pre rad spec	Some Units Fail pre rad spec	~30-50% decrease at 50k	TID units decrease less (~25% decrease at 100k)
Threshold DAC=0 Output (If input is VEE/2 during TID) at VCC=11.4V	-0.05	0	0.05	V	All Units Fail pre rad spec	All Units Fail pre rad spec	~0.15-0.2V decrease at 50k	TID units decrease more (~0.45-0.5V decrease)
Hysteresis DAC=0 Output (If input is VEE/2 during TID) at VCC=11.4V	0.075	0.112	0.150	V	All Units Pass pre rad spec	Some Units Fail pre rad spec	~40% decrease at 50k	TID units decrease less (~15mV decrease at 100k)

Detailed Data Charts of specified parameters

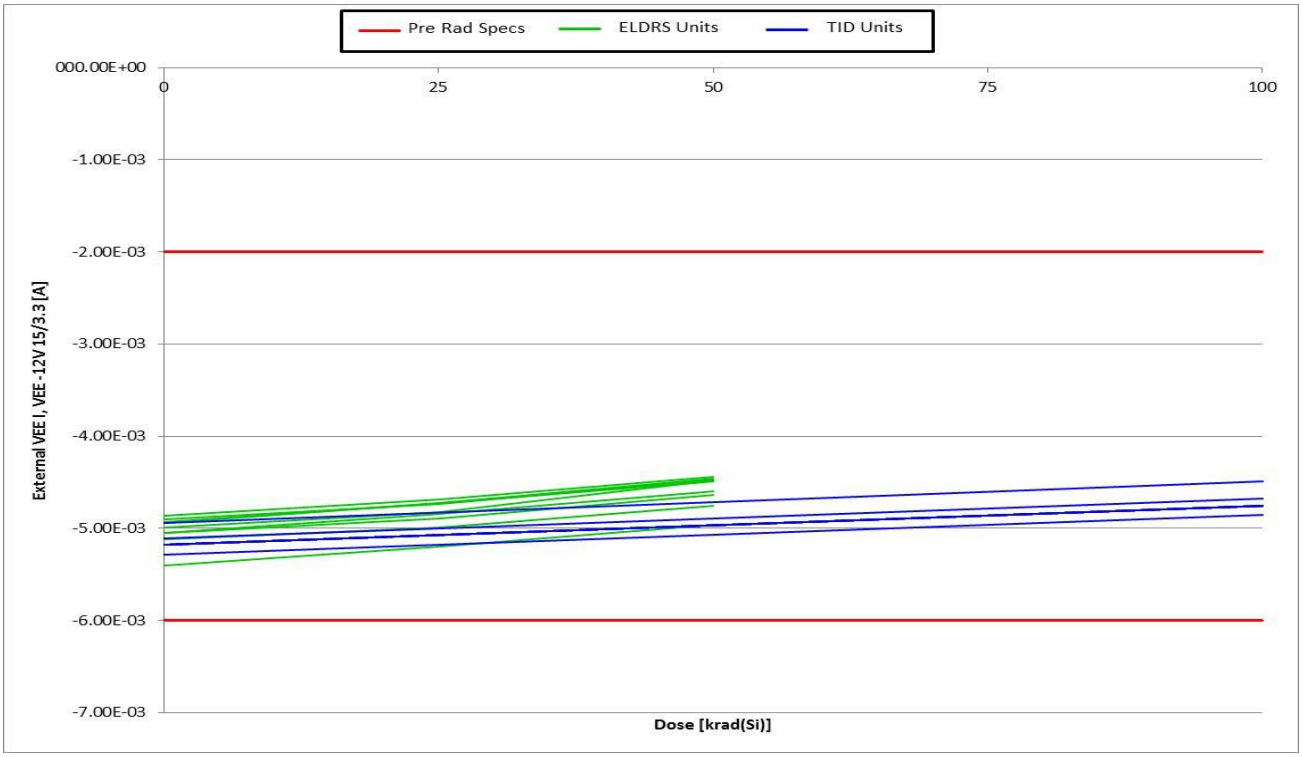
VCC Normal Current



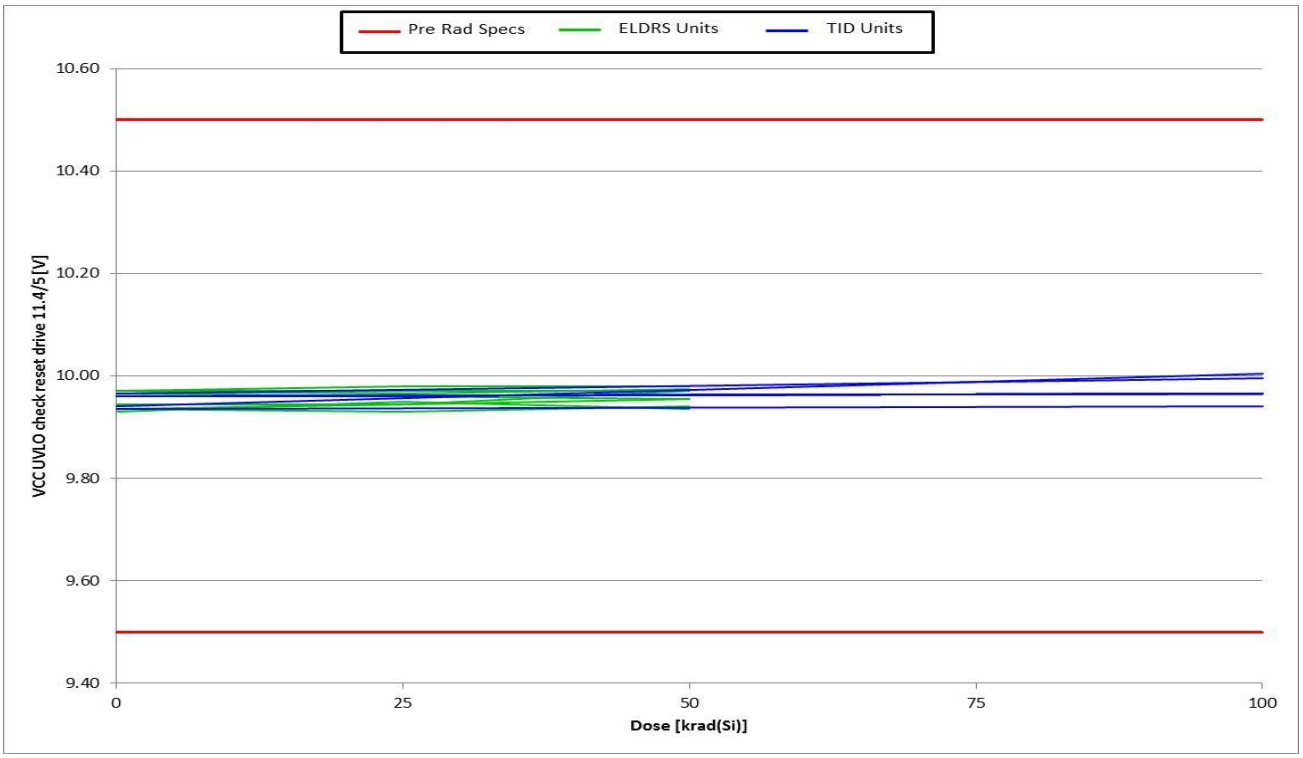
VCC Standby Current


Pre Rad Specs
ELDRS Units
TID Units
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
000.00E+00
ICC Standby Internal VEE 15/3.3 [A]
0
25
50
75
100
Dose [krad(Si)]

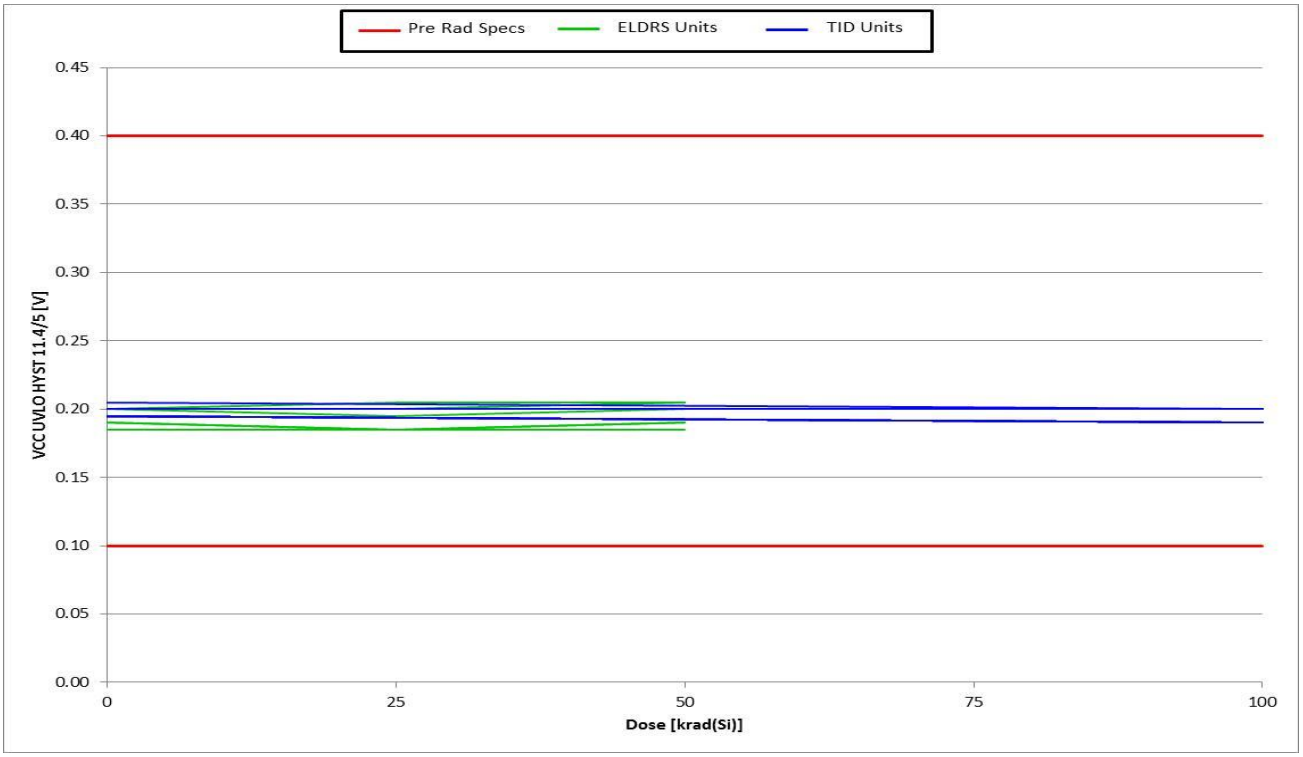
VEE Current


Pre Rad Specs
ELDRS Units
TID Units
000.00E+00
-1.00E-03
-2.00E-03
-3.00E-03
-4.00E-03
-5.00E-03
-6.00E-03
-7.00E-03
External VEE I, VEE -12V 15/3.3 [A]
0
25
50
75
100
Dose [krad(Si)]

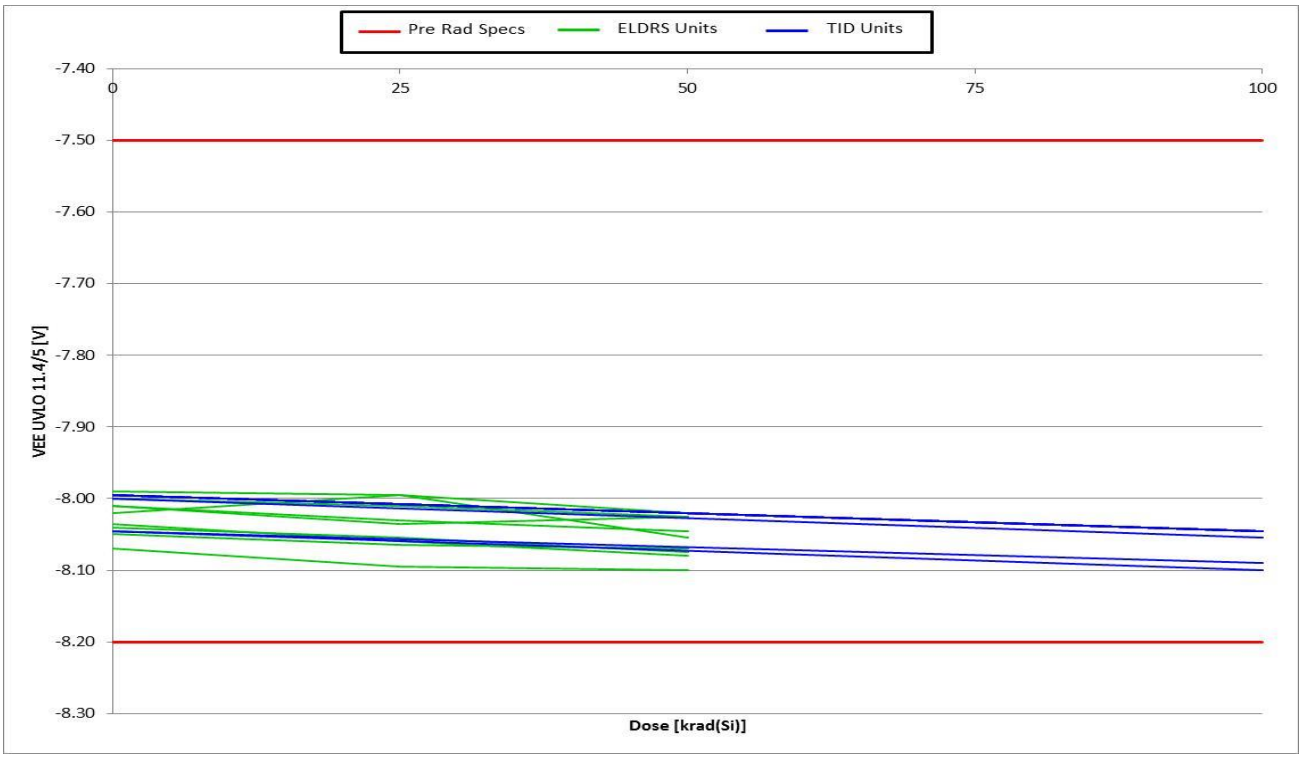
VCC UVLO Threshold



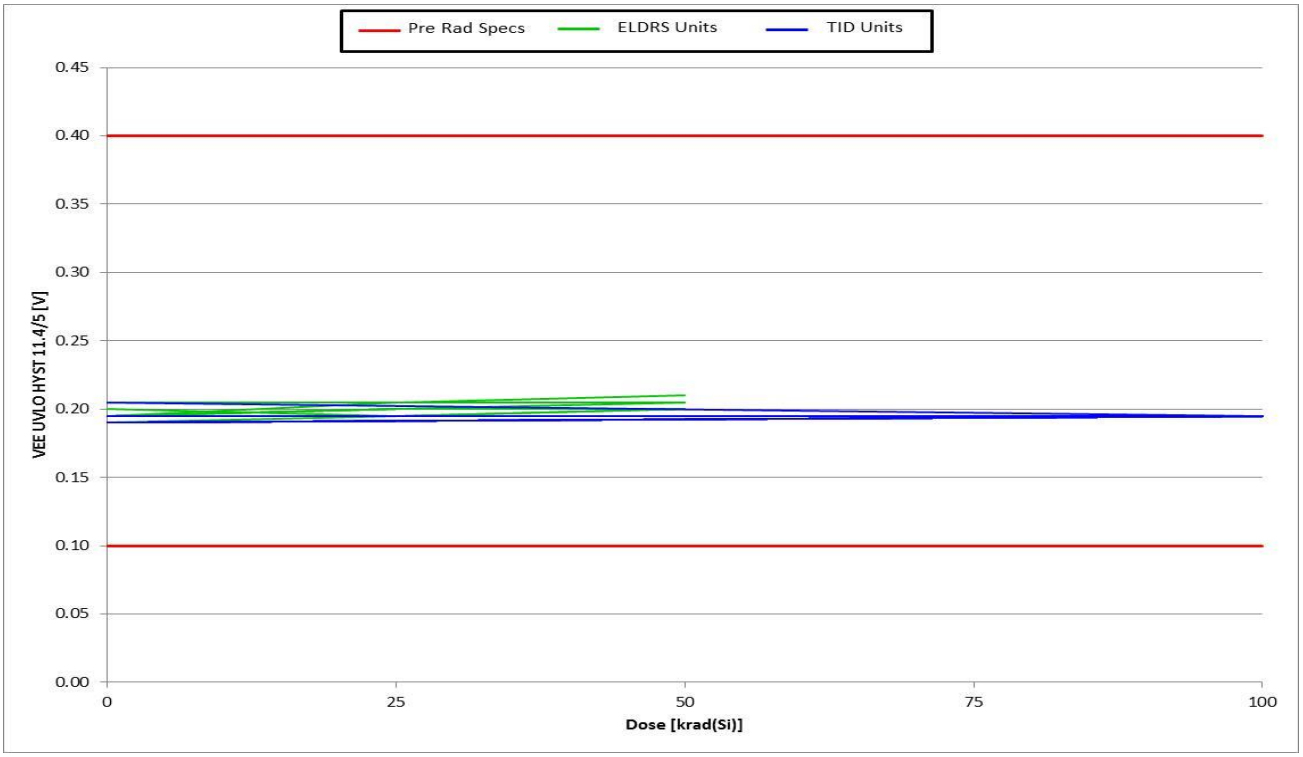
VCC UVLO Threshold Hysteresis



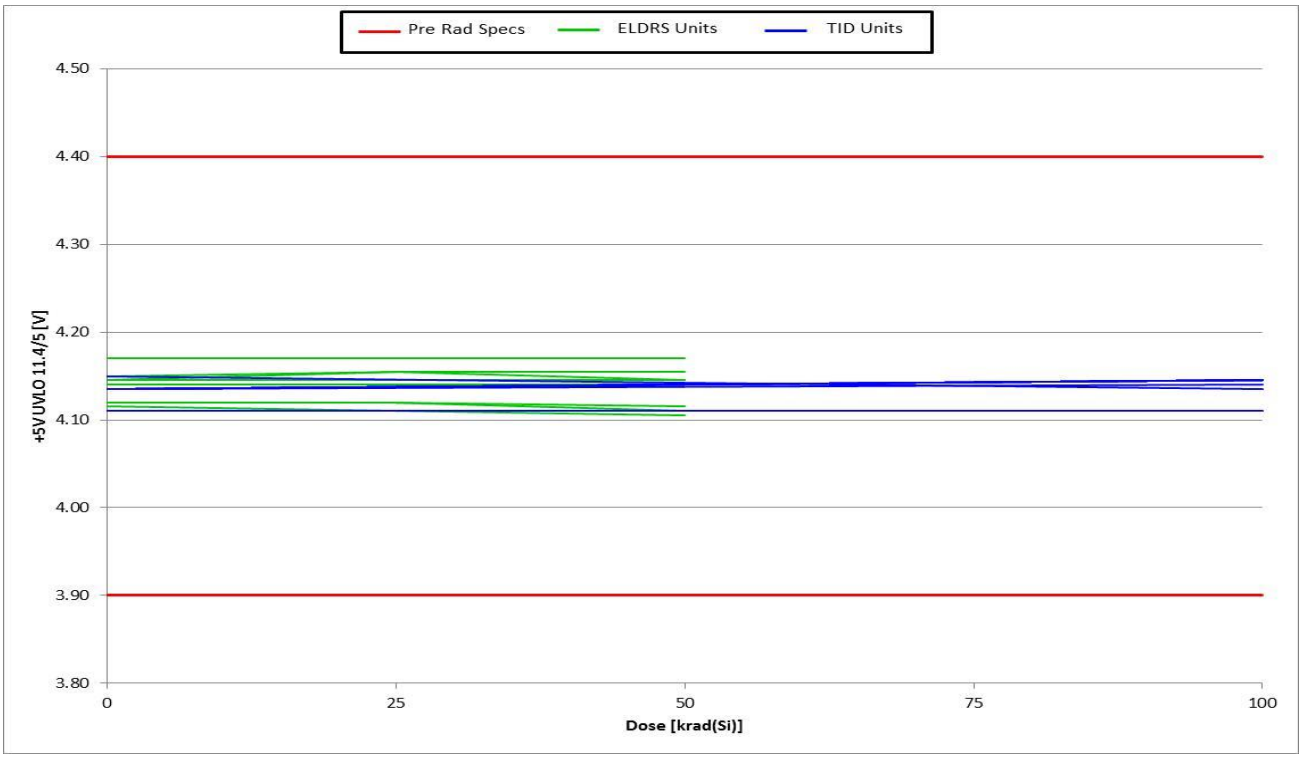
VEE UVLO Threshold



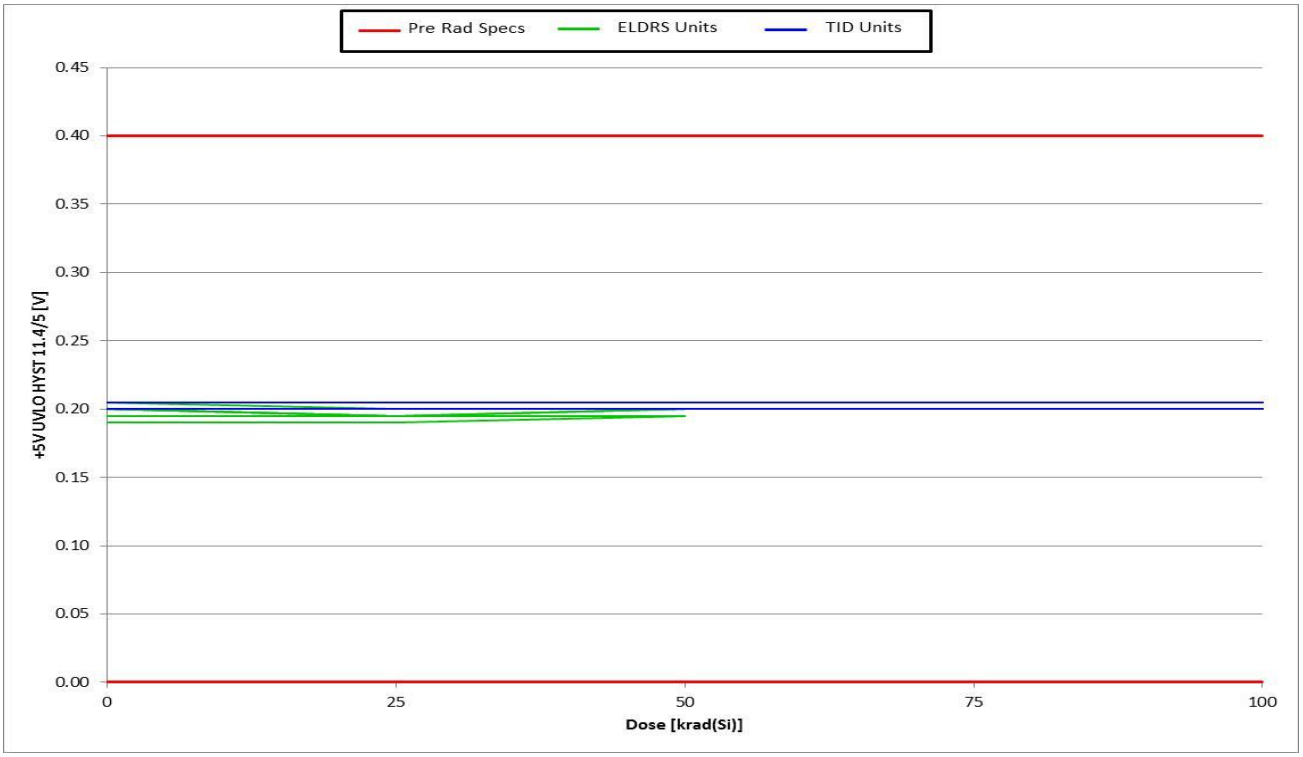
VEE UVLO Threshold Hysteresis



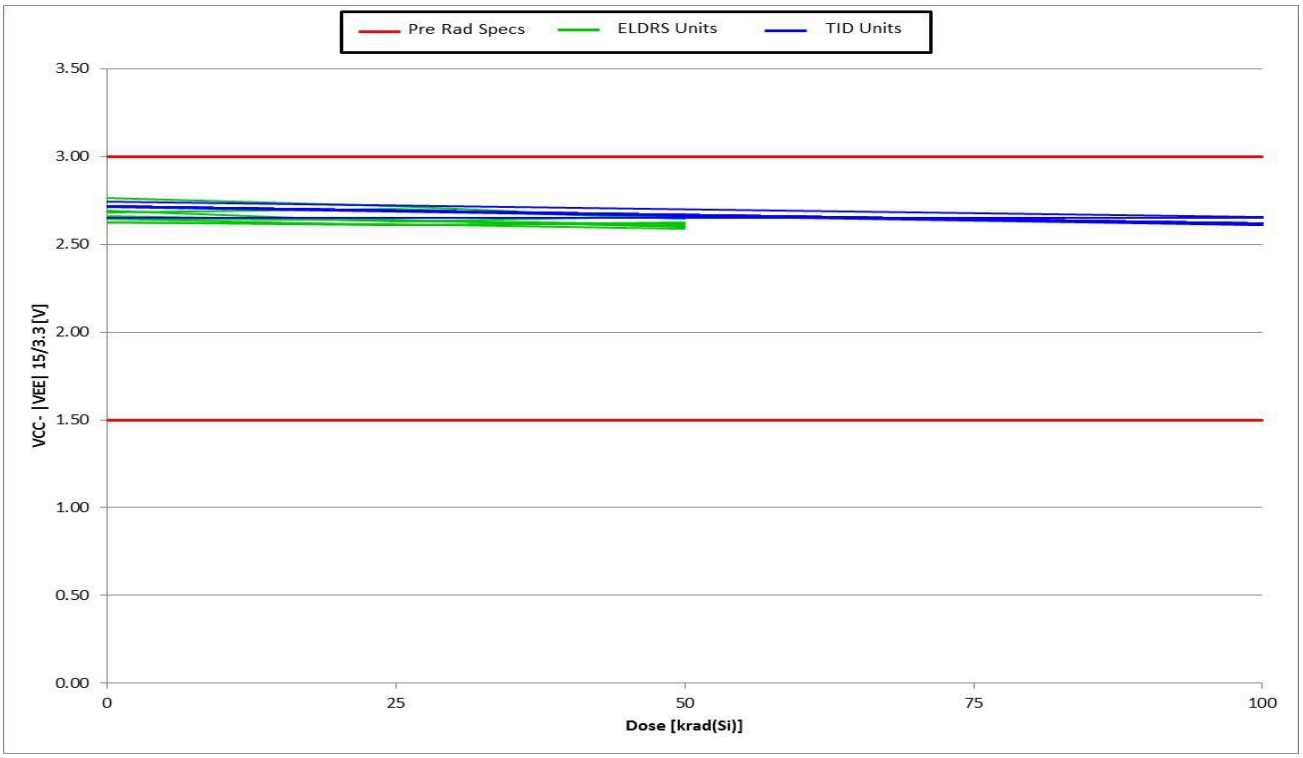
+5V UVLO Threshold



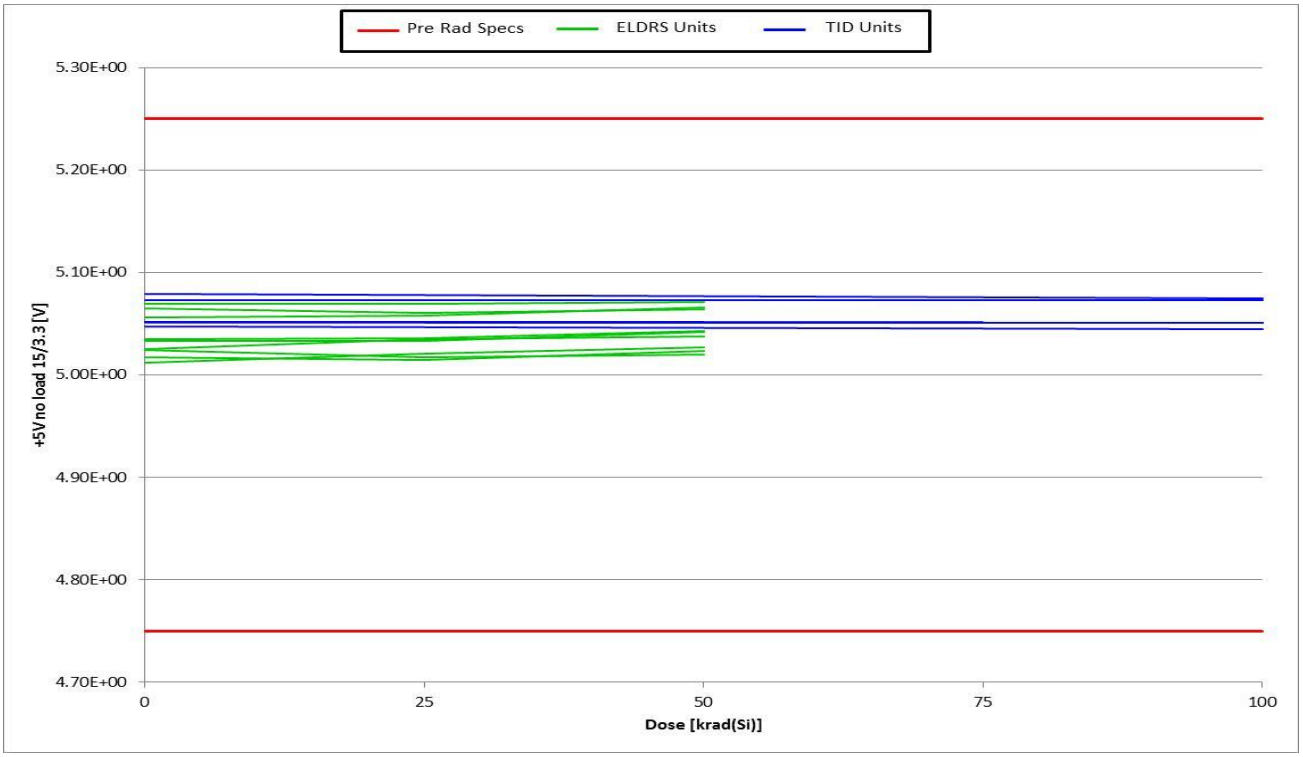
+5V UVLO Threshold Hysteresis



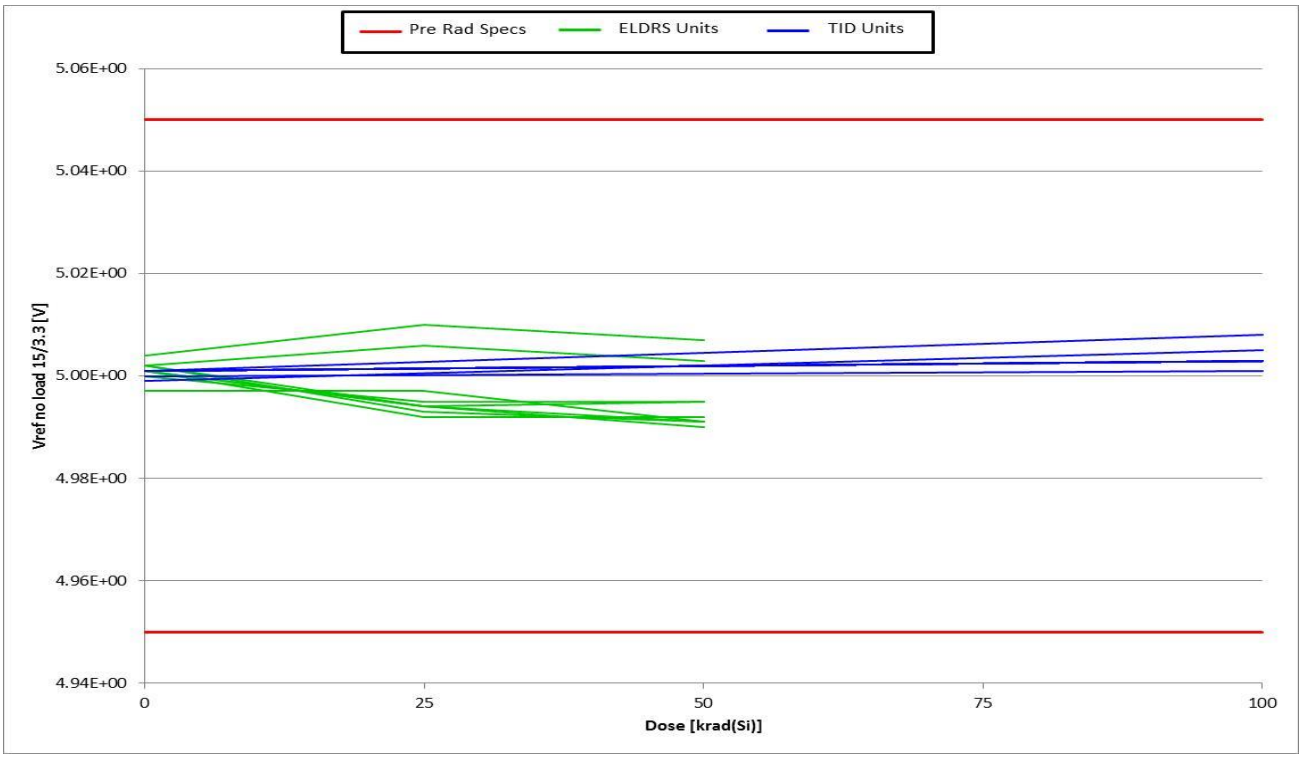
VCC to VEE voltage drop



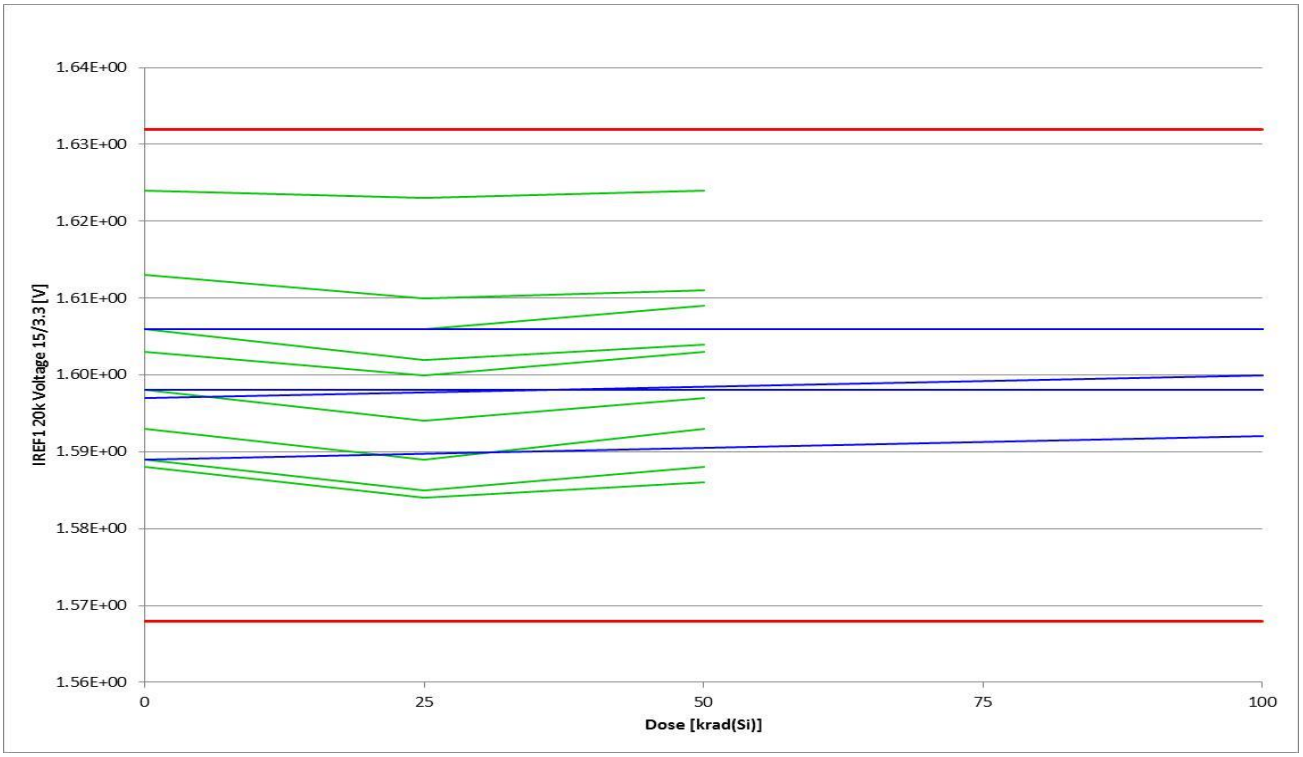
+5V voltage



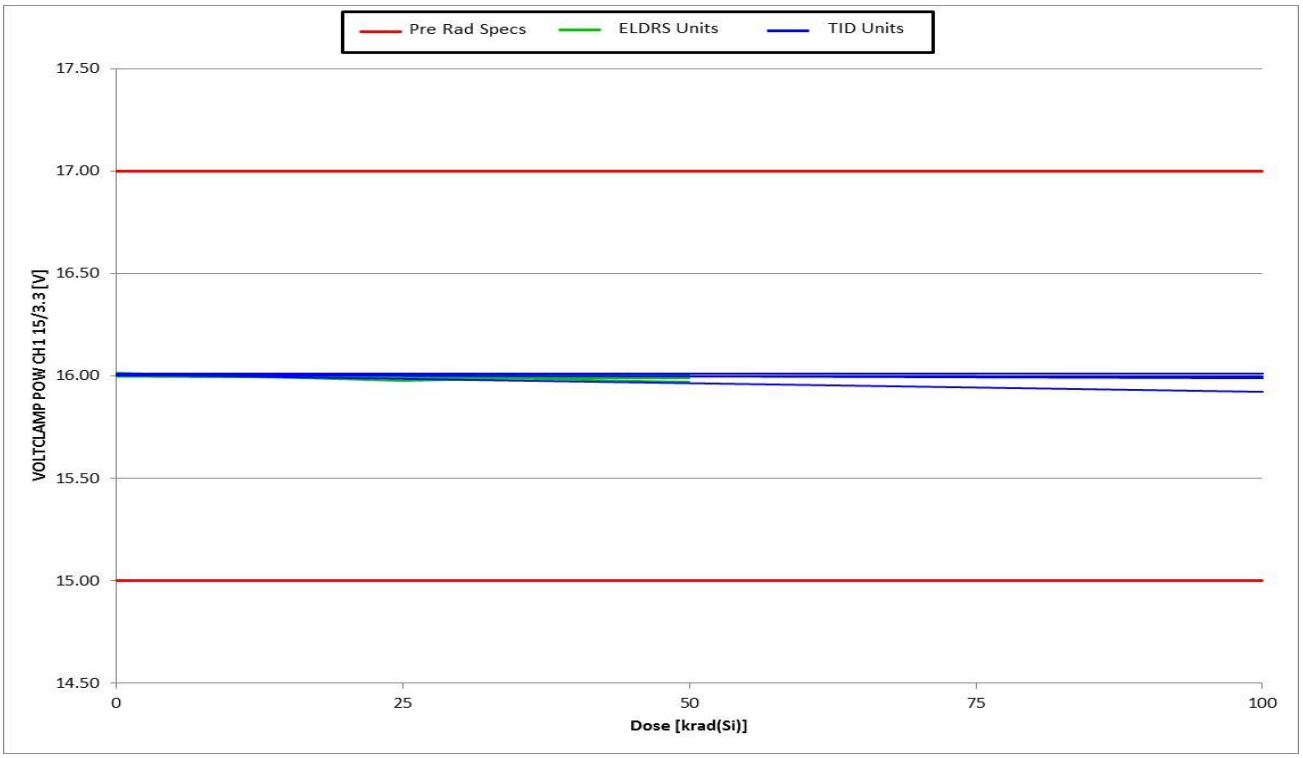
VREF voltage



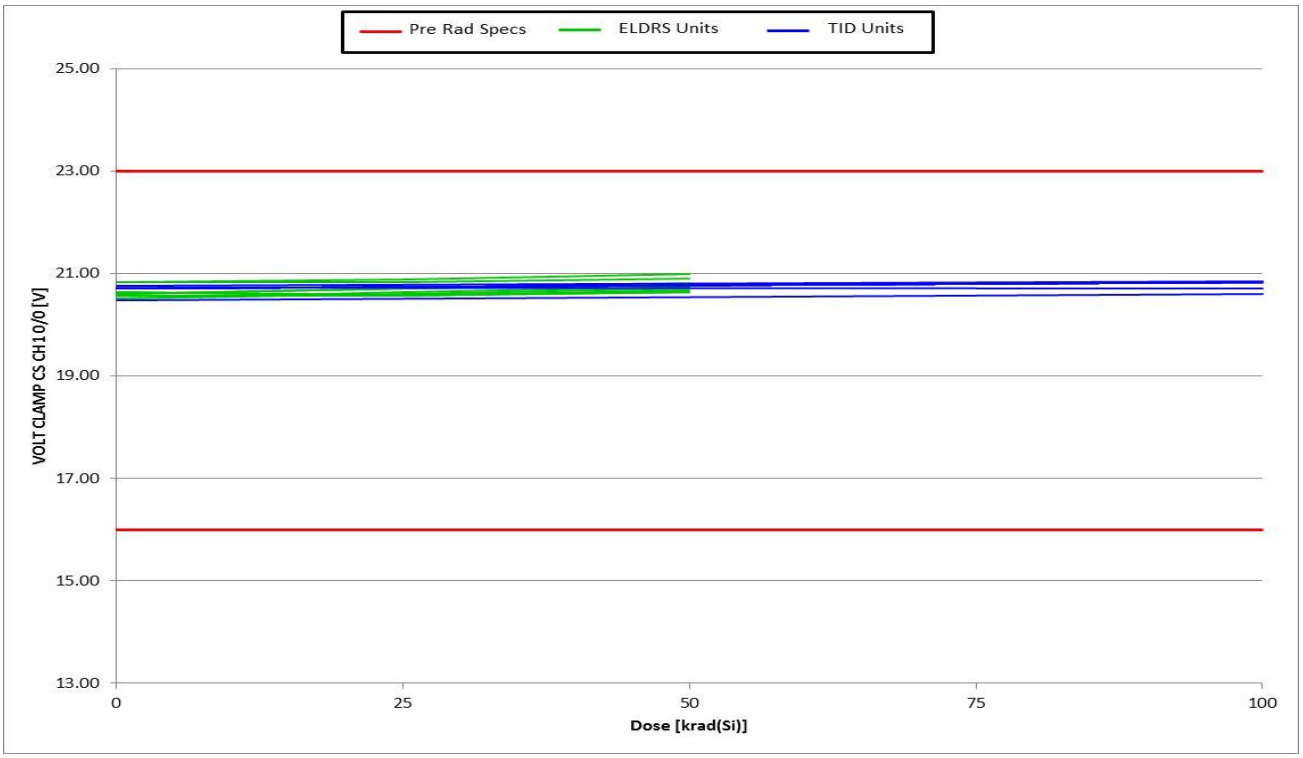
IREF voltage

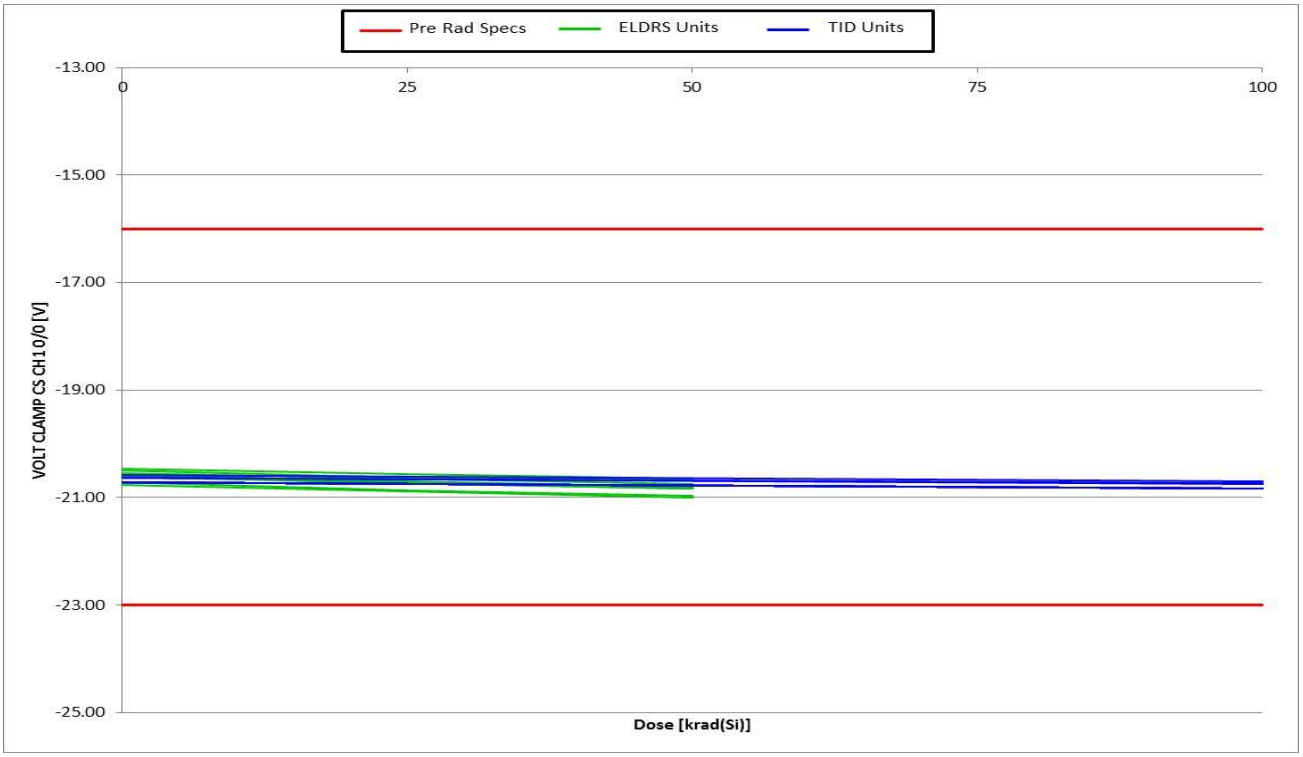


Analog Mux Voltage Clamp - power applied

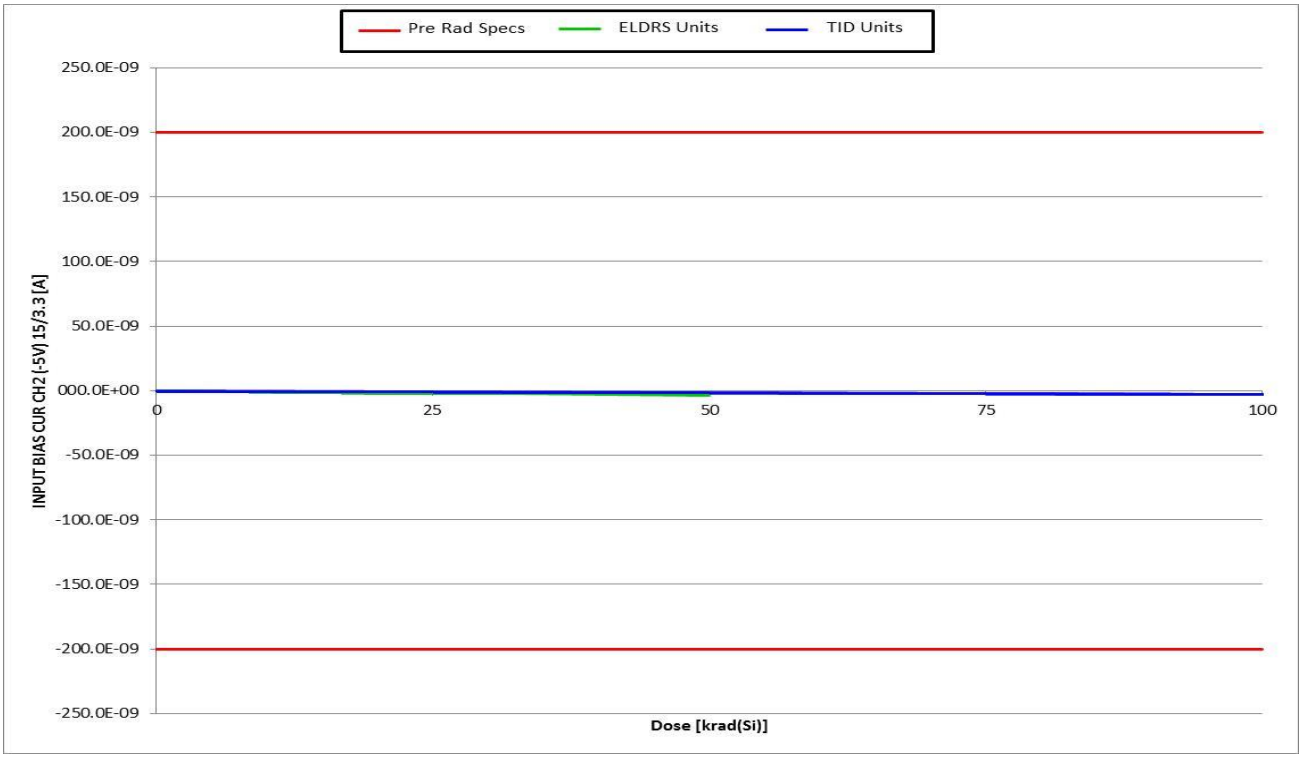


Analog Mux Voltage Clamp VEE=VCC=0V

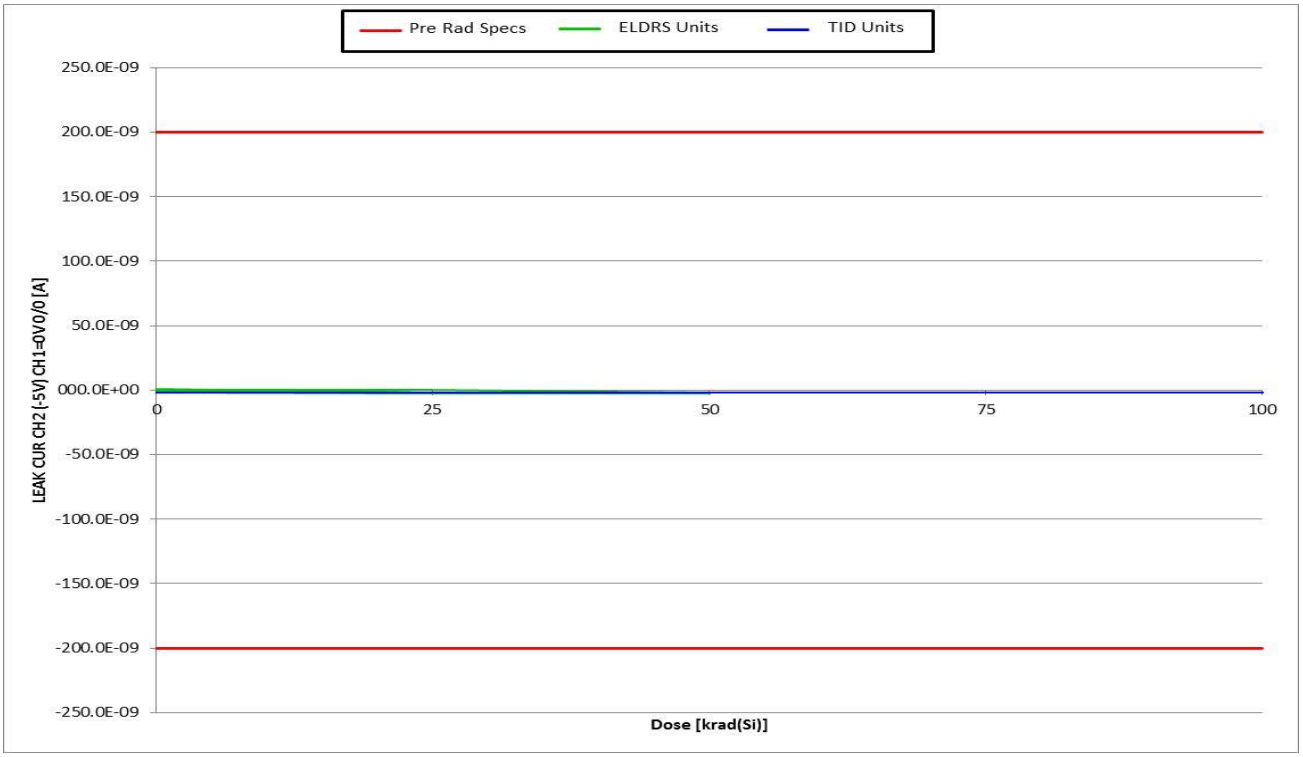




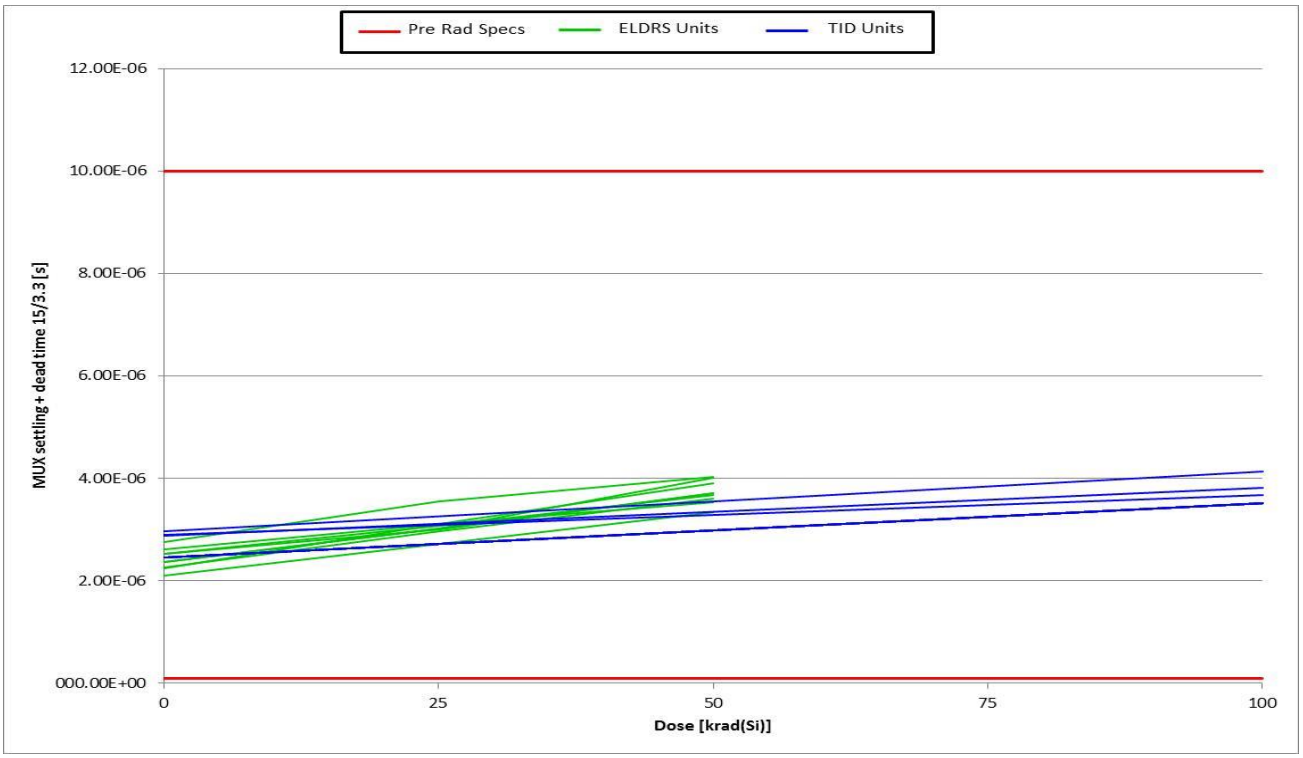
Analog Mux Input Bias Current



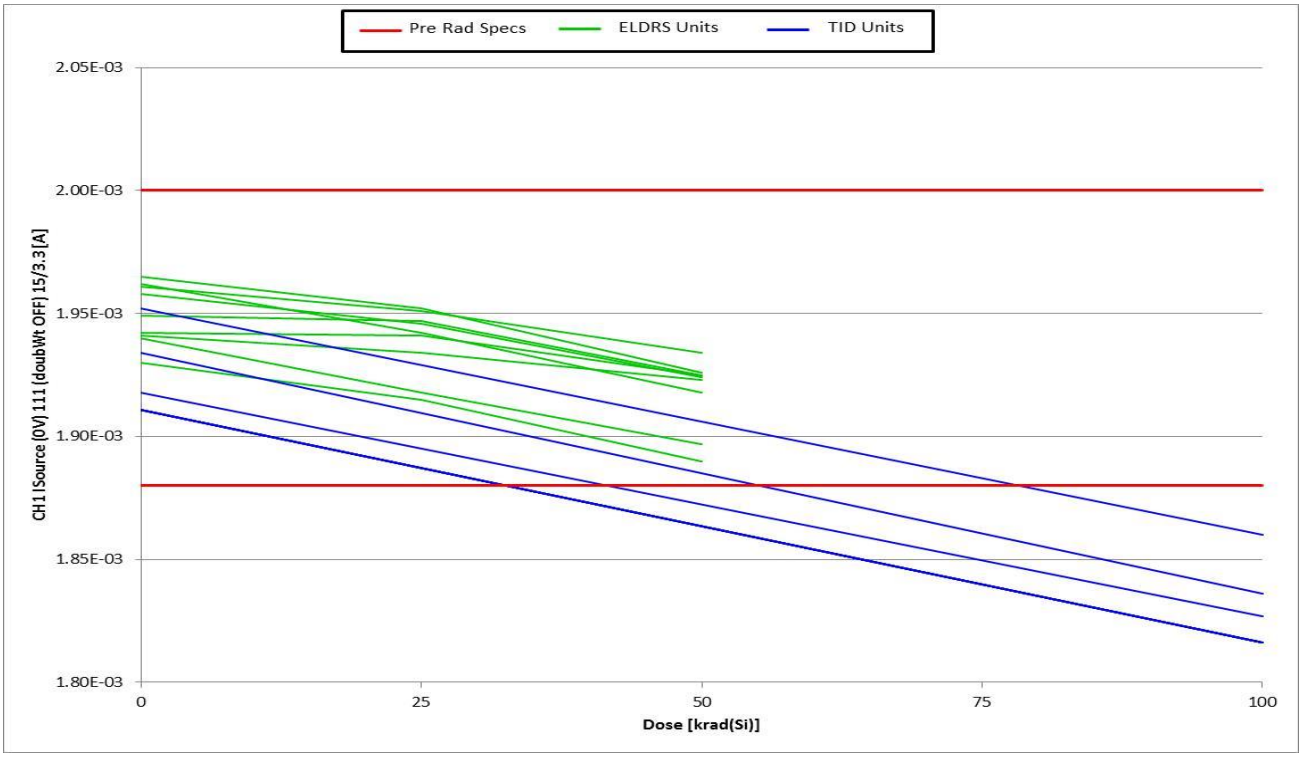
Analog Mux Input Leakage Current



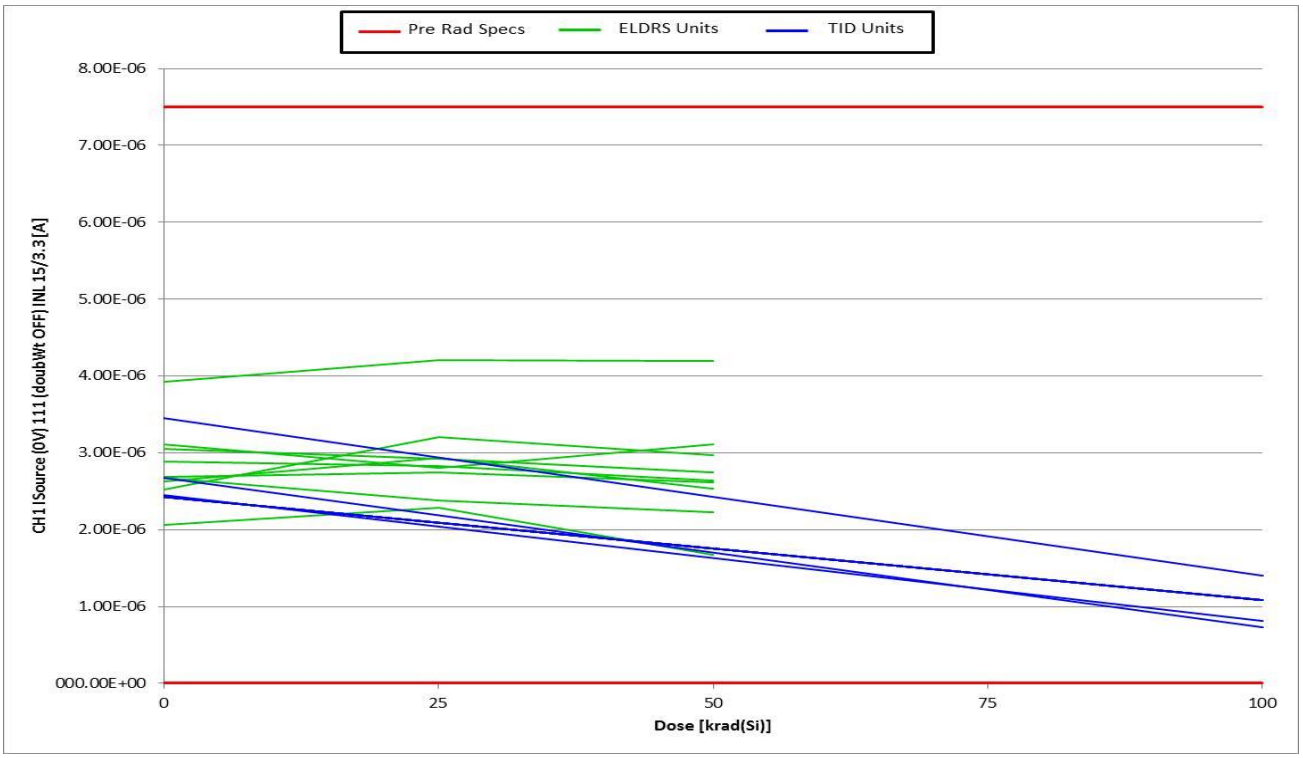
Analog Mux Settling Time



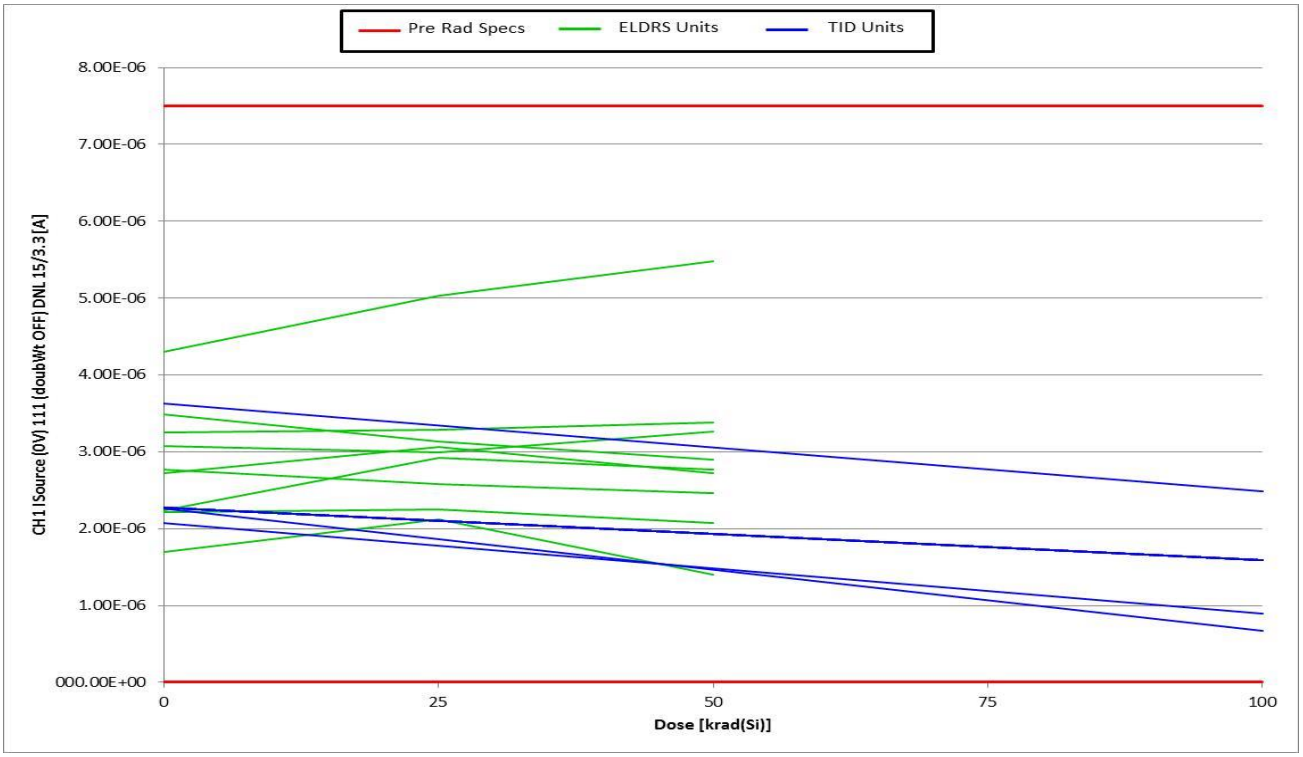
Programmable Current Source Full scale current (doubWt OFF)



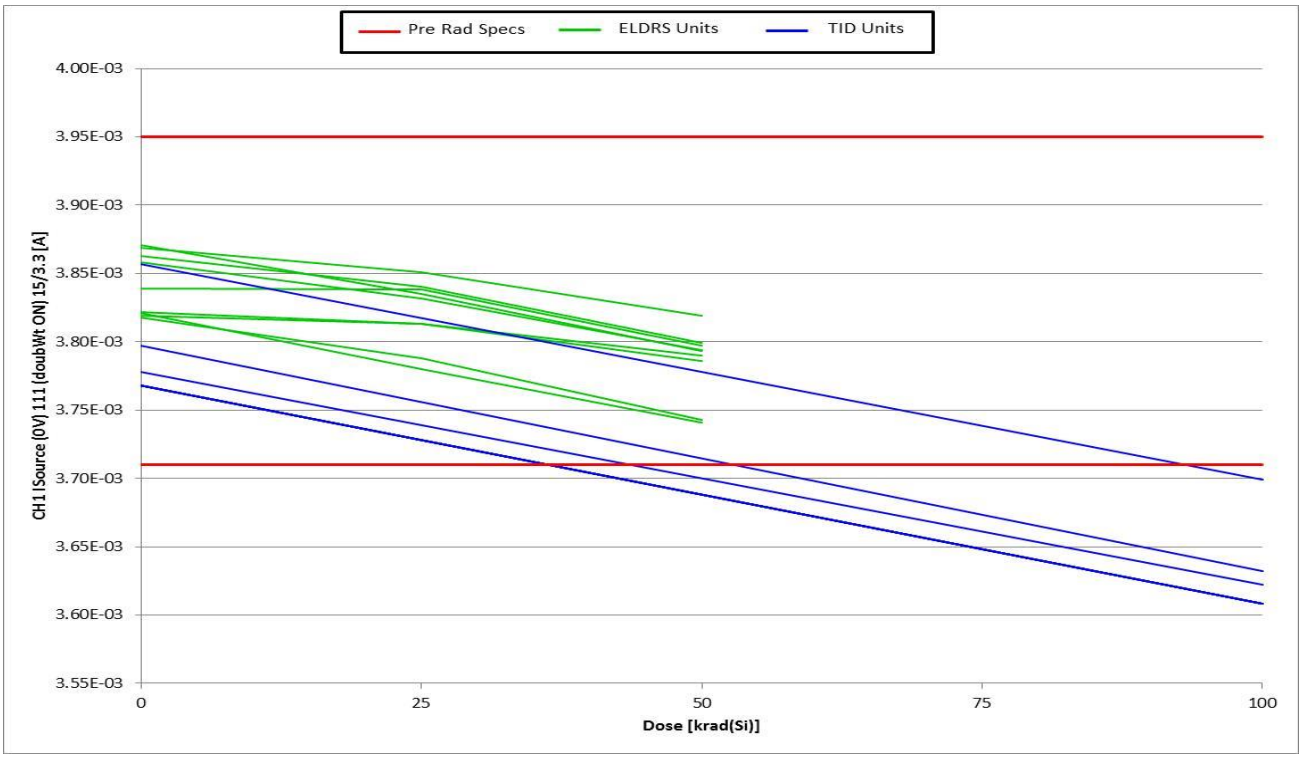
Programmable Current Source INL (doubWt OFF)



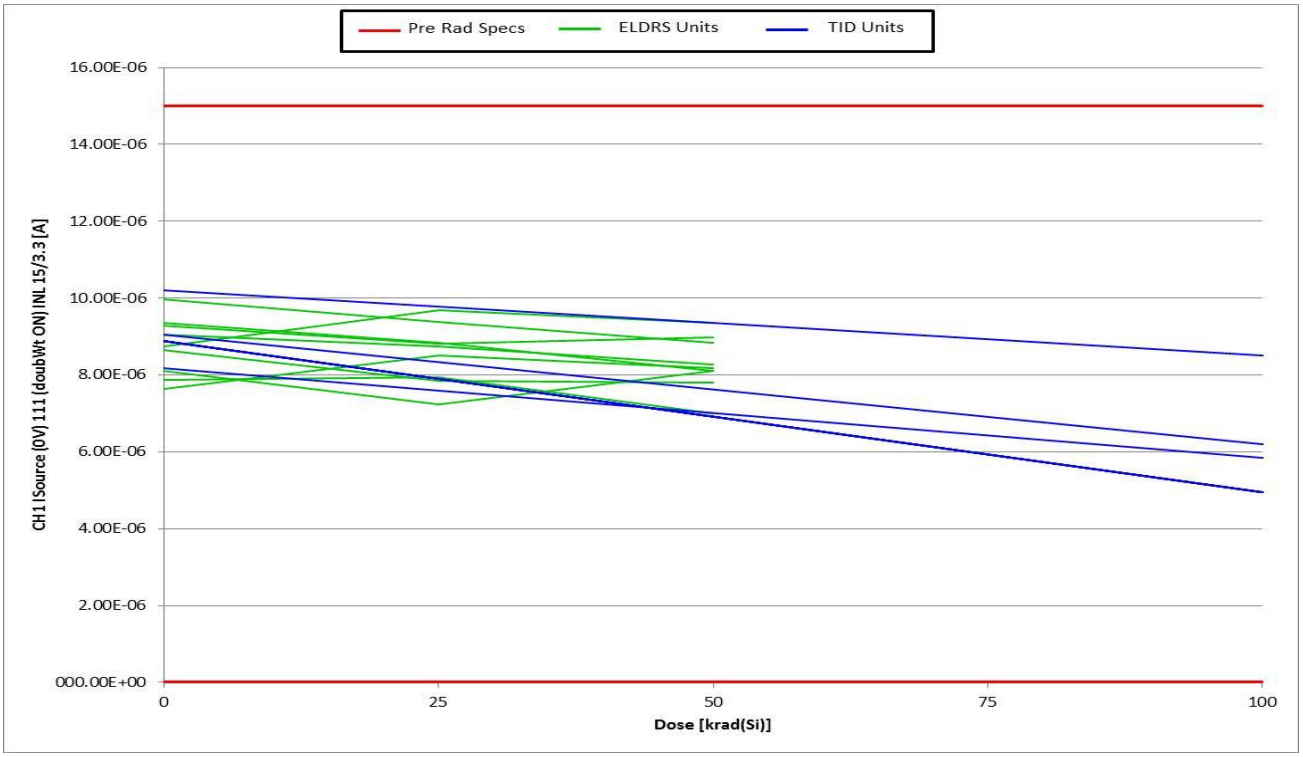
Programmable Current Source DNL (doubWt OFF)



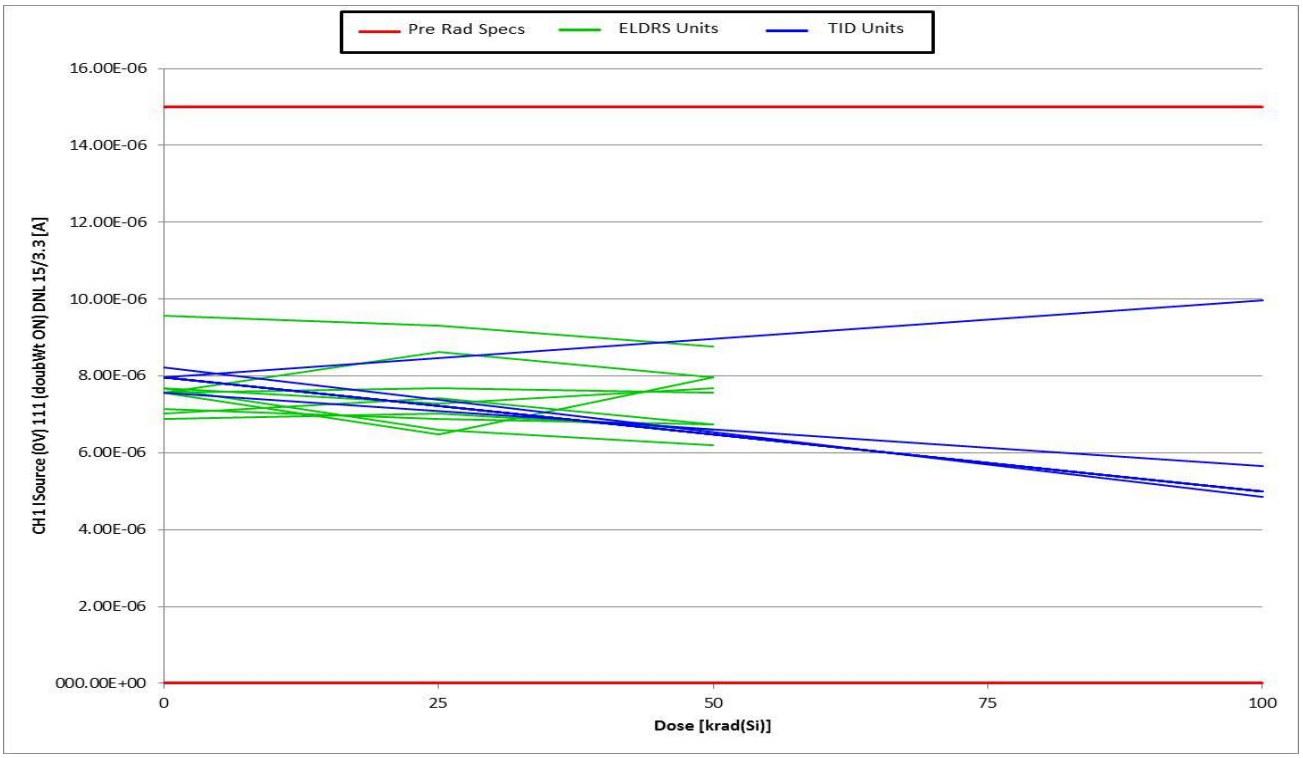
Programmable Current Source Full scale current (doubWt ON)



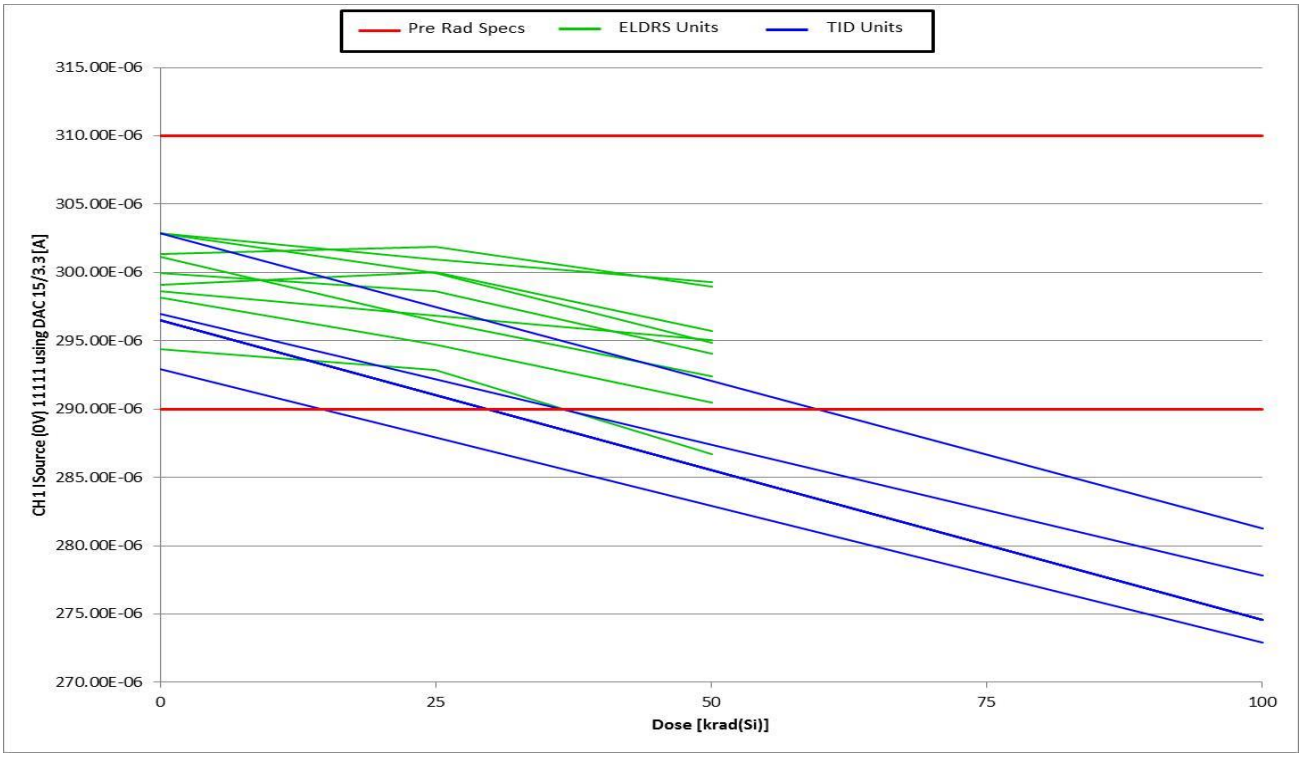
Programmable Current Source INL (doubWt ON)



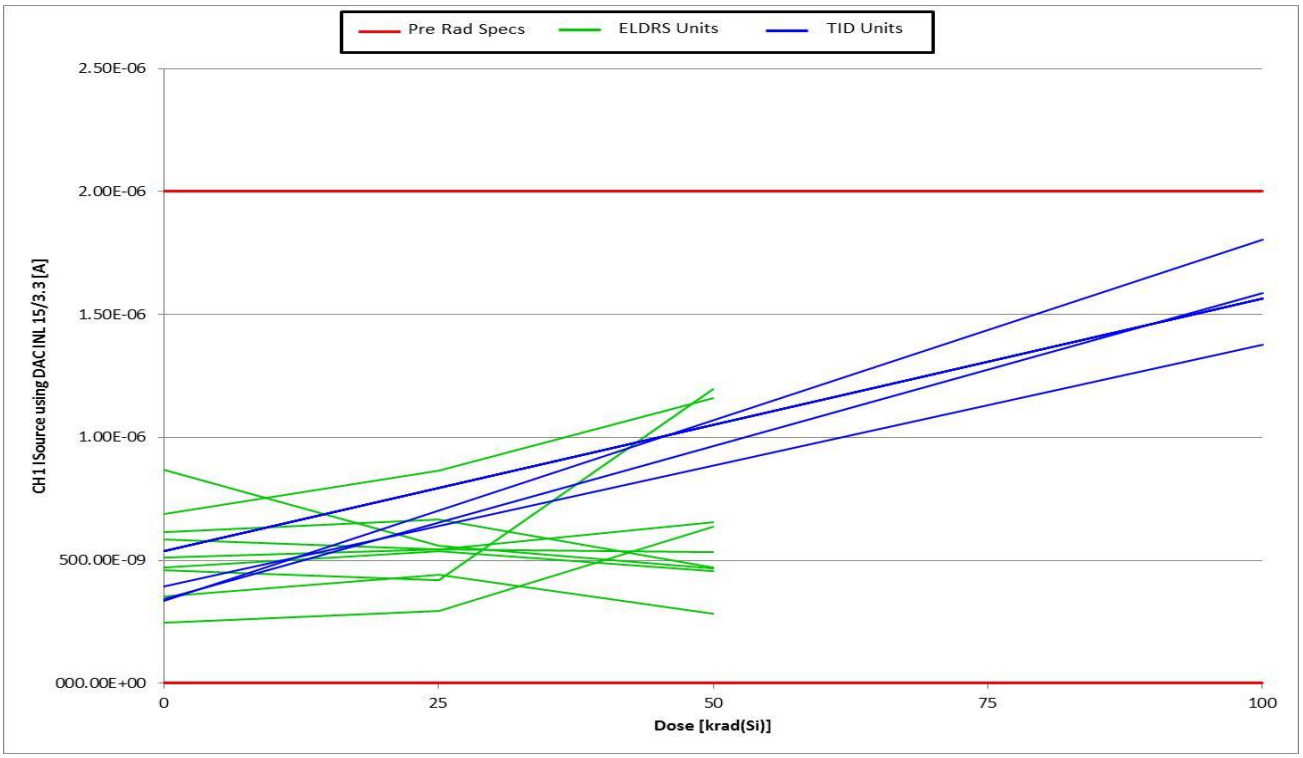
Programmable Current Source DNL (doubWt ON)



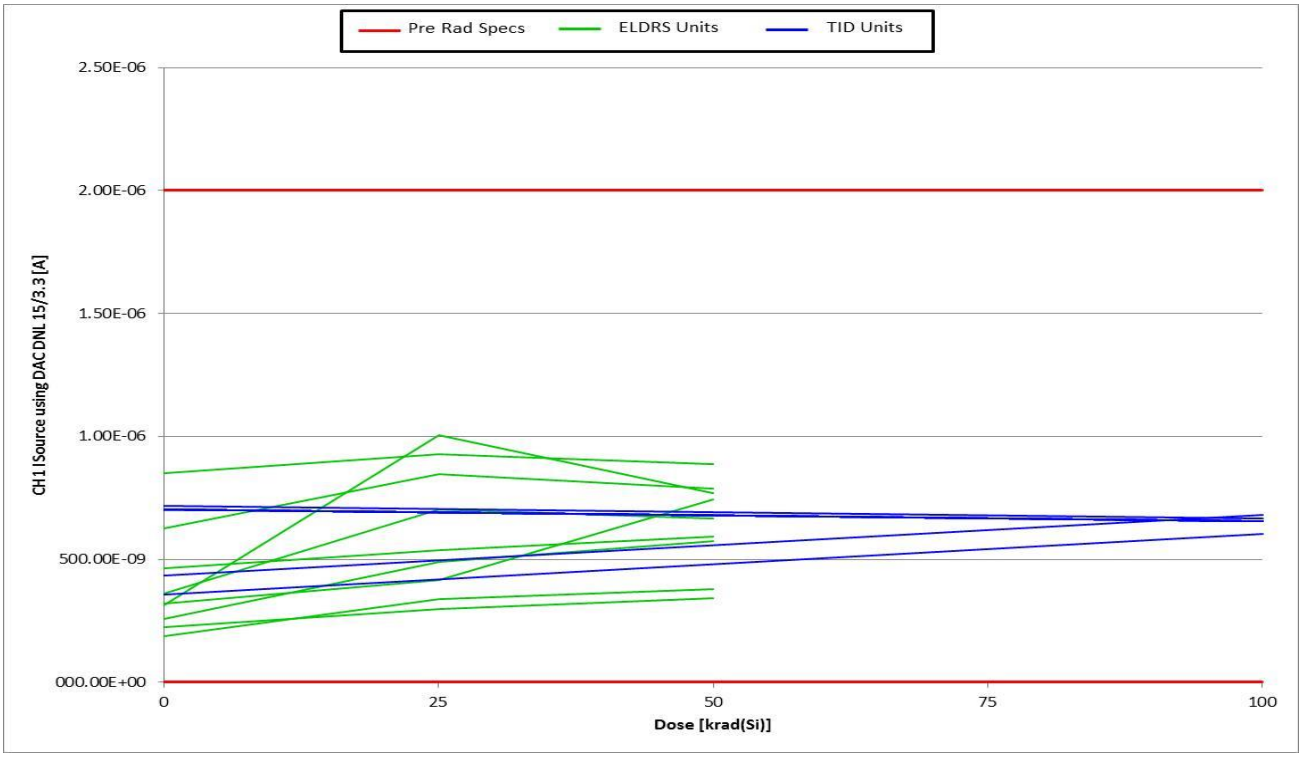
Programmable Current Source at DAC=31



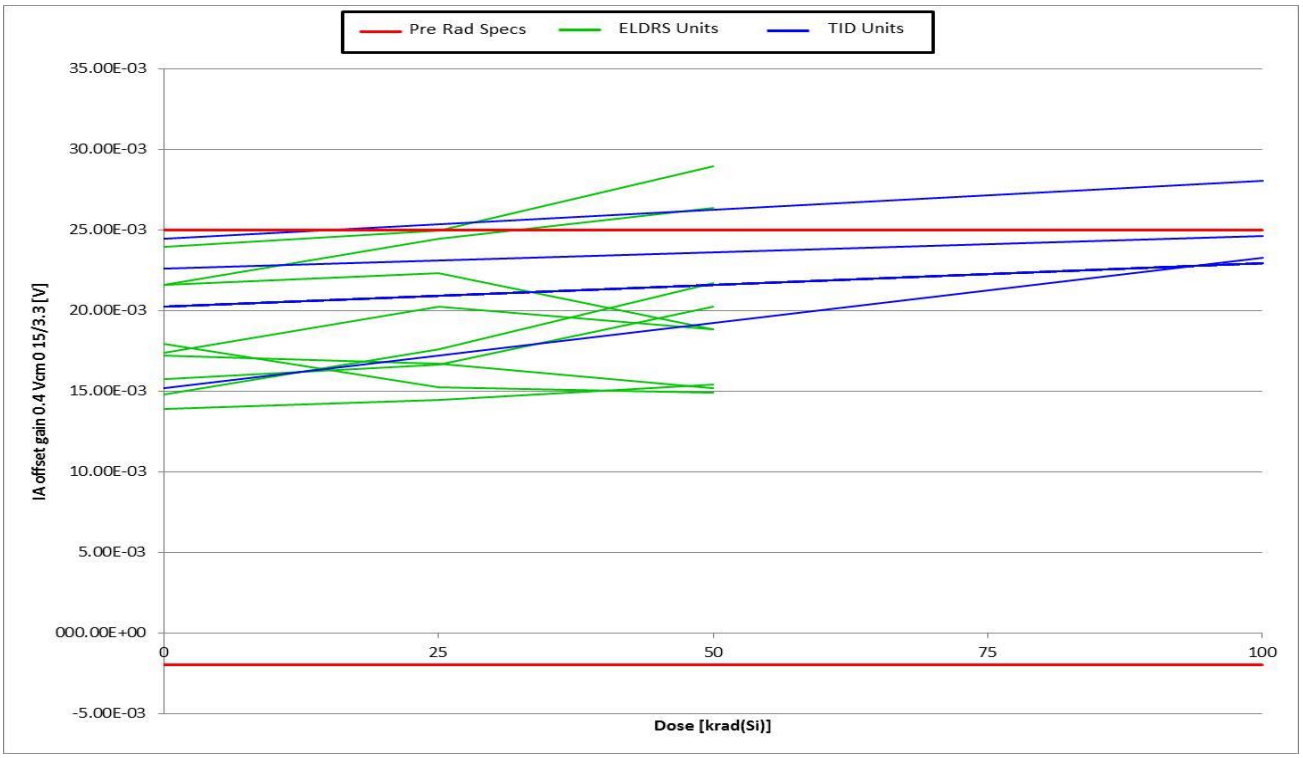
Programmable Current Source INL (DAC)



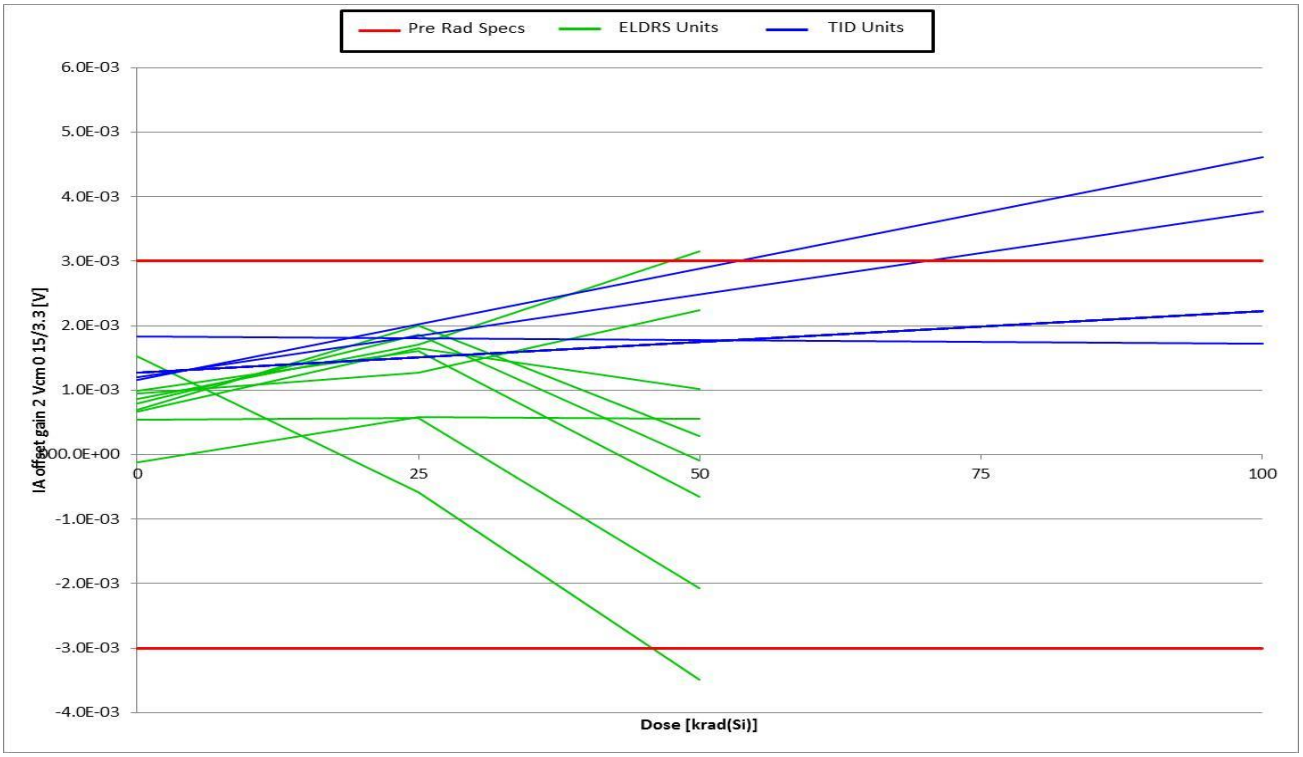
Programmable Current Source DNL (DAC)



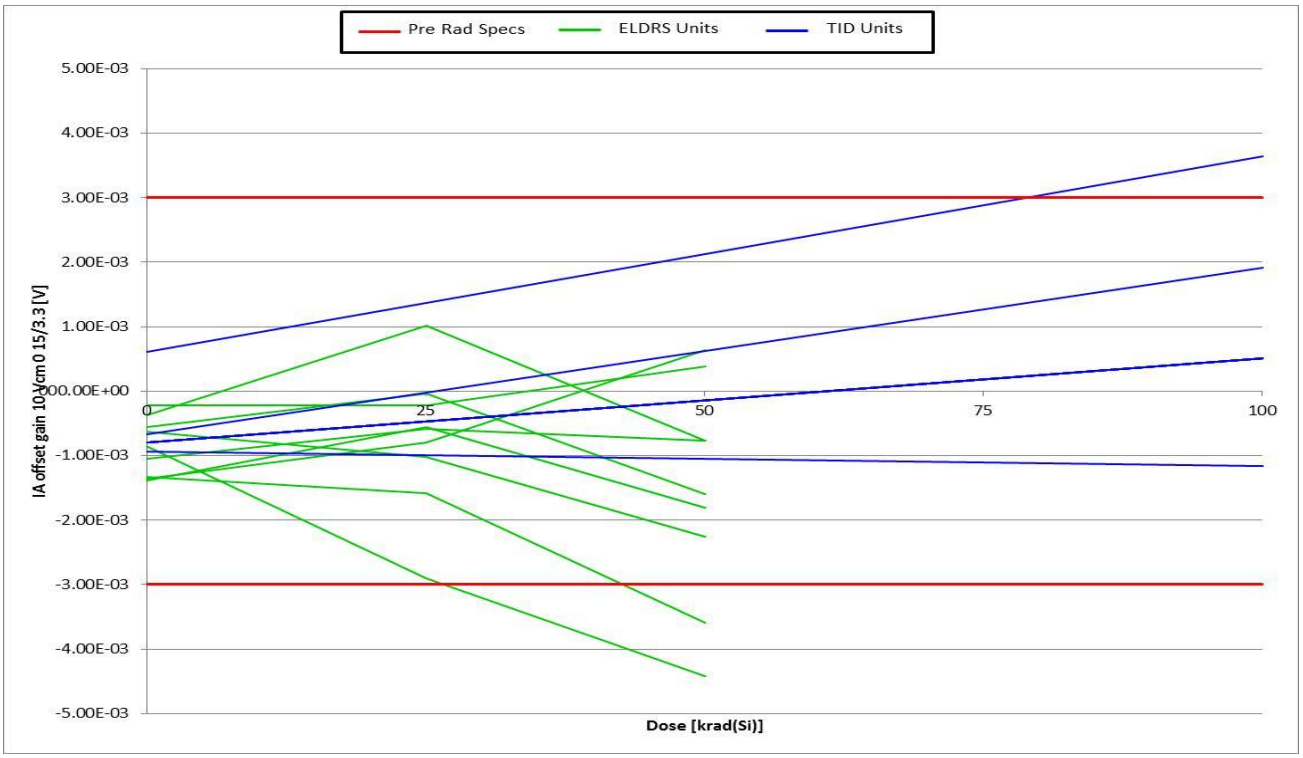
Instrumentation Amplifier Offset Voltage at Gain = 0.4



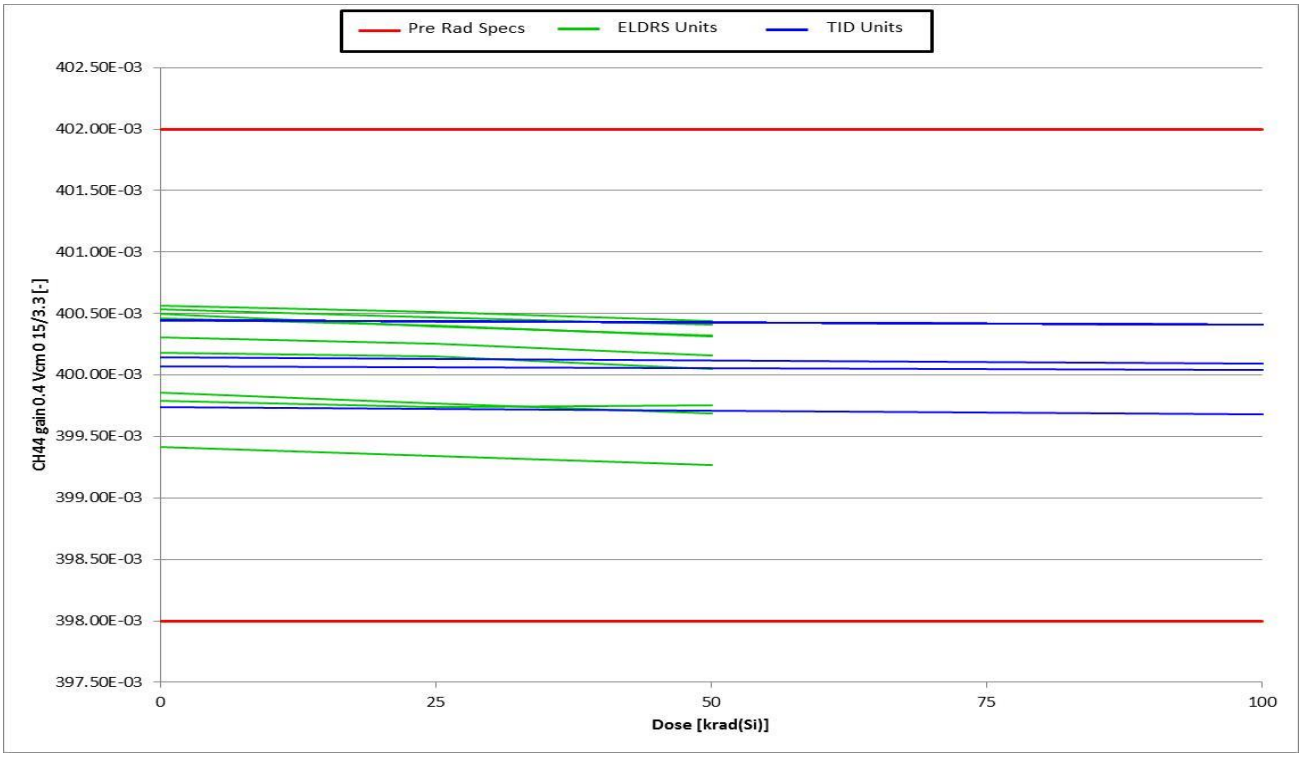
Instrumentation Amplifier Offset Voltage at Gain = 2



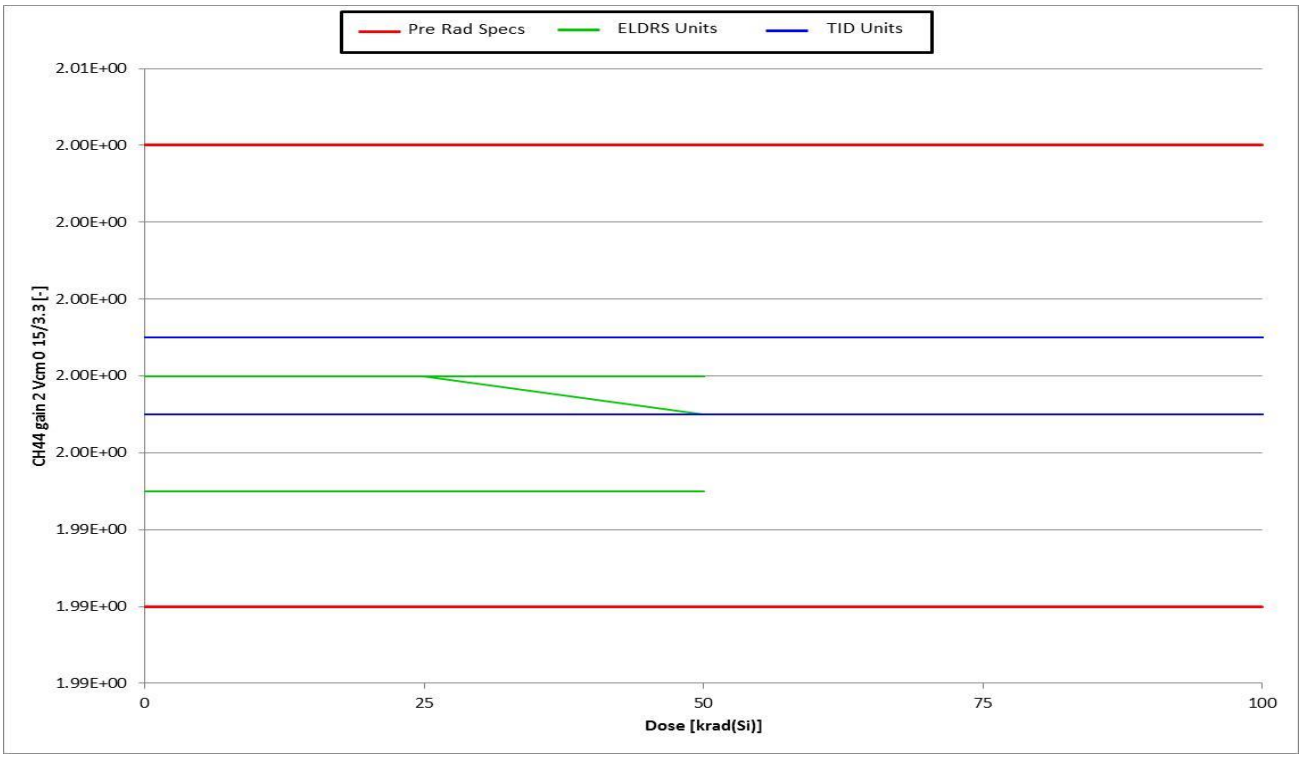
Instrumentation Amplifier Offset Voltage at Gain = 10



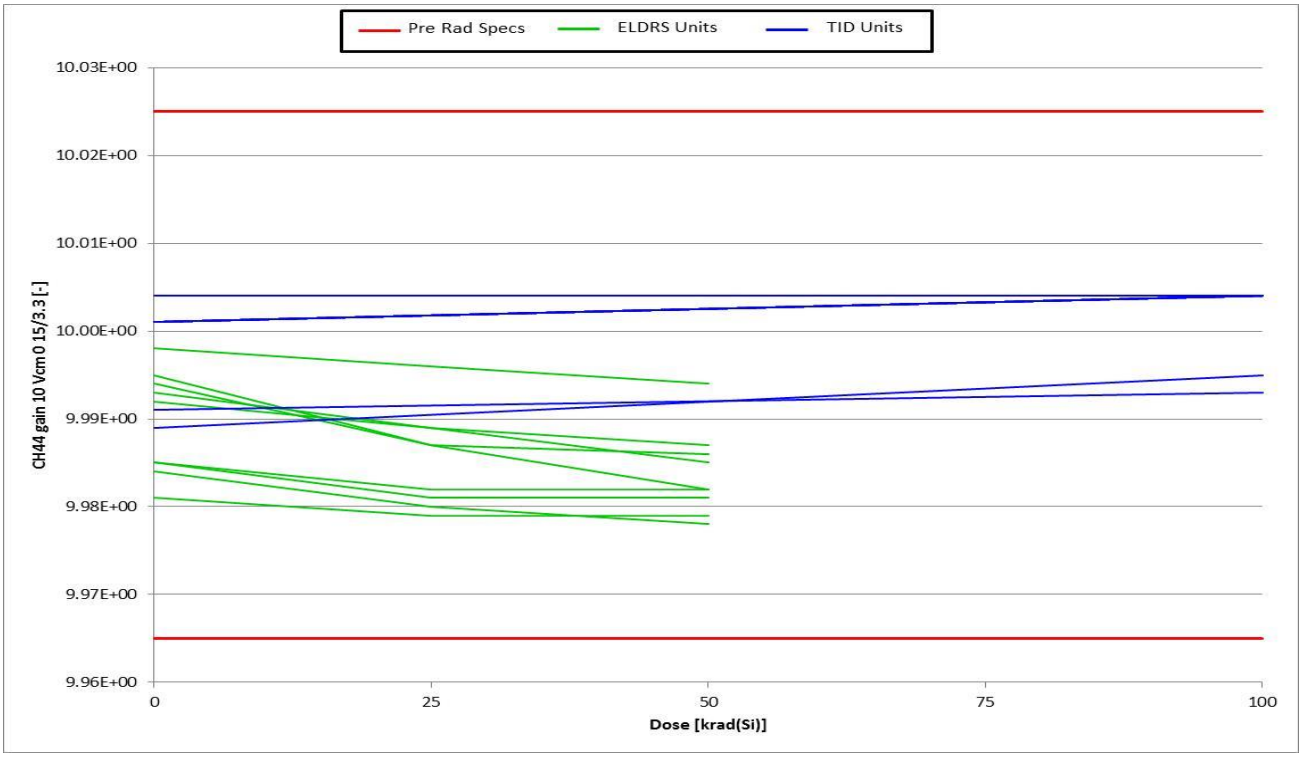
Instrumentation Amplifier Gain Accuracy at Gain = 0.4



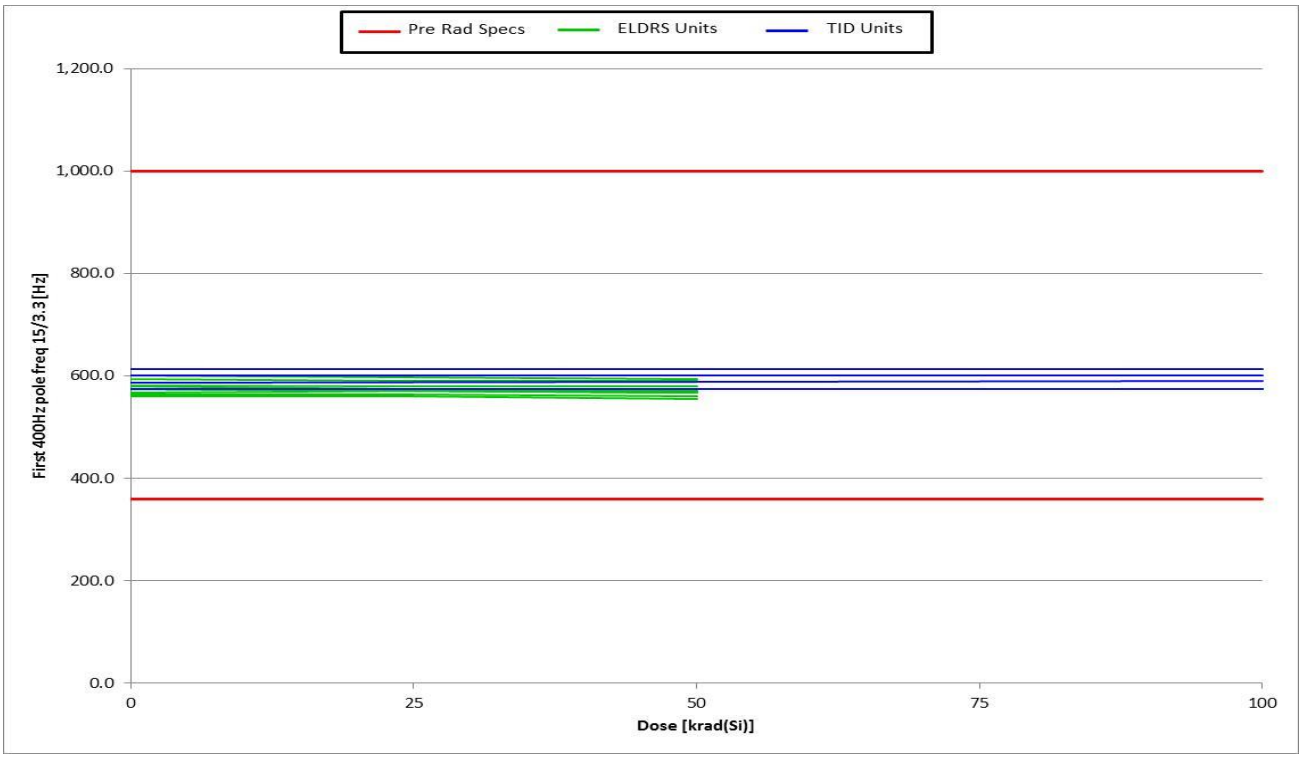
Instrumentation Amplifier Gain Accuracy at Gain = 2



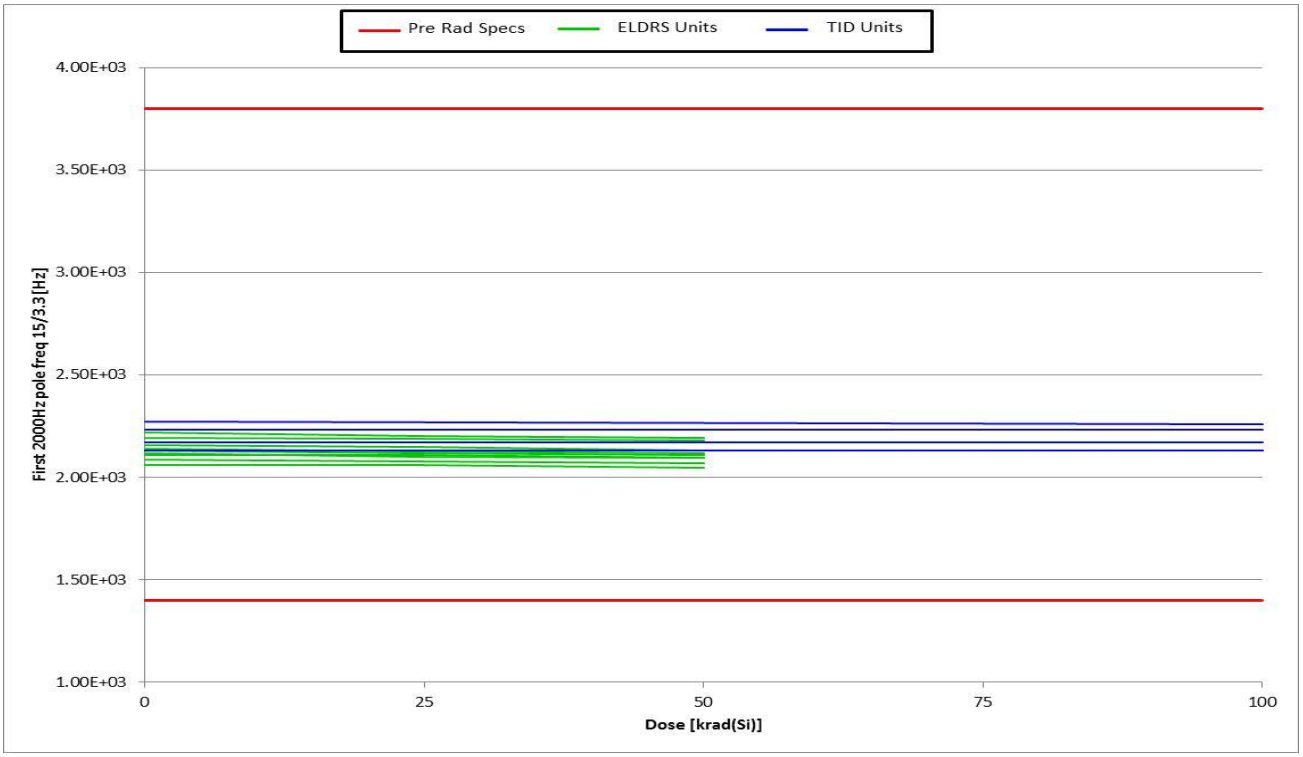
Instrumentation Amplifier Gain Accuracy at Gain = 10



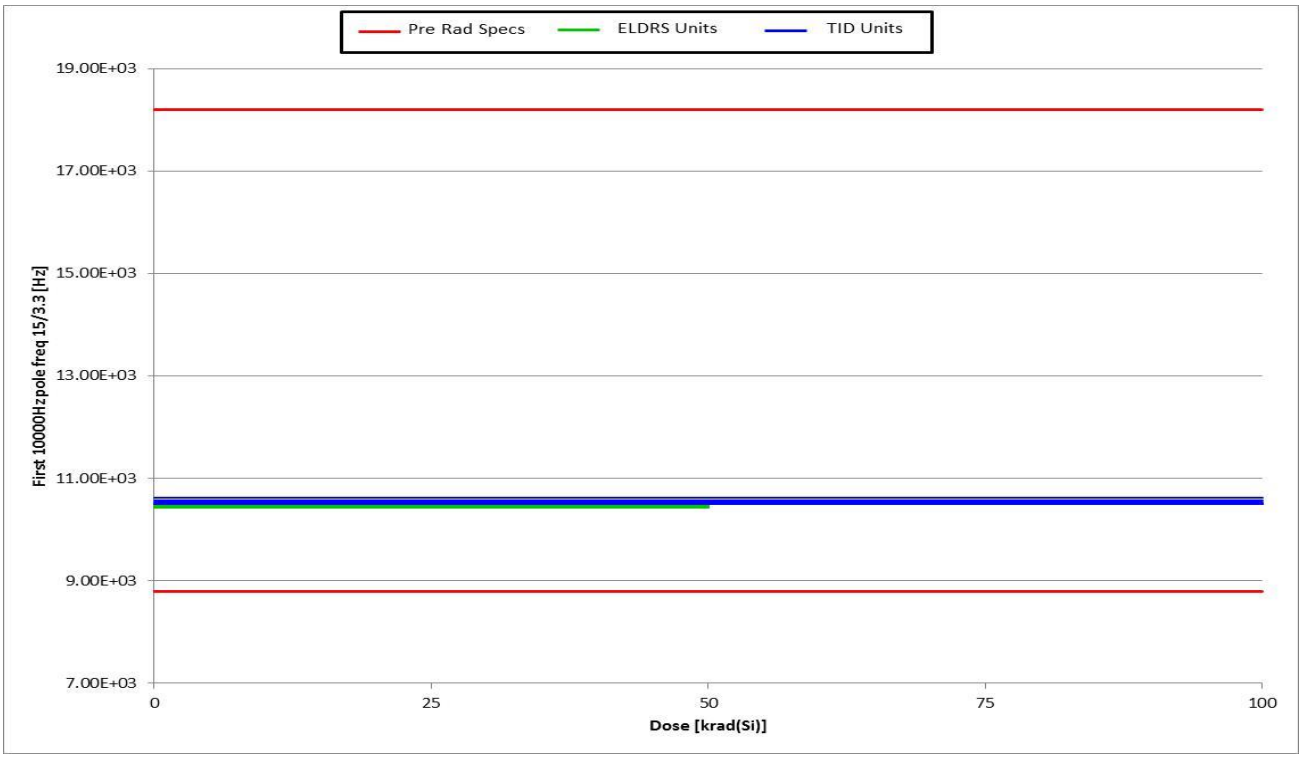
Instrumentation Amplifier First Pole Frequency (400Hz)



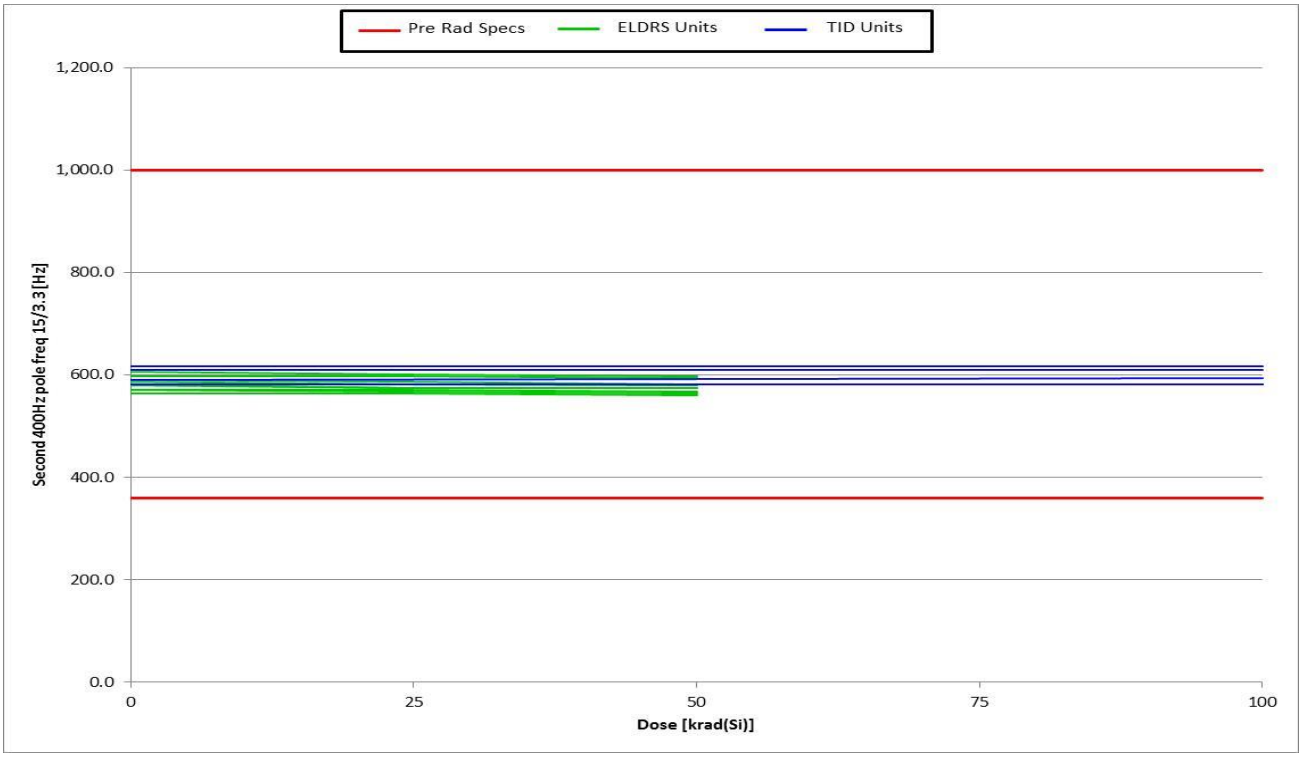
Instrumentation Amplifier First Pole Frequency (2000Hz)



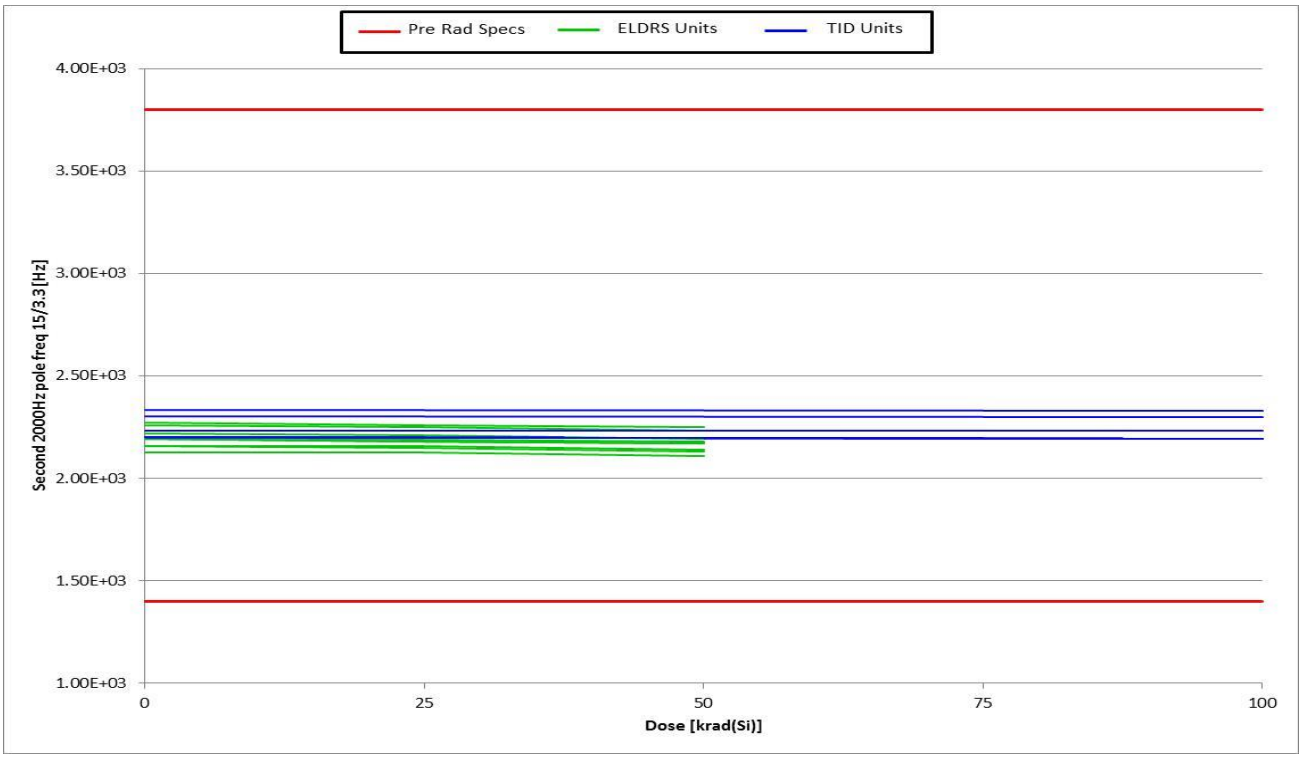
Instrumentation Amplifier First Pole Frequency (10000Hz)



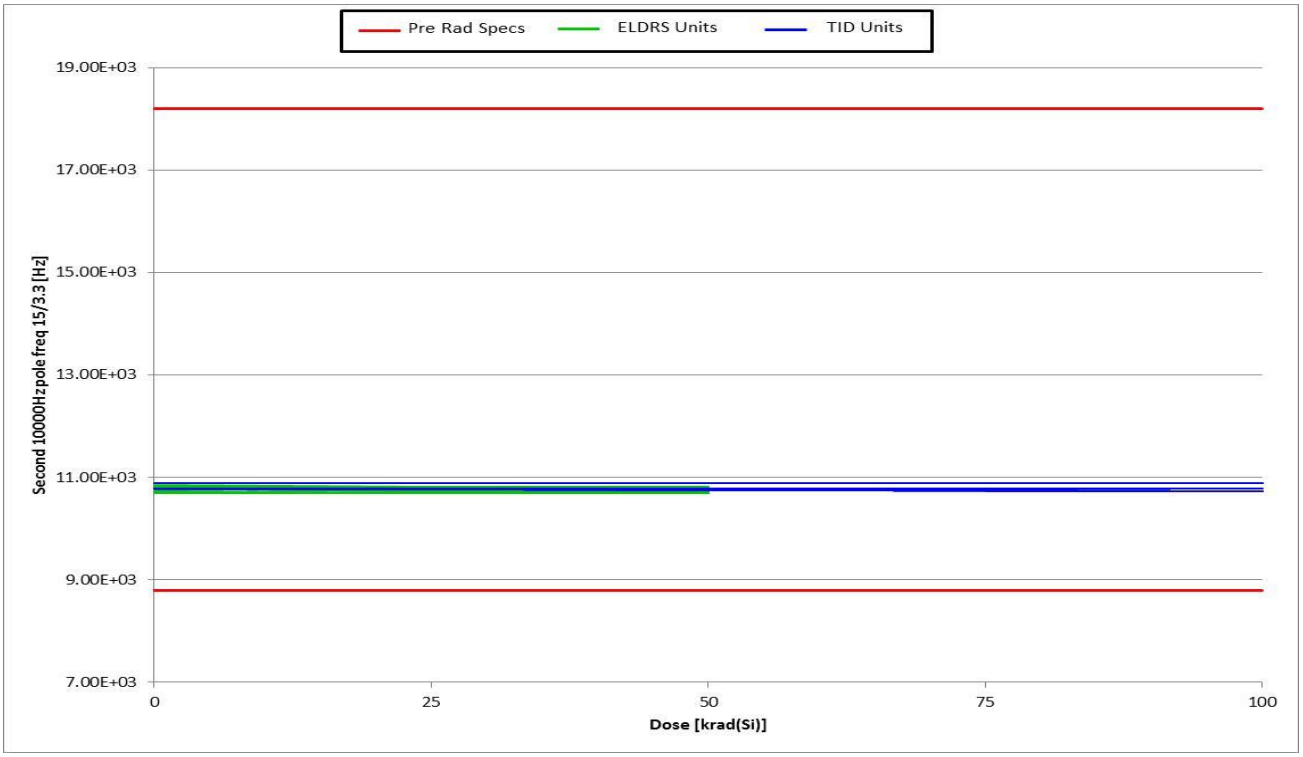
Instrumentation Amplifier Second Pole Frequency (400Hz)



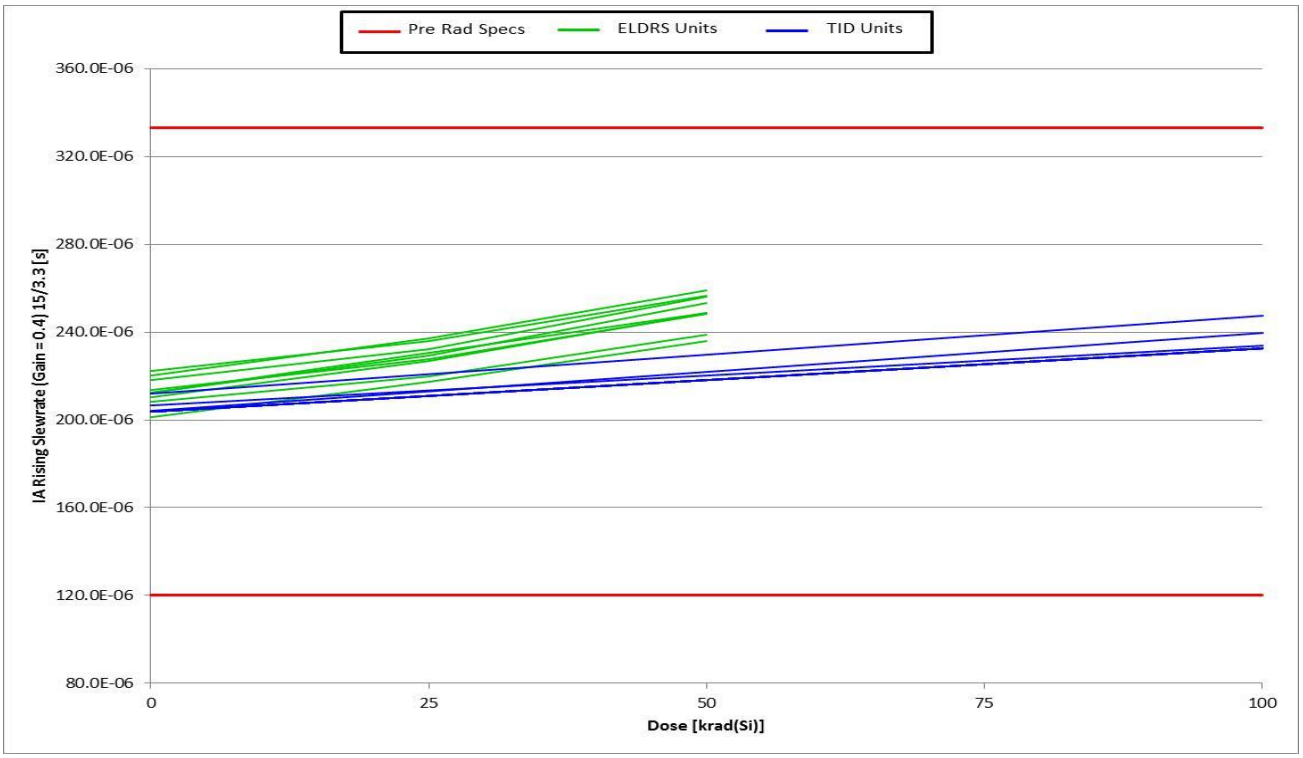
Instrumentation Amplifier Second Pole Frequency (2000Hz)



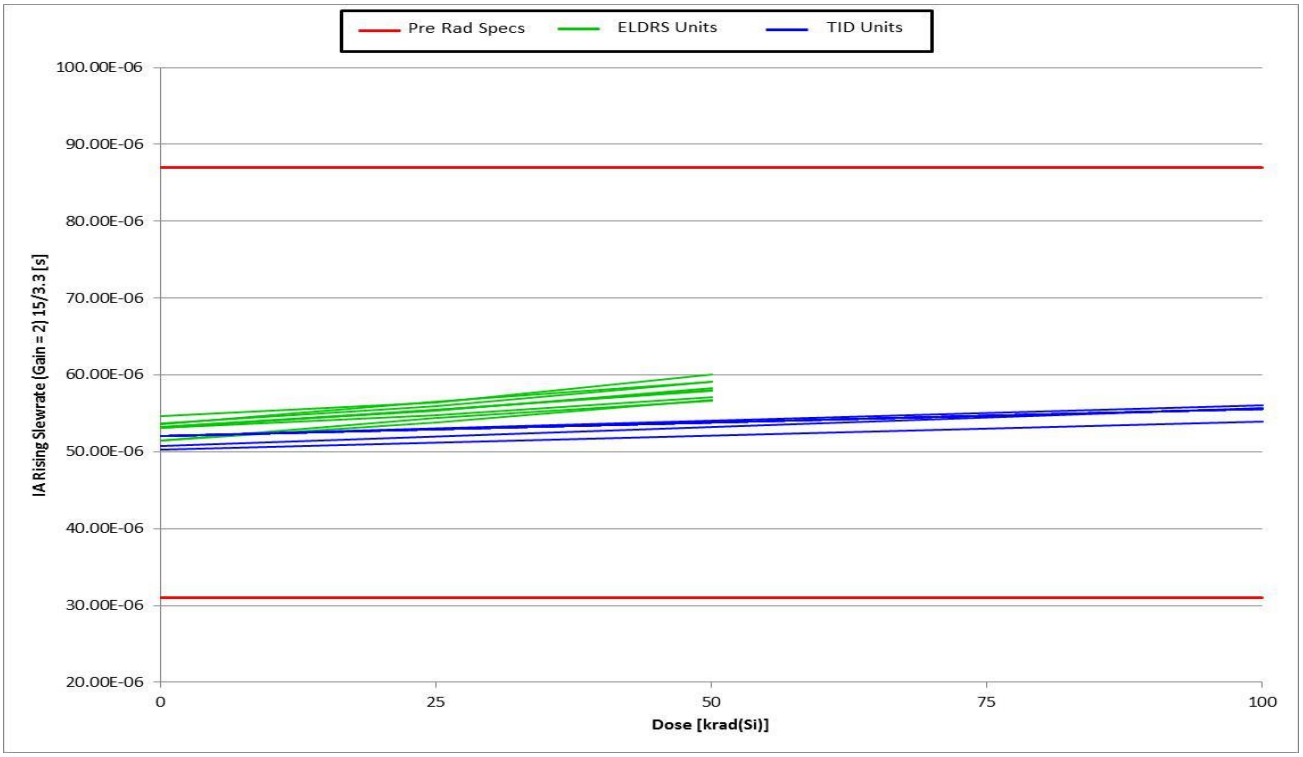
Instrumentation Amplifier Second Pole Frequency (10000Hz)



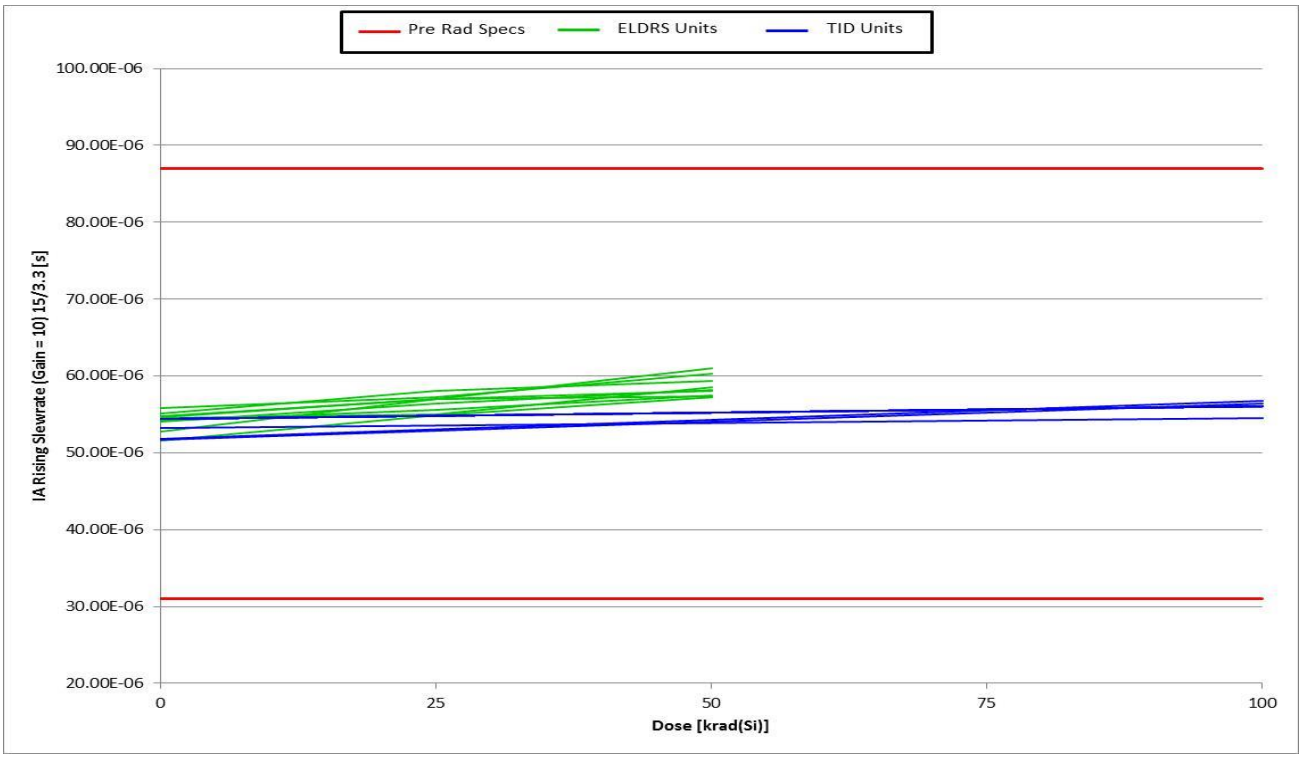
Instrumentation Amplifier Output Step Rise Time (G=0.4)



Instrumentation Amplifier Output Step Rise Time (G=2)

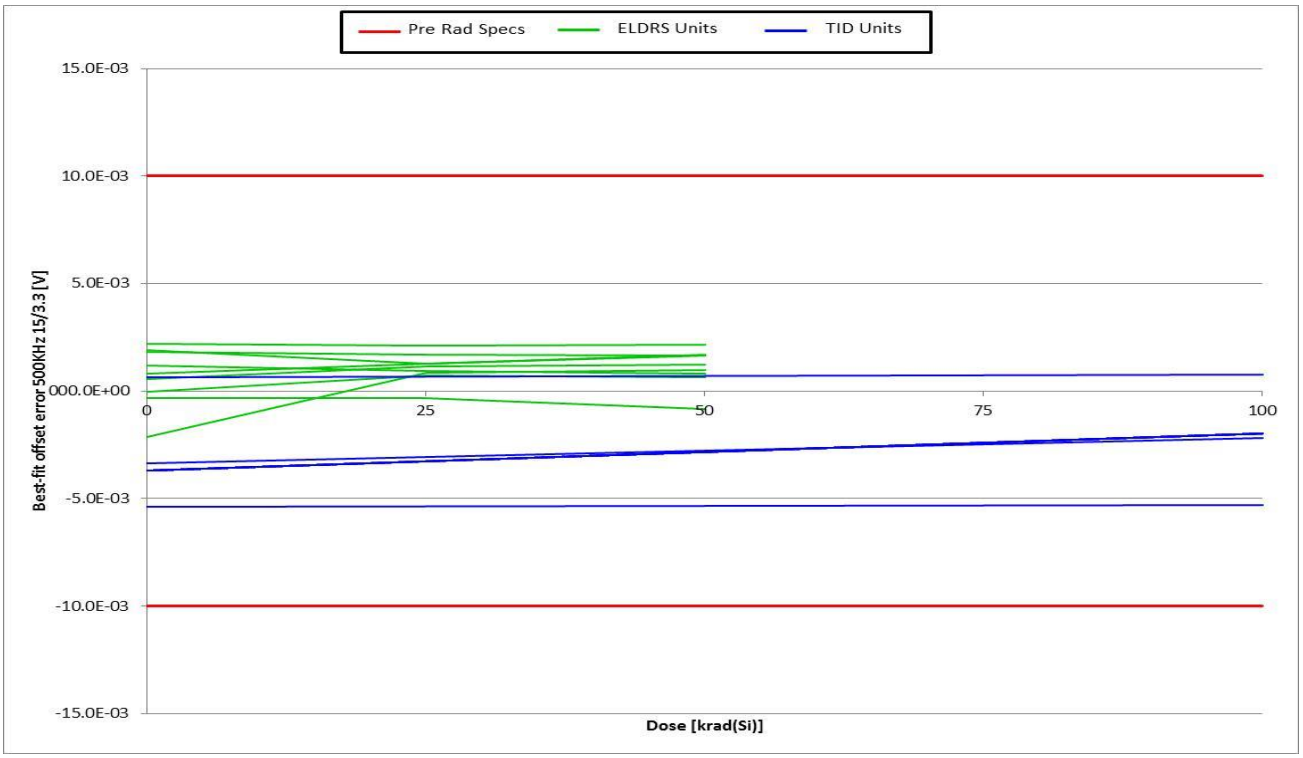


Instrumentation Amplifier Output Step Rise Time (G=10)

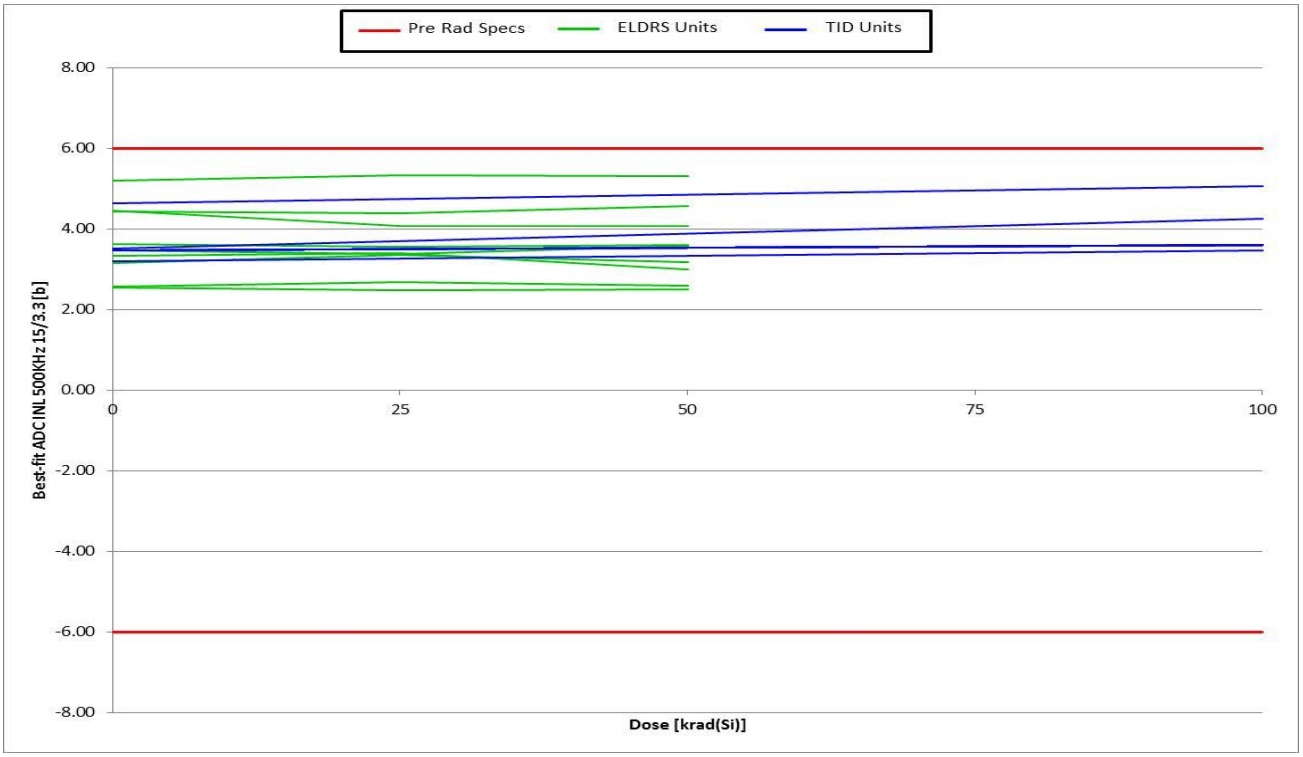


ADC Full Scale Error

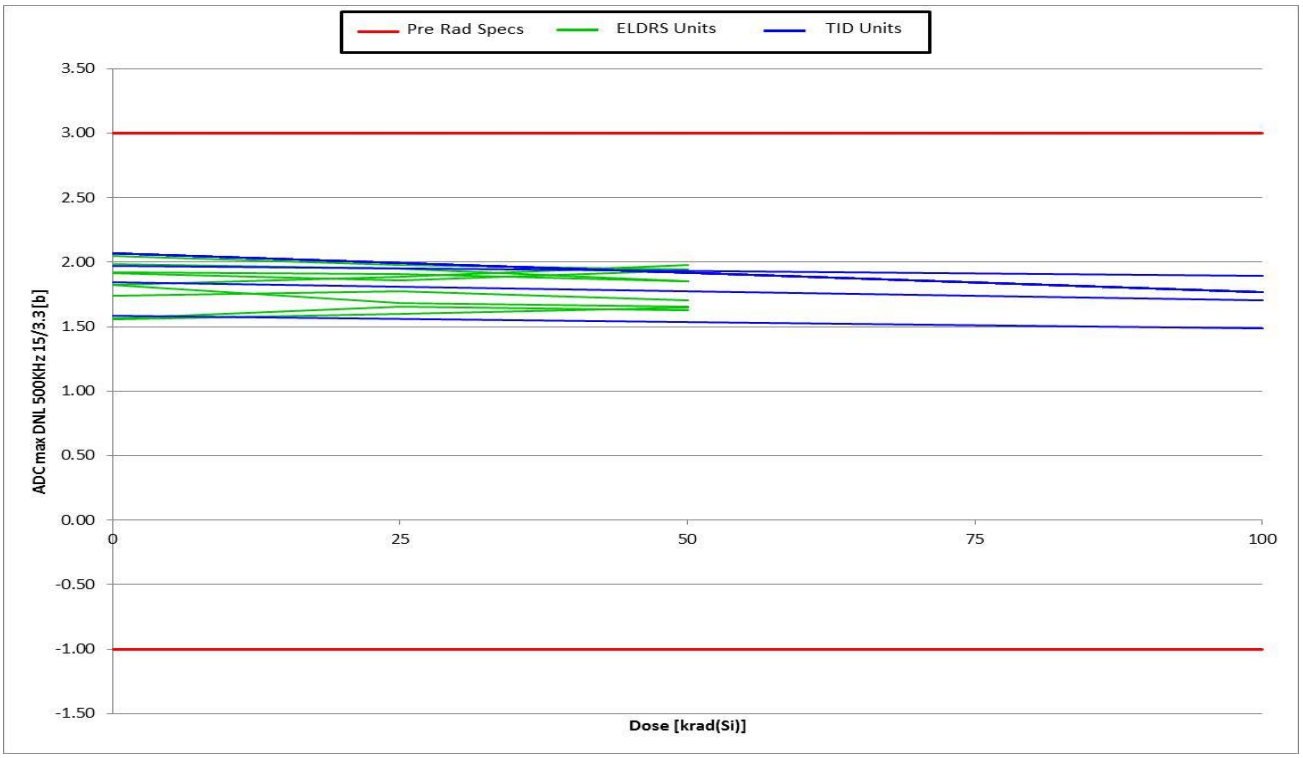
ADC Offset Error



ADC INL

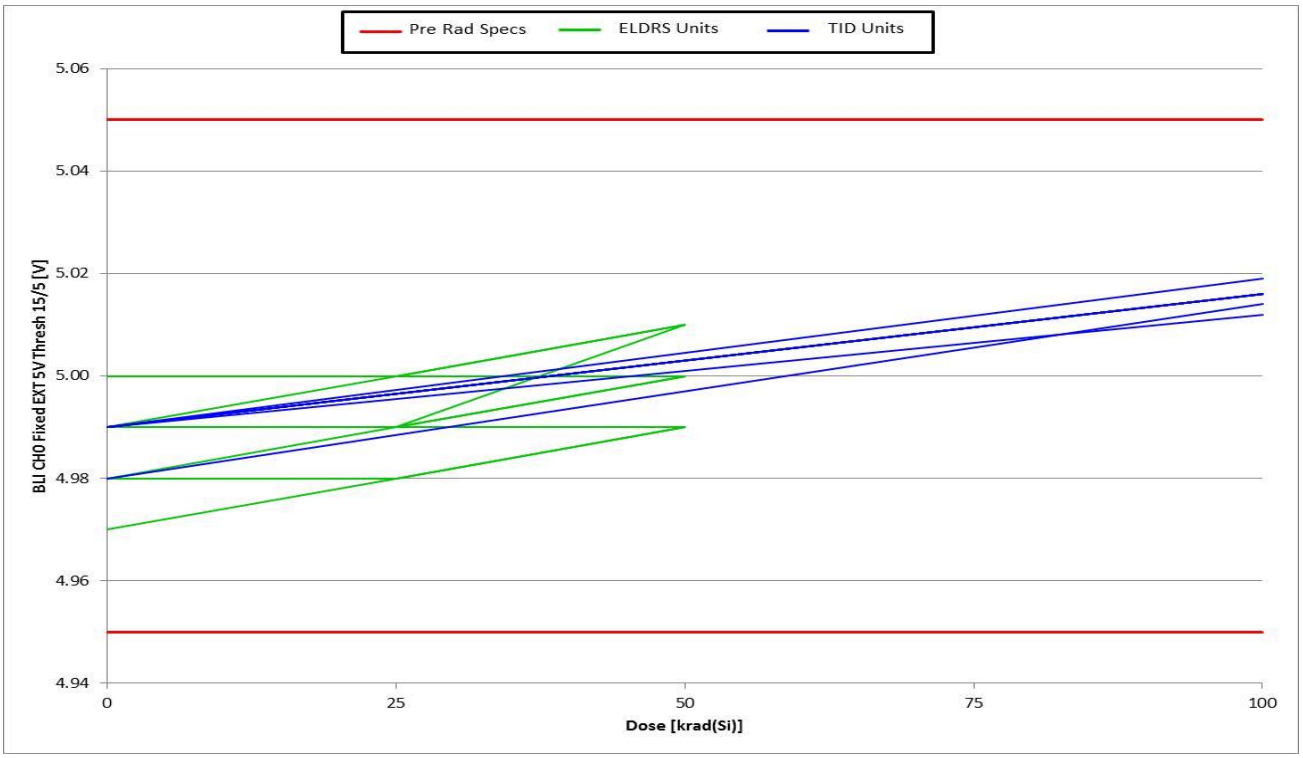


ADC DNL

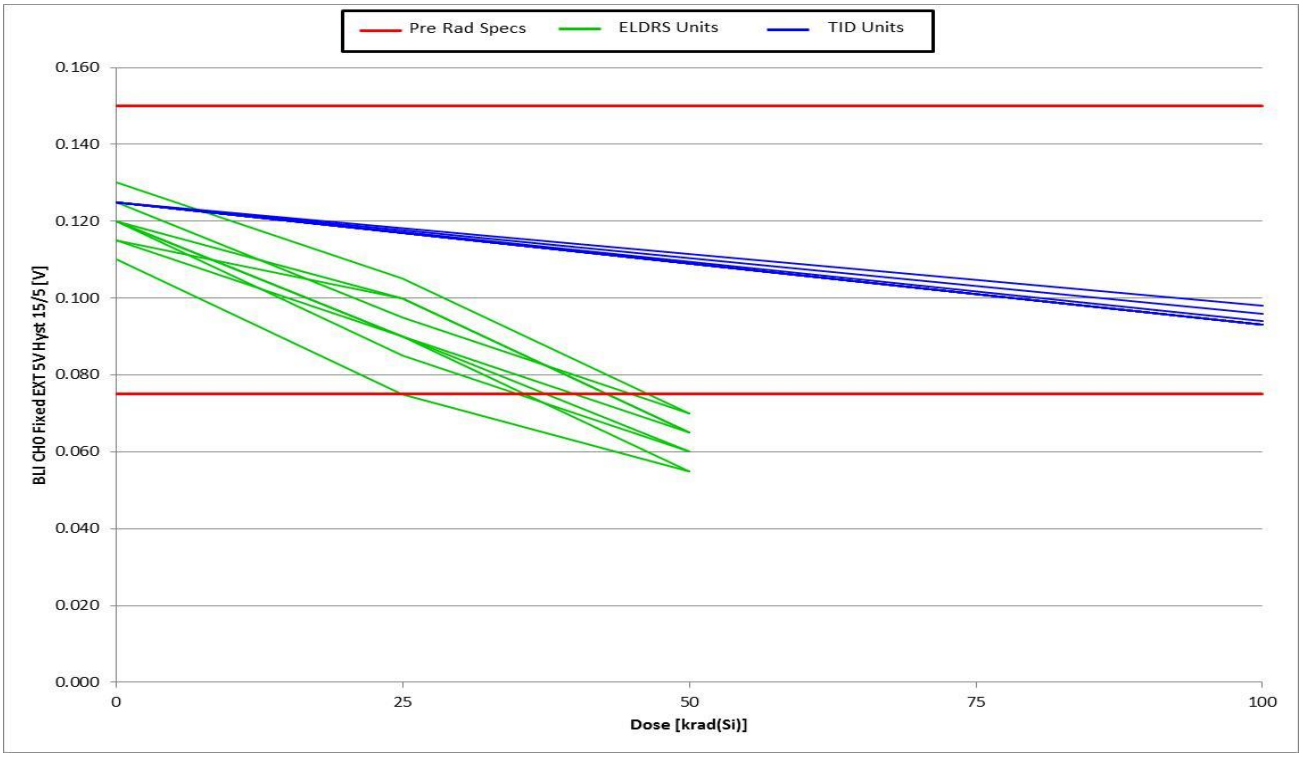


ADC Input Leakage

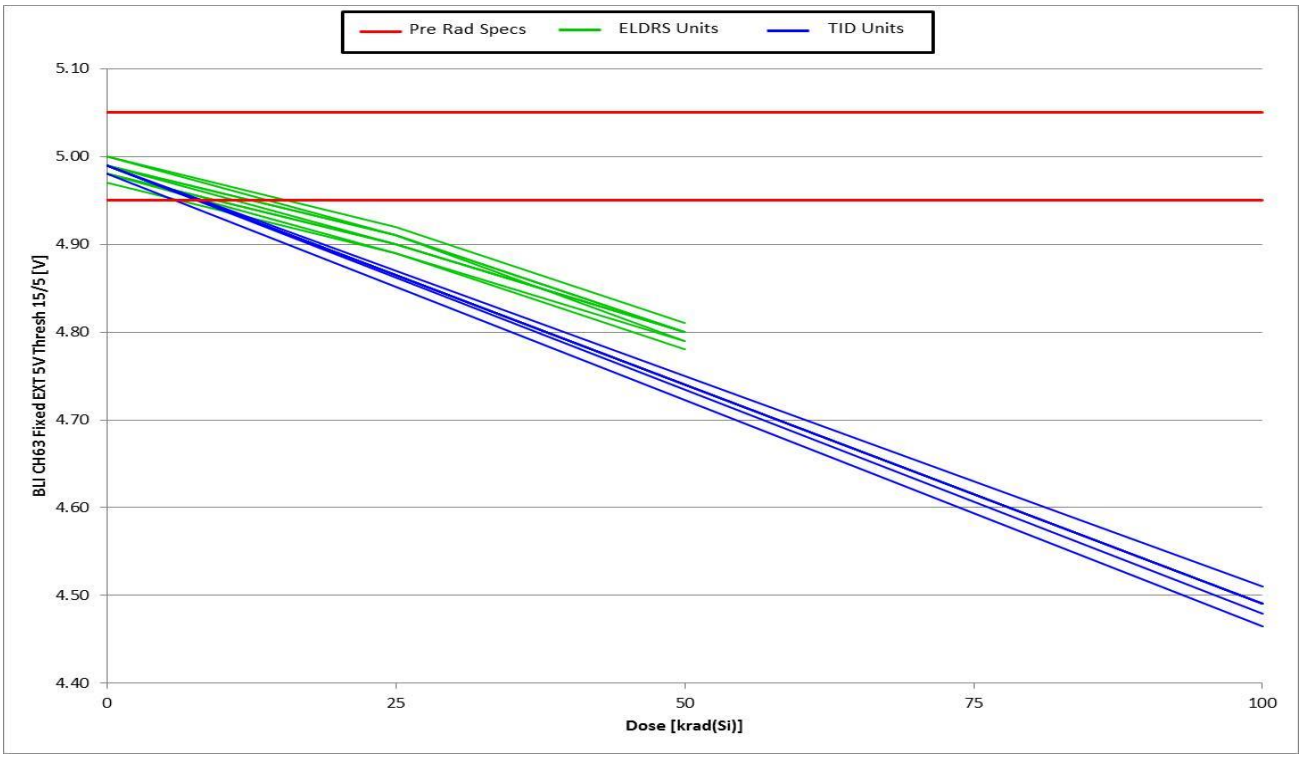
Adjustable threshold Bi-level MUX Threshold at DAC Max Output (If input >=0V during exposure)



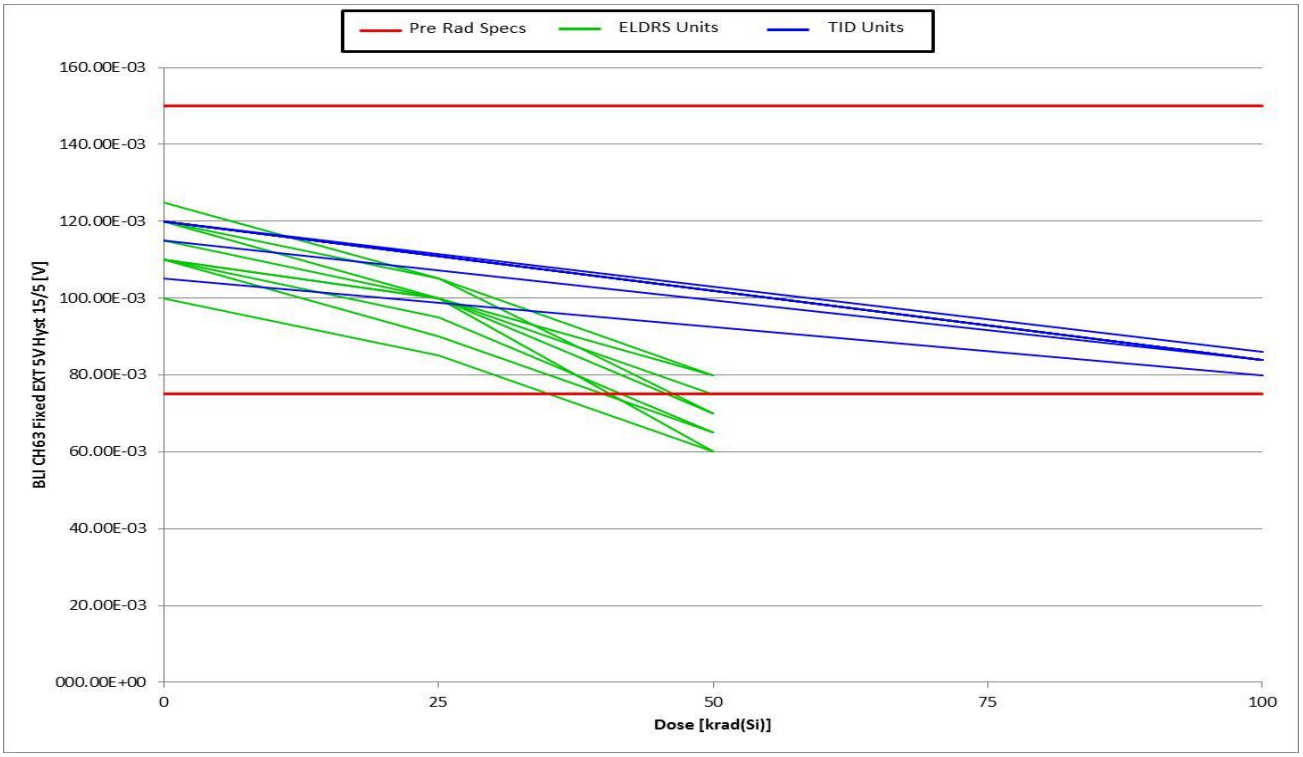
Adjustable threshold Bi-level MUX Threshold Hysteresis at DAC Max Output (If input >=0V during exposure)



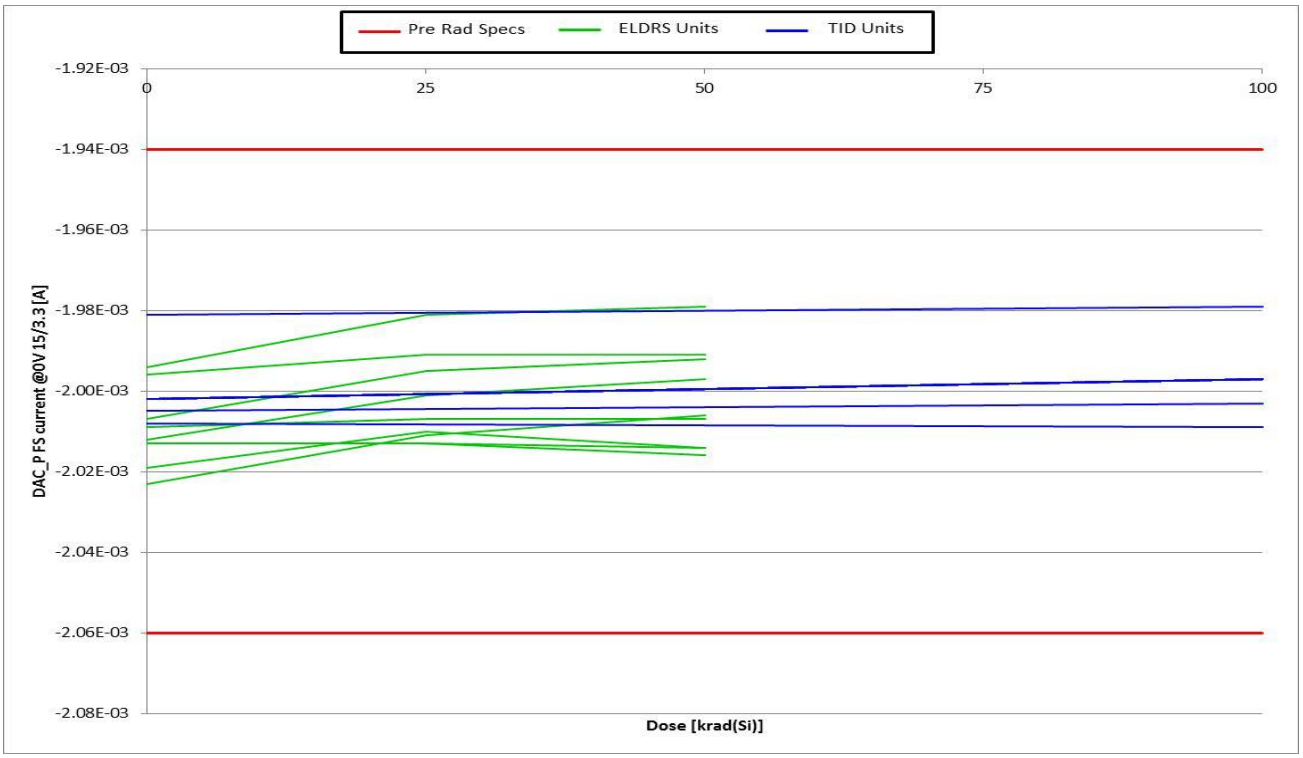
Adjustable threshold Bi-level MUX Threshold at DAC Max Output (If input = VEE/2 during exposure)



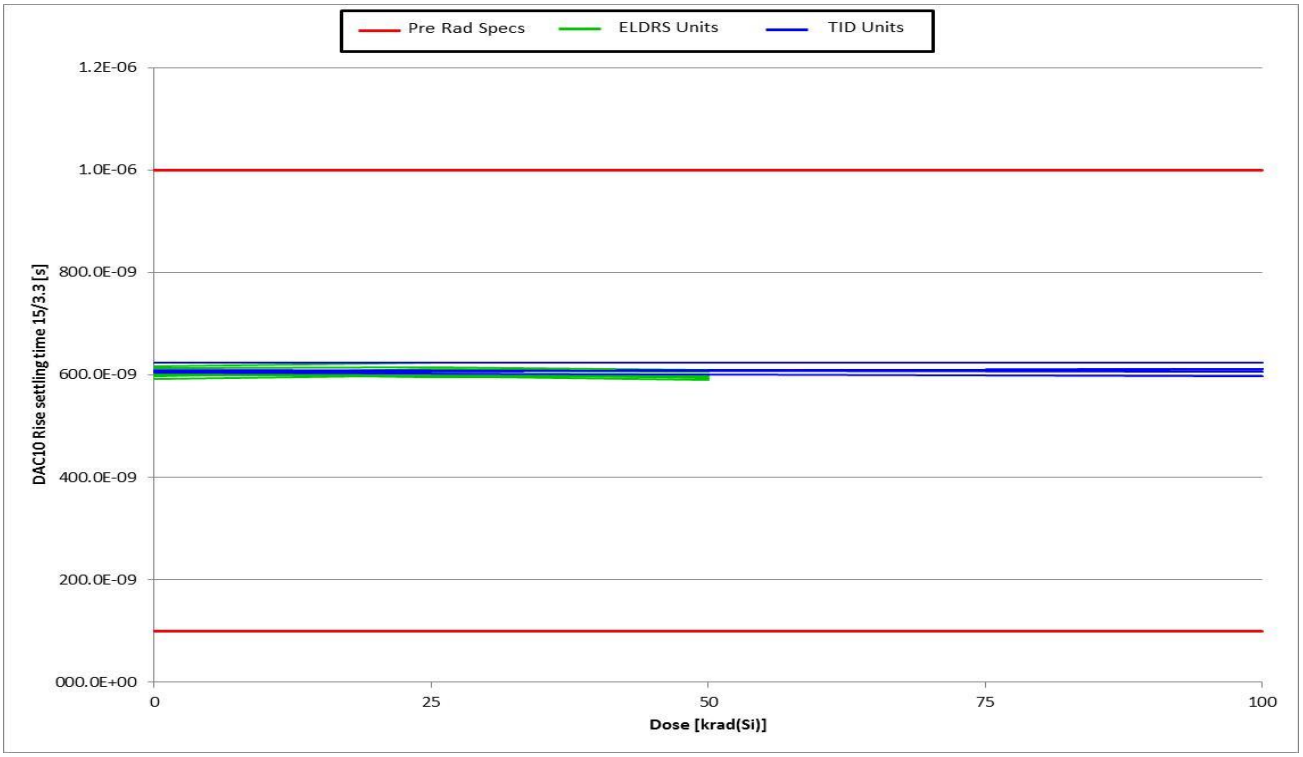
Adjustable threshold Bi-level MUX Threshold Hysteresis at DAC Max Output (If input = VEE/2 during exposure)



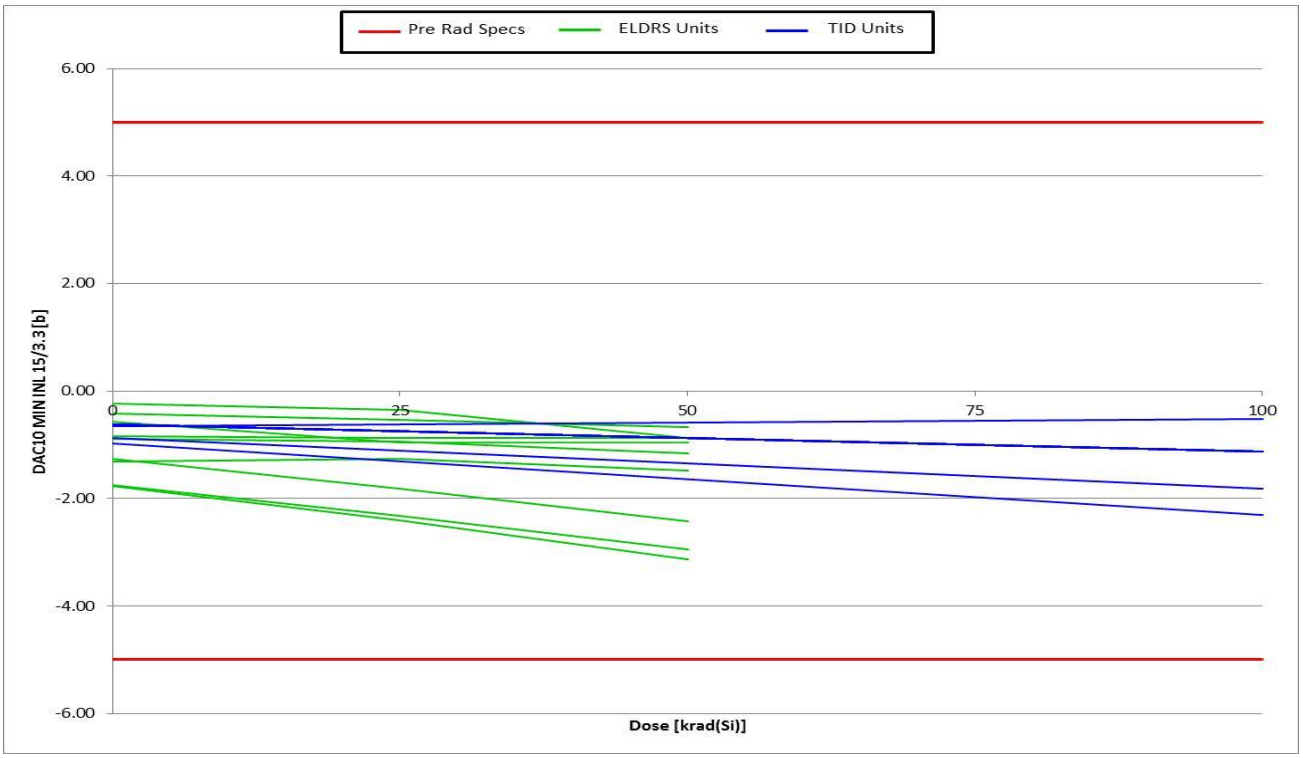
10 Bit Current DAC Full Scale



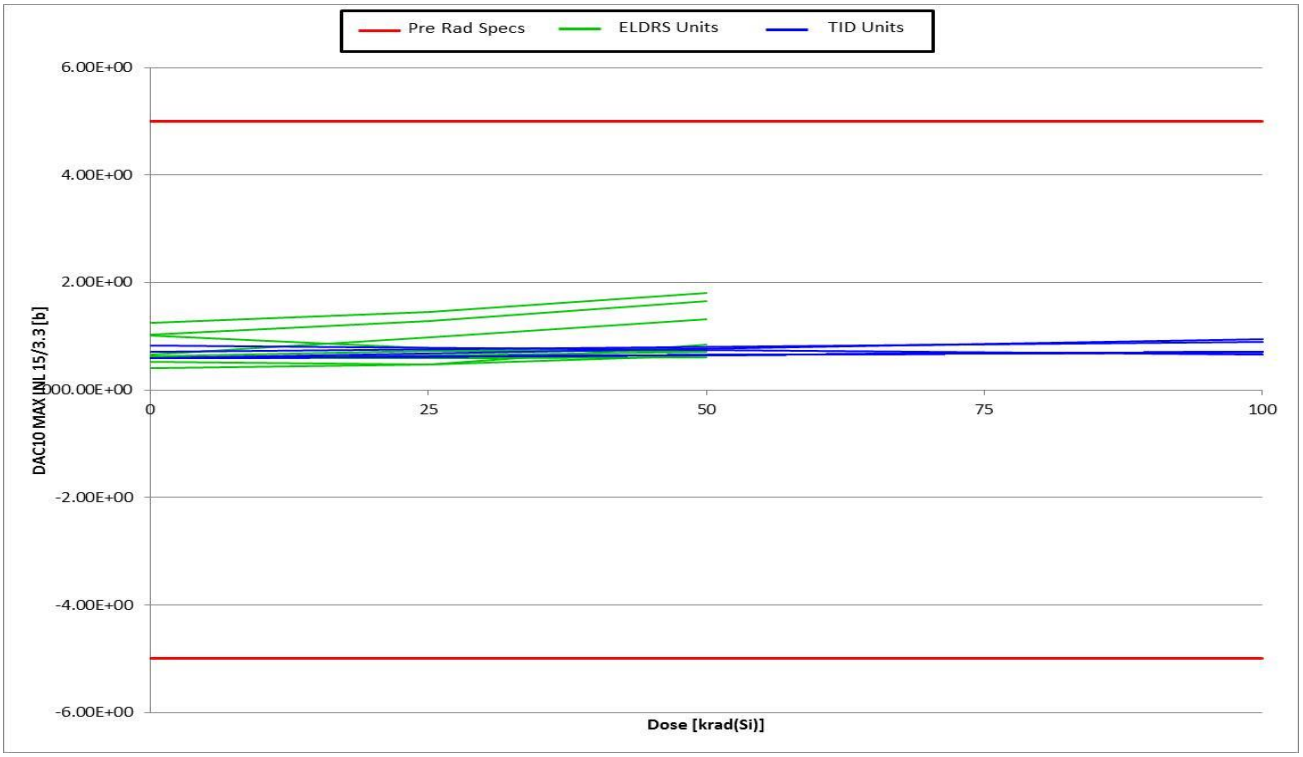
10 Bit Current DAC Settling Time



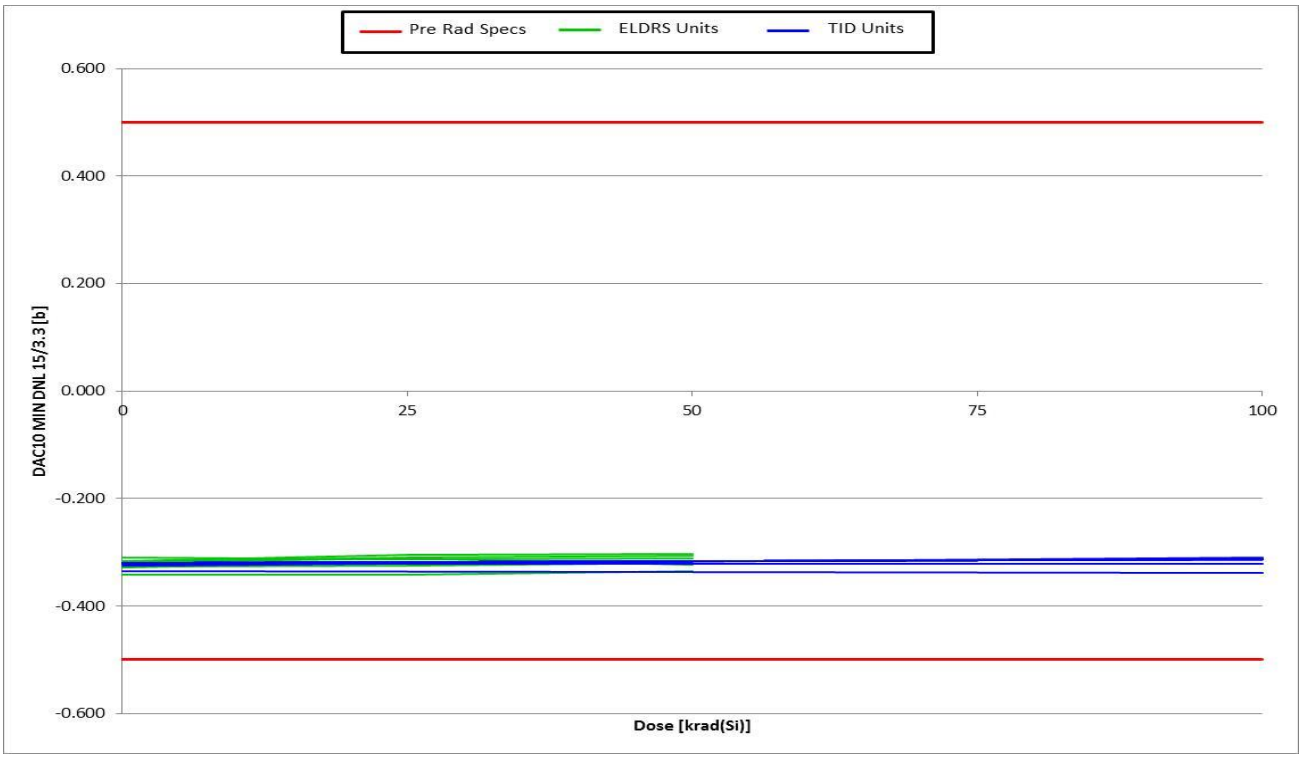
10 Bit Current DAC INL Min



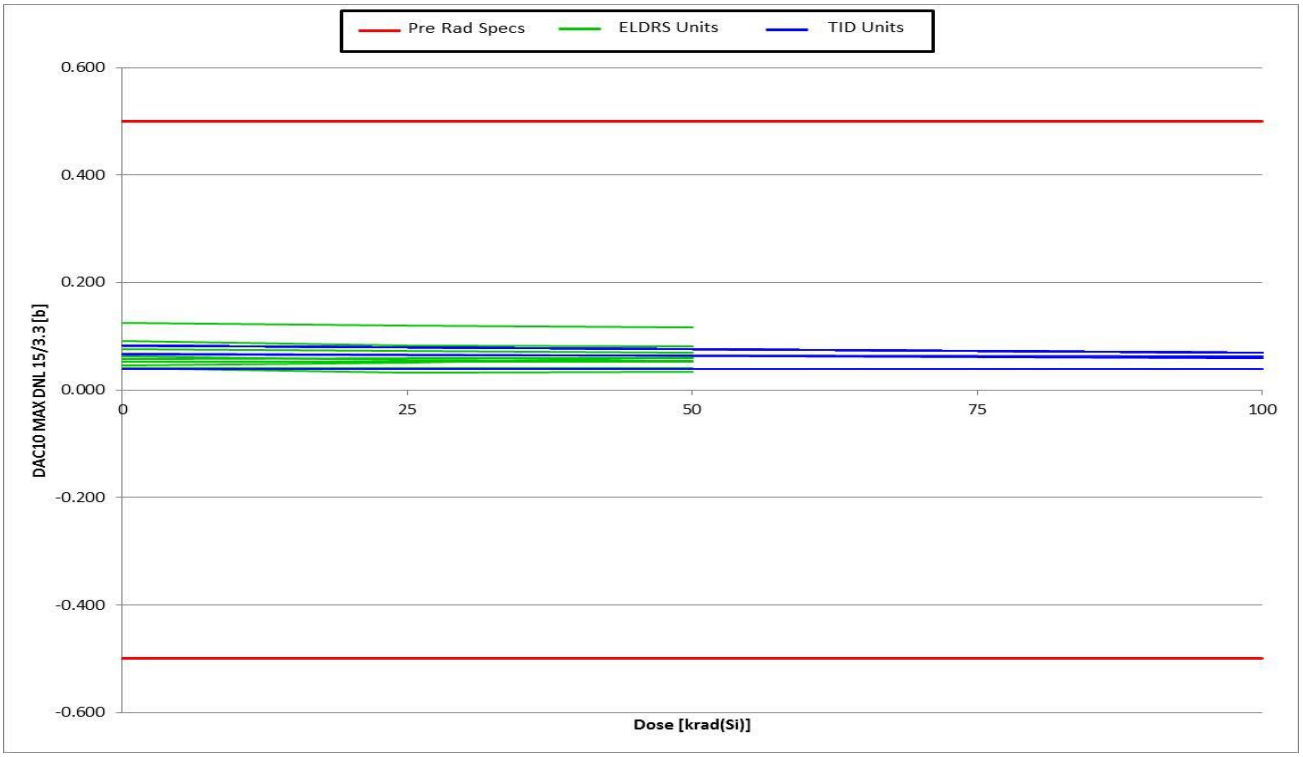
10 Bit Current DAC INL Max



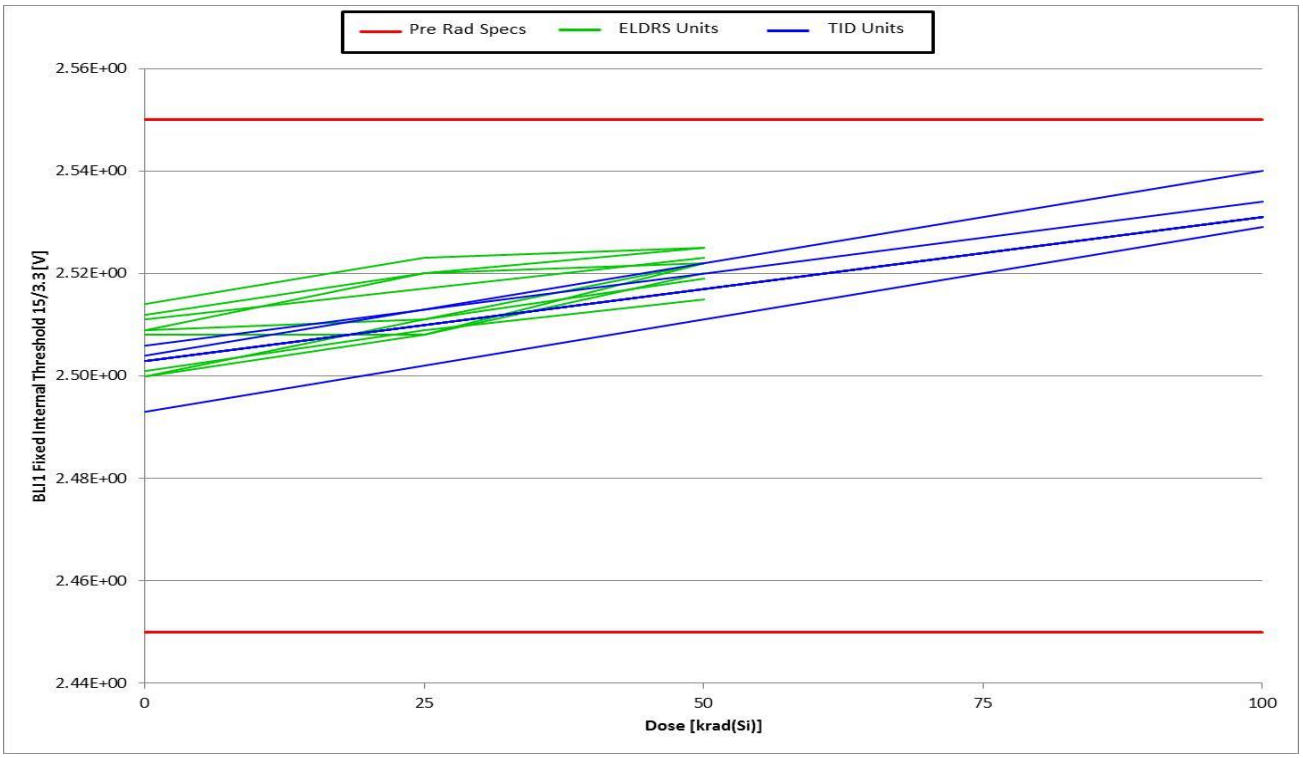
10 Bit Current DAC DNL Min



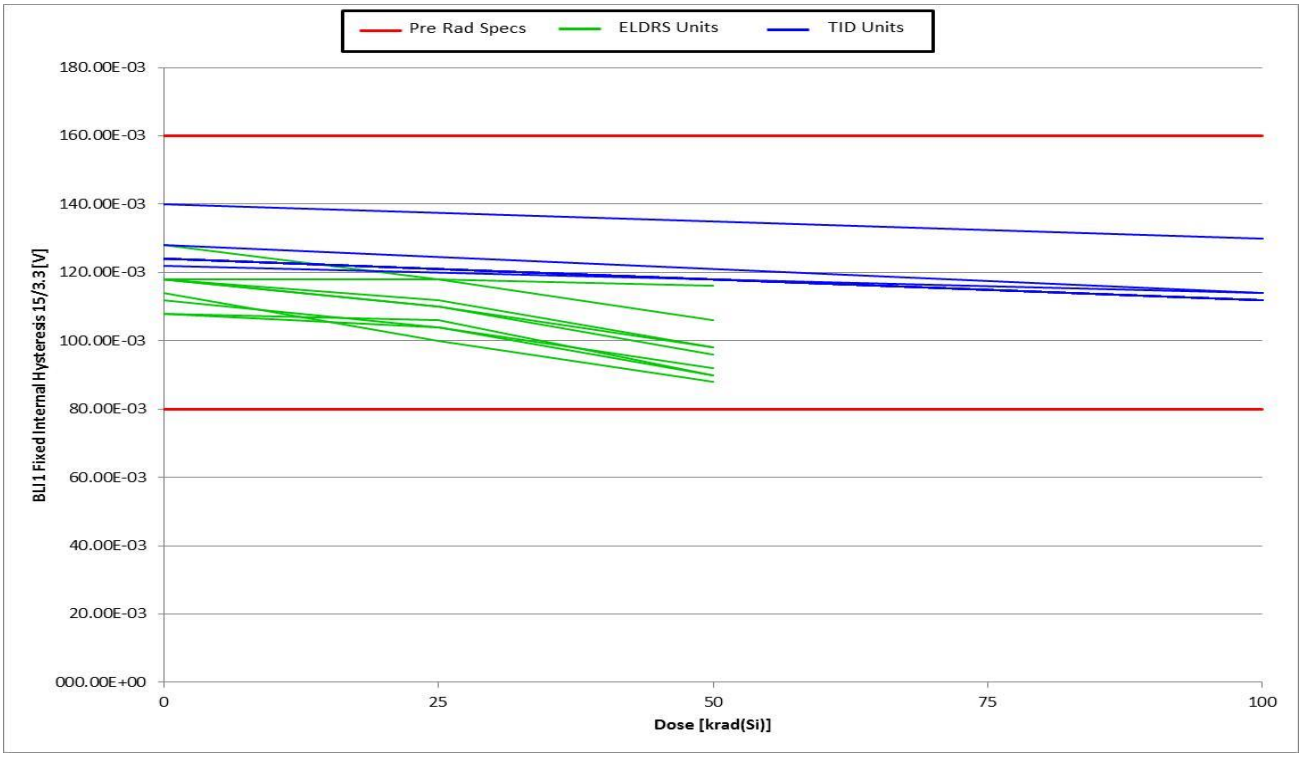
10 Bit Current DAC DNL Min



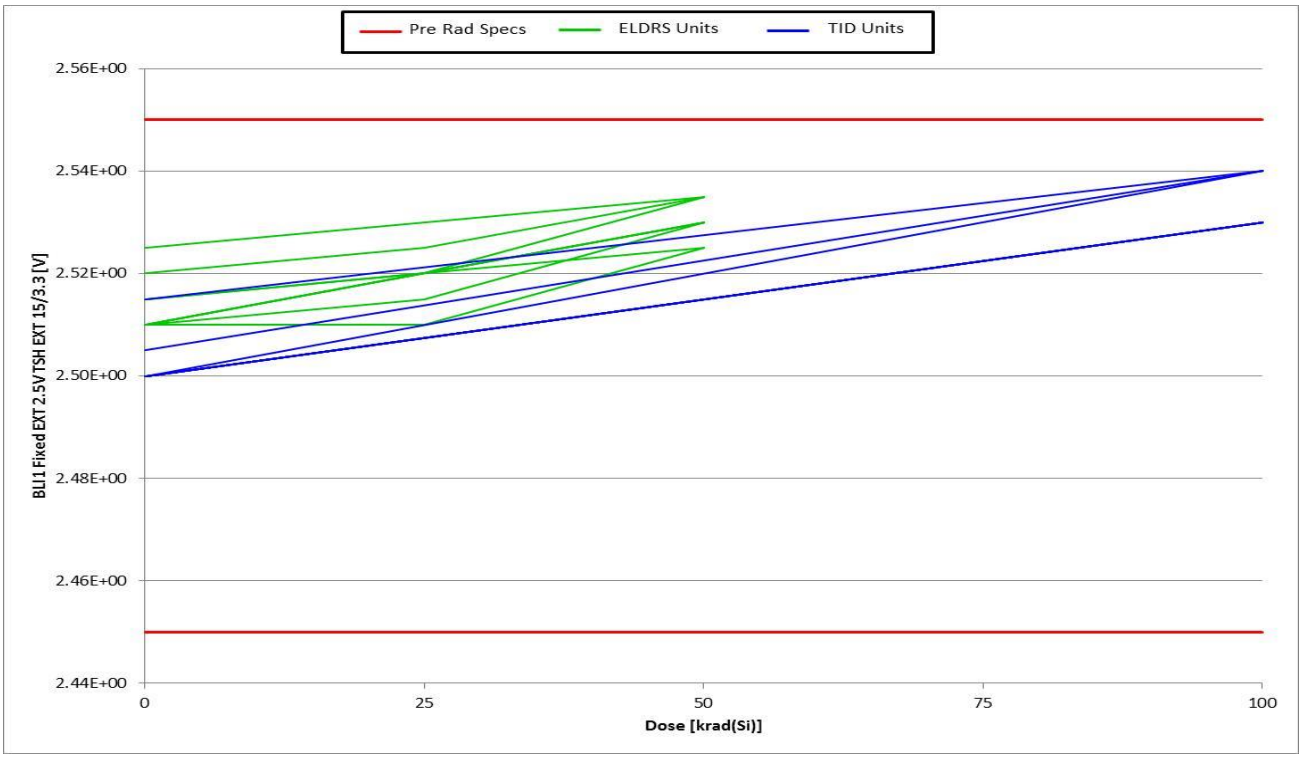
Fixed Threshold Bi-Level Inputs Threshold – Internal ref (Rising Voltage)



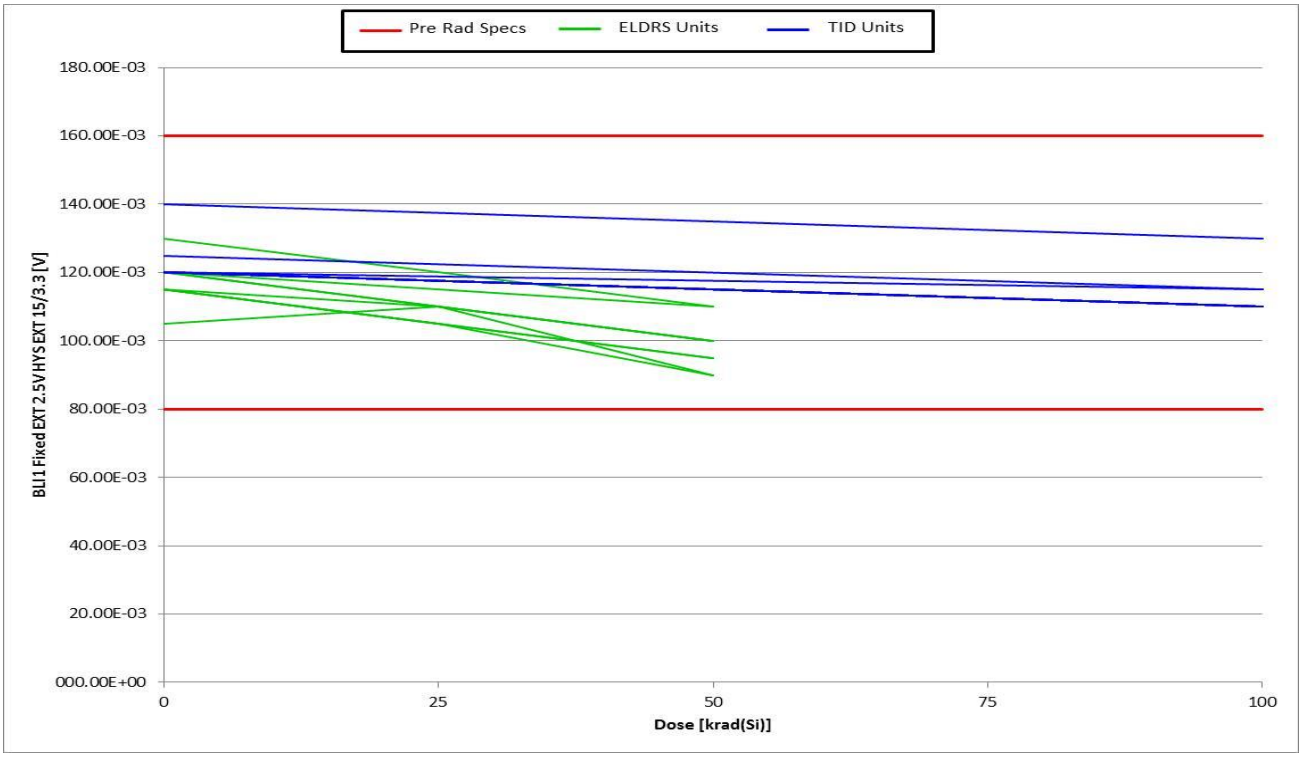
Fixed Threshold Bi-Level Inputs Hysteresis – Internal ref (Rising Voltage)



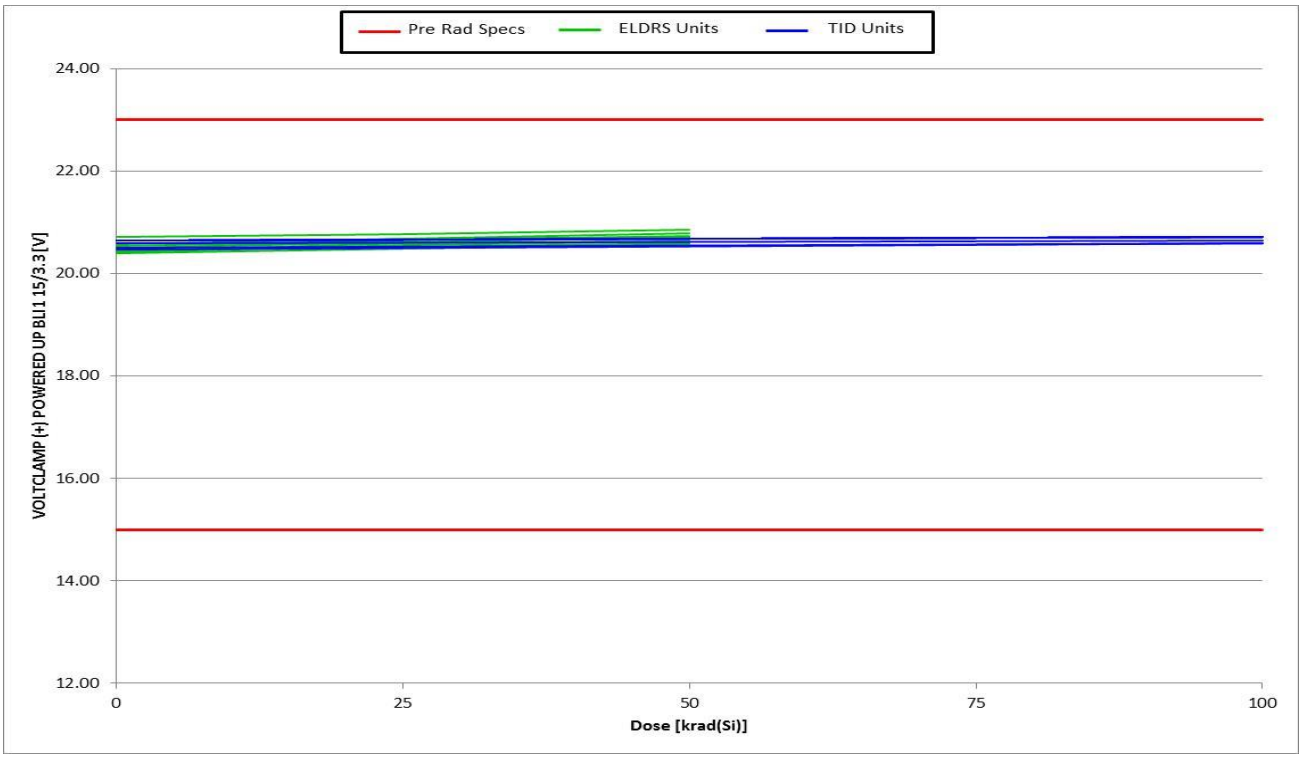
Fixed Threshold Bi-Level Inputs Threshold – External 2.5V ref (Rising Voltage)



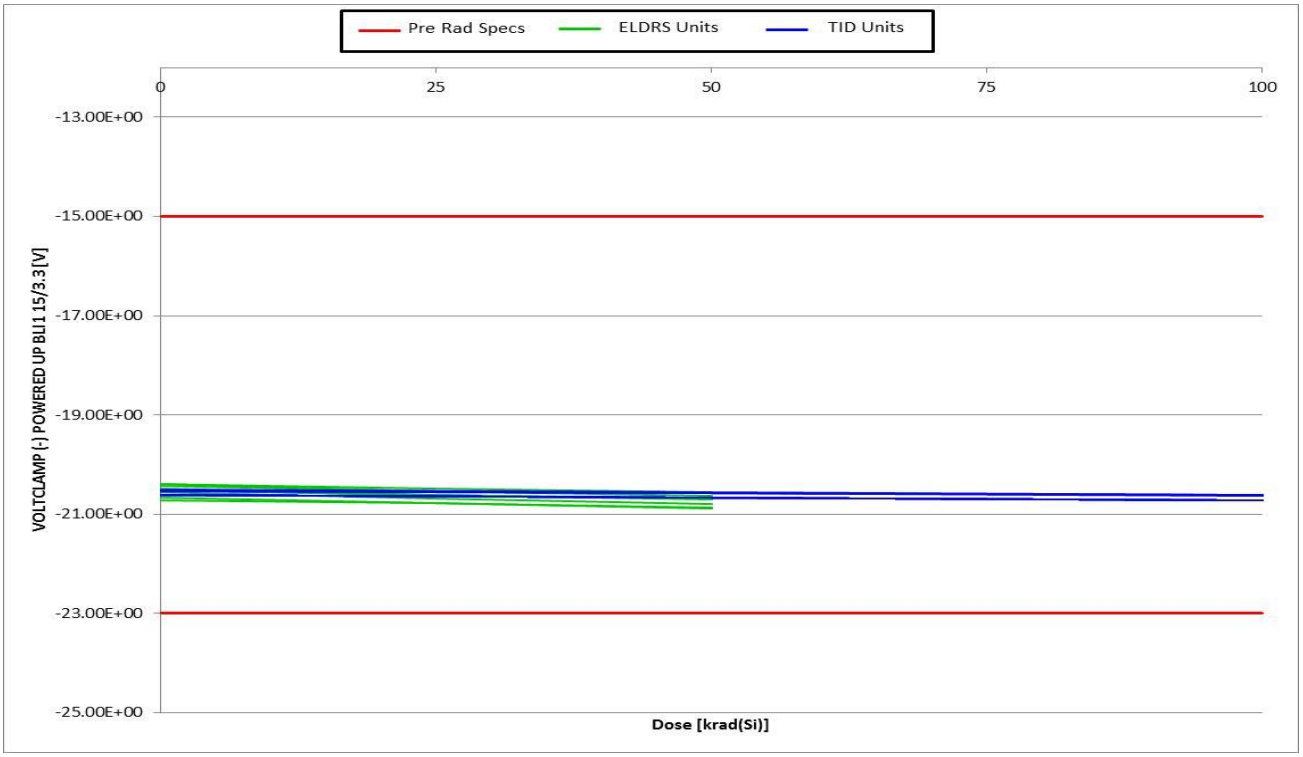
Fixed Threshold Bi-Level Inputs Hysteresis – External 2.5V ref (Rising Voltage)



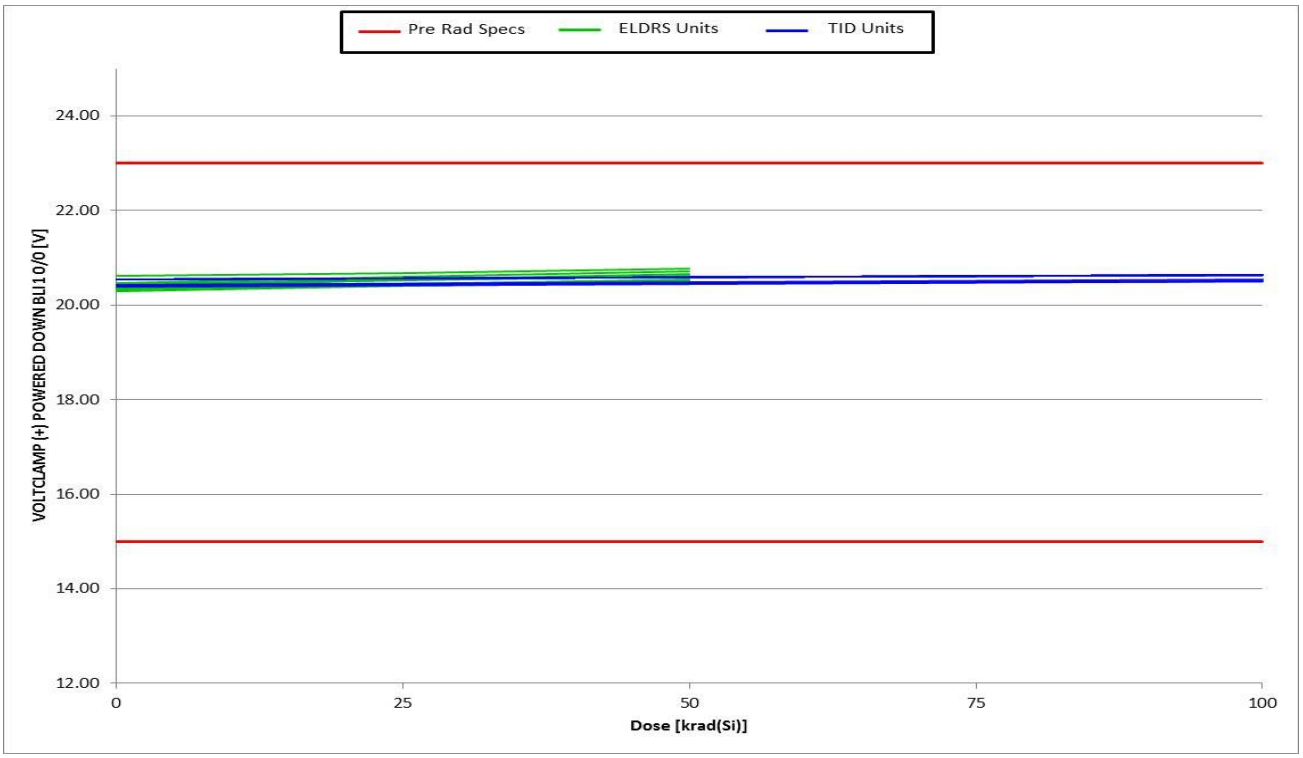
Fixed Threshold Bi-Level Inputs Voltage Clamp (power applied) – 1mA into the pin



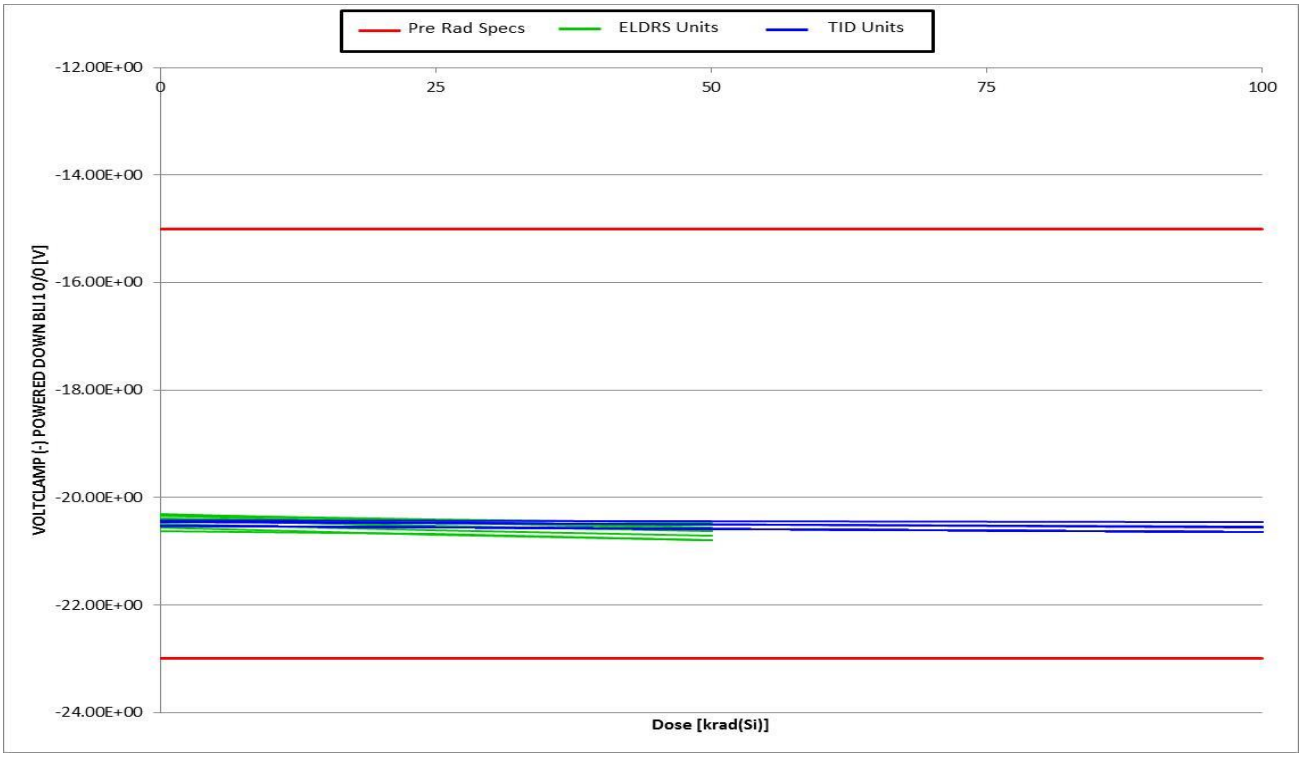
Fixed Threshold Bi-Level Inputs Voltage Clamp (power applied) – 1mA out of the pin



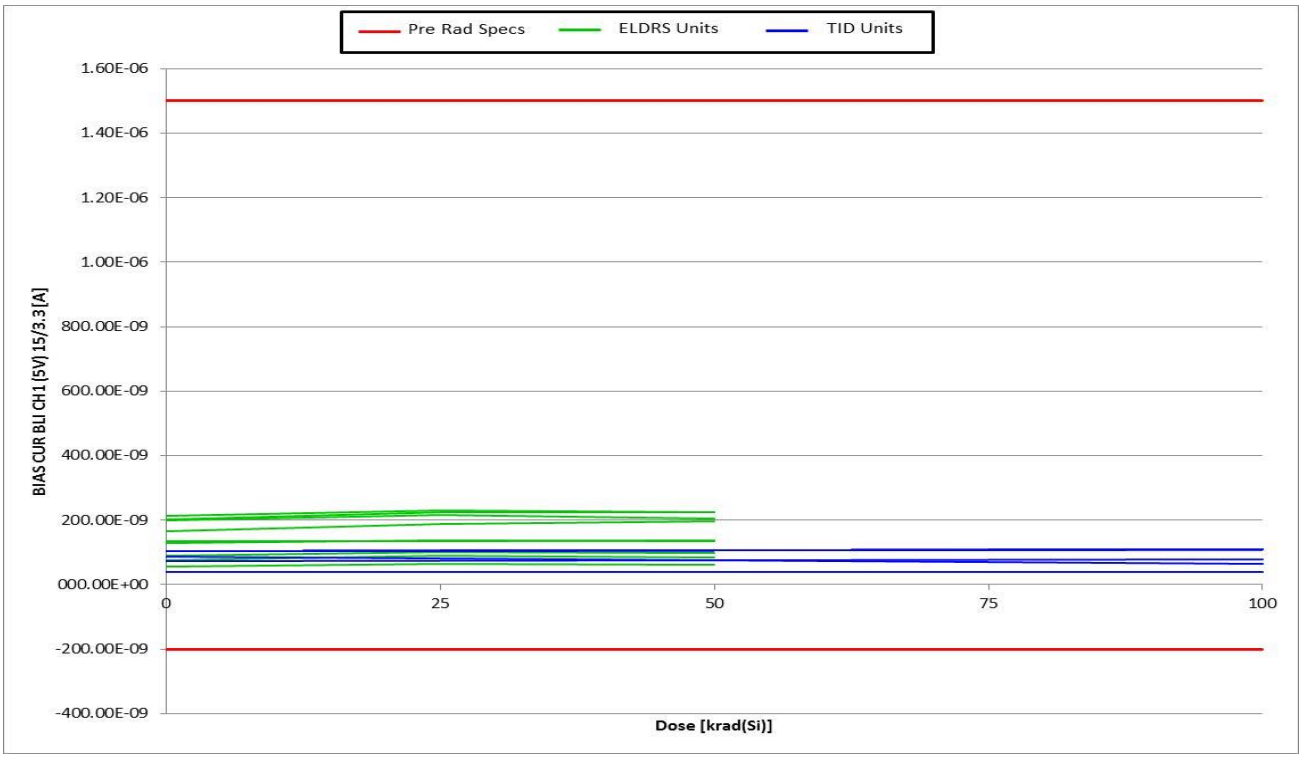
Fixed Threshold Bi-Level Inputs Voltage Clamp (power remove) – 1mA into the pin



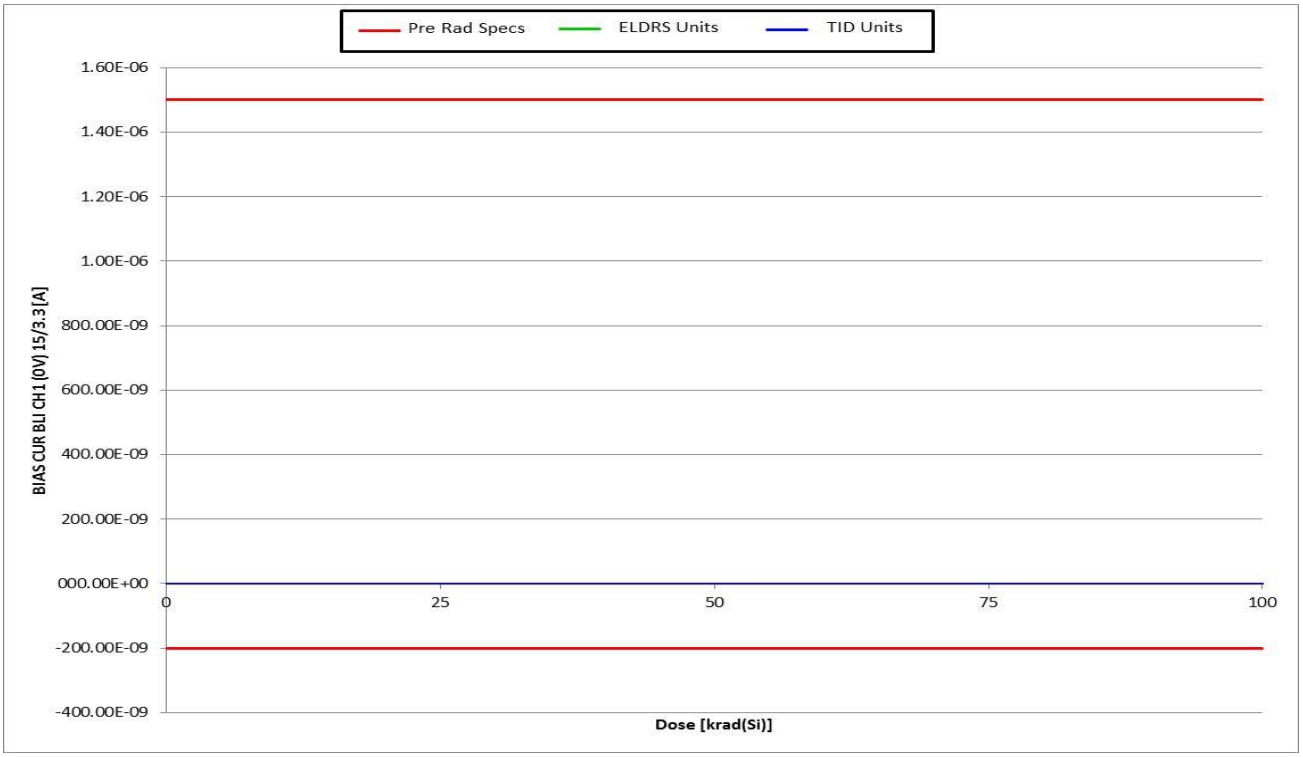
Fixed Threshold Bi-Level Inputs Voltage Clamp (power remove) – 1mA out of the pin



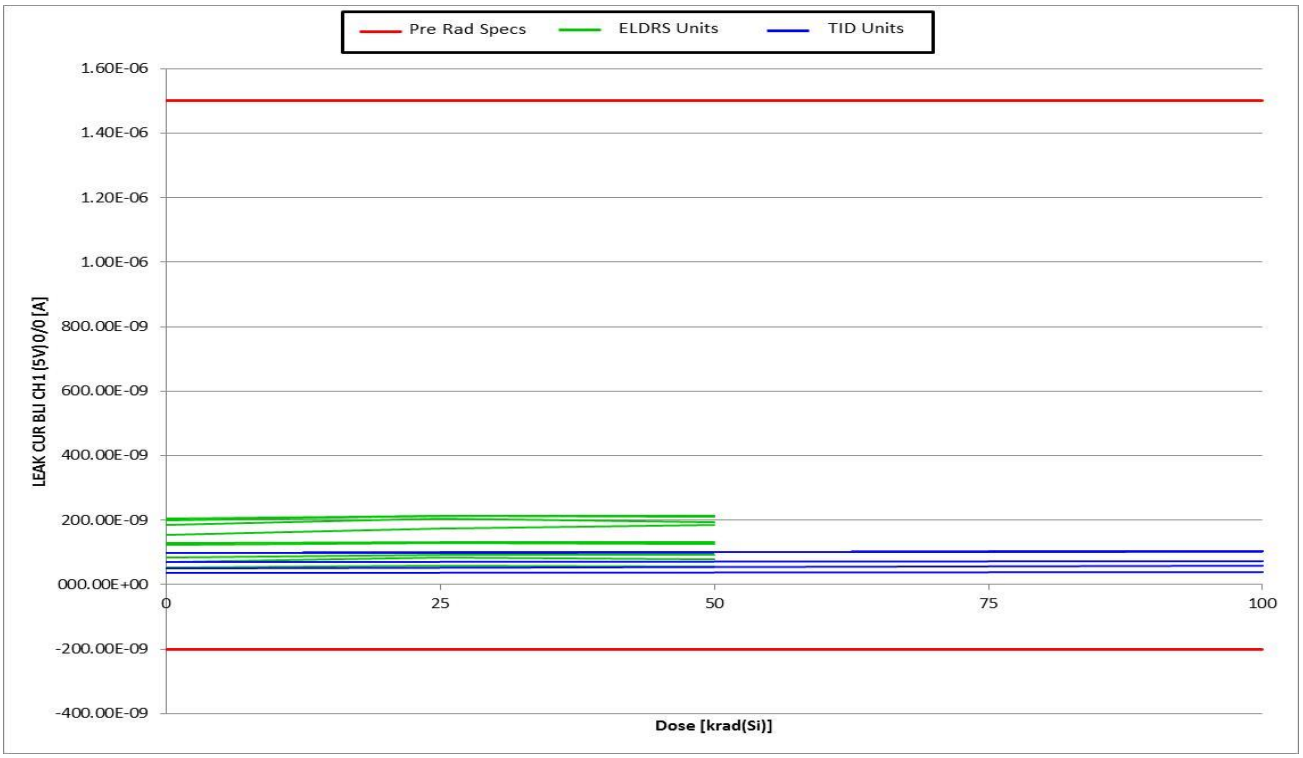
Fixed Threshold Bi-Level Inputs Bias Current at 5V



Fixed Threshold Bi-Level Inputs Bias Current at 0V

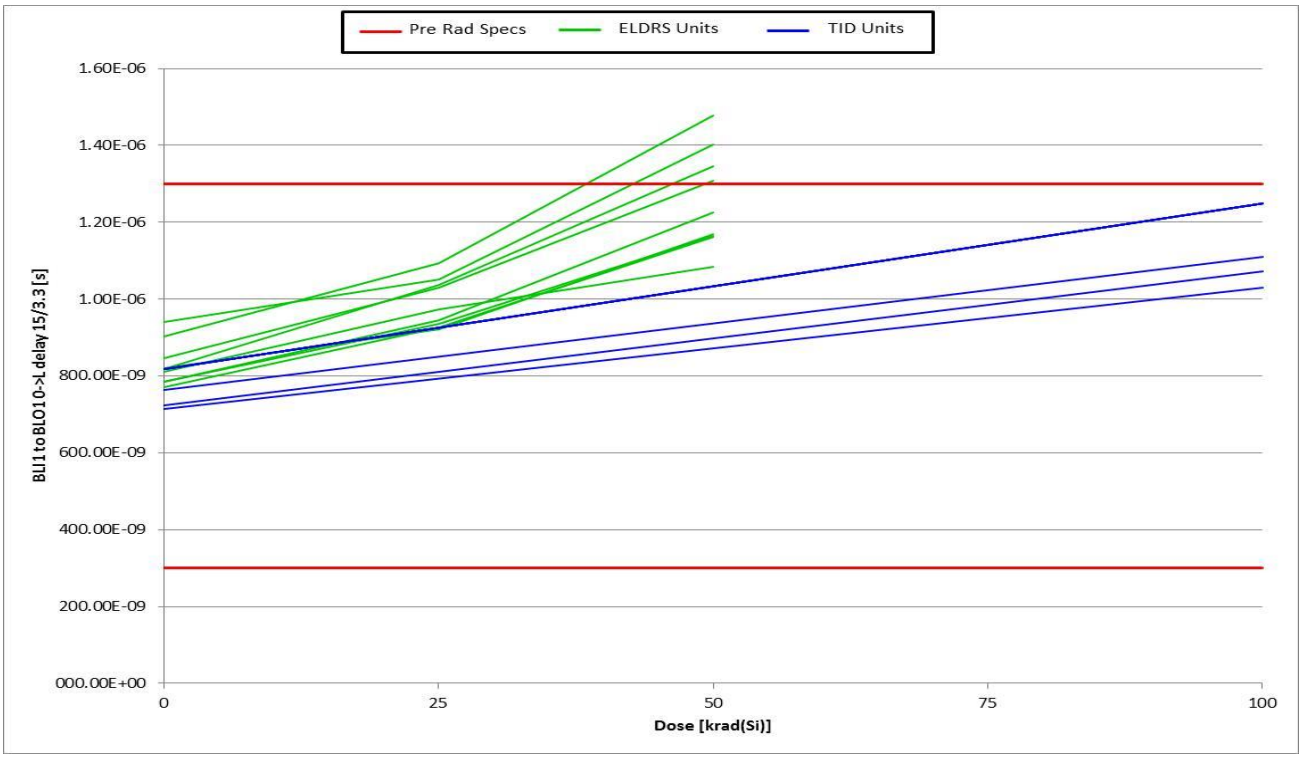


Fixed Threshold Bi-Level Inputs Leakage Current at 5V

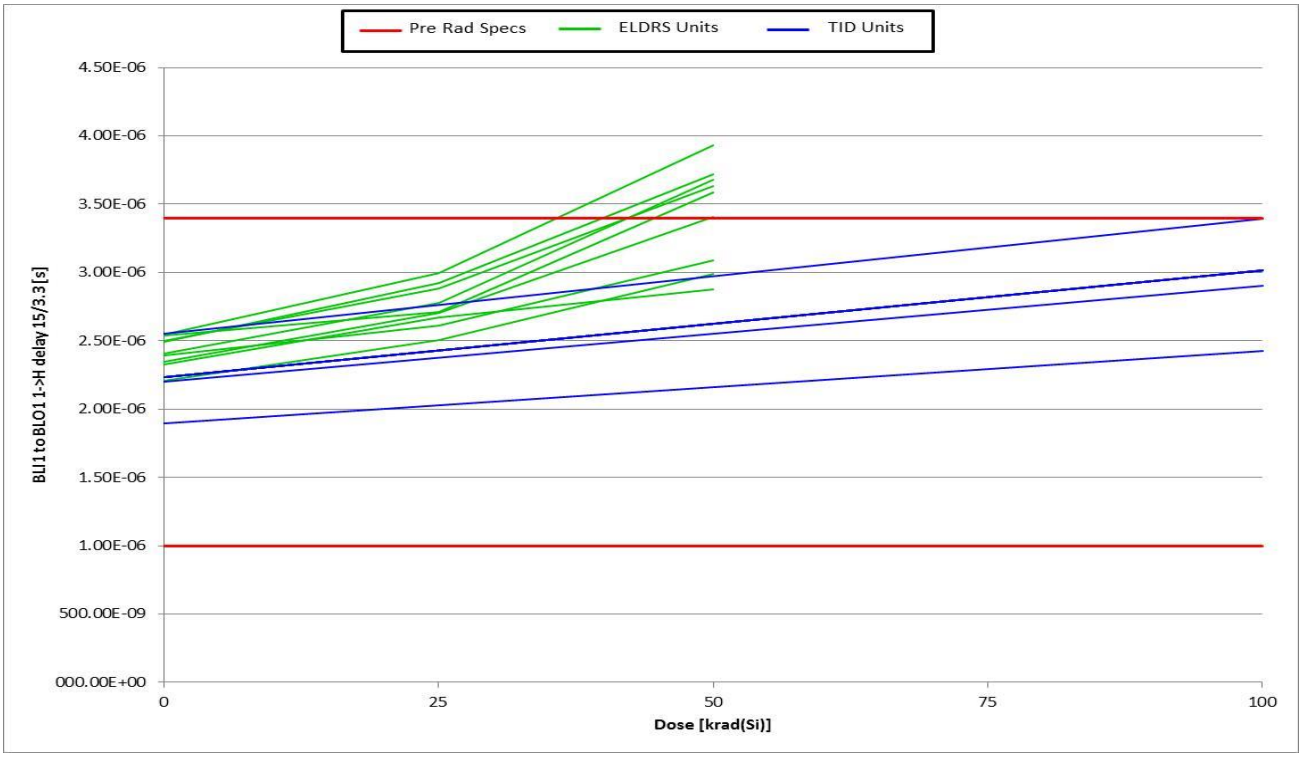


Fixed Threshold Bi-Level Inputs Leakage Current at 0V

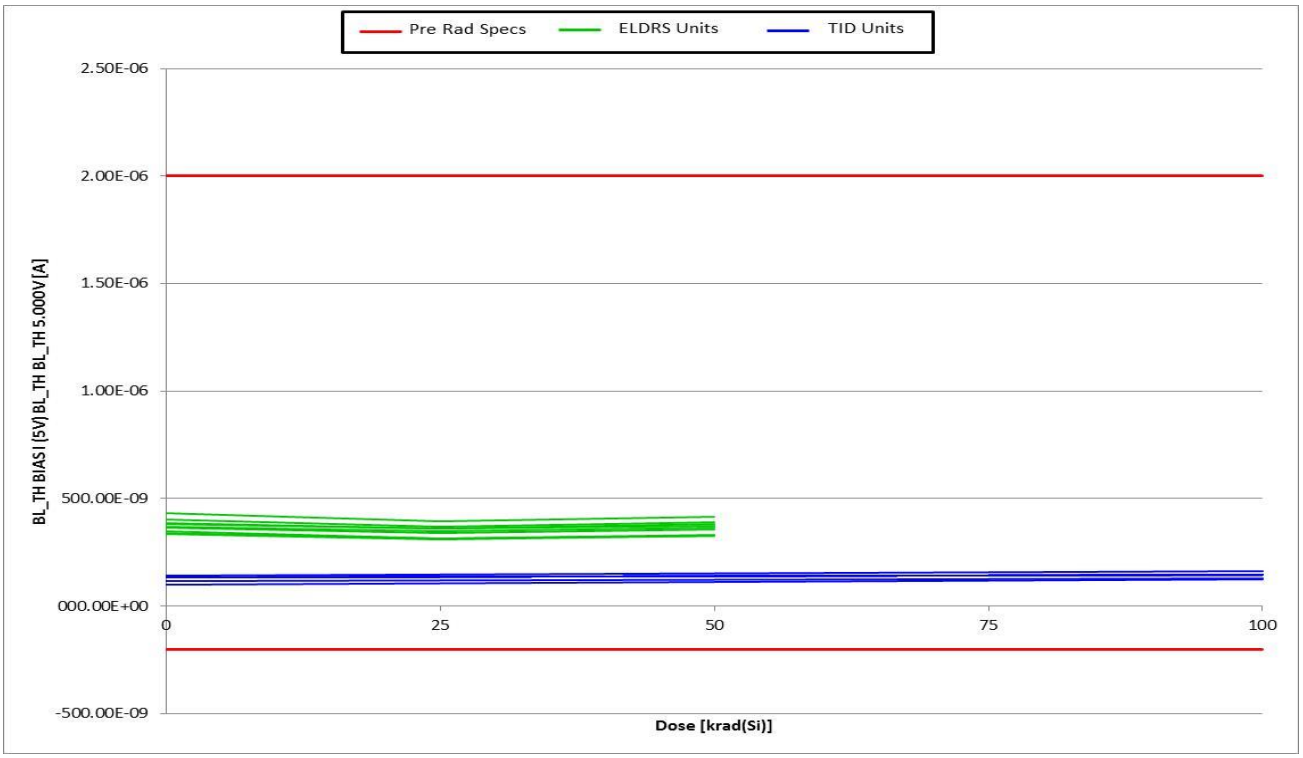
Fixed Threshold Bi-Level Propagation Delay - High to Low transition



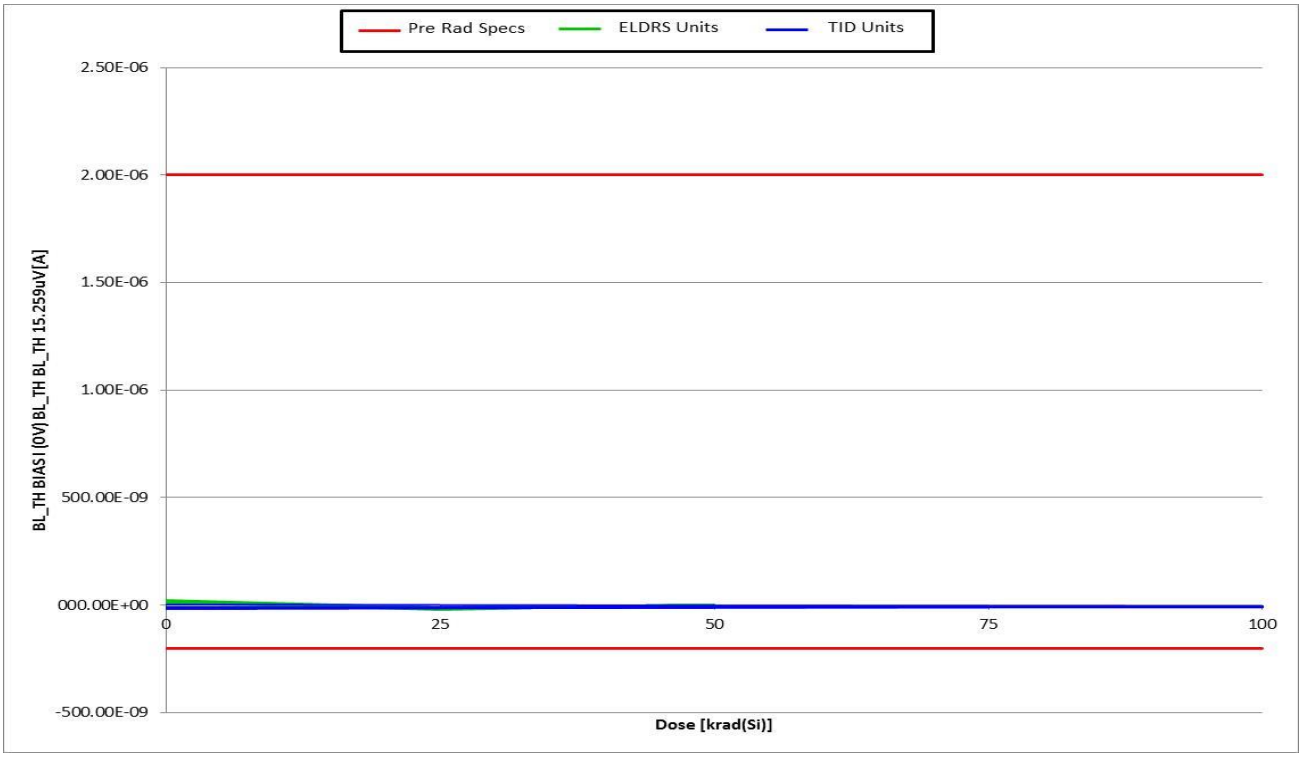
Fixed Threshold Bi-Level Propagation Delay - Low to High transition



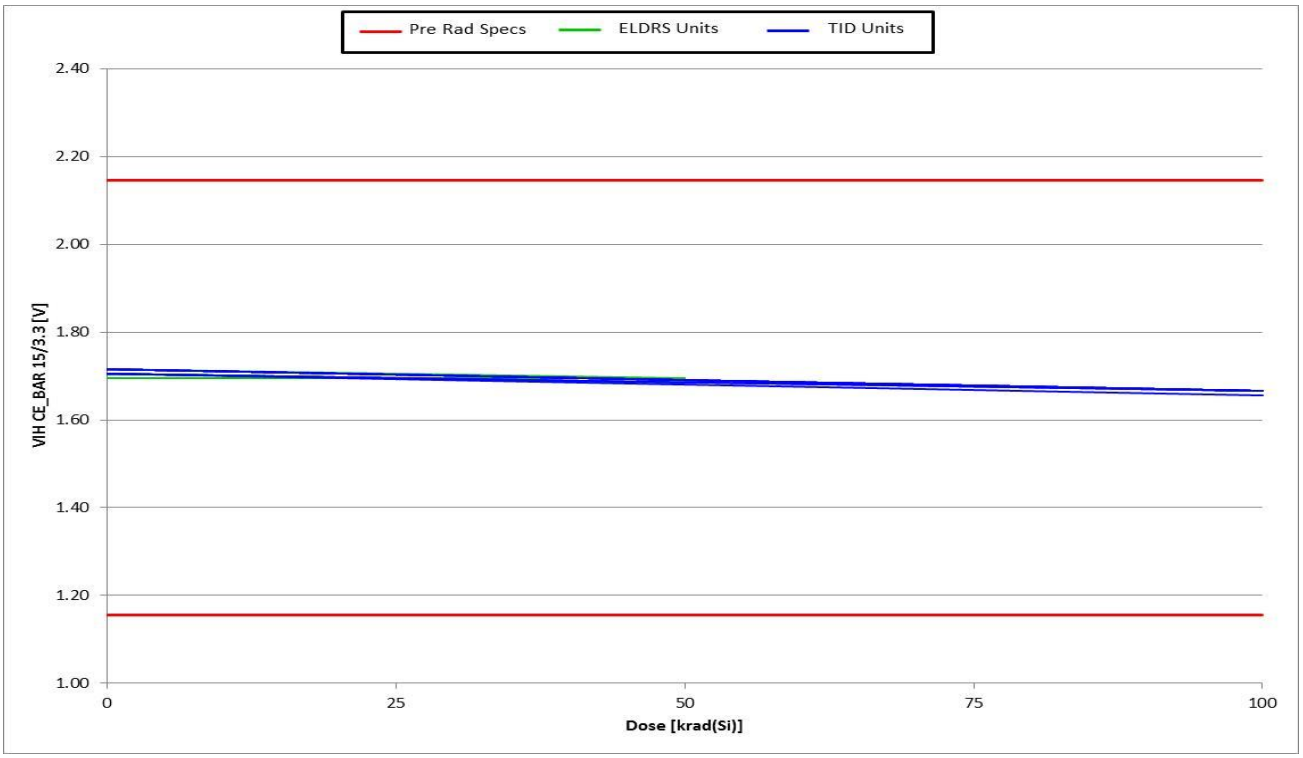
Fixed Threshold Bi-Level Threshold Pin Leakage at 5V

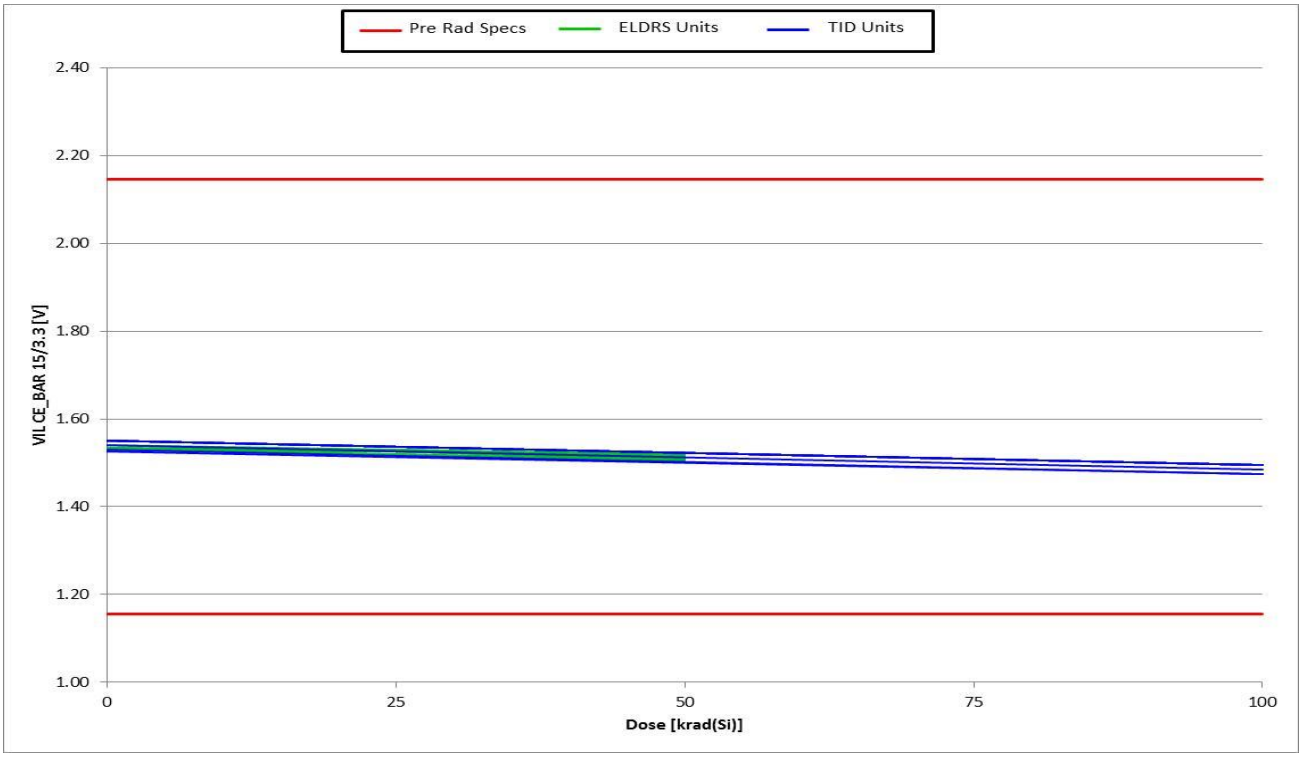


Fixed Threshold Bi-Level Threshold Pin Leakage at 0V

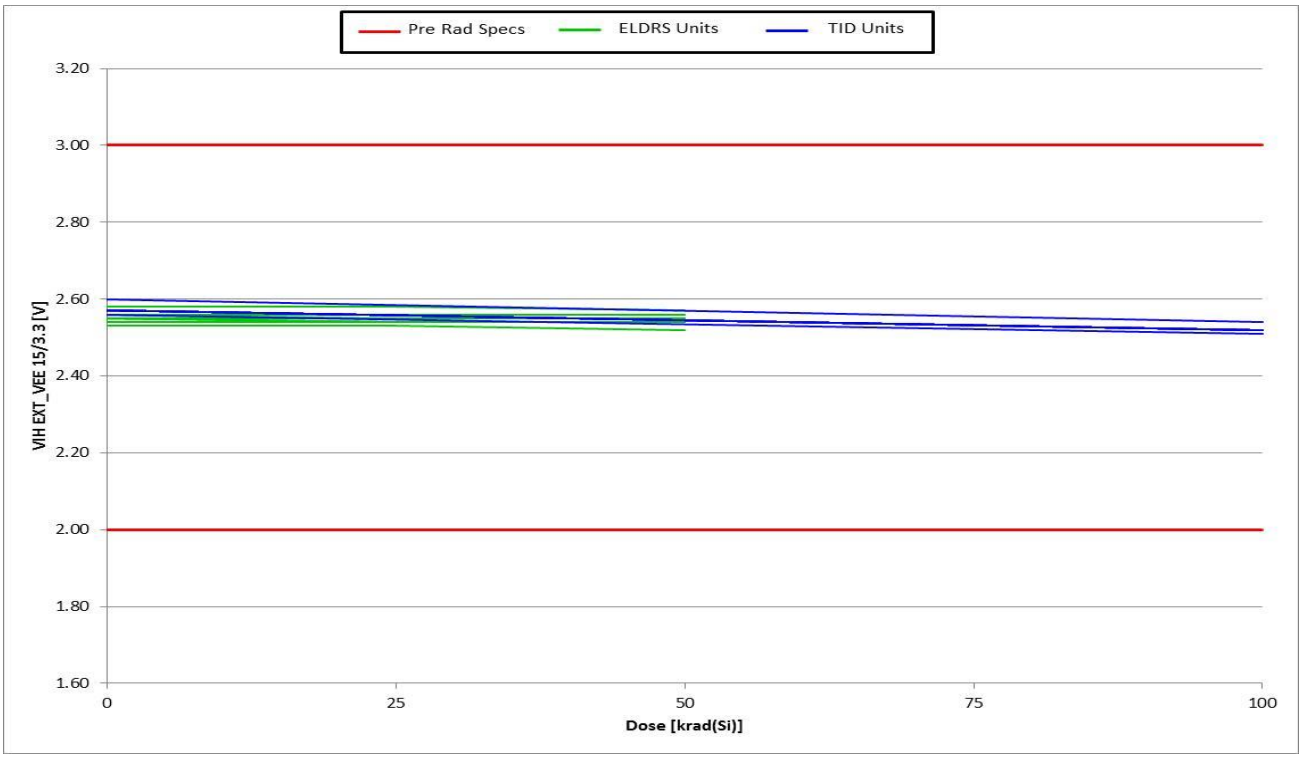


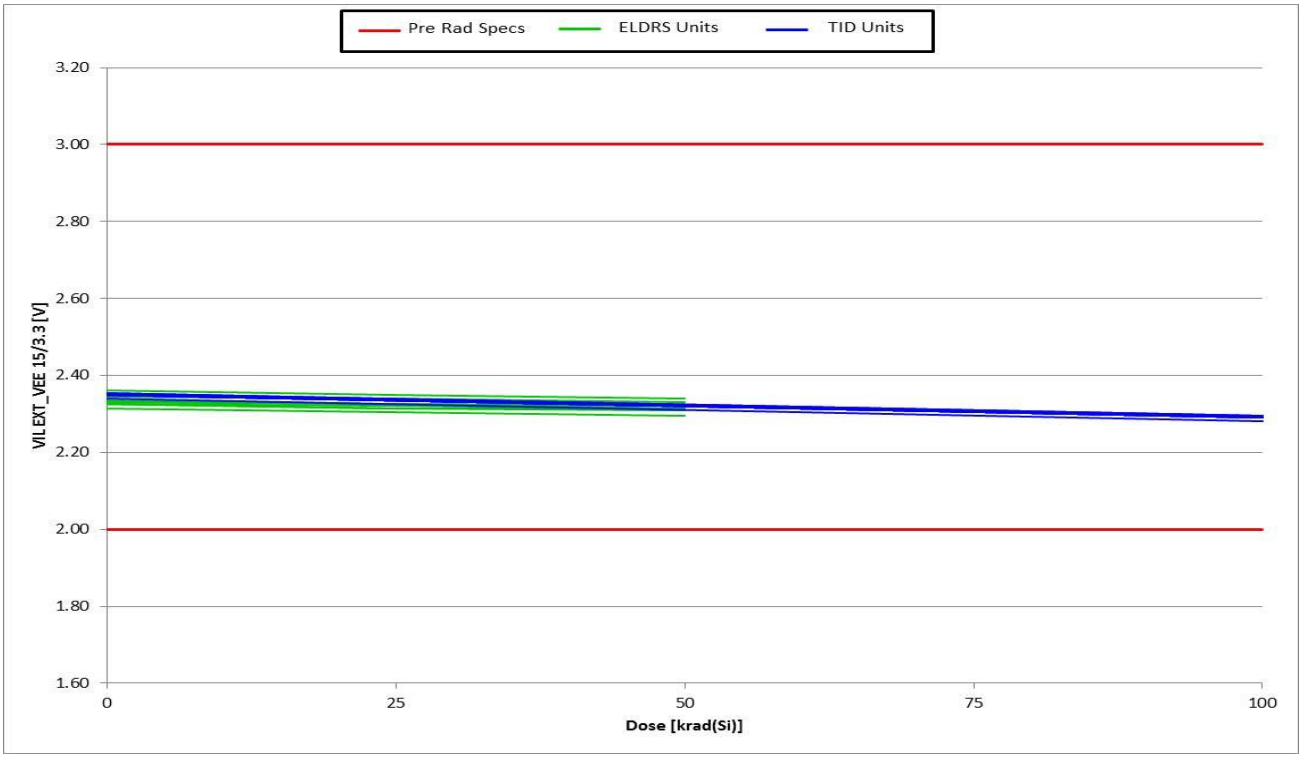
Logic Levels for FPGA Interface I/Os - Input Logic Threshold at 3.3V



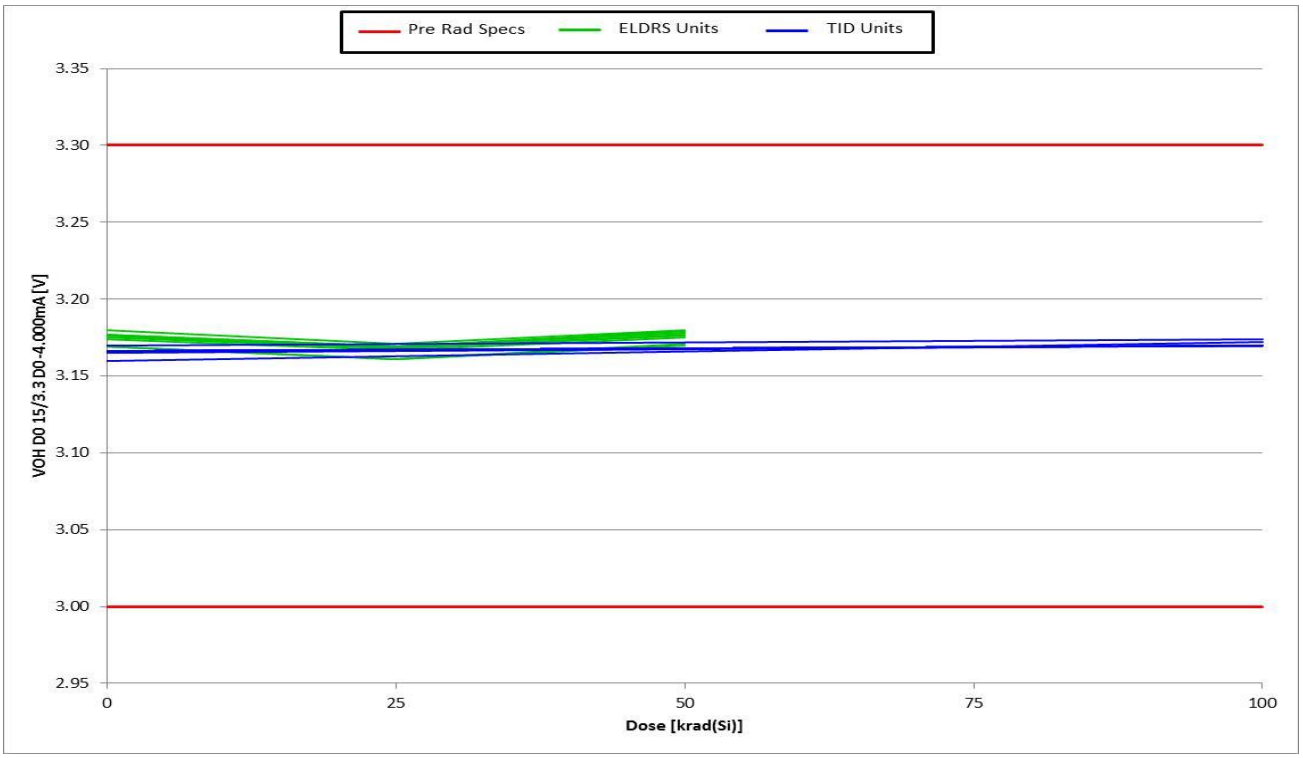


Logic Levels for FPGA Interface I/Os - Program pins Threshold

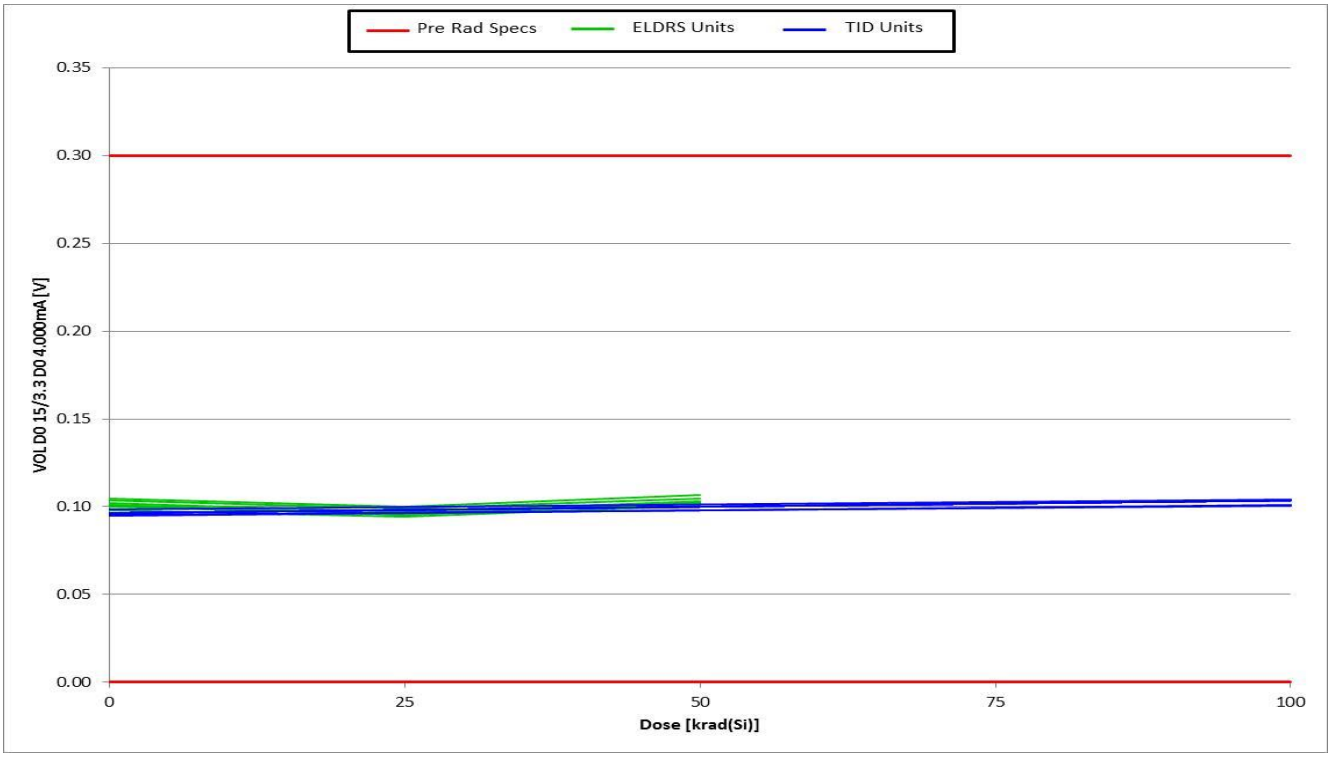




Logic Levels for FPGA Interface I/Os - Logic Output VOH at 100uA at 3.3V

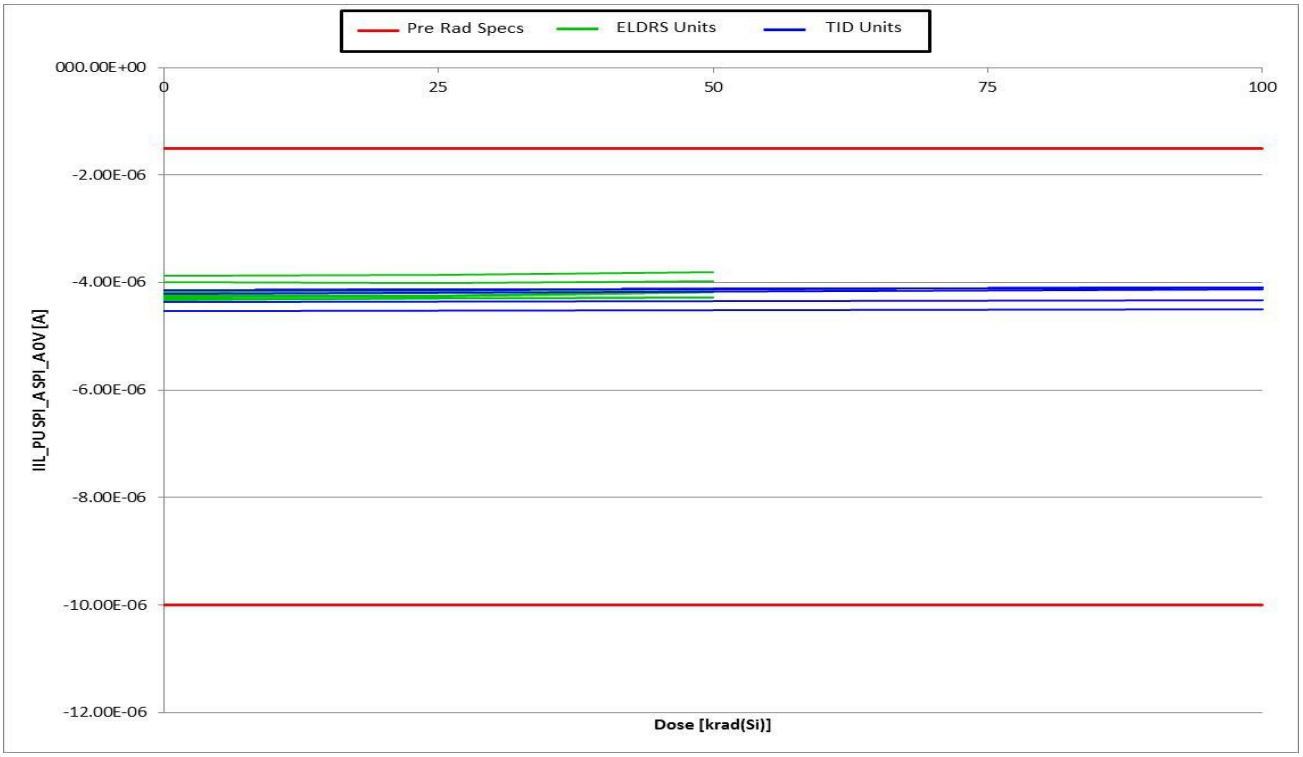


Logic Levels for FPGA Interface I/Os - Logic Output VOl at 100uA at 3.3V

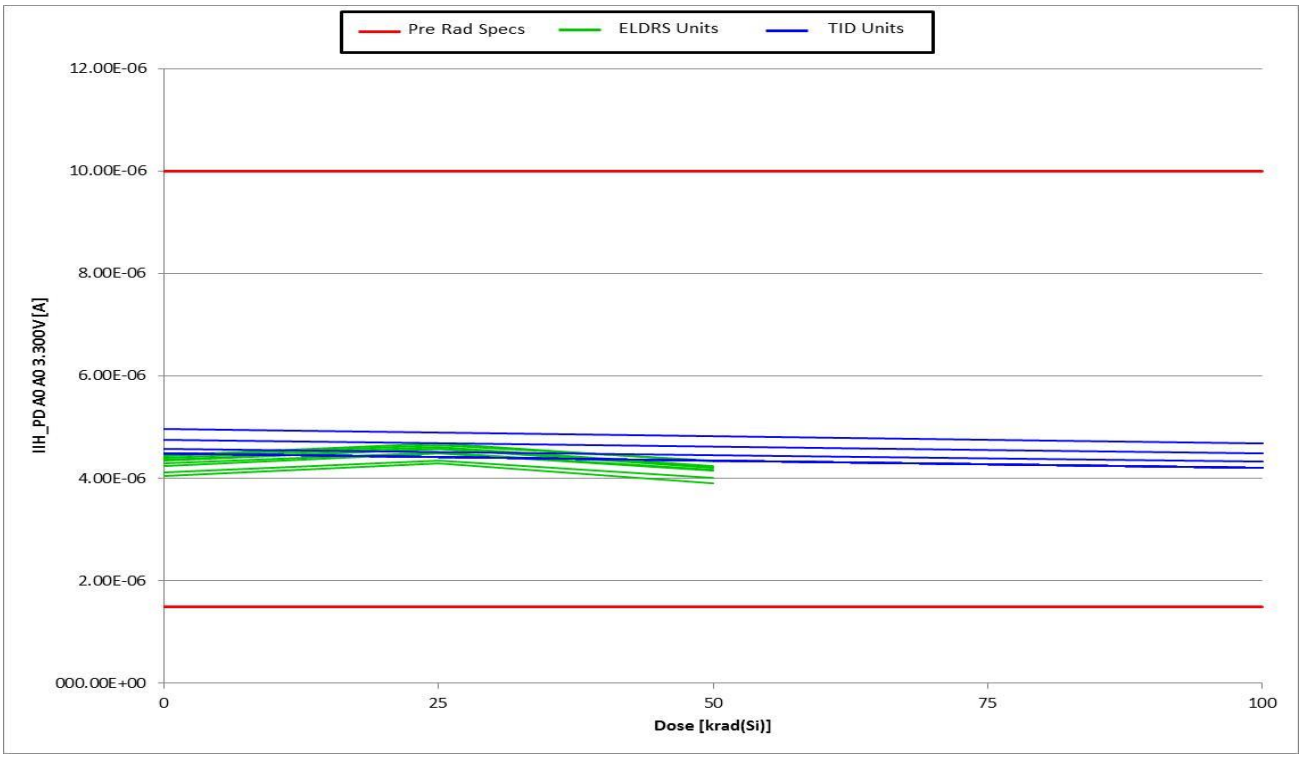


Logic Levels for FPGA Interface I/Os - IIH SPI_A, SPI_B (3.3V)

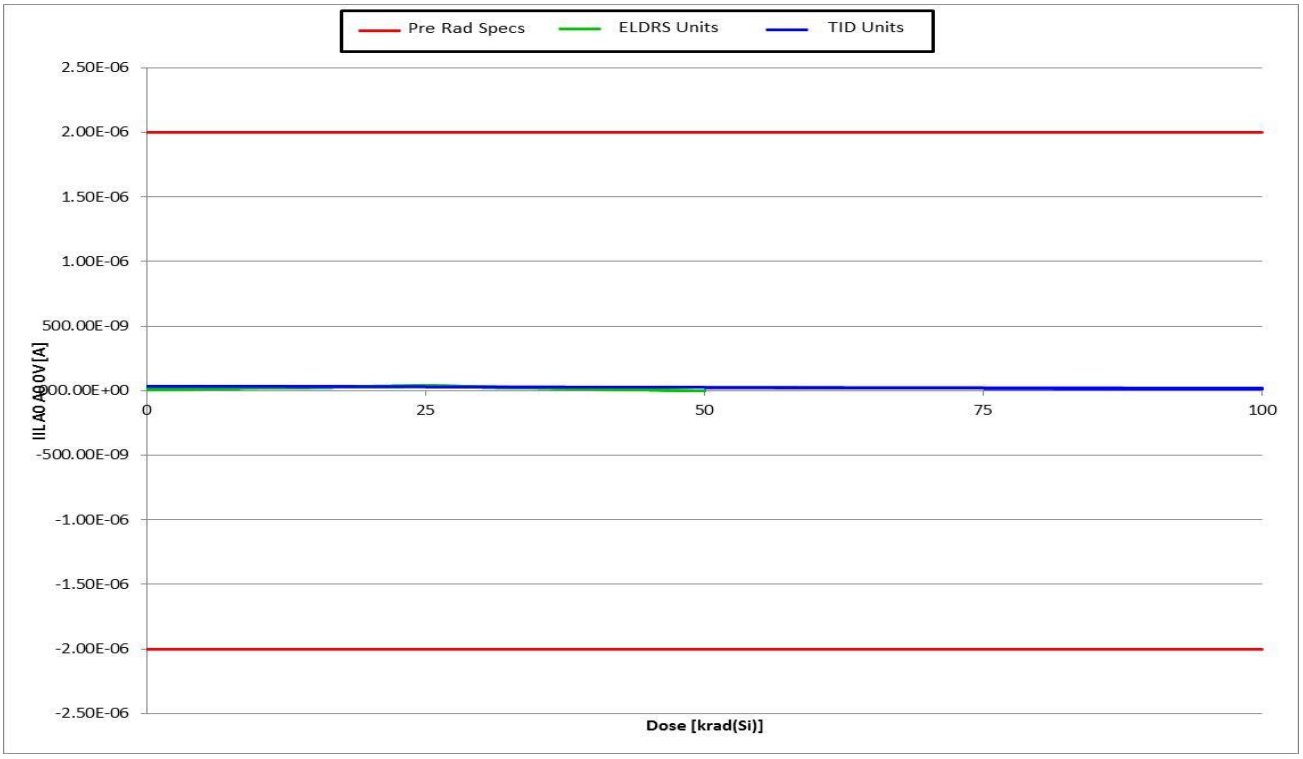
Logic Levels for FPGA Interface I/Os - IIL SPI_A, SPI_B (0V)



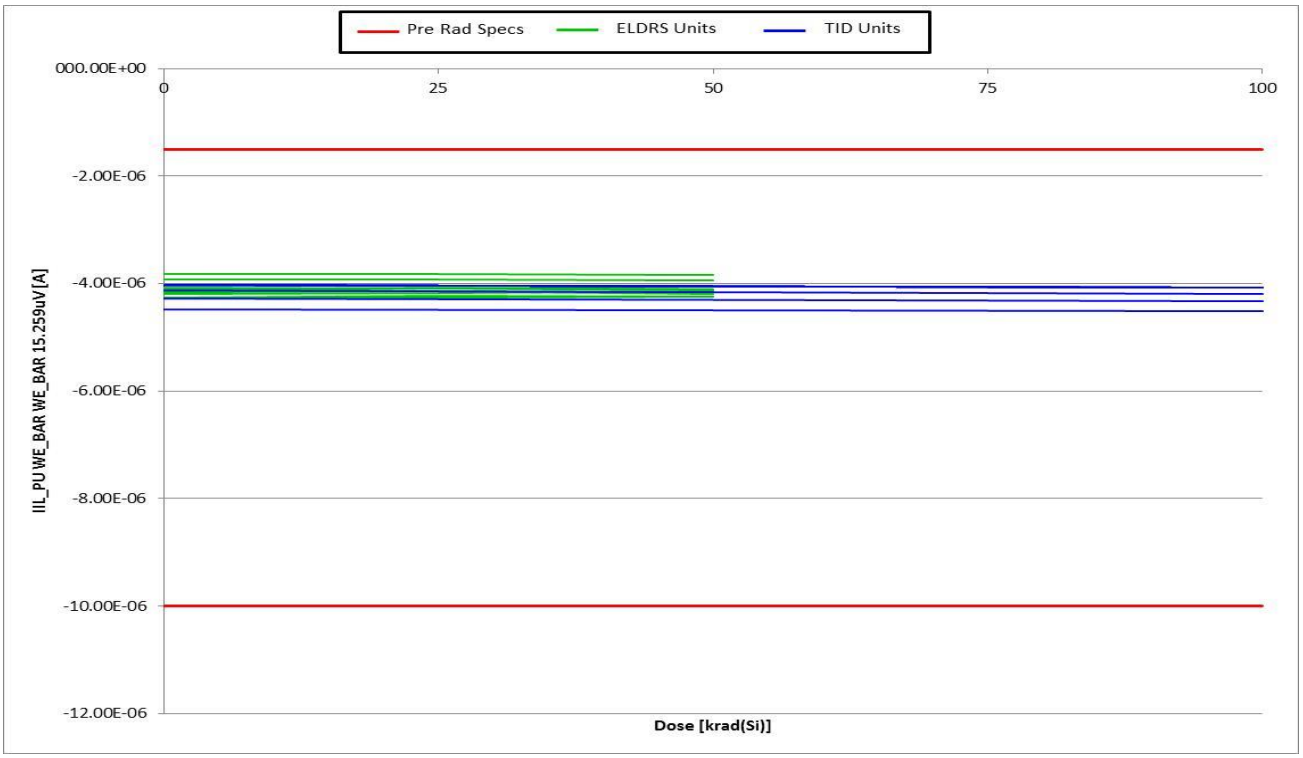
Logic Levels for FPGA Interface I/Os - IIH Pins 2,6,8-10,14-21, 22: I/O as input (3.3V)



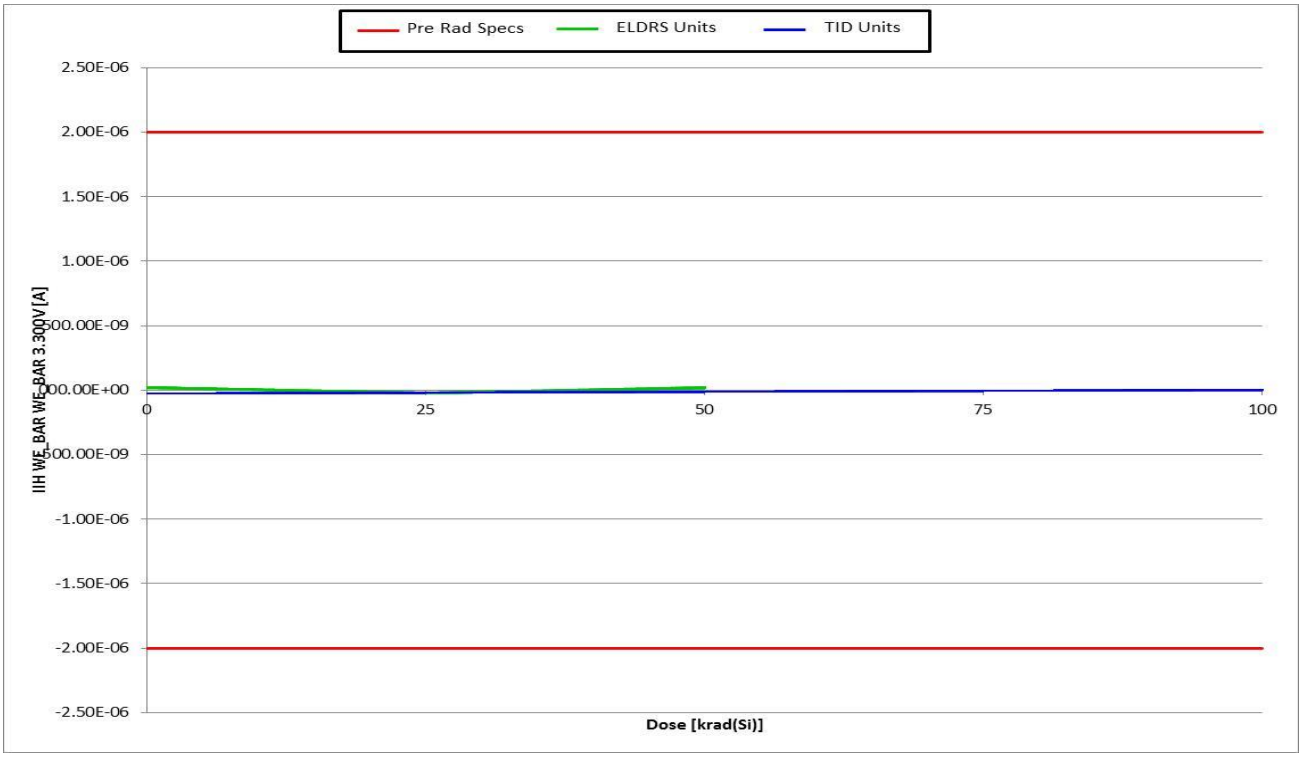
Logic Levels for FPGA Interface I/Os - IIL Pins 2,6,8-10,14-21, 22: I/O as input (0V)



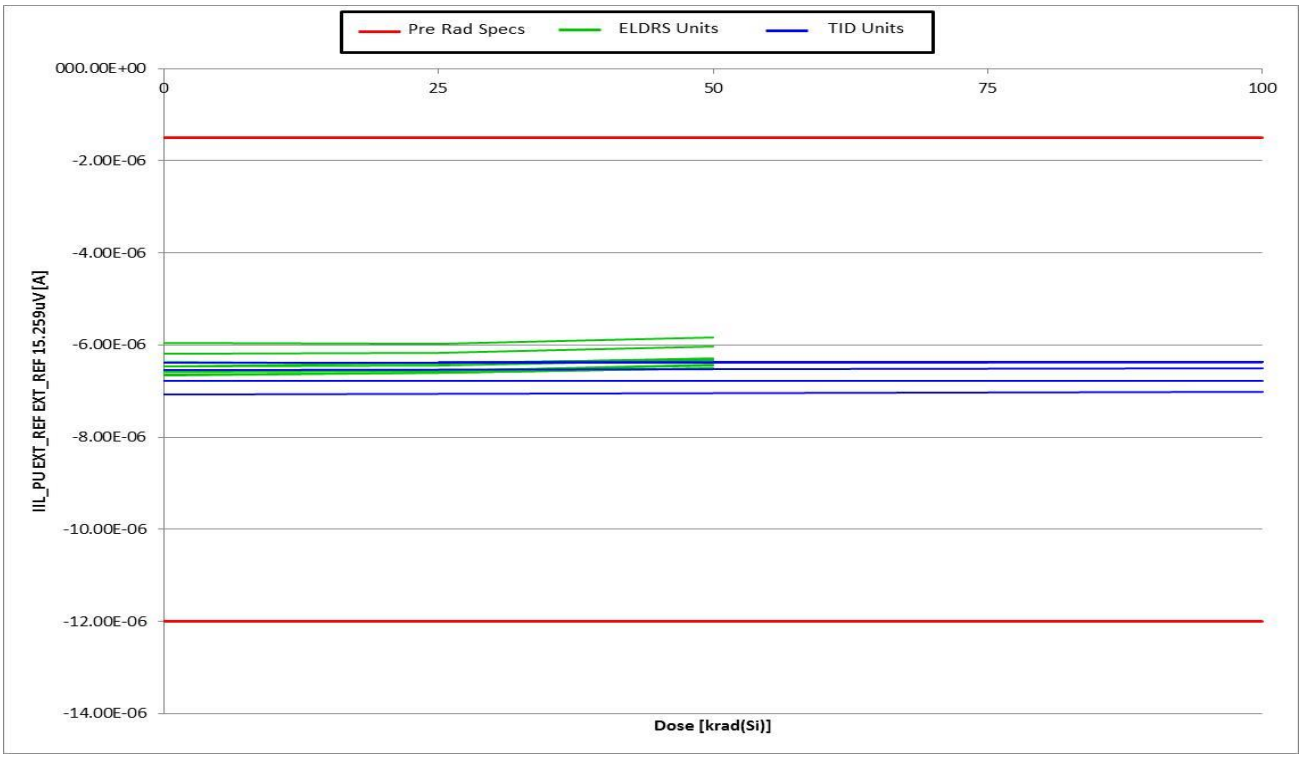
Logic Levels for FPGA Interface I/Os - IIL Pins 3-5, 7: I/O as input (0V)



Logic Levels for FPGA Interface I/Os - IIH Pins 3-5, 7: I/O as input (3.3V)

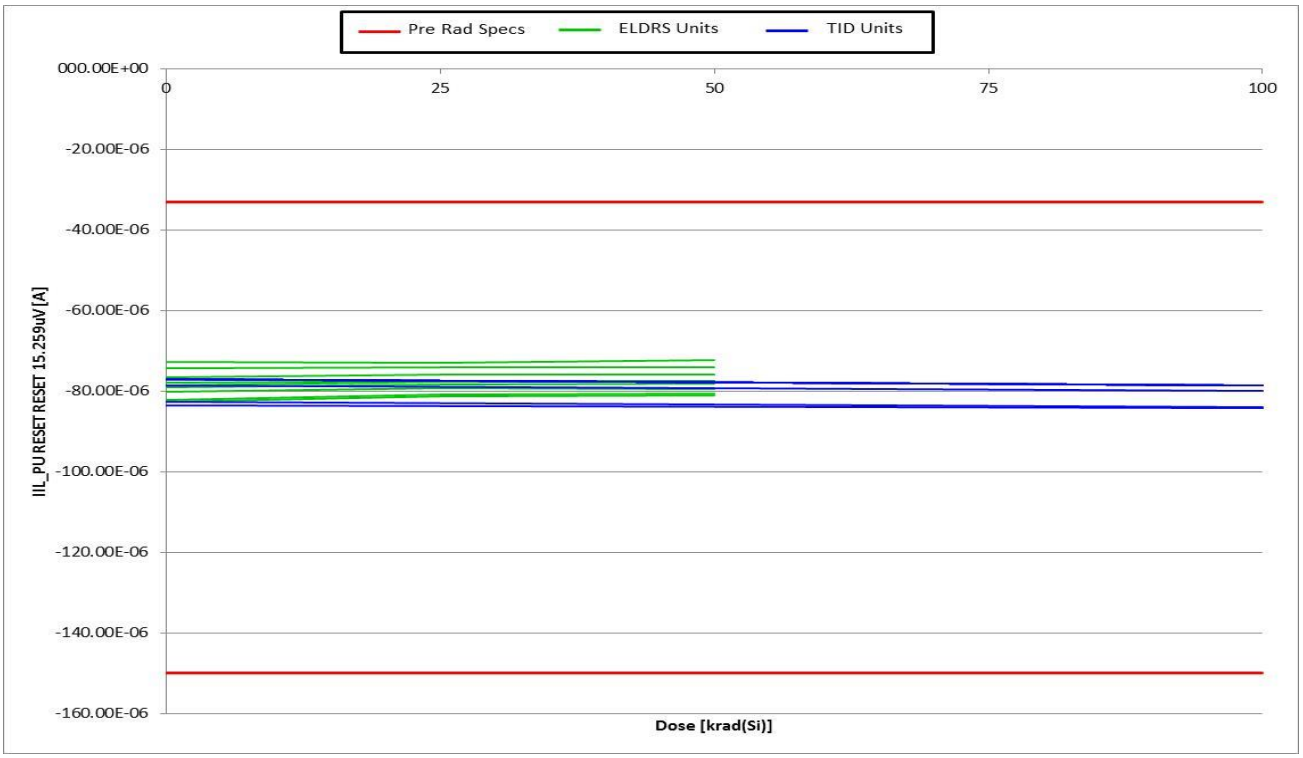


Logic Levels for FPGA Interface I/Os - IIL /EXT_VREF or /EXT_VEE = 0V

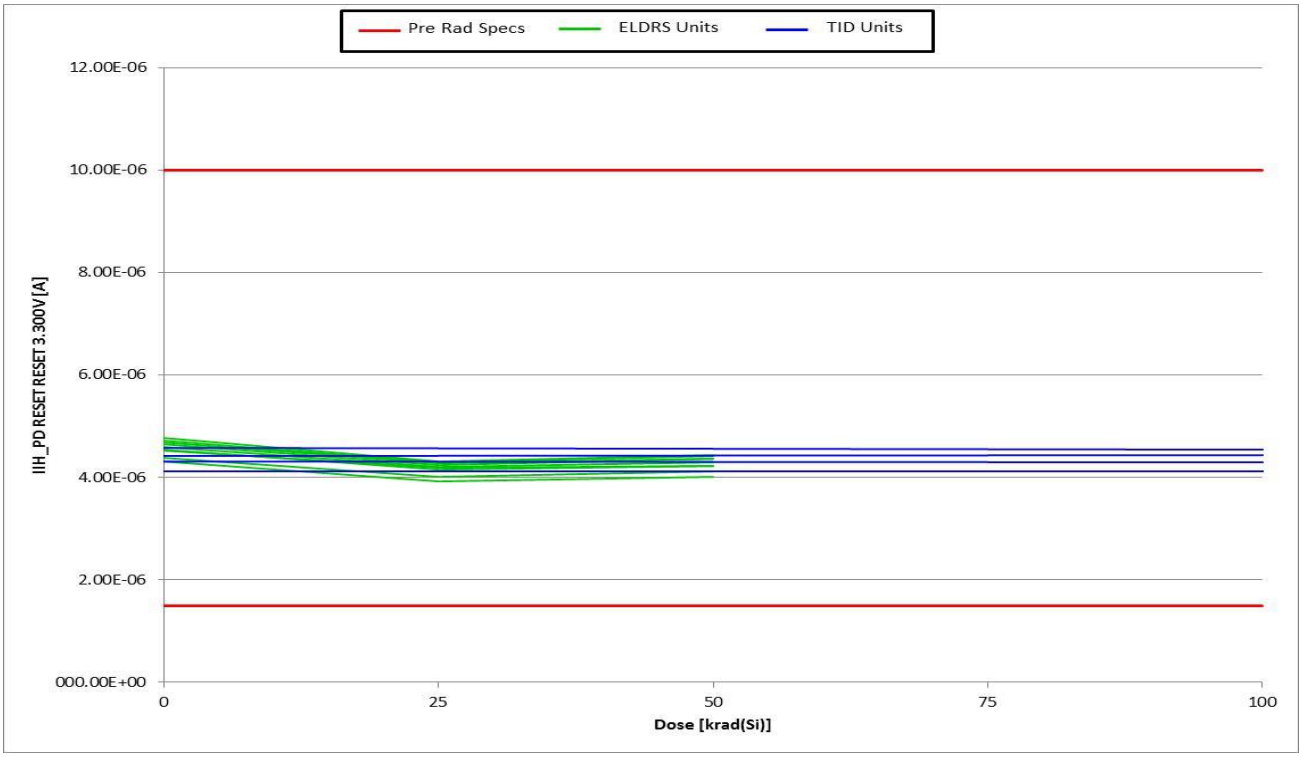


Logic Levels for FPGA Interface I/Os - IIH /EXT_VREF or /EXT_VEE = 5V

Logic Levels for FPGA Interface I/Os - IIH /RESET (5V)

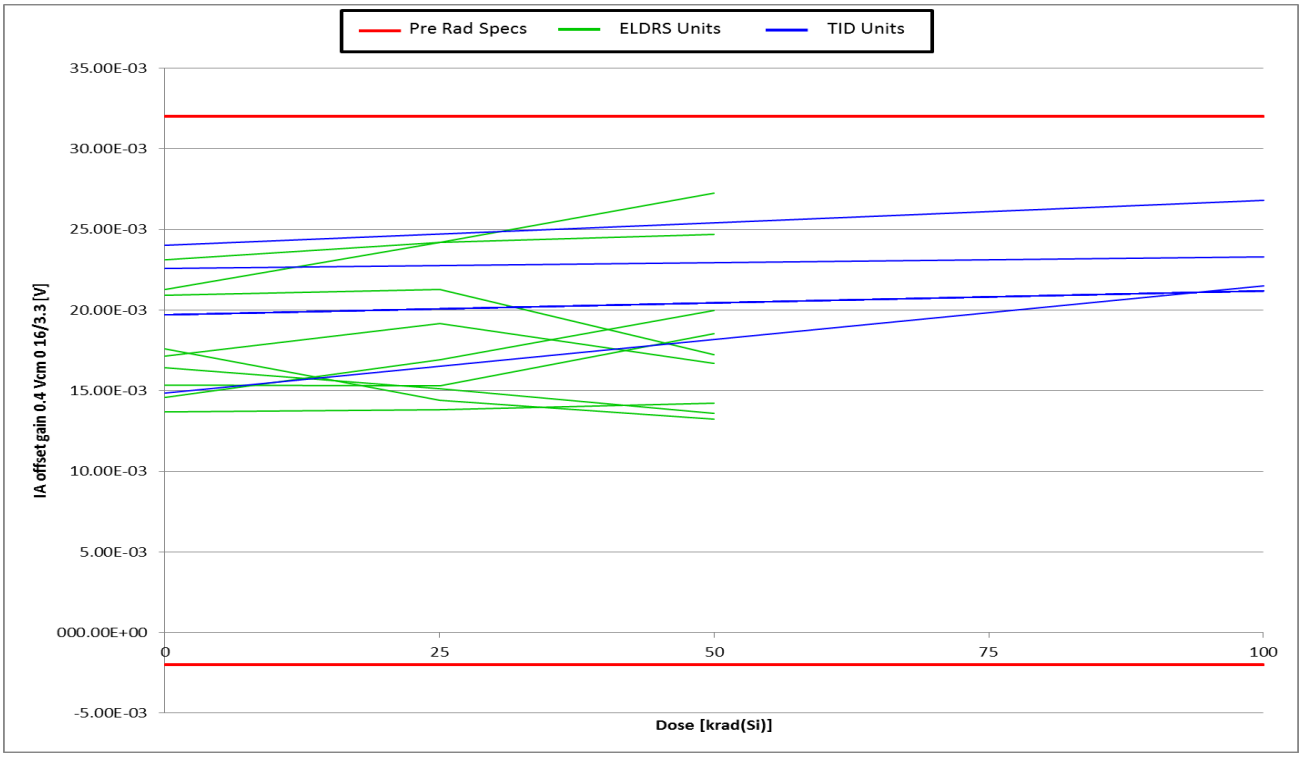


Logic Levels for FPGA Interface I/Os - IIL /RESET (0V)

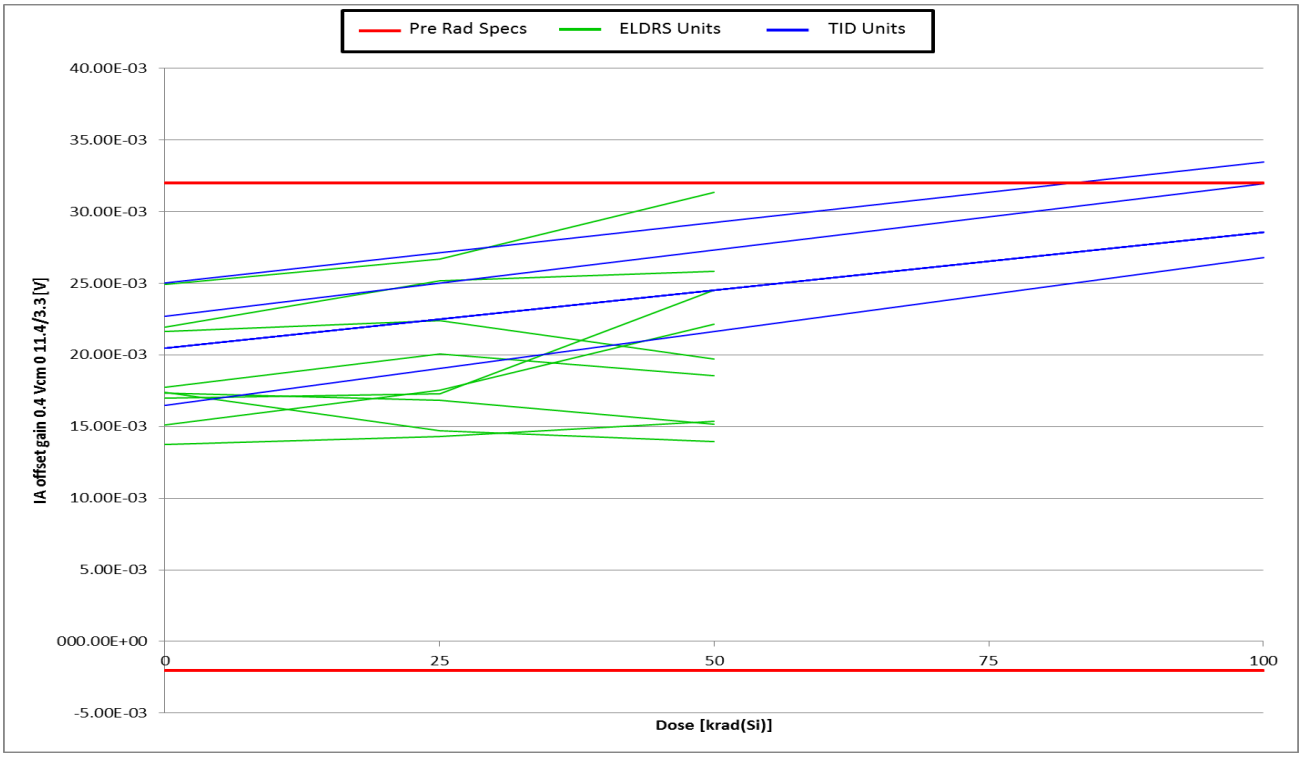


Detailed Data Charts of specified parameters

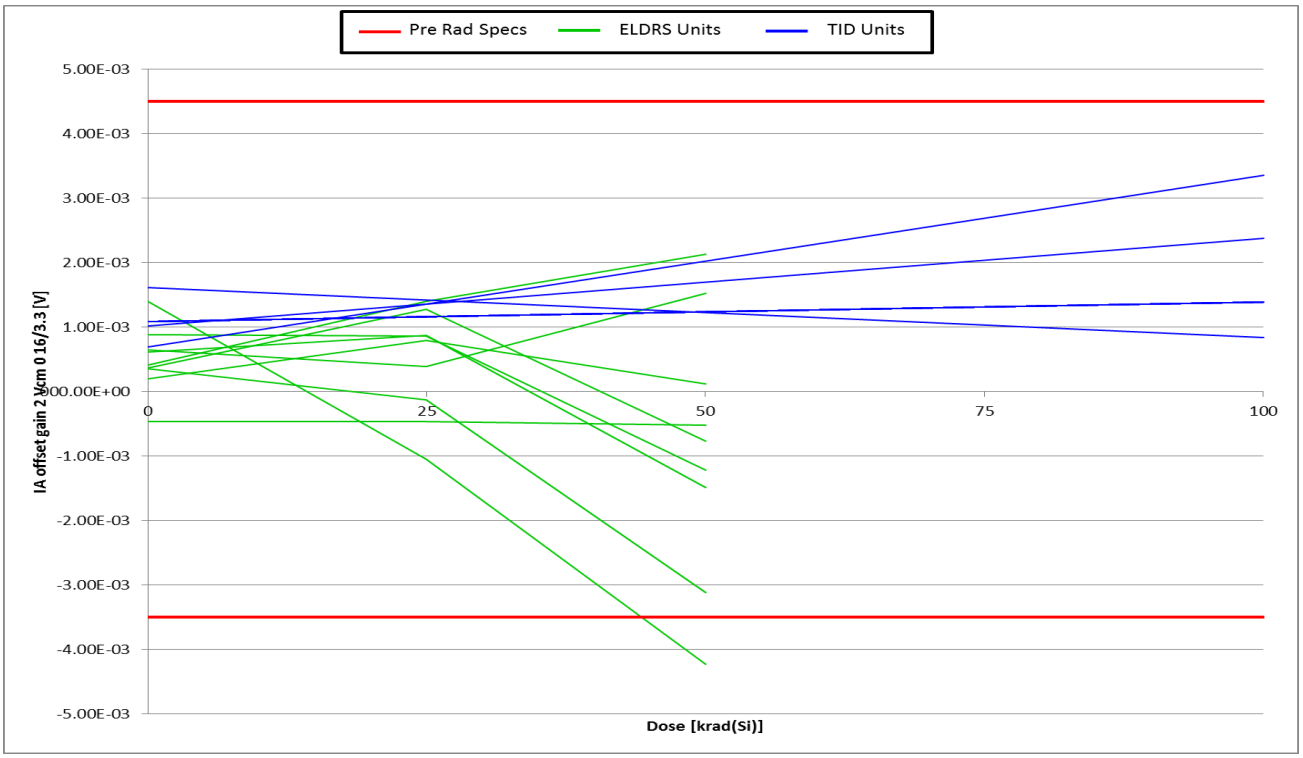
Instrumentation Amplifier Offset at Gain = 0.4, VCC=16V



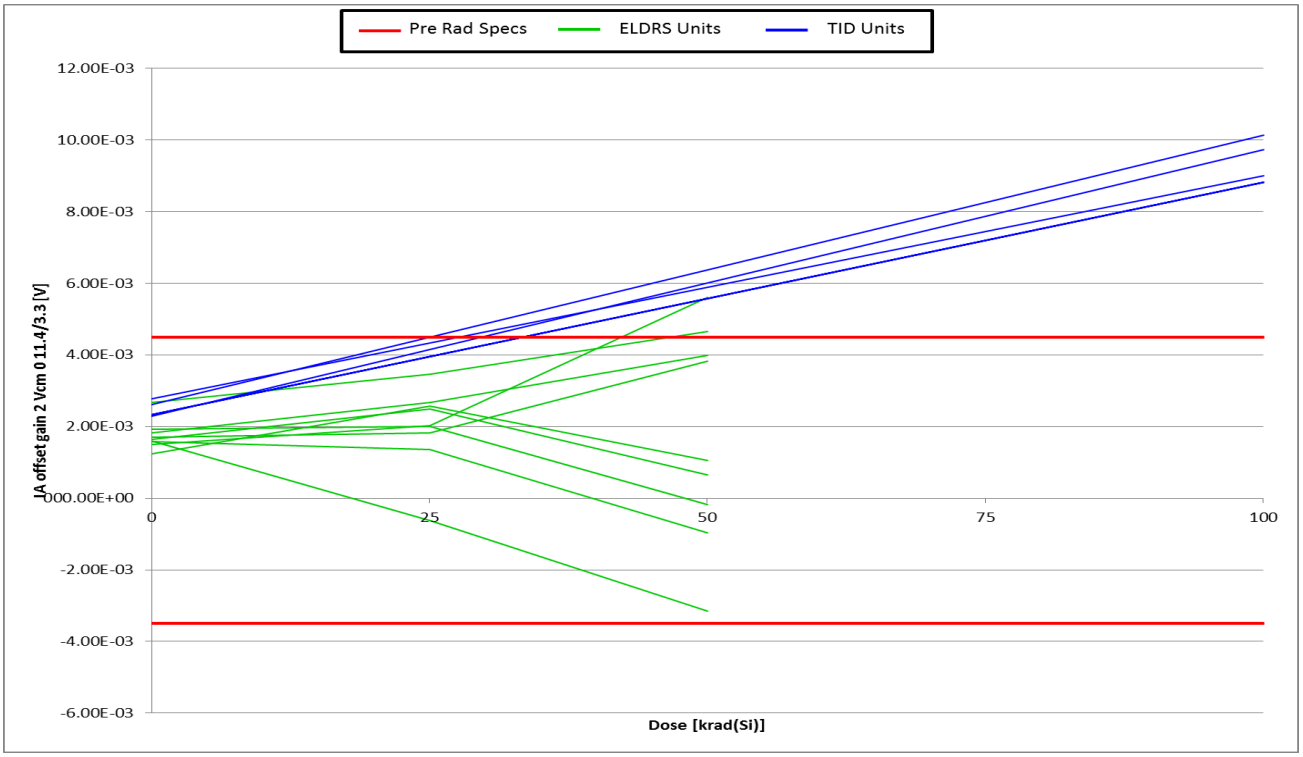
Instrumentation Amplifier Offset at Gain = 0.4, VCC=11.4V



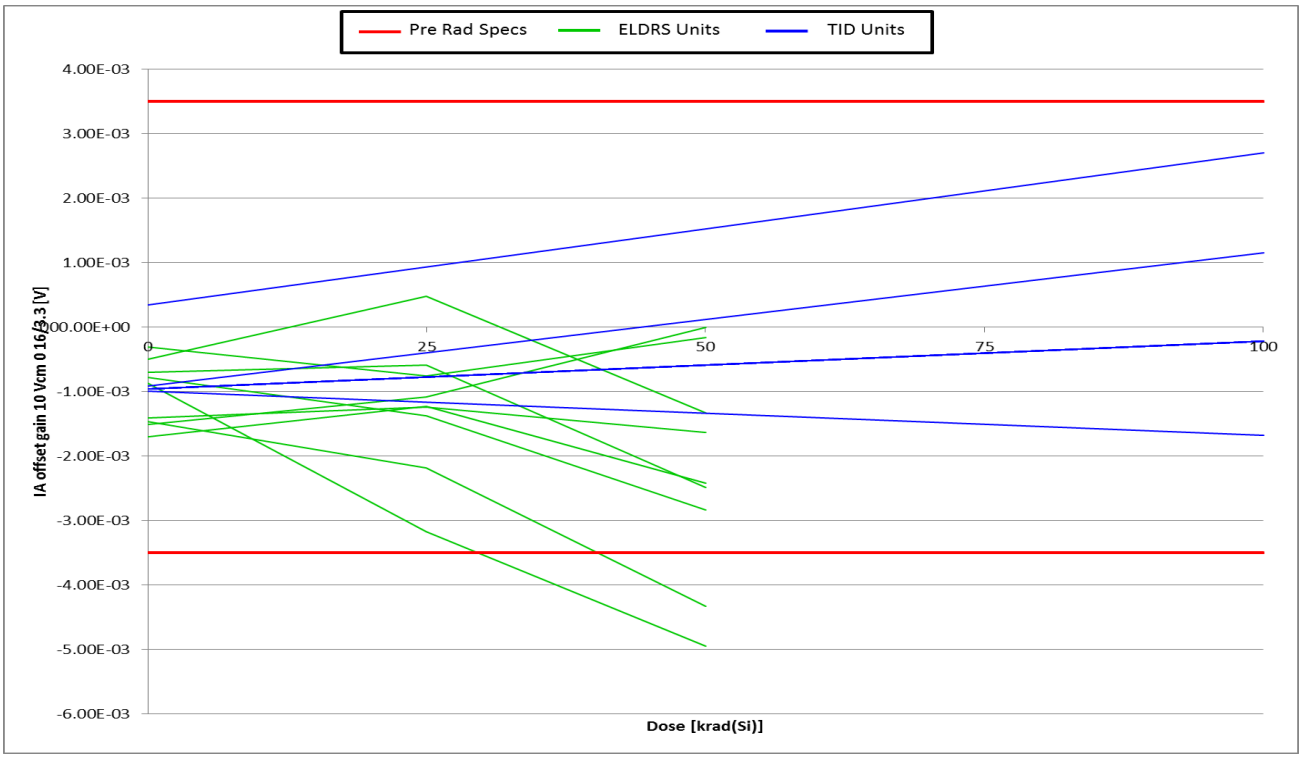
Instrumentation Amplifier Offset at Gain = 2, VCC=16V



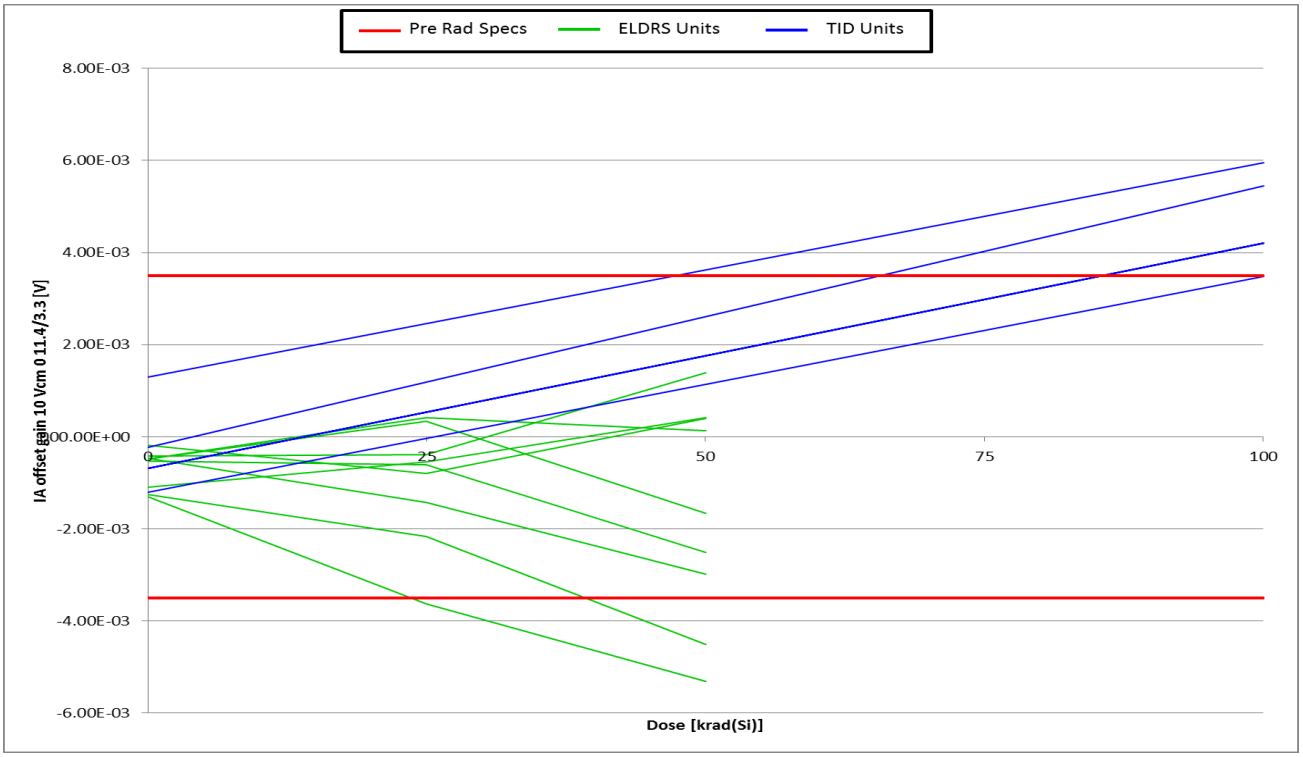
Instrumentation Amplifier Offset at Gain = 2, VCC=11.4V



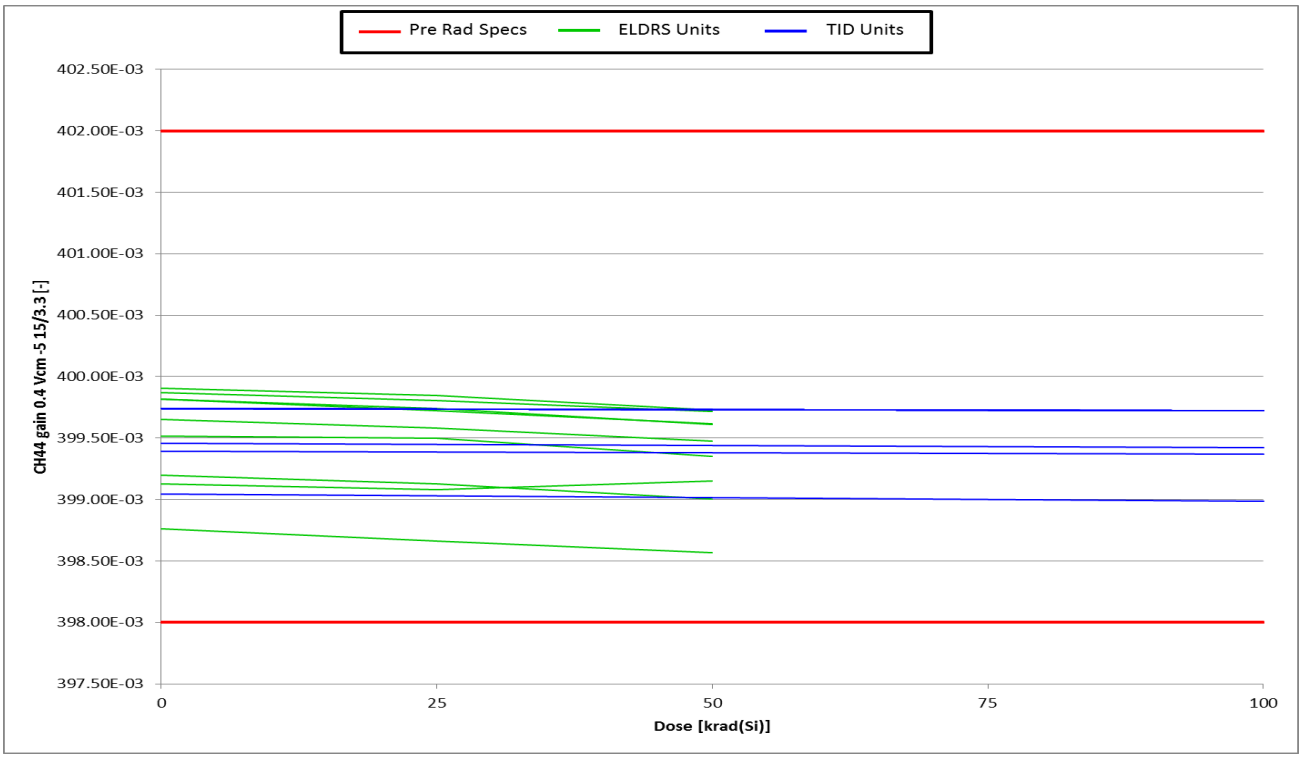
Instrumentation Amplifier Offset at Gain = 10, VCC=16V



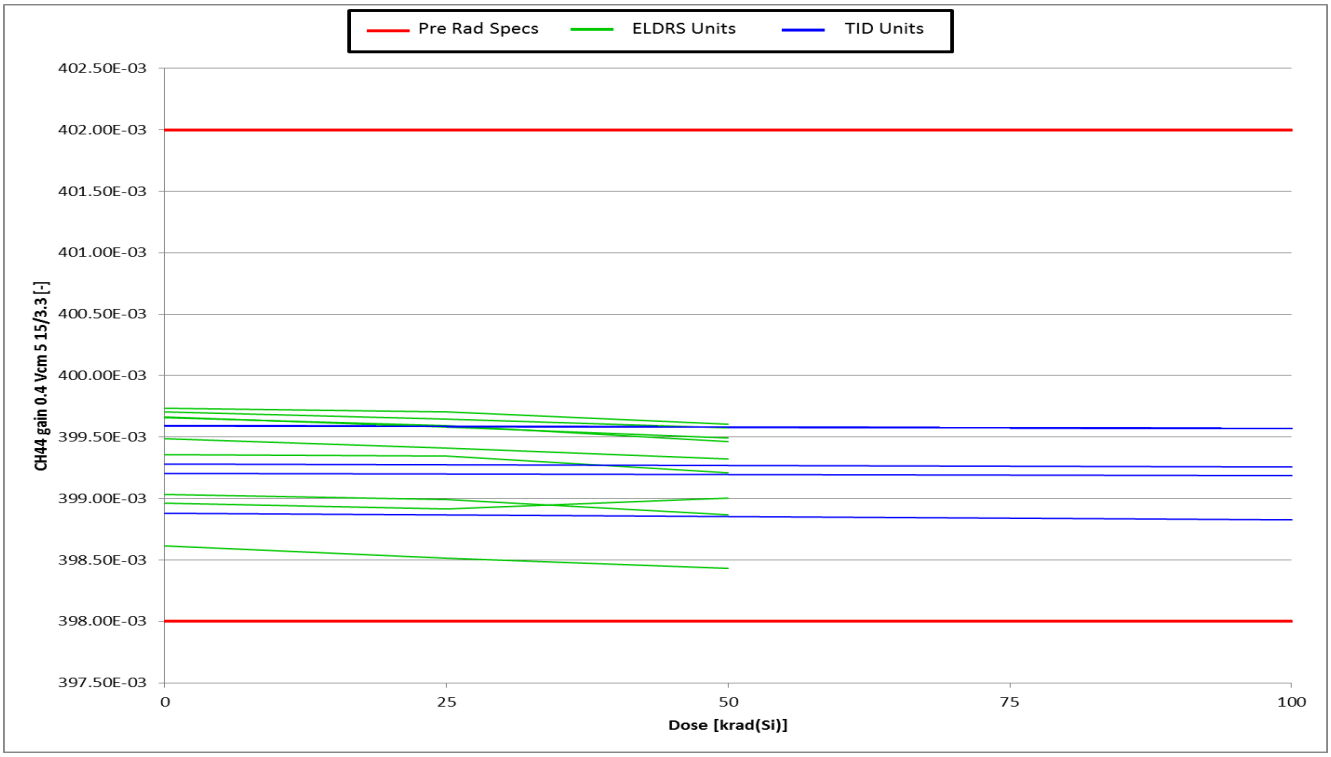
Instrumentation Amplifier Offset at Gain = 10, VCC=11.4V



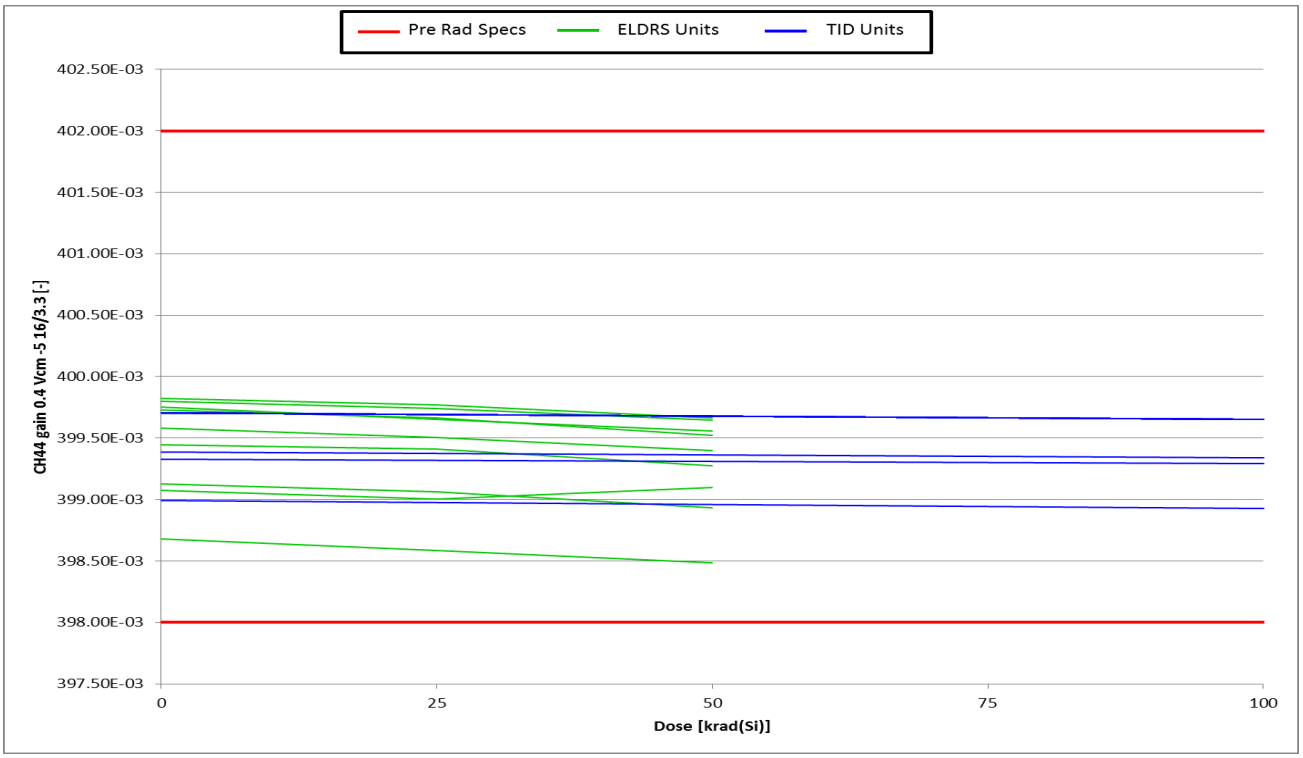
Instrumentation Amplifier Gain Accuracy at Gain = 0.4, VCC=15V, CM=-5V



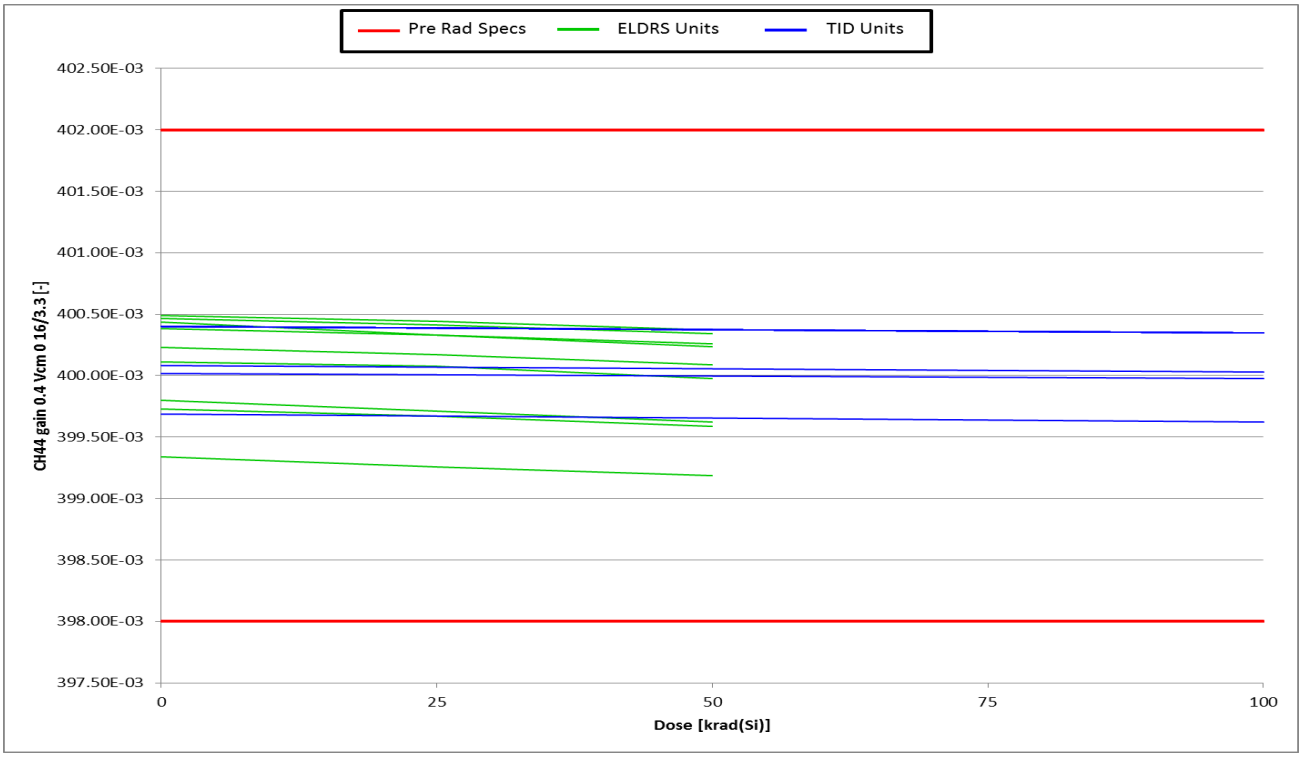
Instrumentation Amplifier Gain Accuracy at Gain = 0.4, VCC=15V, CM=5V



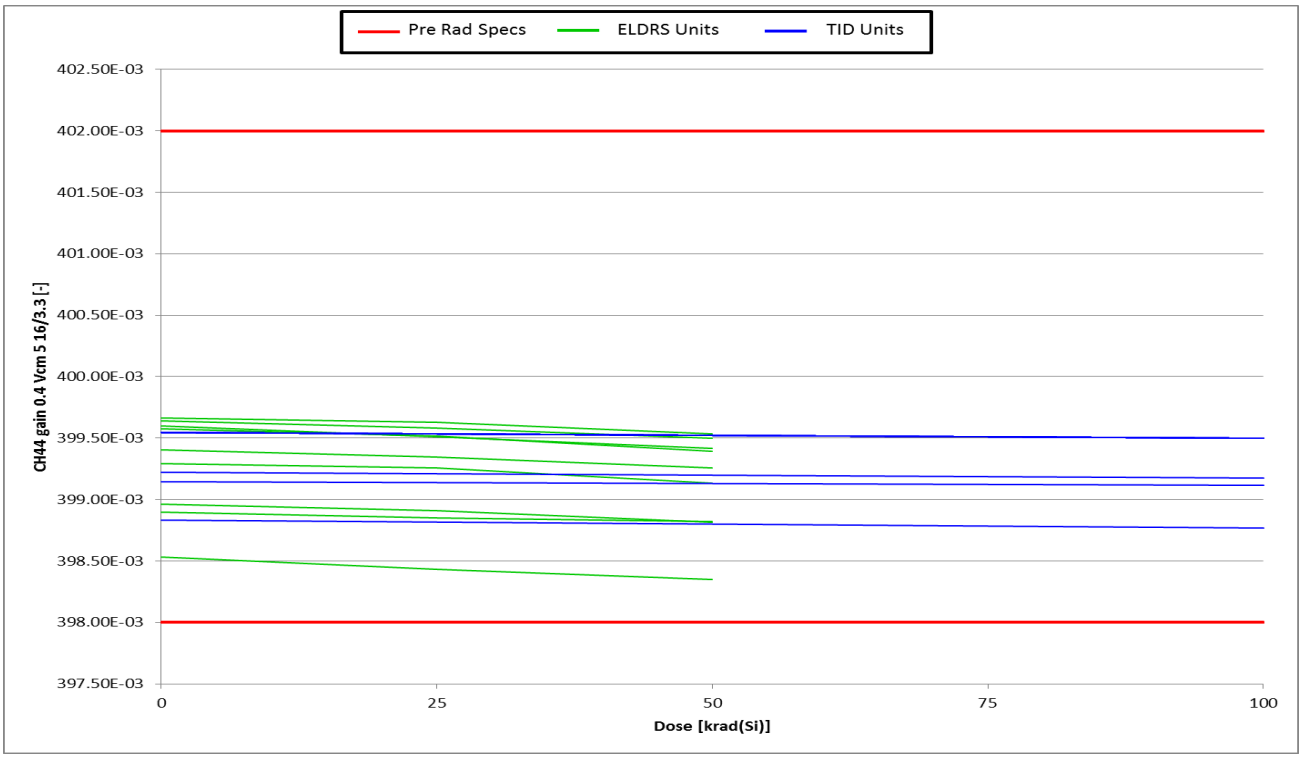
Instrumentation Amplifier Gain Accuracy at Gain = 0.4, VCC=16V, CM=-5V



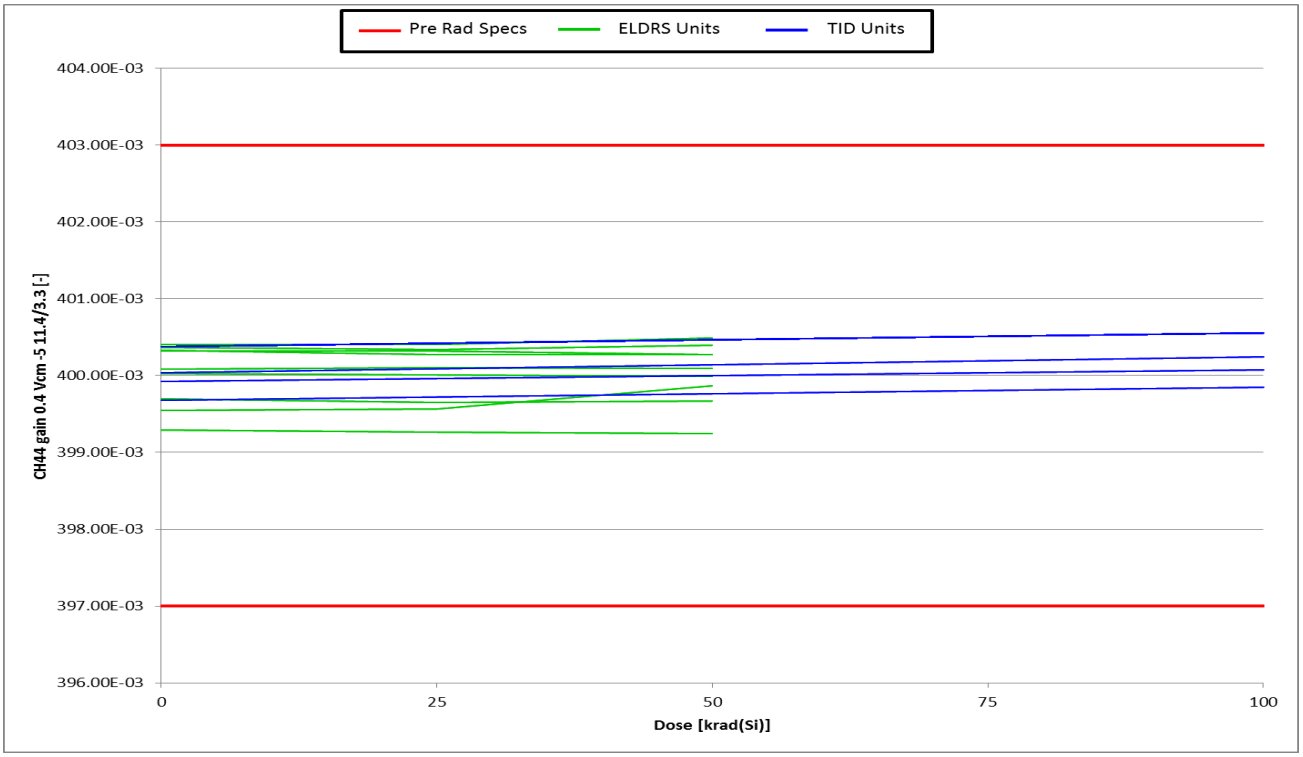
Instrumentation Amplifier Gain Accuracy at Gain = 0.4, VCC=16V, CM=0V



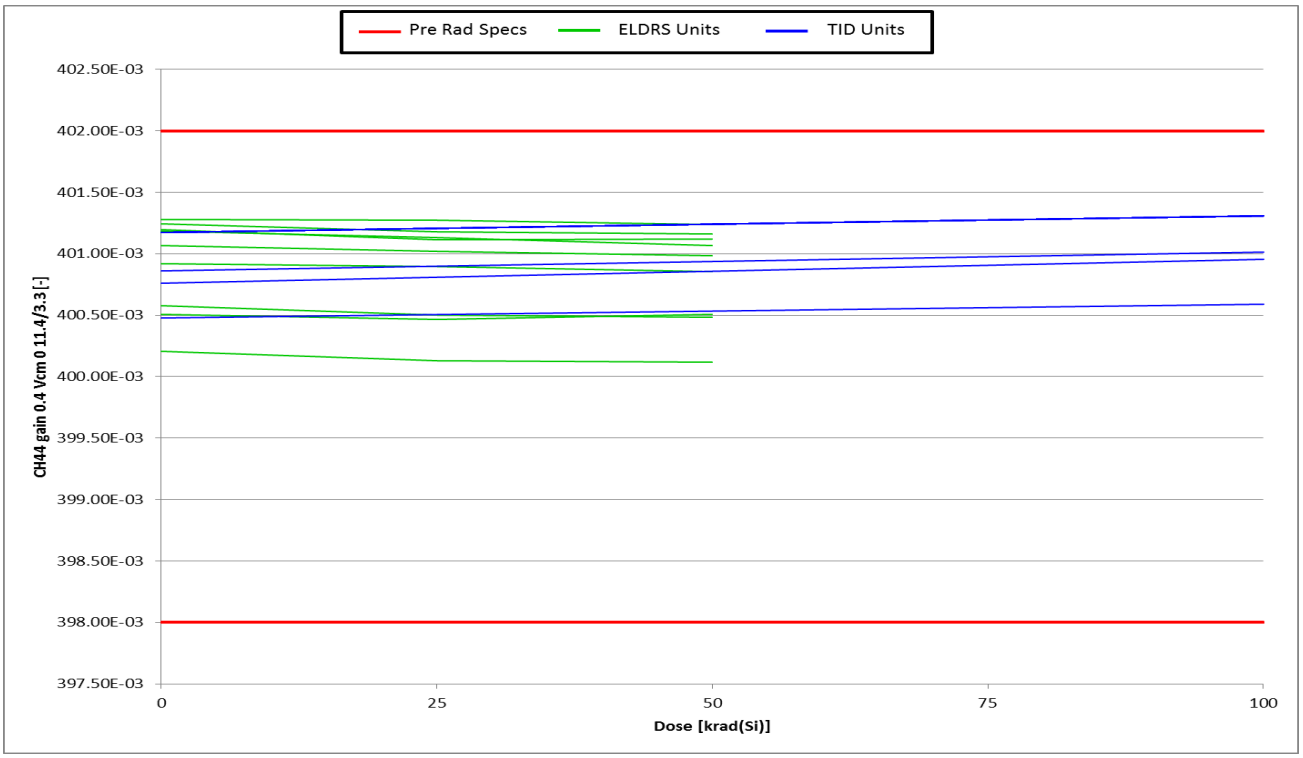
Instrumentation Amplifier Gain Accuracy at Gain = 0.4, VCC=16V, CM=5V



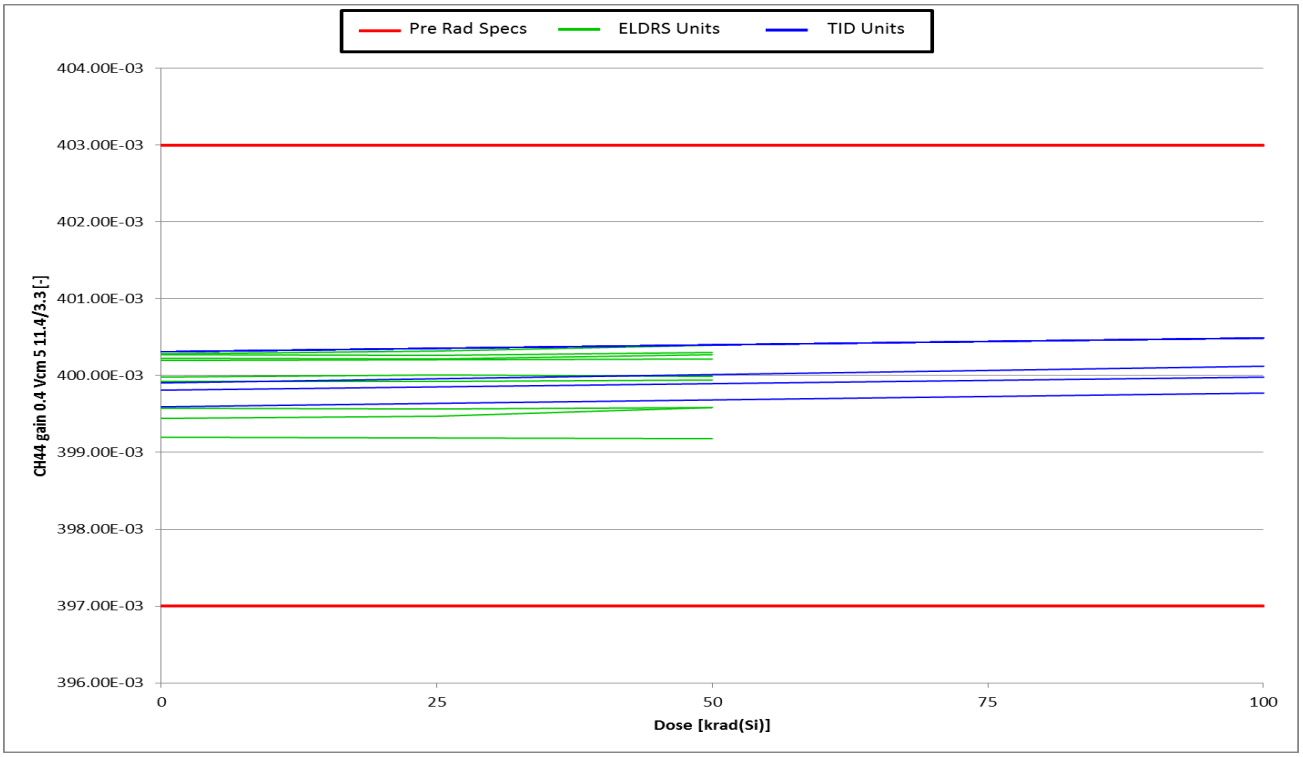
Instrumentation Amplifier Gain Accuracy at Gain = 0.4, VCC=11.4V, CM=5V



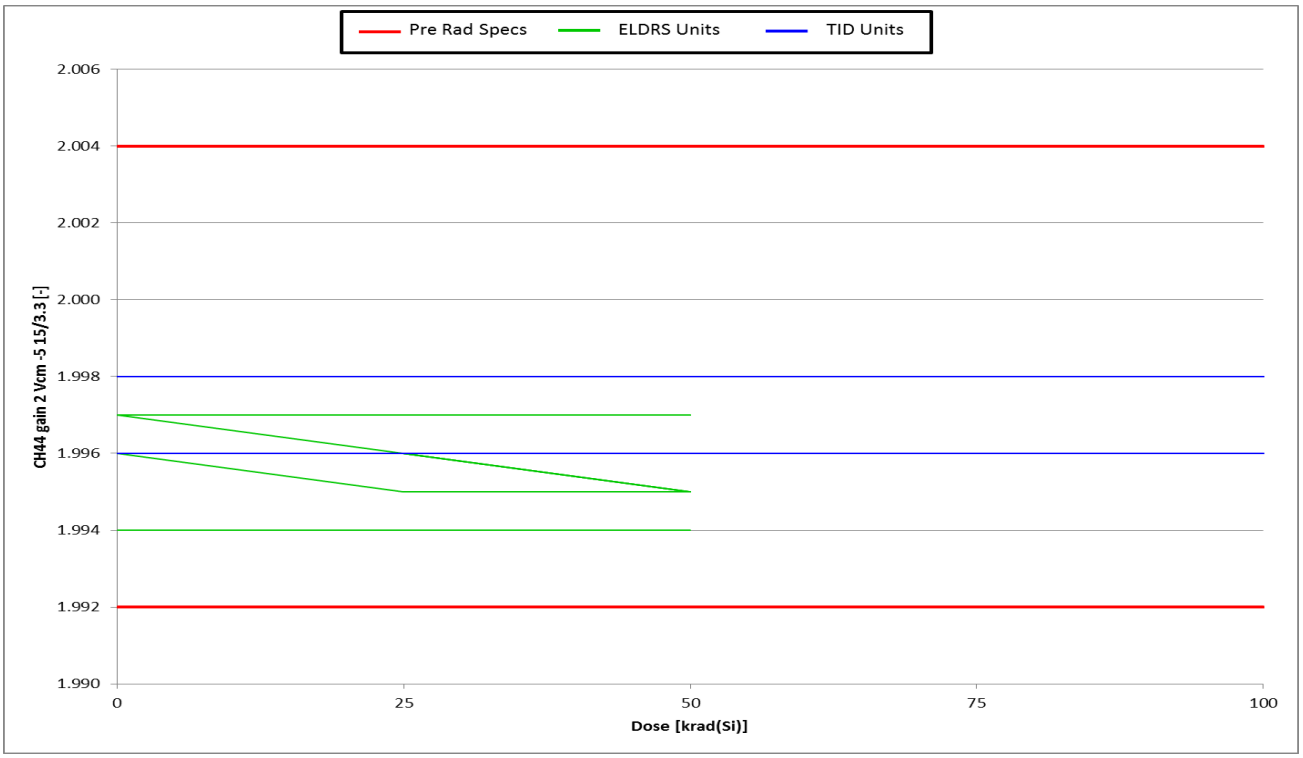
Instrumentation Amplifier Gain Accuracy at Gain = 0.4, VCC=11.4V, CM=5V



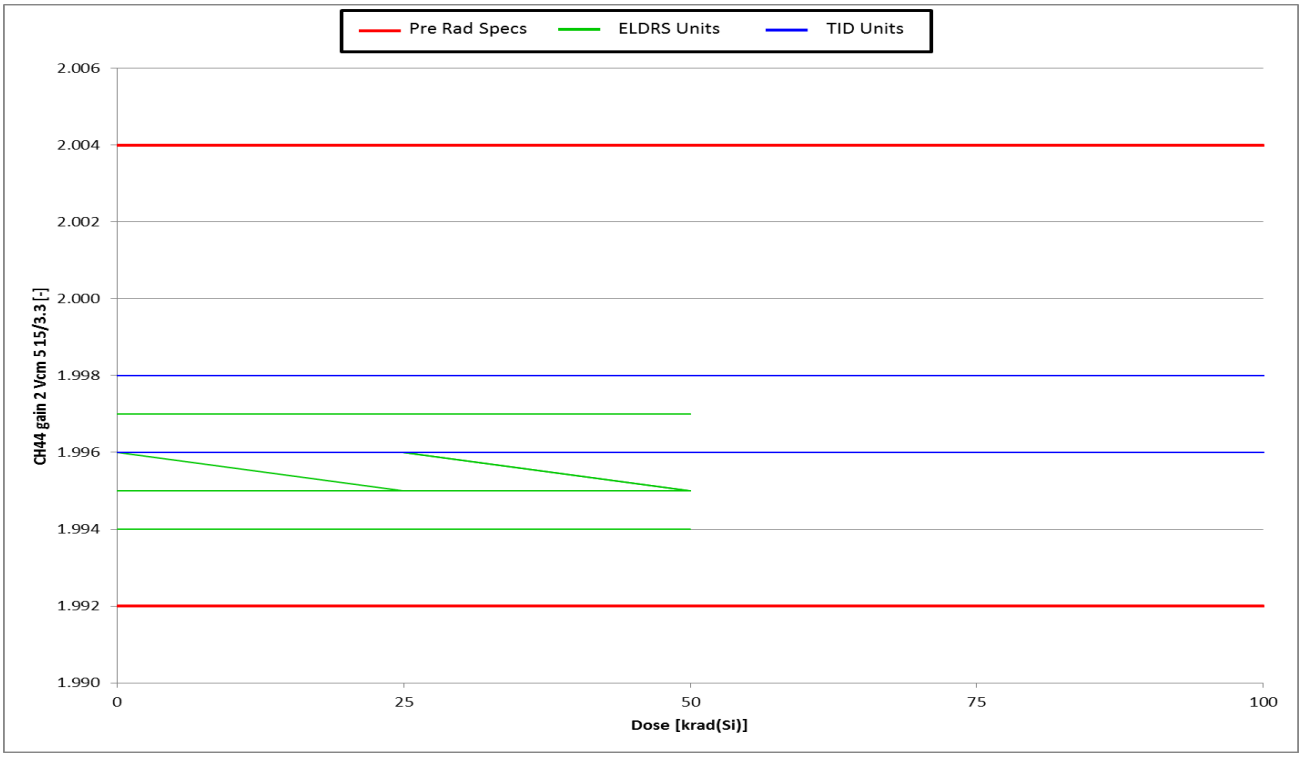
Instrumentation Amplifier Gain Accuracy at Gain = 0.4, VCC=11.4V, CM=5V



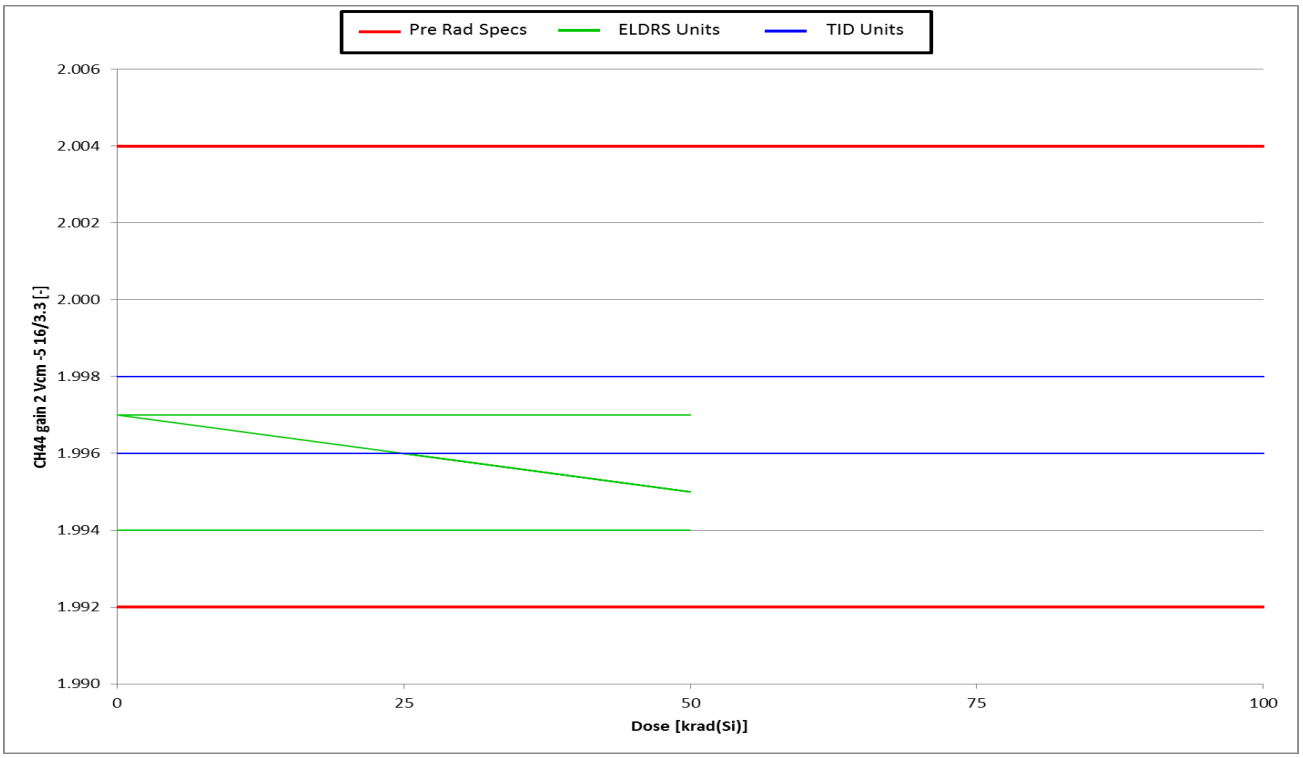
Instrumentation Amplifier Gain Accuracy at Gain = 2, VCC=15V, CM=-5V



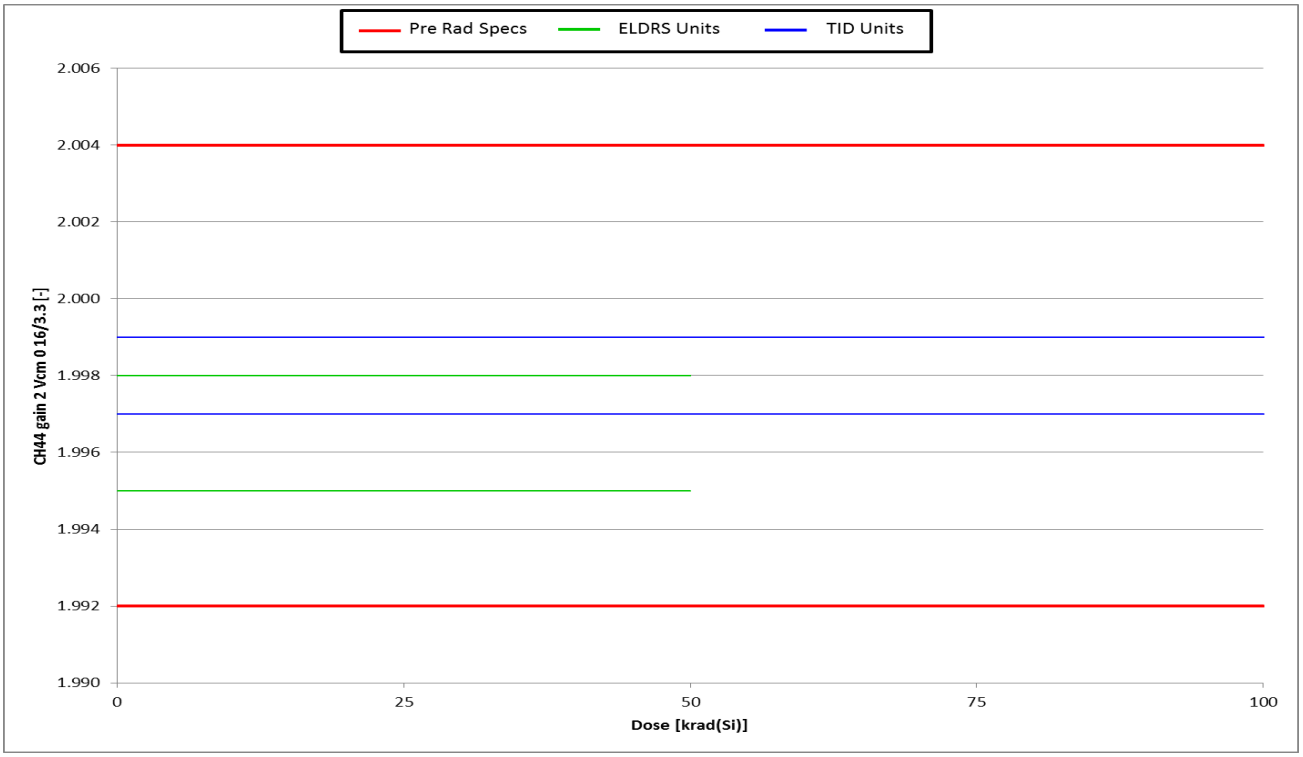
Instrumentation Amplifier Gain Accuracy at Gain = 2, VCC=15V, CM=5V



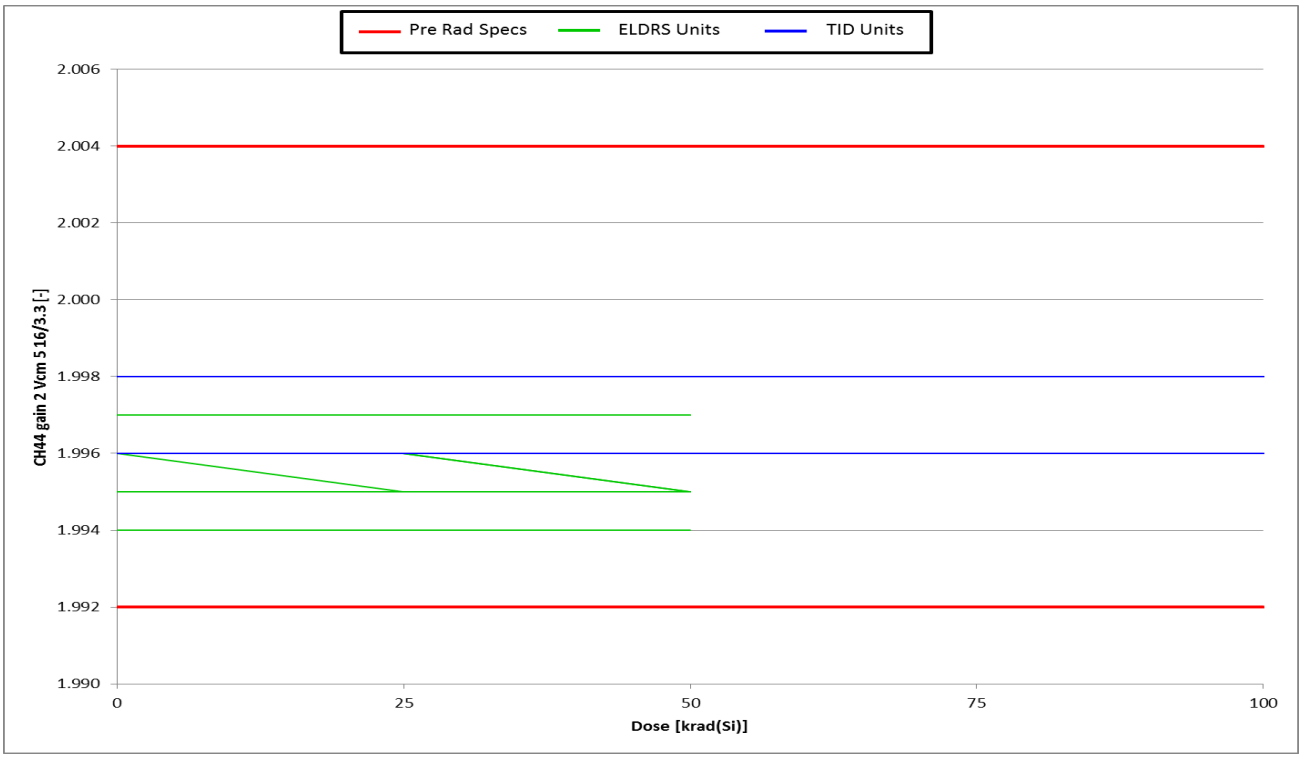
Instrumentation Amplifier Gain Accuracy at Gain = 2, VCC=16V, CM=-5V



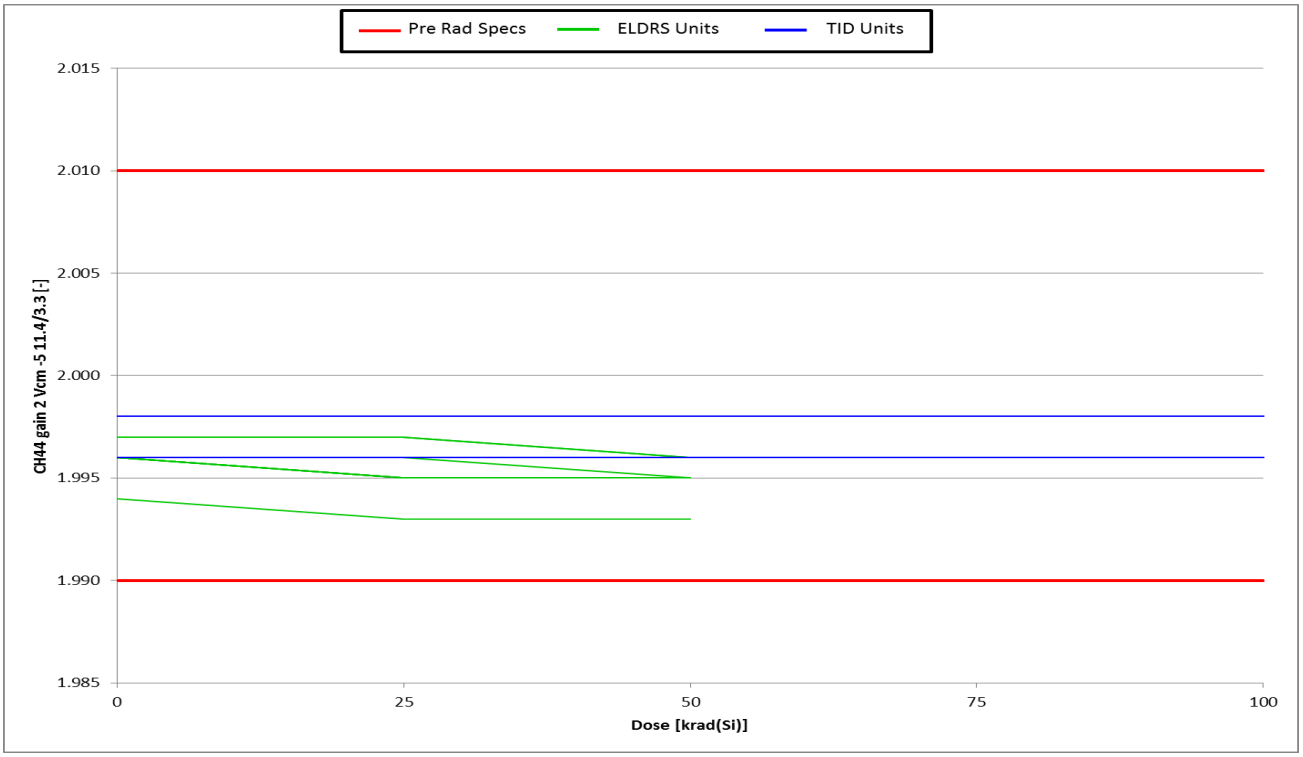
Instrumentation Amplifier Gain Accuracy at Gain = 2, VCC=16V, CM=0V



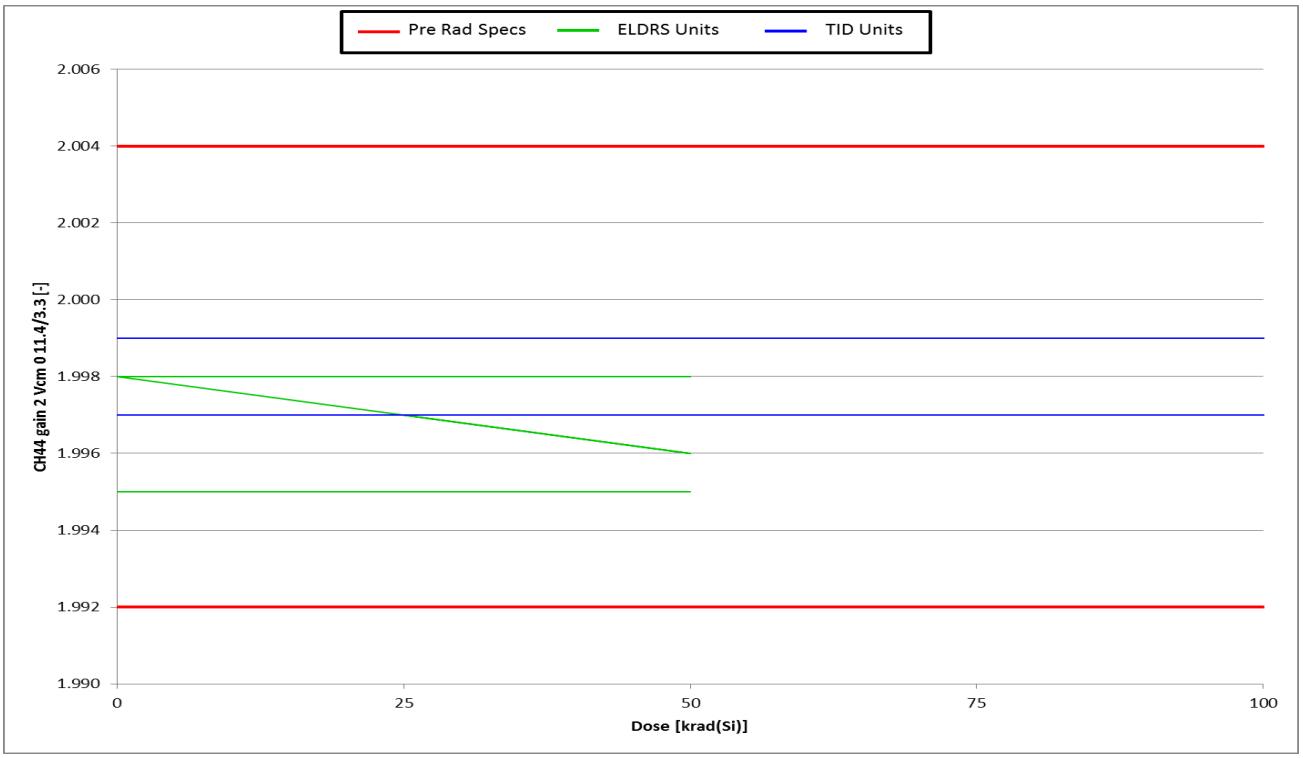
Instrumentation Amplifier Gain Accuracy at Gain = 2, VCC=16V, CM=5V



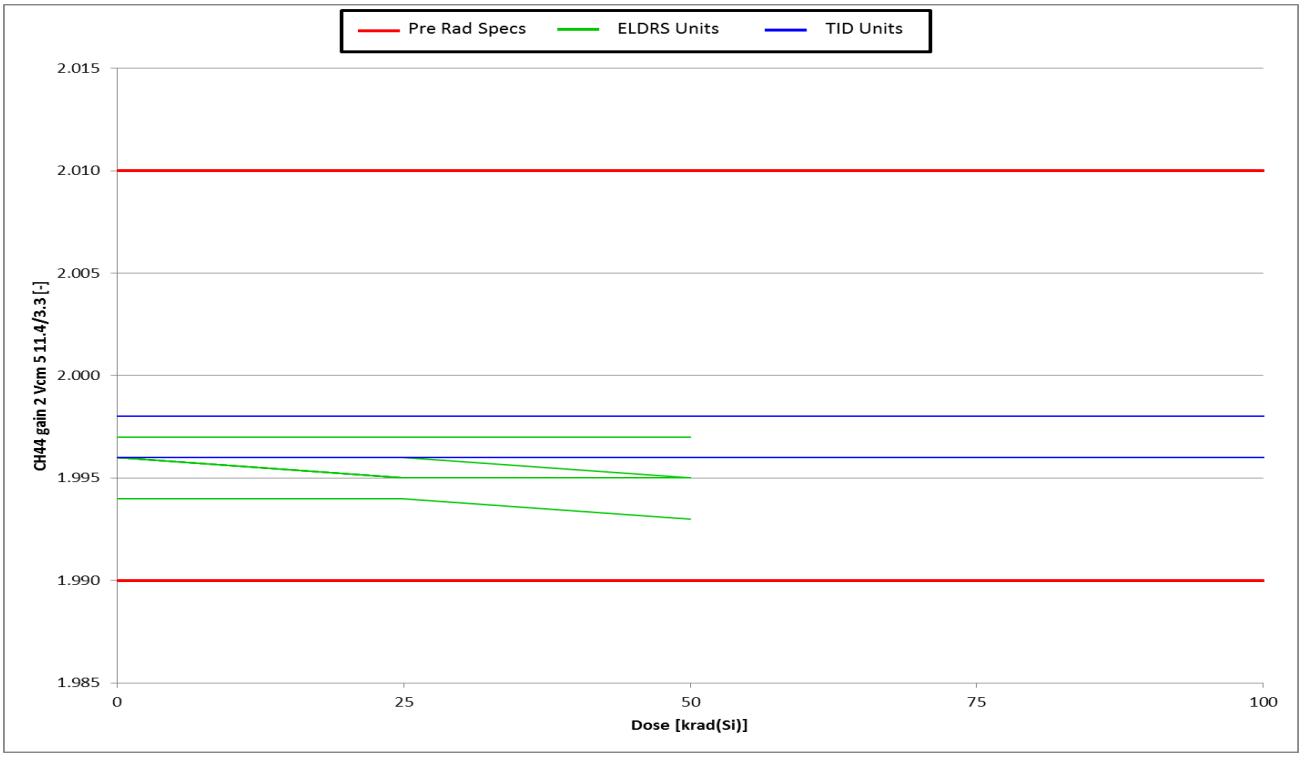
Instrumentation Amplifier Gain Accuracy at Gain = 2, VCC=11.4V, CM=-5V



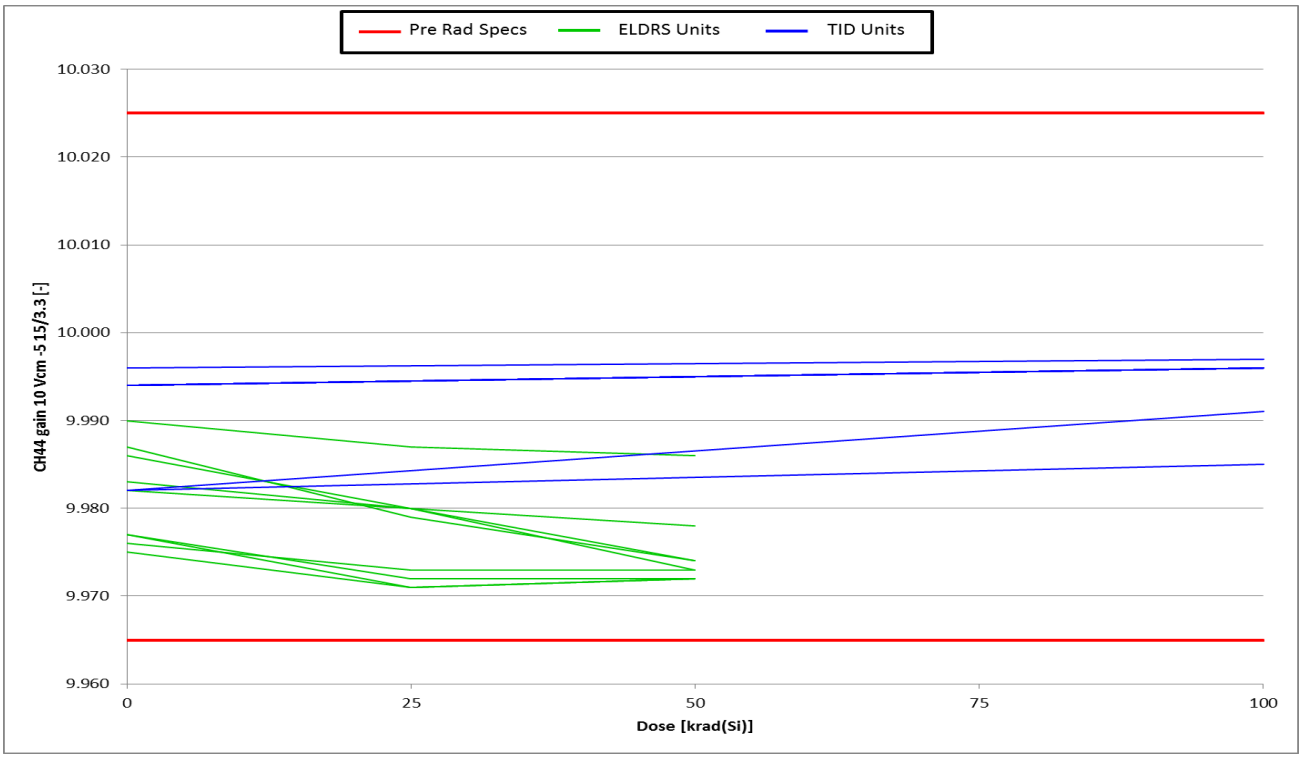
Instrumentation Amplifier Gain Accuracy at Gain = 2, VCC=11.4V, CM=0V



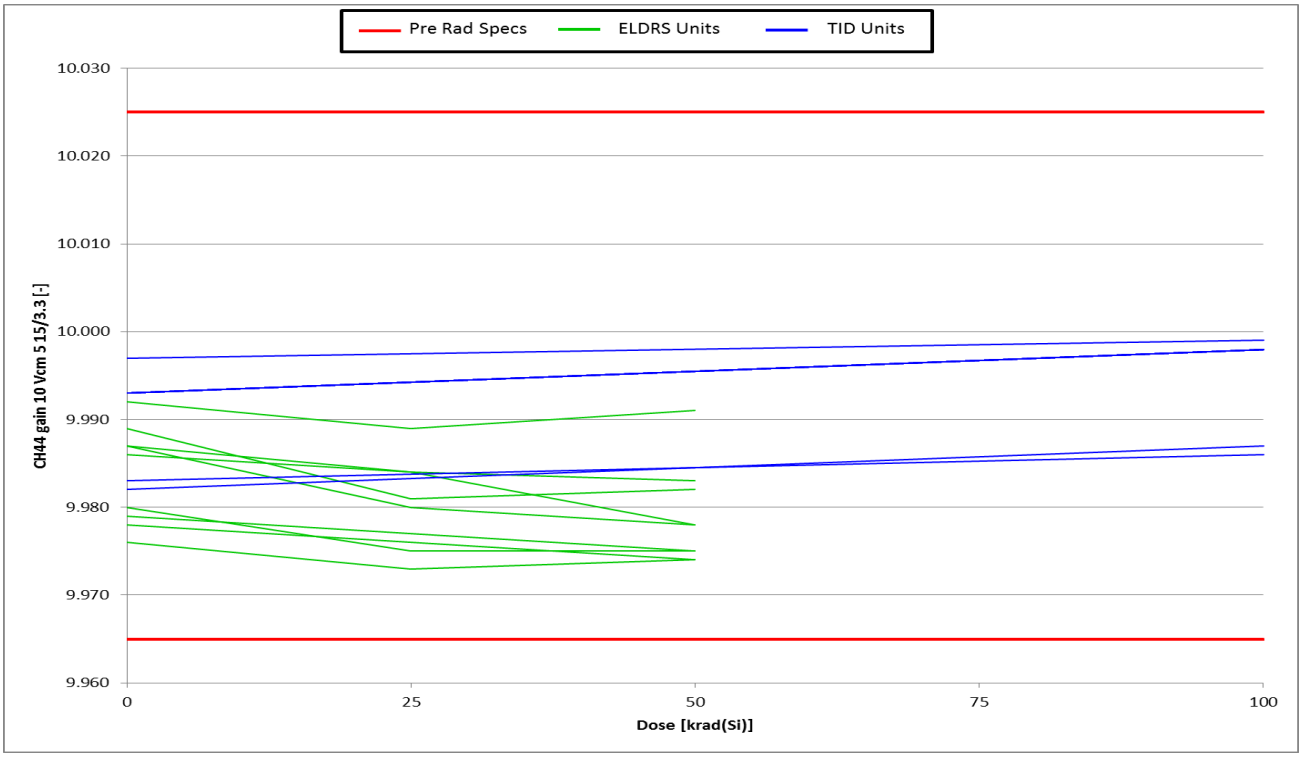
Instrumentation Amplifier Gain Accuracy at Gain = 2, VCC=11.4V, CM=5V



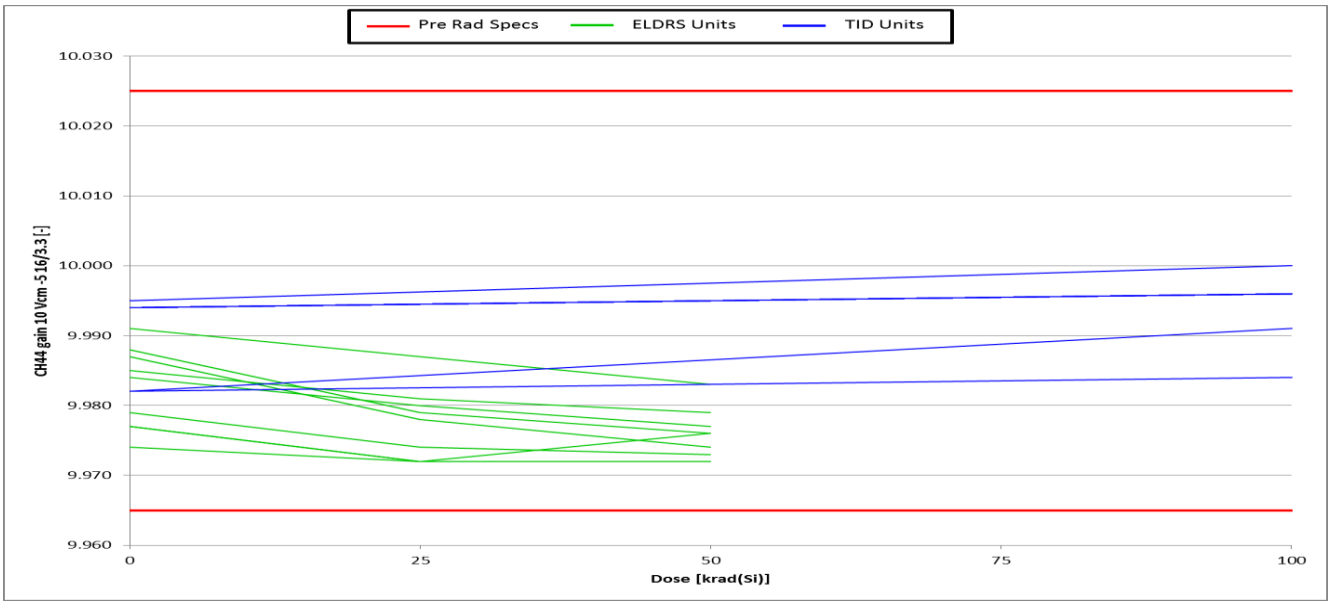
Instrumentation Amplifier Gain Accuracy at Gain = 10, VCC=15V, CM=-5V



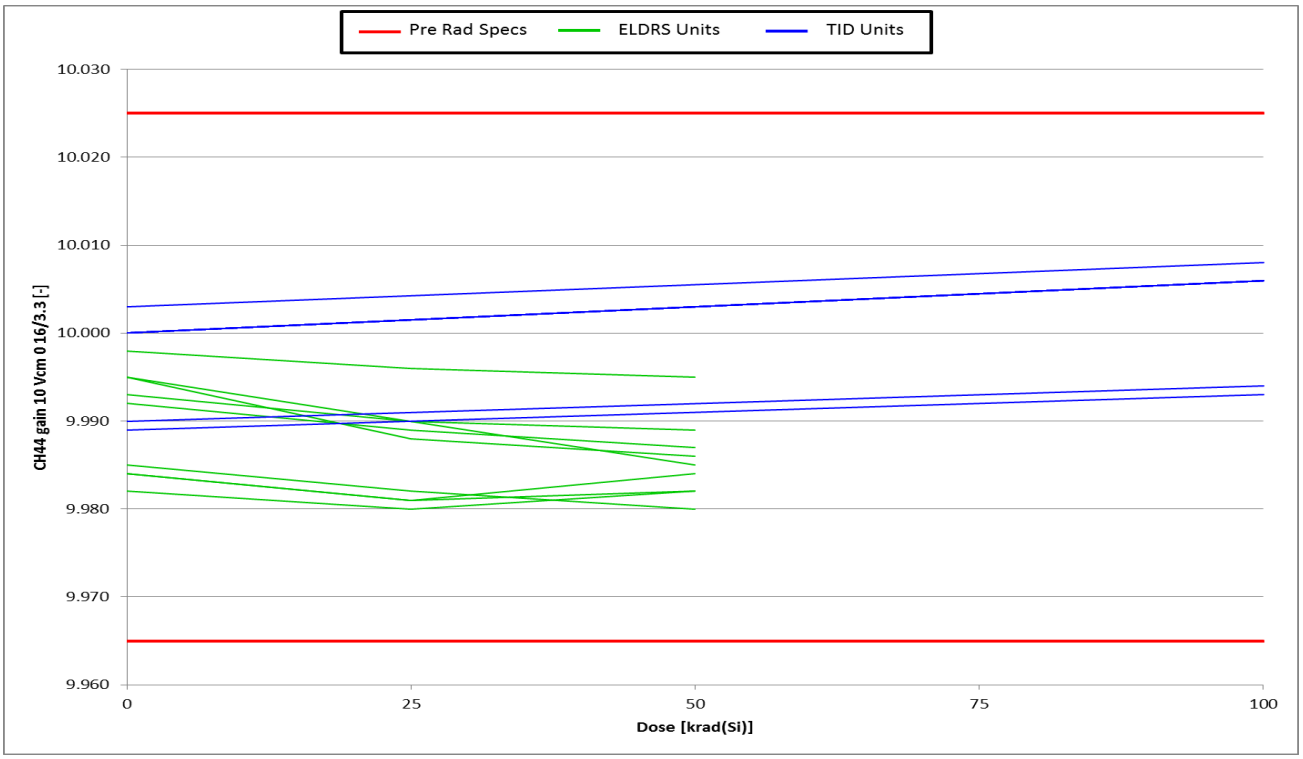
Instrumentation Amplifier Gain Accuracy at Gain = 10, VCC=15V, CM=5V



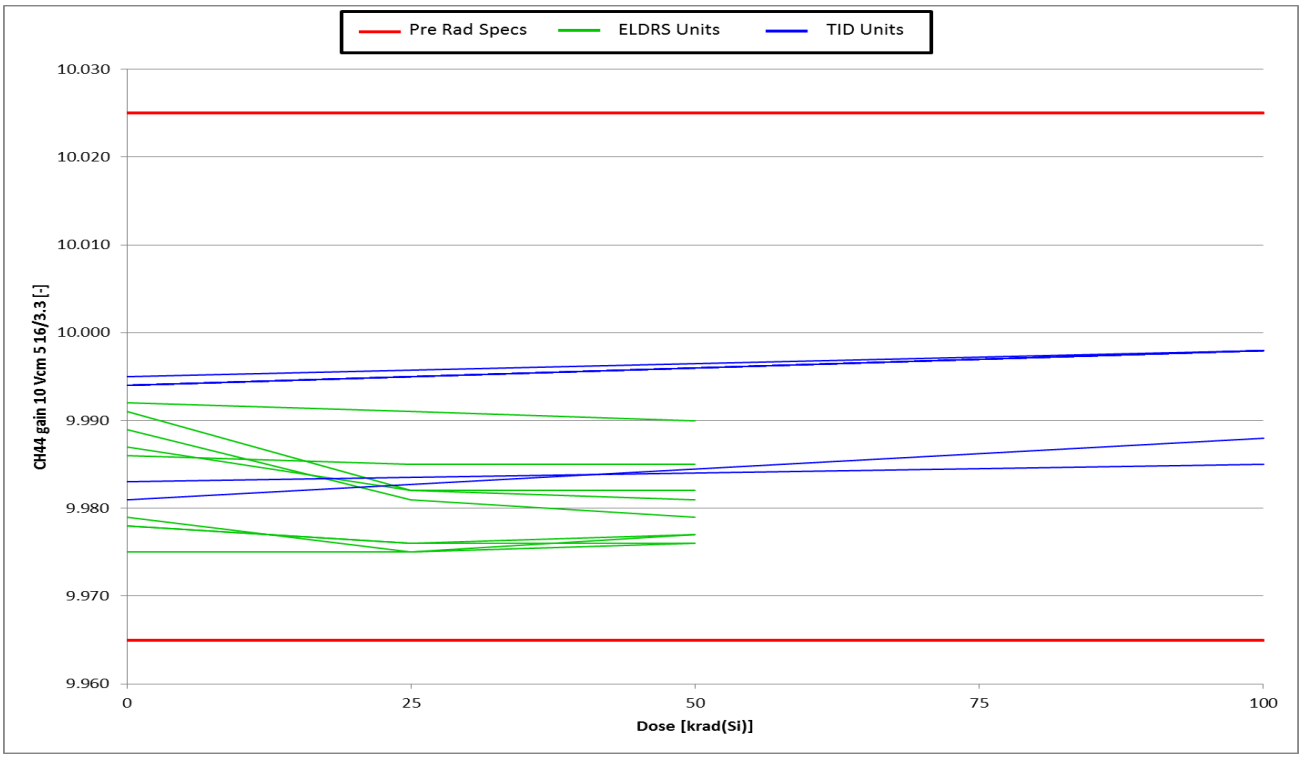
Instrumentation Amplifier Gain Accuracy at Gain = 10, VCC=16V, CM=-5V



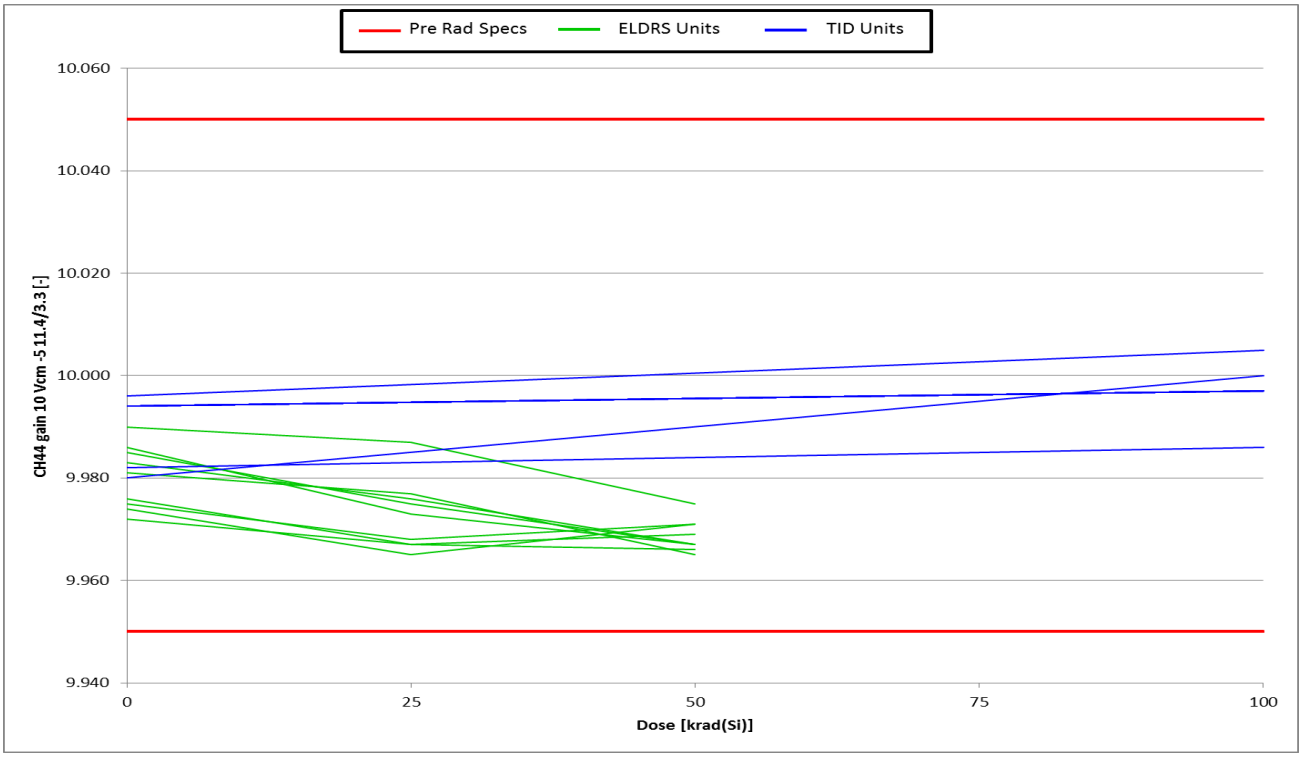
Instrumentation Amplifier Gain Accuracy at Gain = 10, VCC=16V, CM=0V



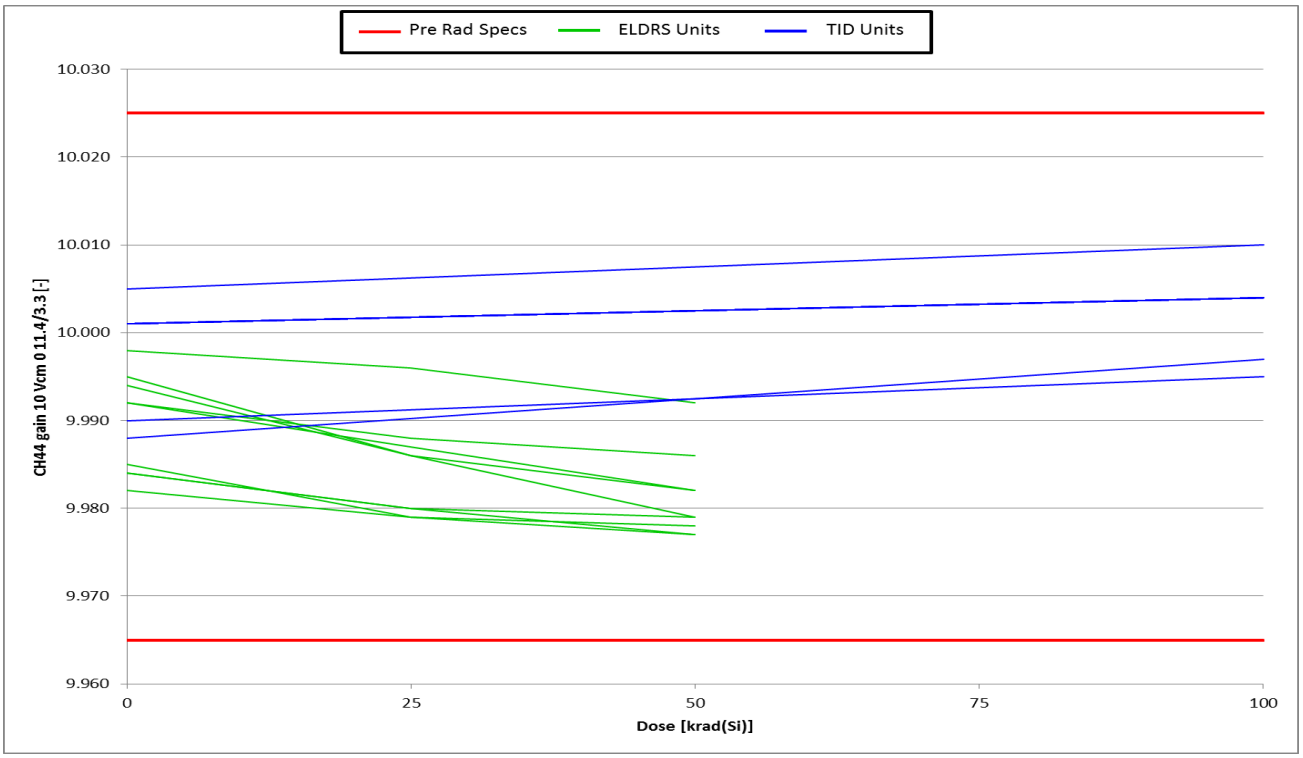
Instrumentation Amplifier Gain Accuracy at Gain = 10, VCC=16V, CM=5V



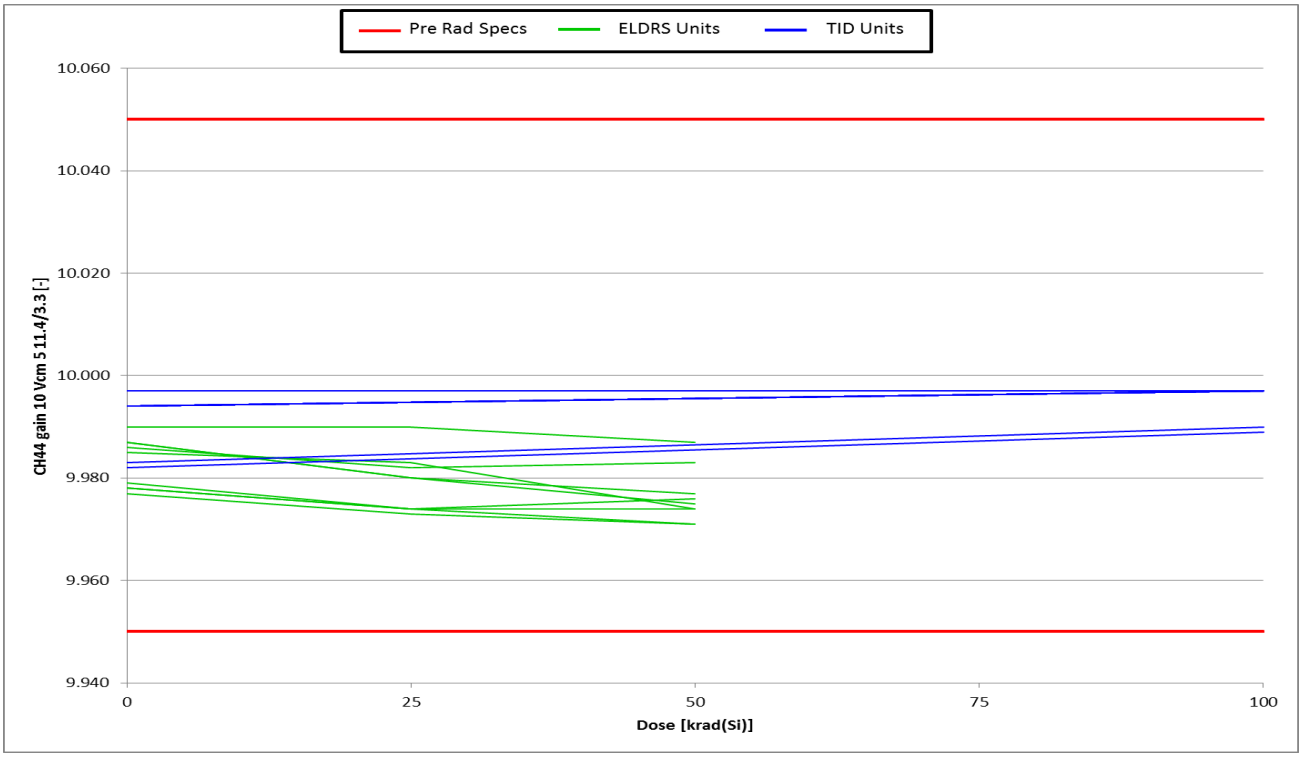
Instrumentation Amplifier Gain Accuracy at Gain = 10, VCC=11.4V, CM=-5V



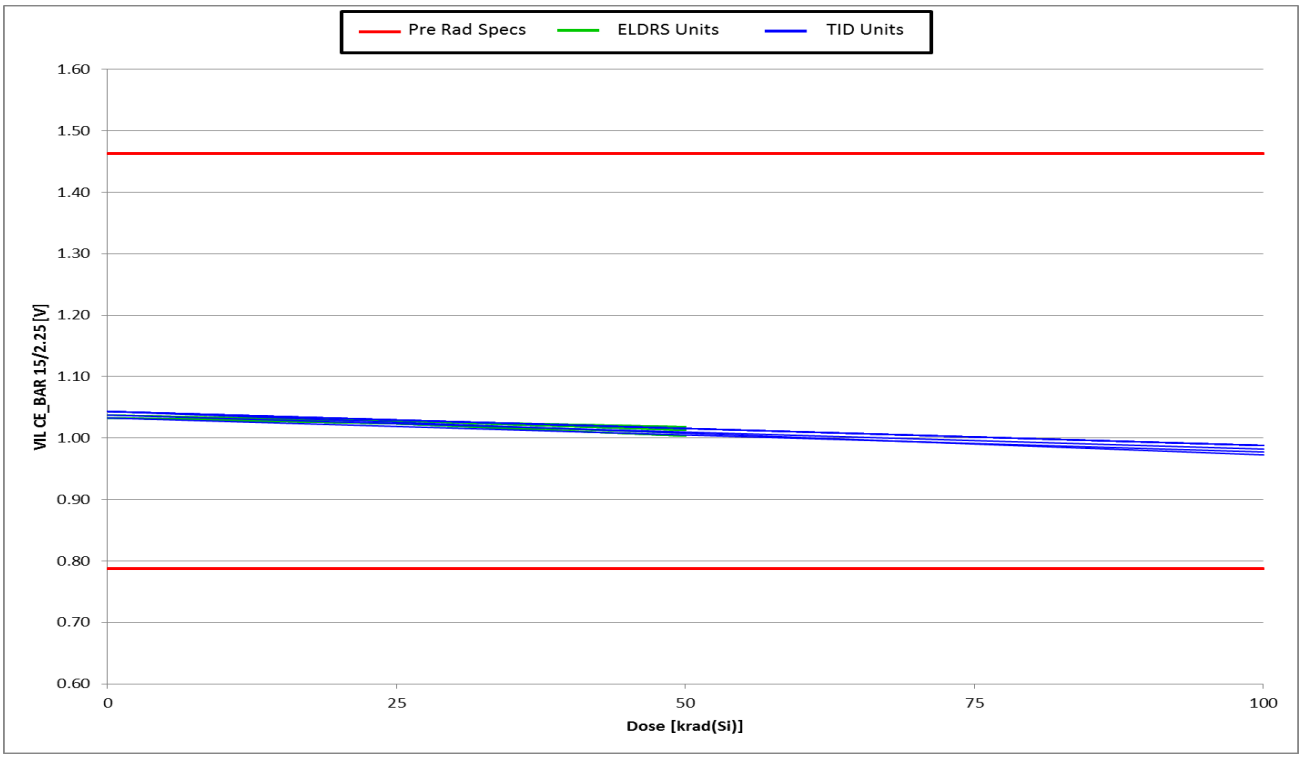
Instrumentation Amplifier Gain Accuracy at Gain = 10, VCC=11.4V, CM=0V

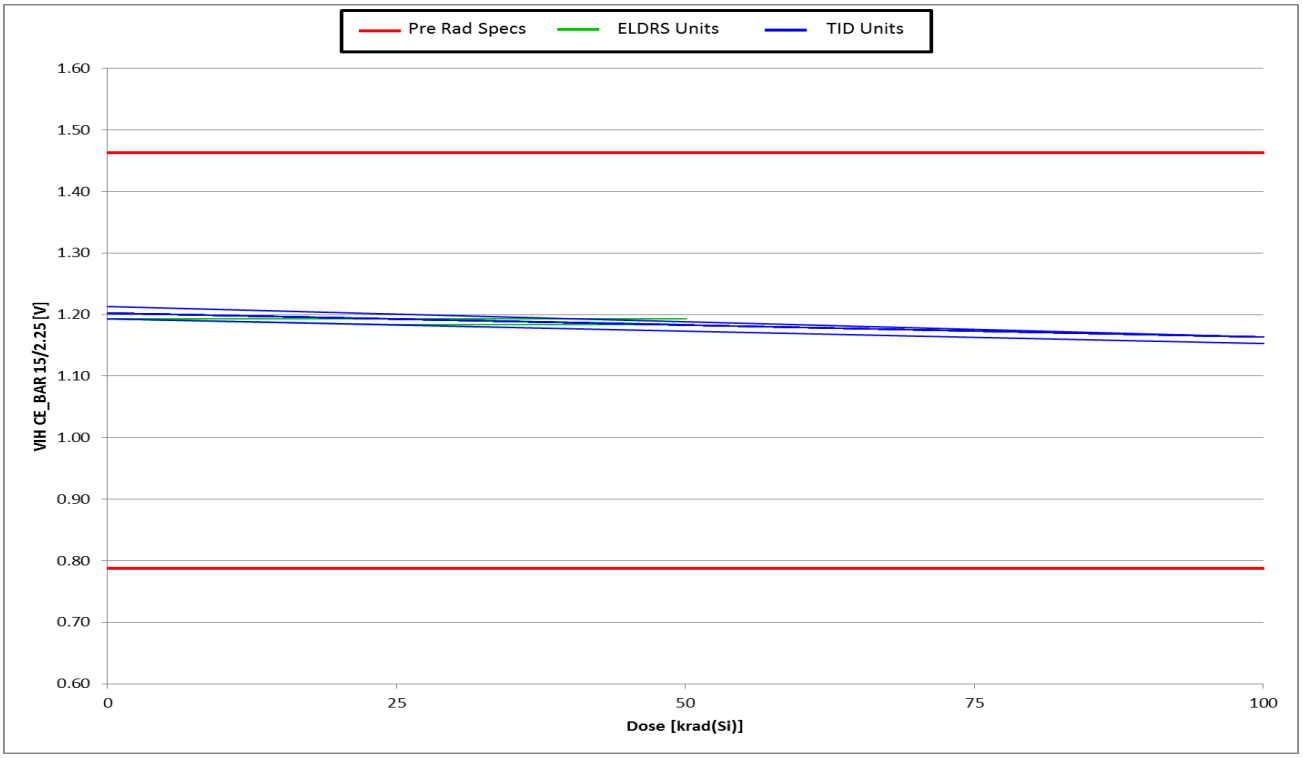


Instrumentation Amplifier Gain Accuracy at Gain = 10, VCC=11.4V, CM=5V

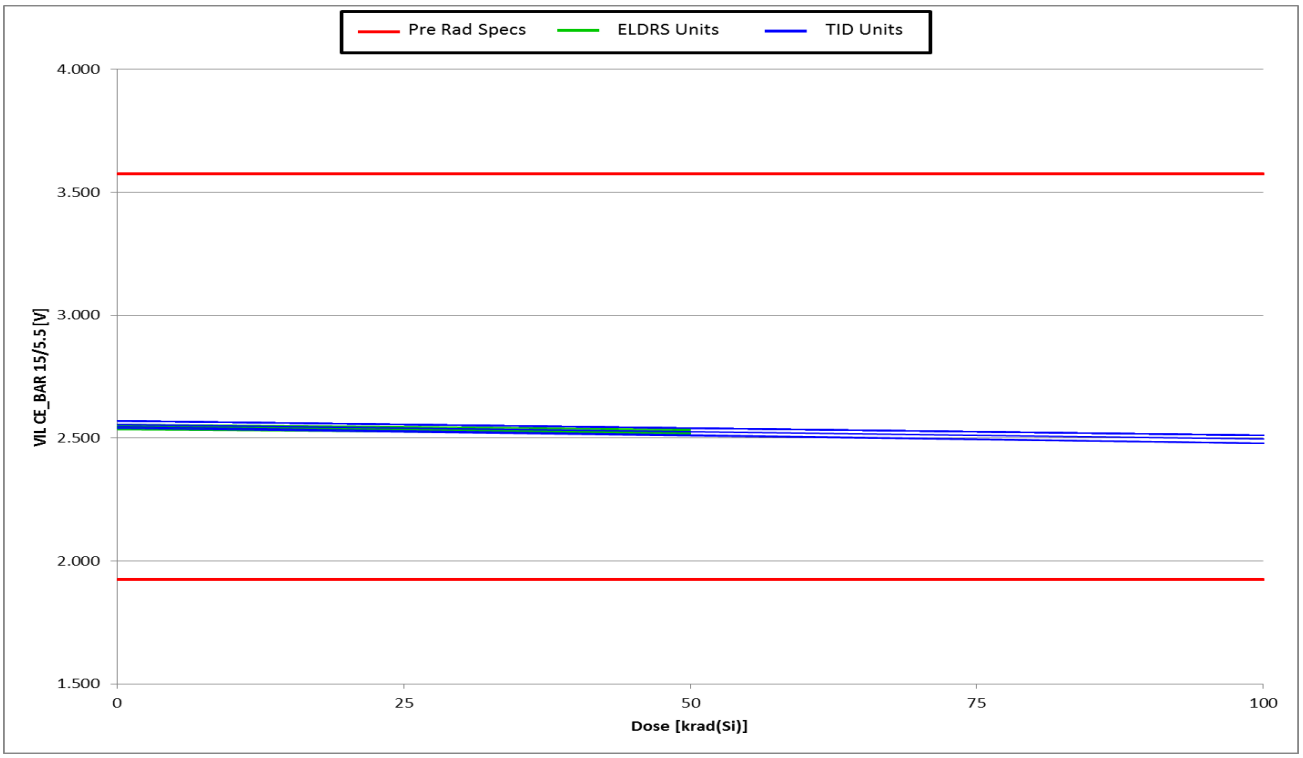


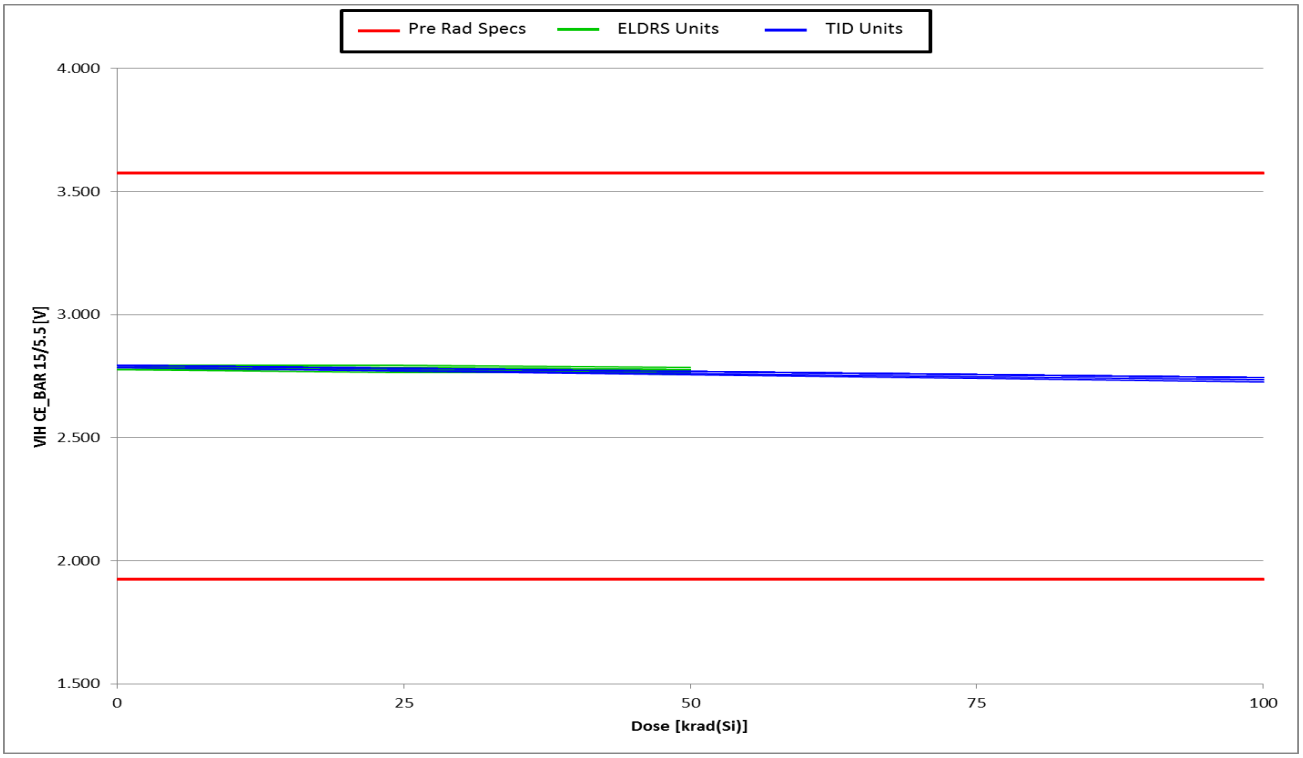
Logic Levels for FPGA Interface I/Os - Input Logic Threshold at VDD=2.25V



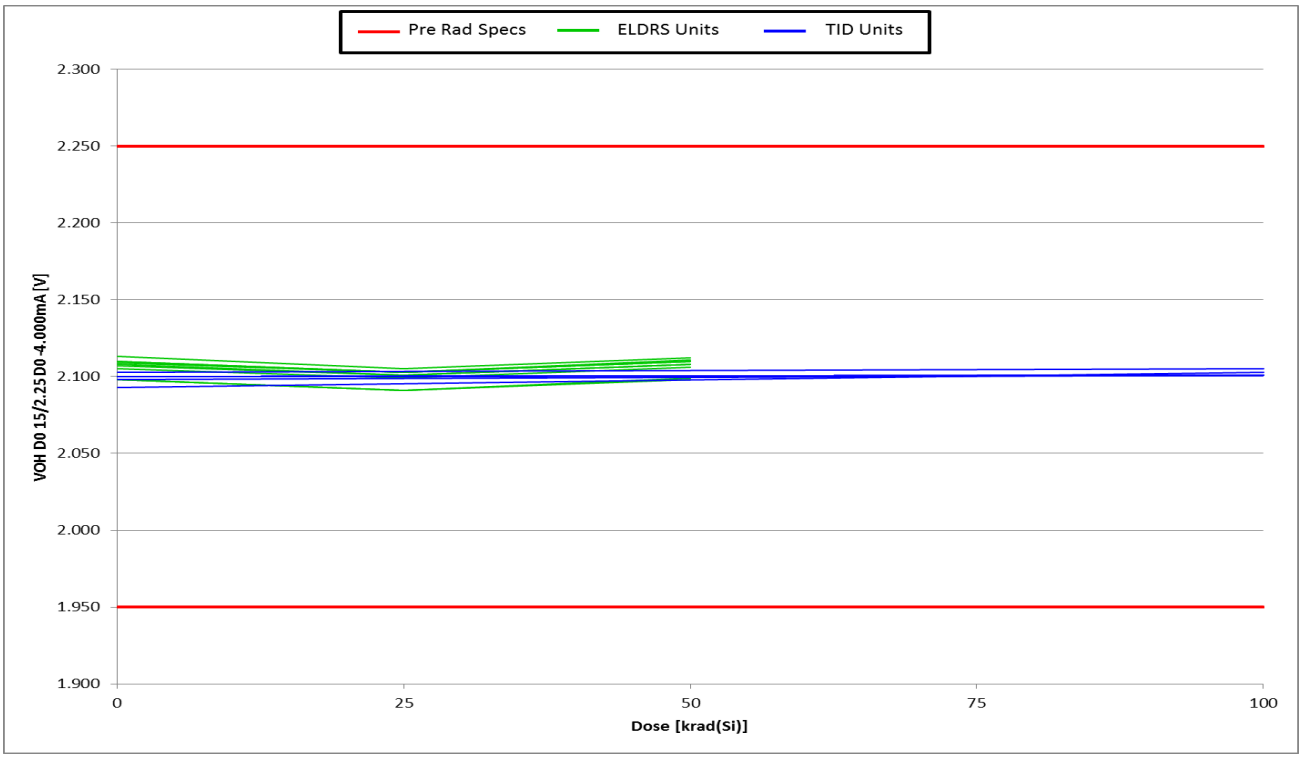


Logic Levels for FPGA Interface I/Os - Input Logic Threshold at VDD=5.5V

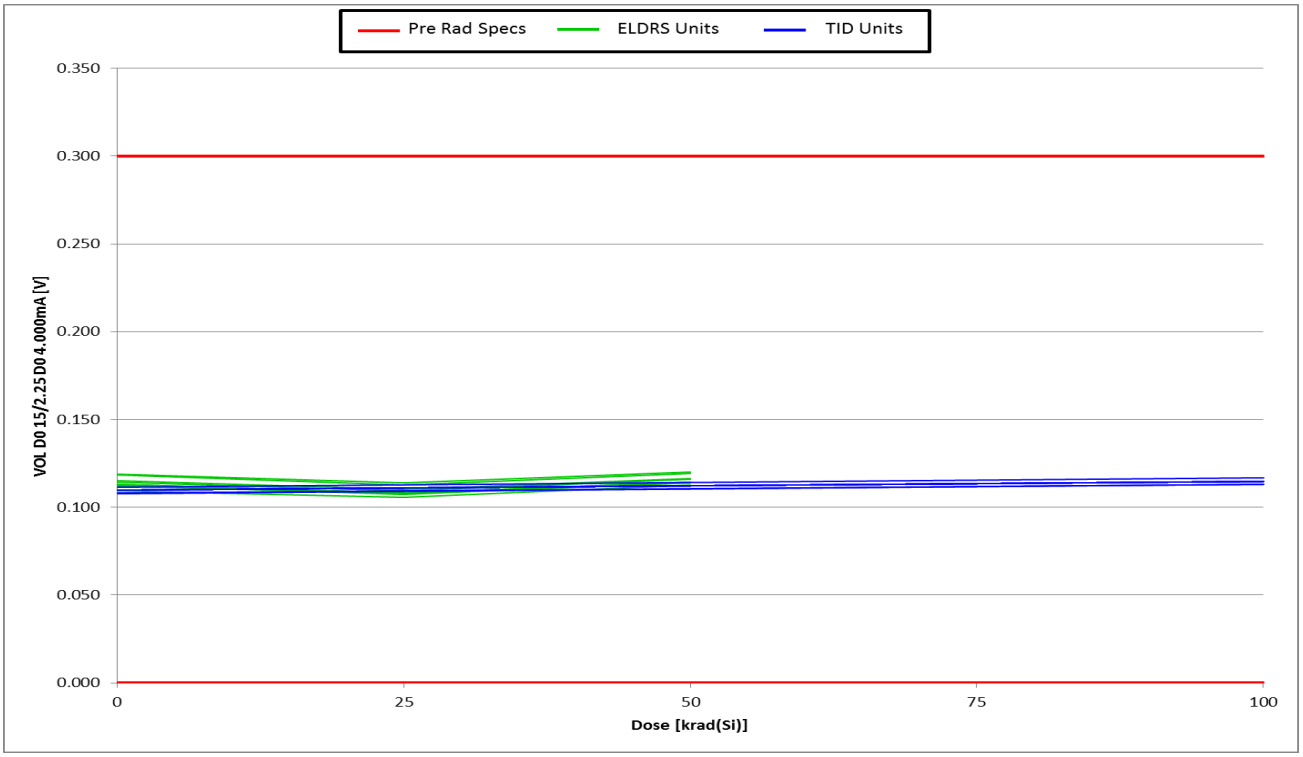




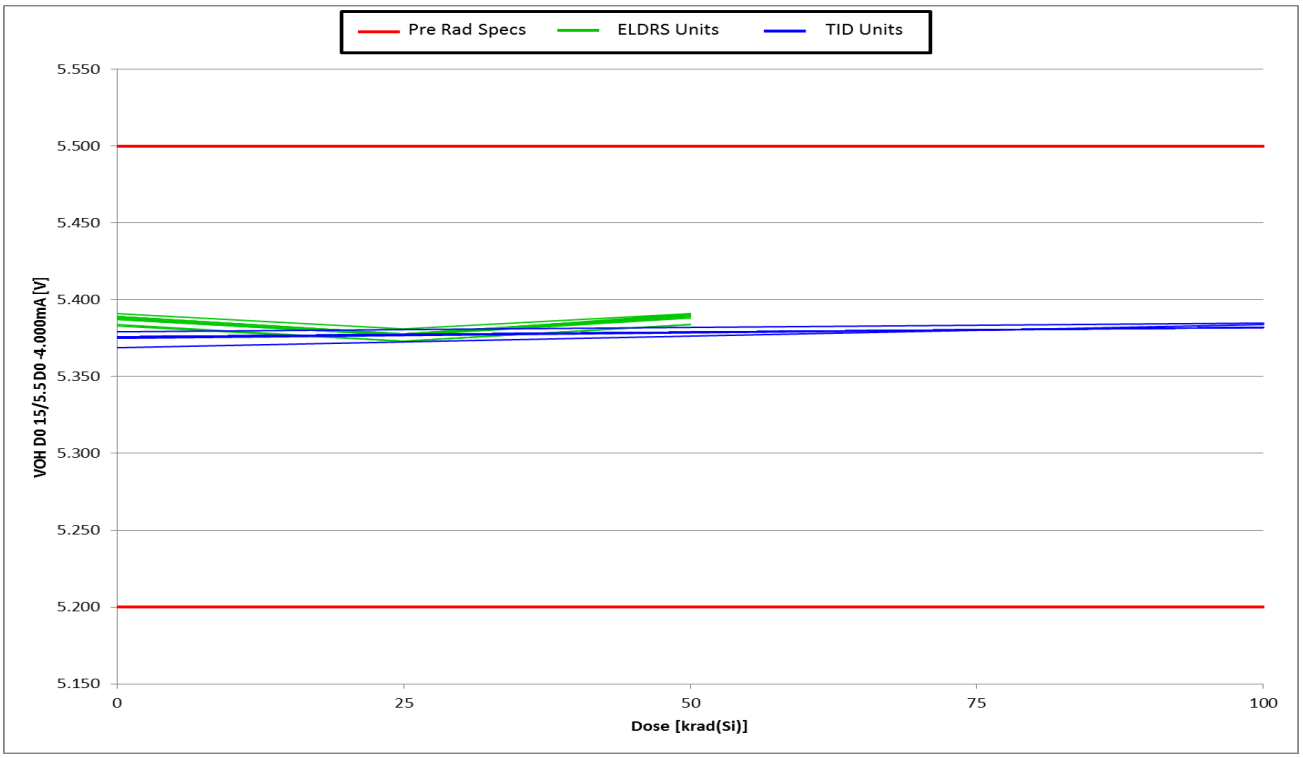
Logic Levels for FPGA Interface I/Os - Logic Output VOH at 100uA at VDD=2.25V



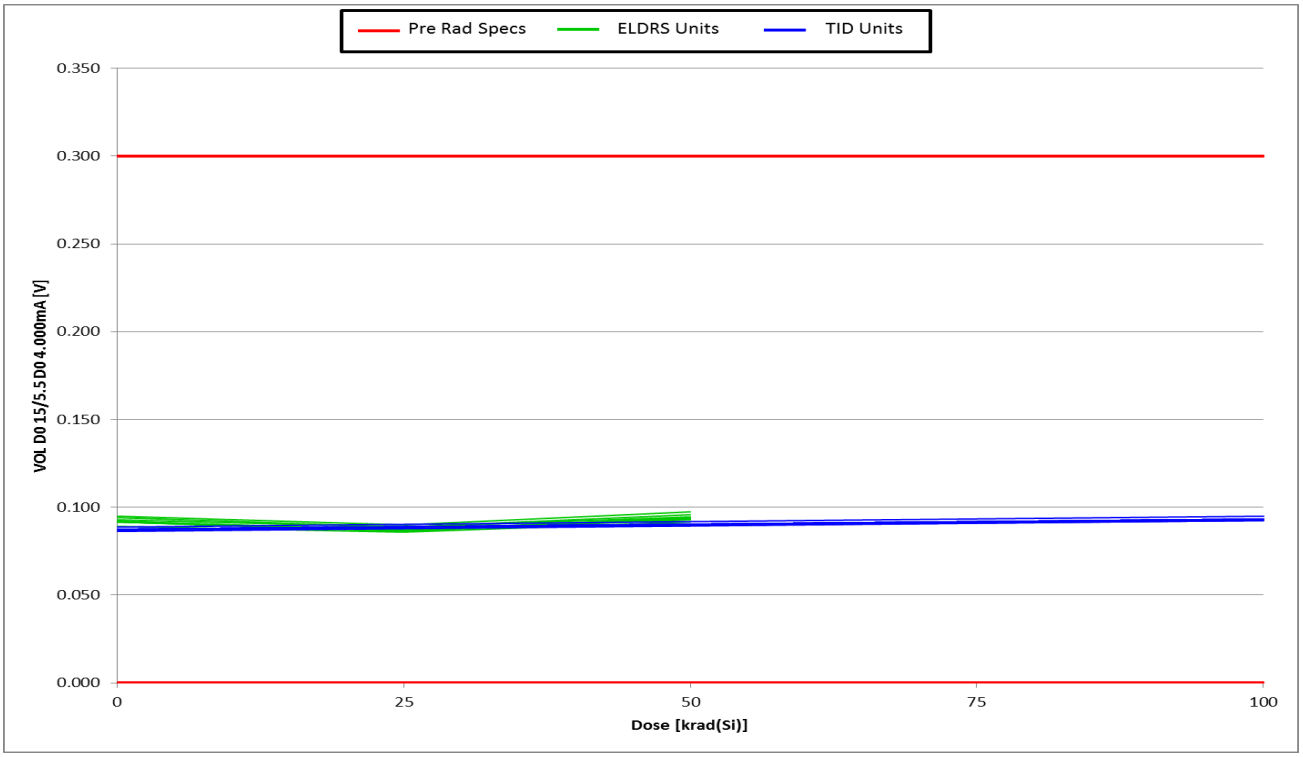
Logic Levels for FPGA Interface I/Os - Logic Output VOL at 100uA at VDD=2.25V



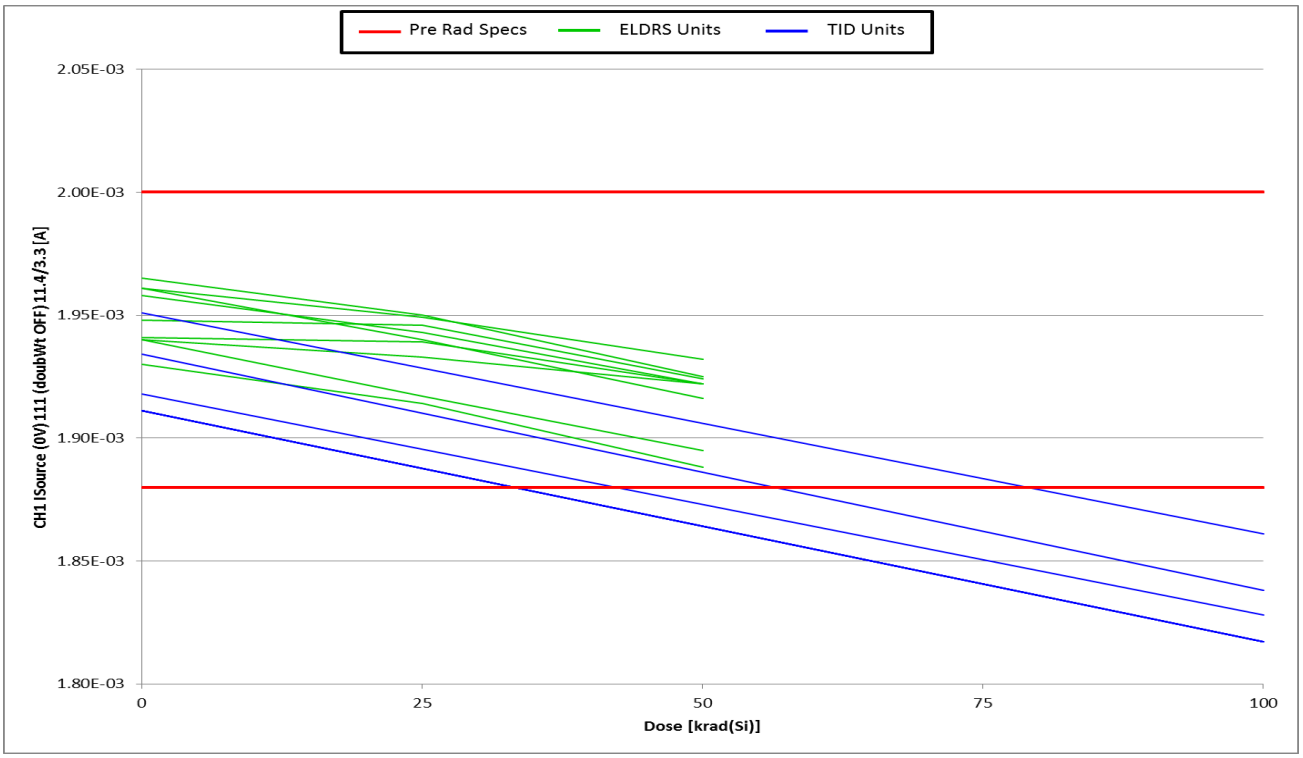
Logic Levels for FPGA Interface I/Os - Logic Output VOH at 100uA at VDD=5.5V



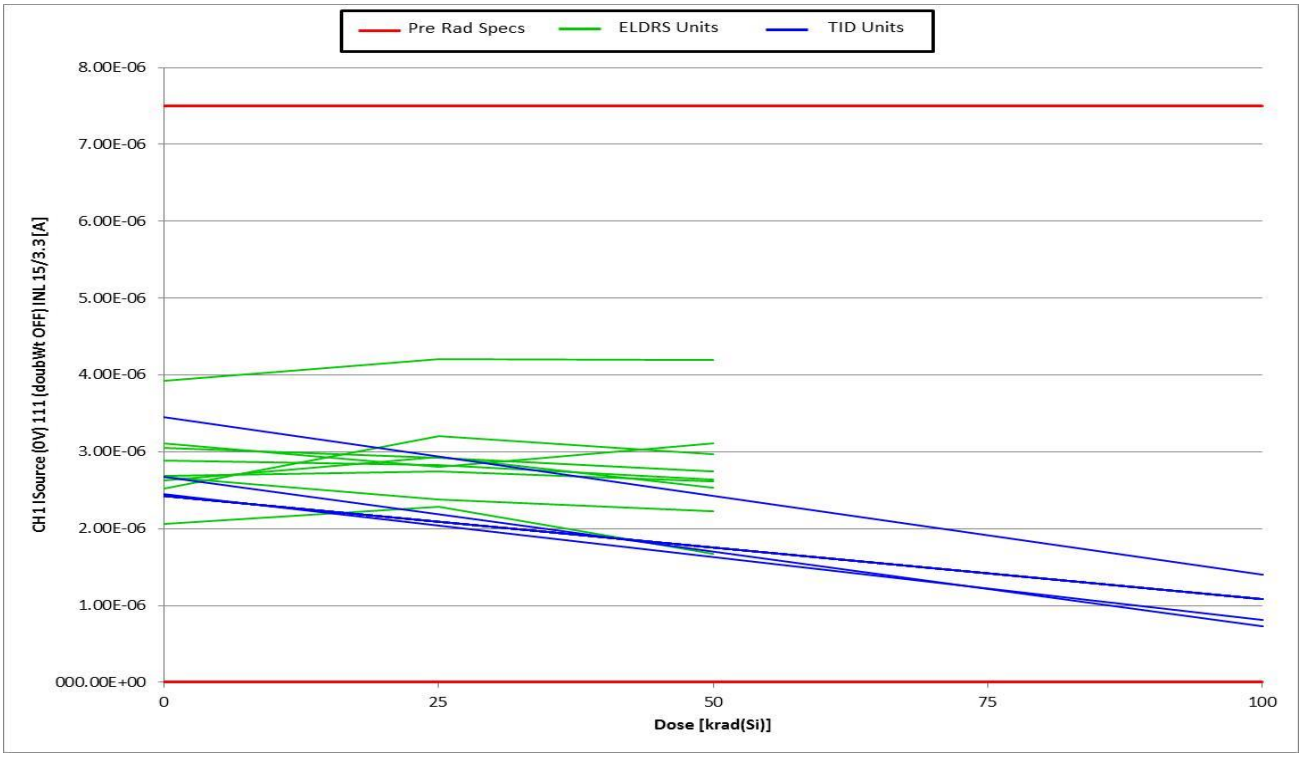
Logic Levels for FPGA Interface I/Os - Logic Output VOL at 100uA at VDD=5.5V



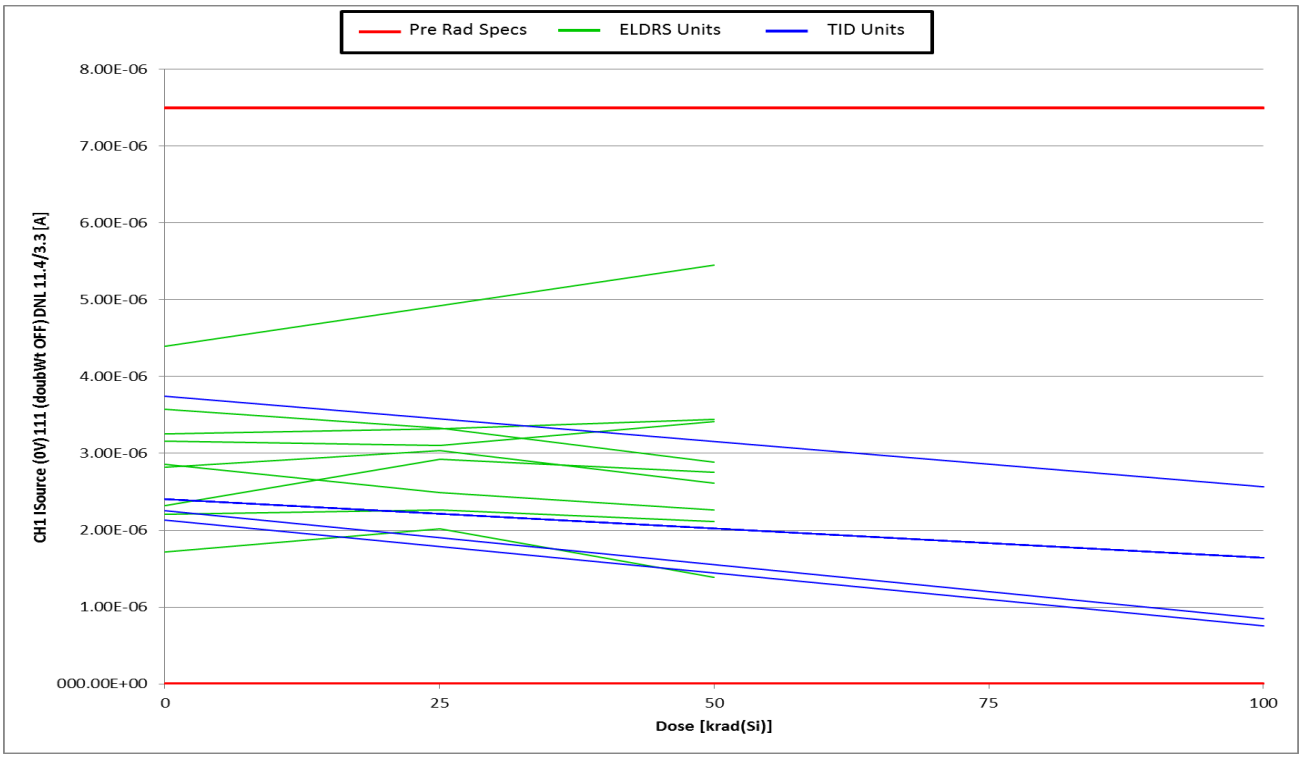
Programmable Current Source Full scale current (doubWt OFF) at VCC=11.4



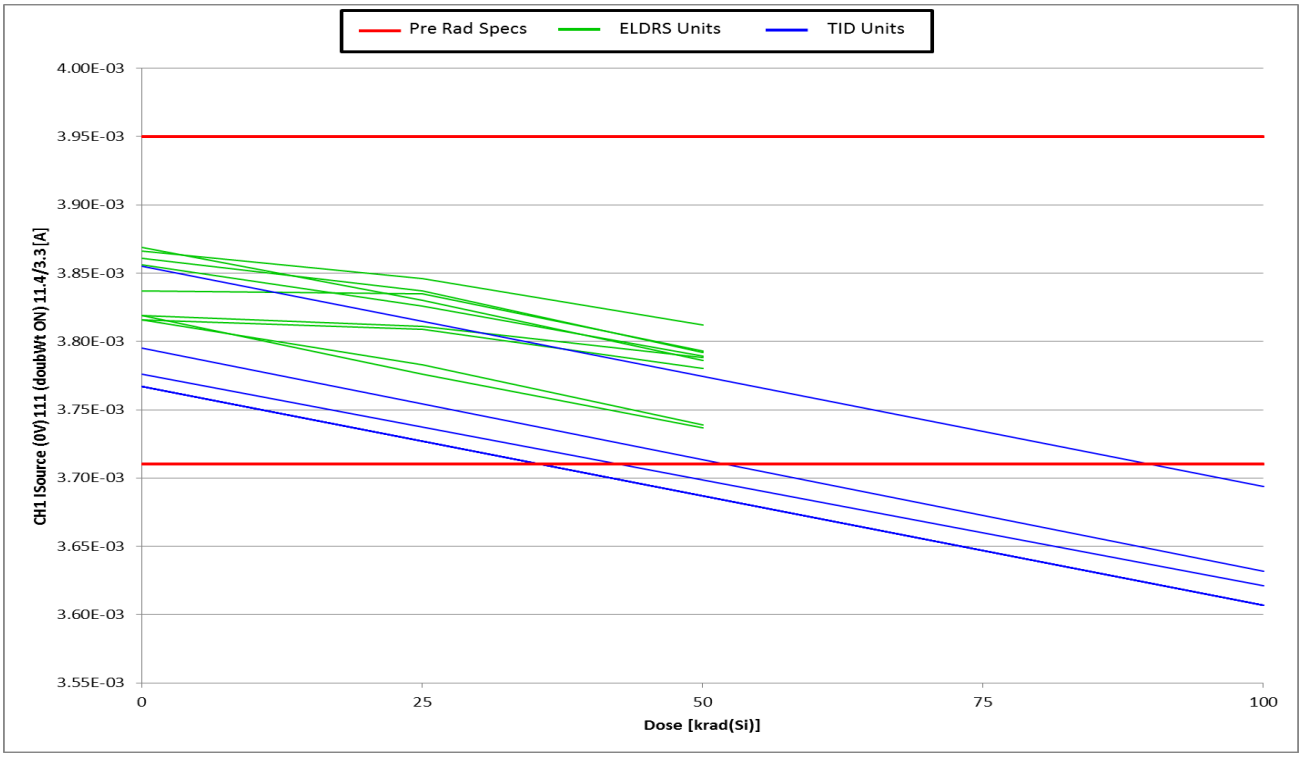
Programmable Current Source INL (doubWt OFF) at VCC=11.4V



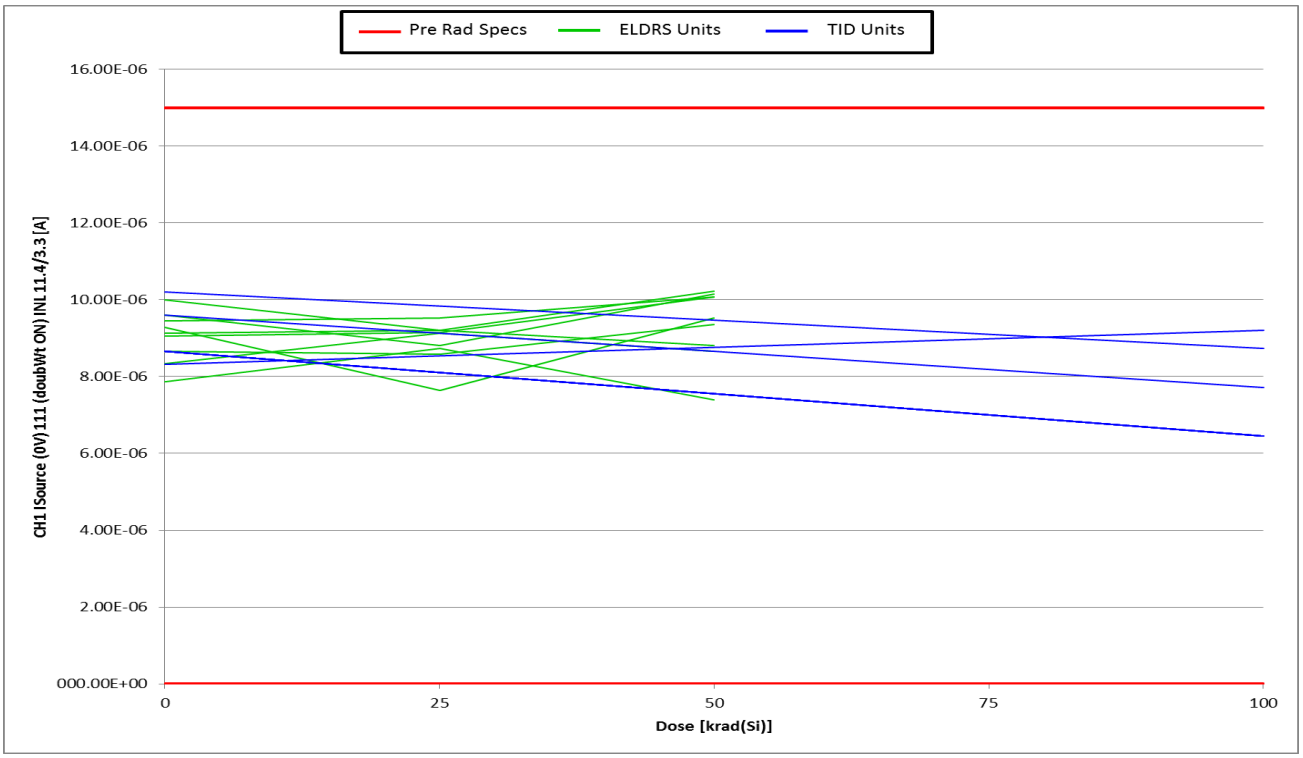
Programmable Current Source DNL (doubWt OFF) at VCC=11.4V



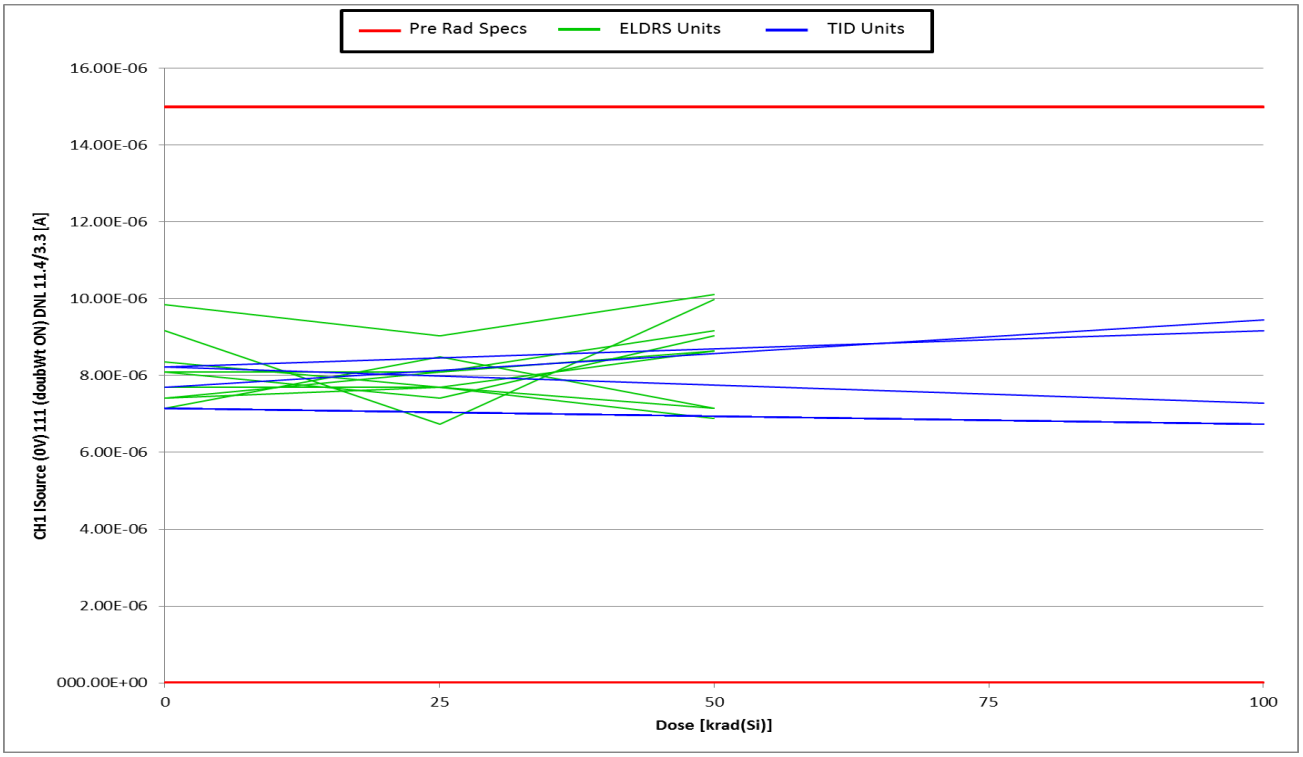
Programmable Current Source Full scale current (doubWt ON) at VCC=11.4V



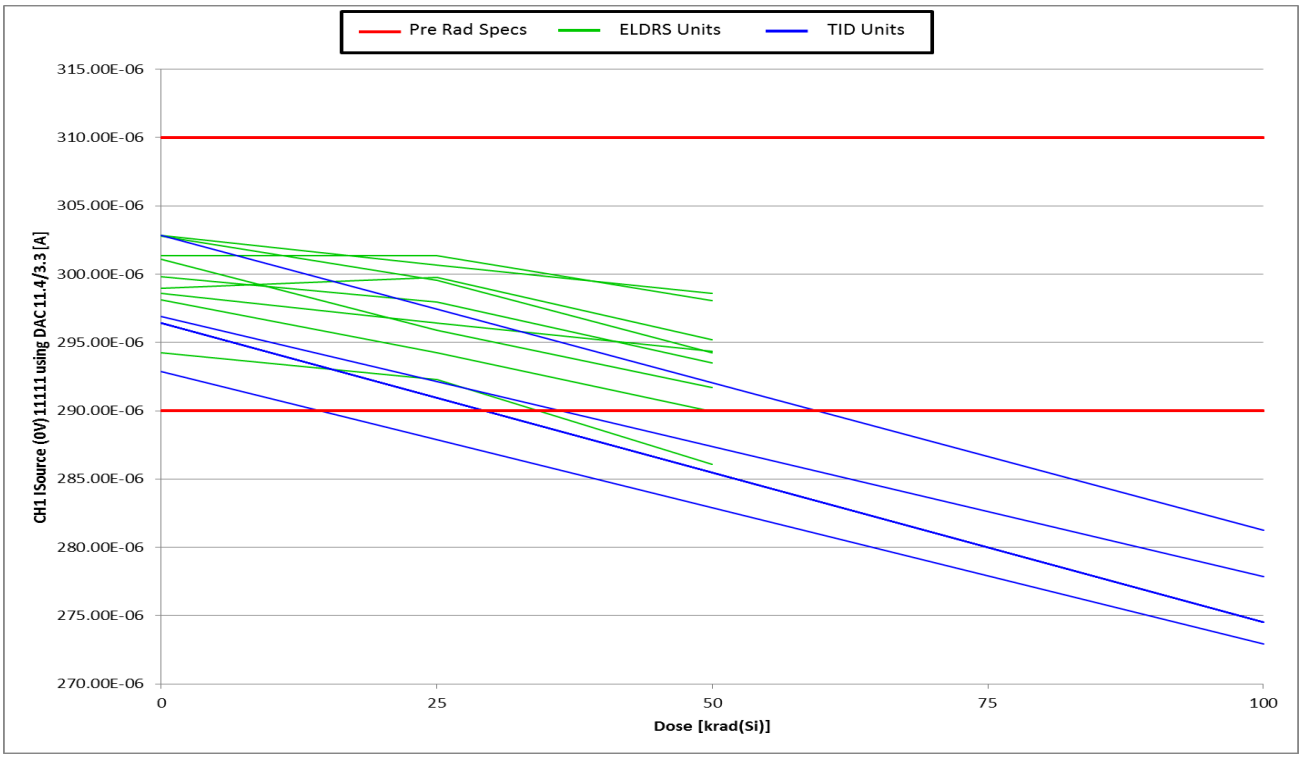
Programmable Current Source INL (doubWt ON) at VCC=11.4V



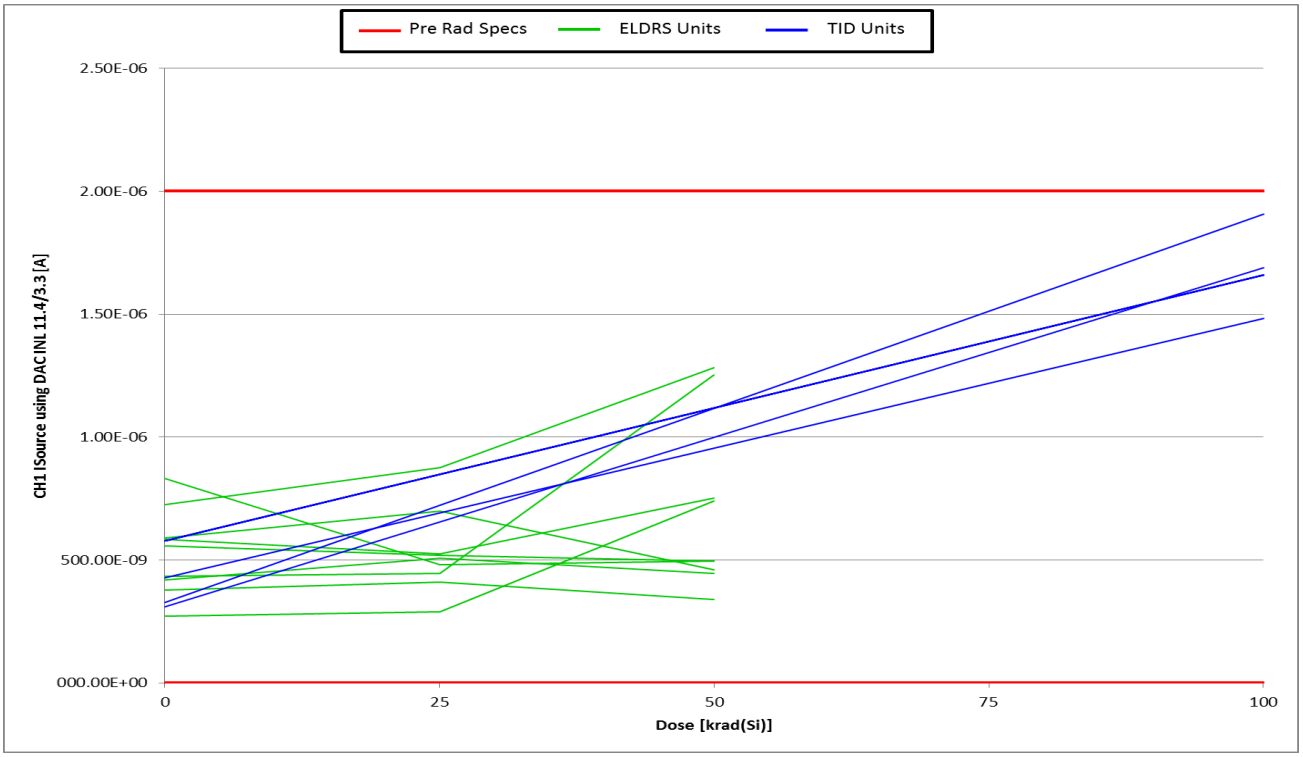
Programmable Current Source DNL (doubWt ON) at VCC=11.4V



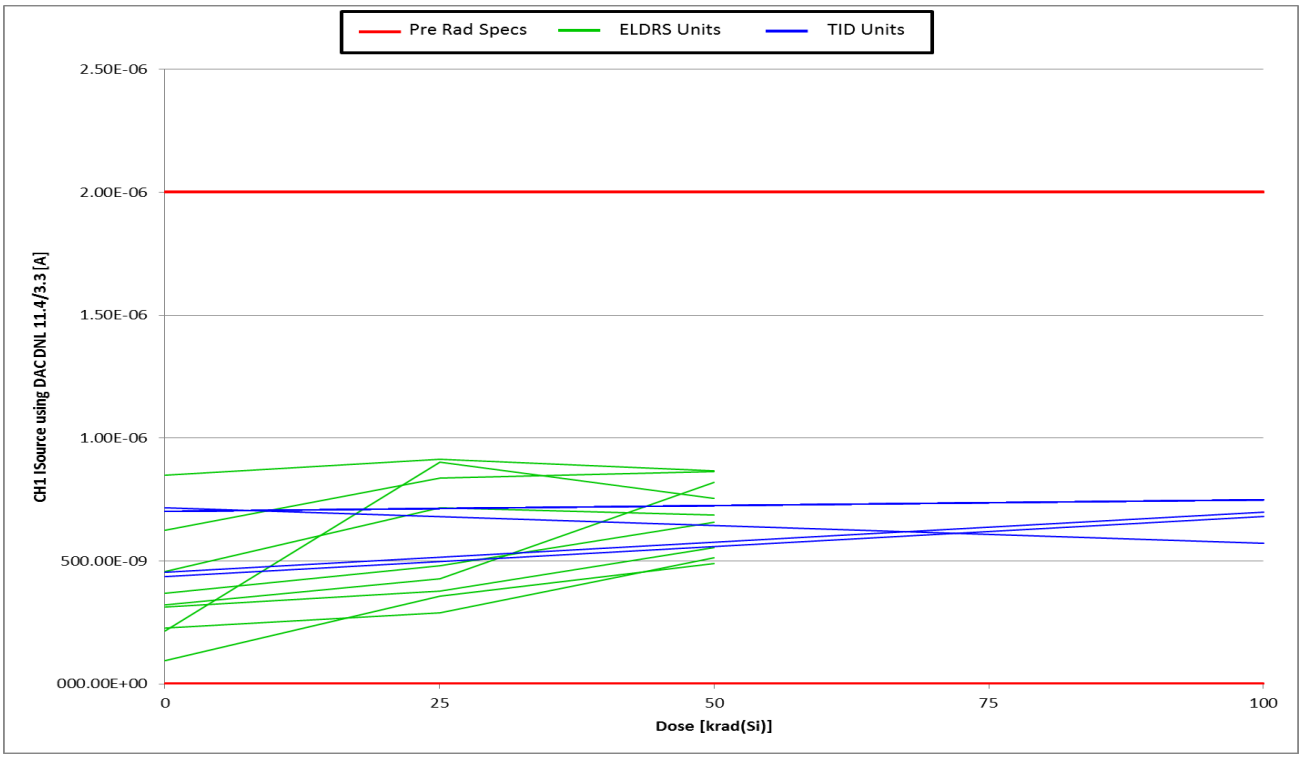
Programmable Current Source at DAC=31 at VCC=11.4V



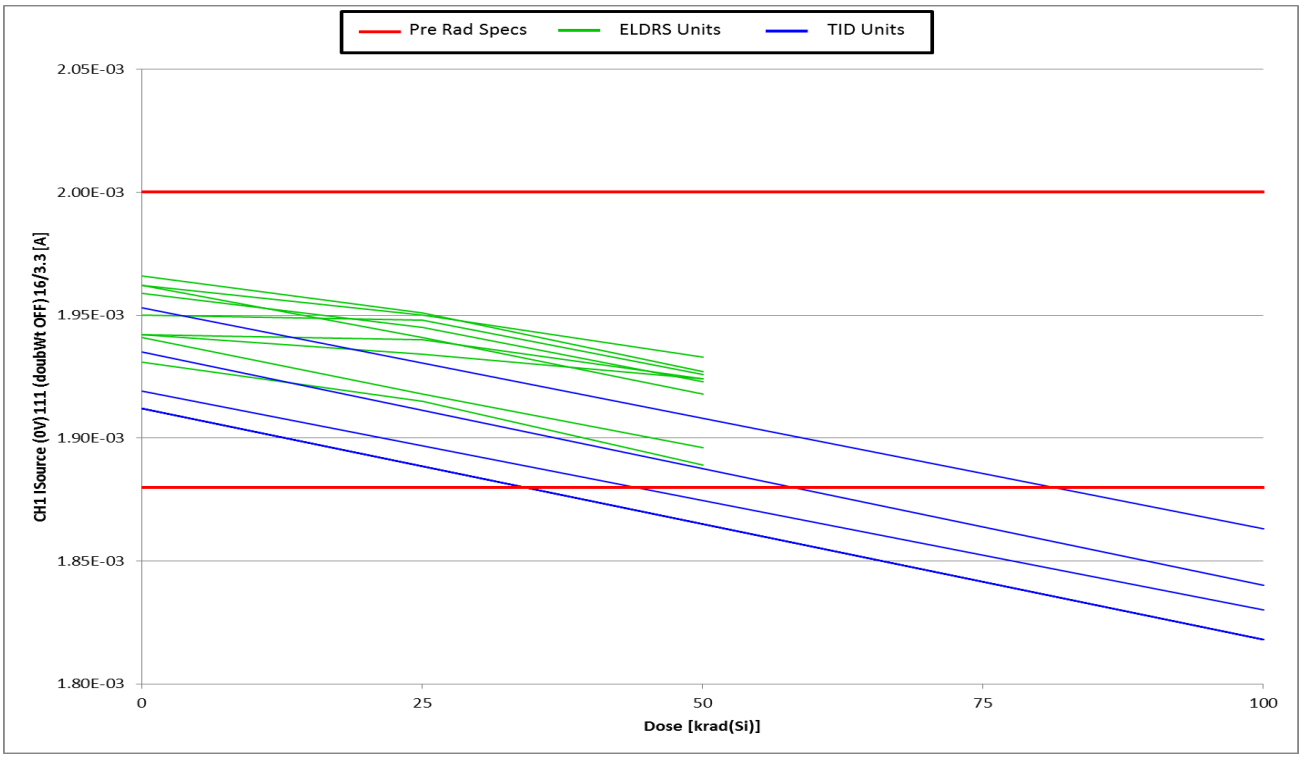
Programmable Current Source INL (DAC) at VCC=11.4V



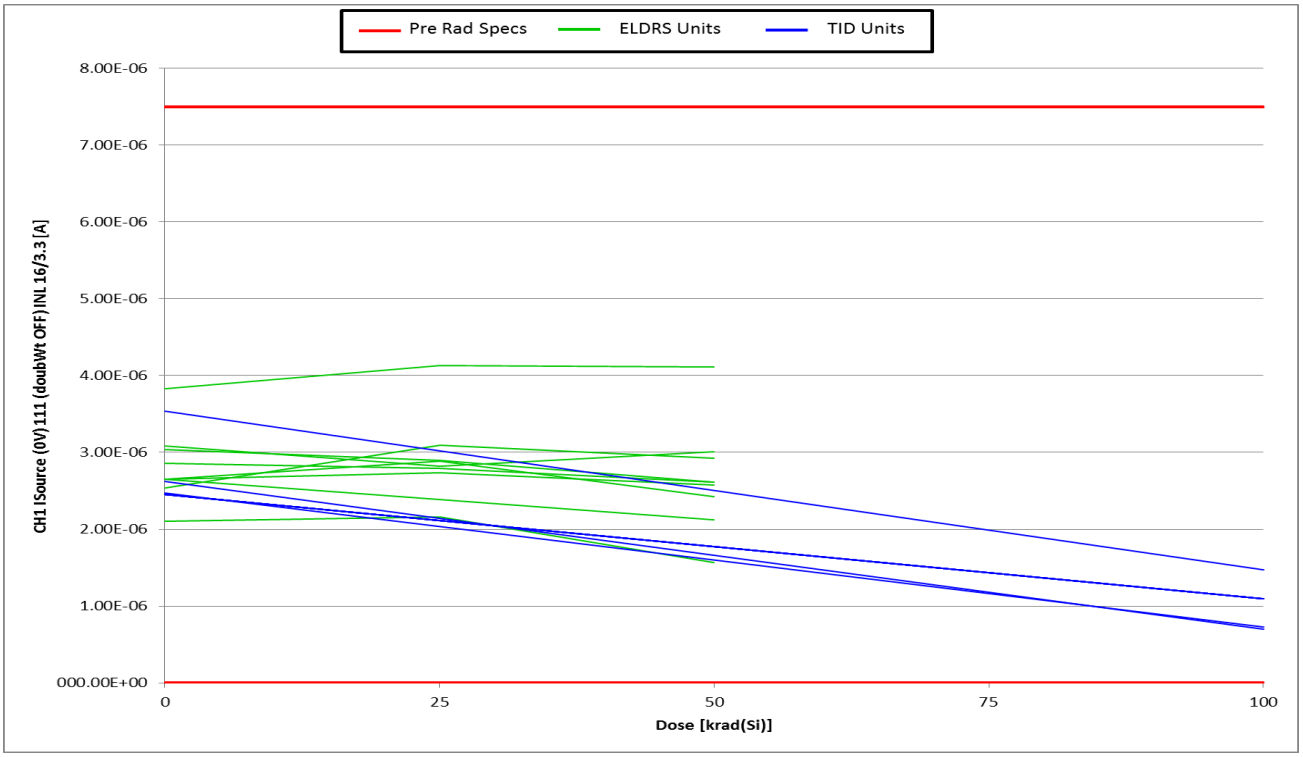
Programmable Current Source DNL (DAC) at VCC=11.4V



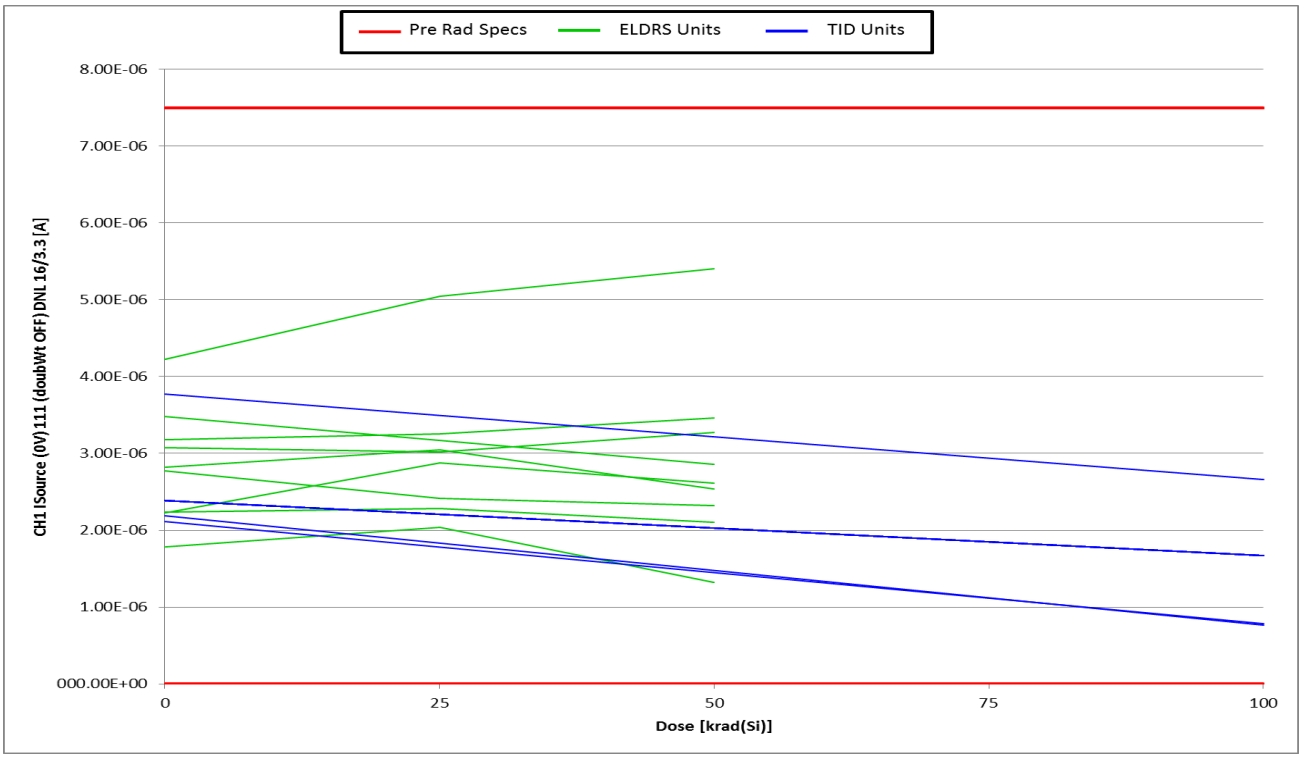
Programmable Current Source Full scale current (doubWt OFF) at VCC=16V



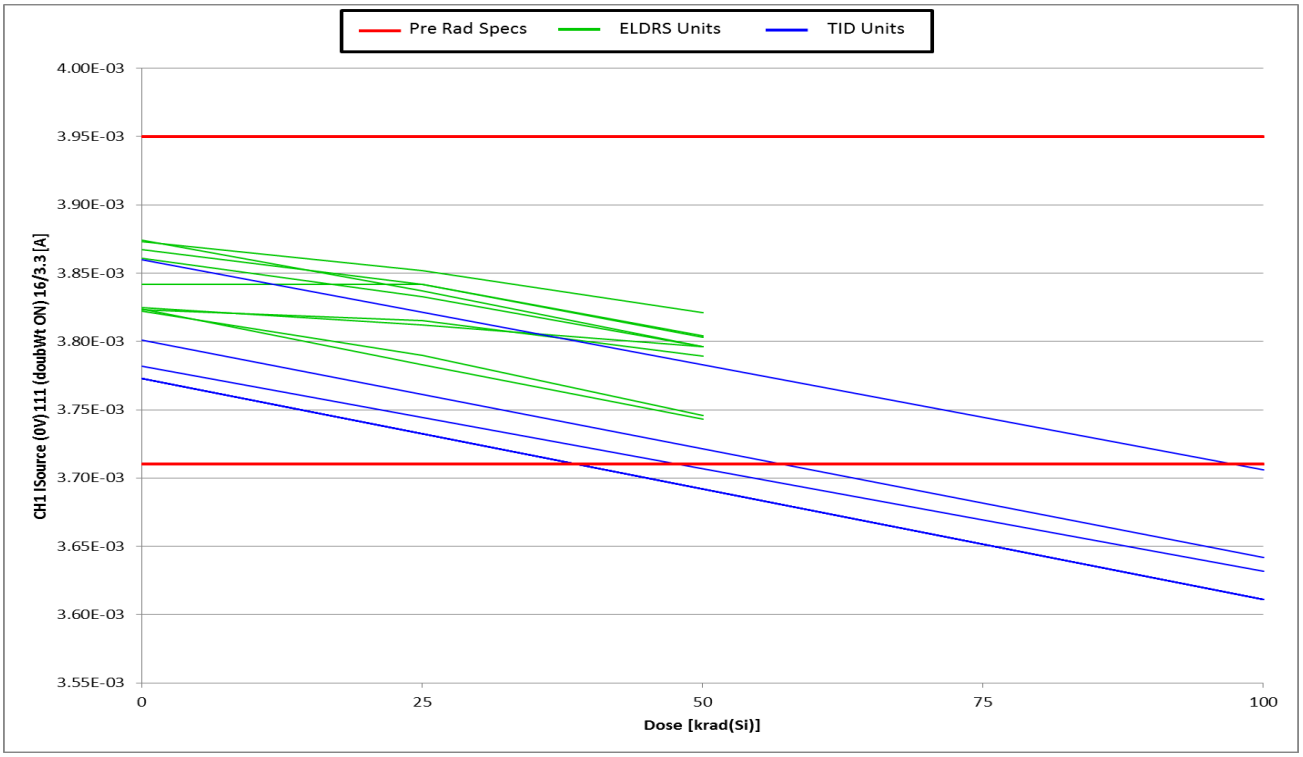
Programmable Current Source INL (doubWt OFF) at VCC=16V



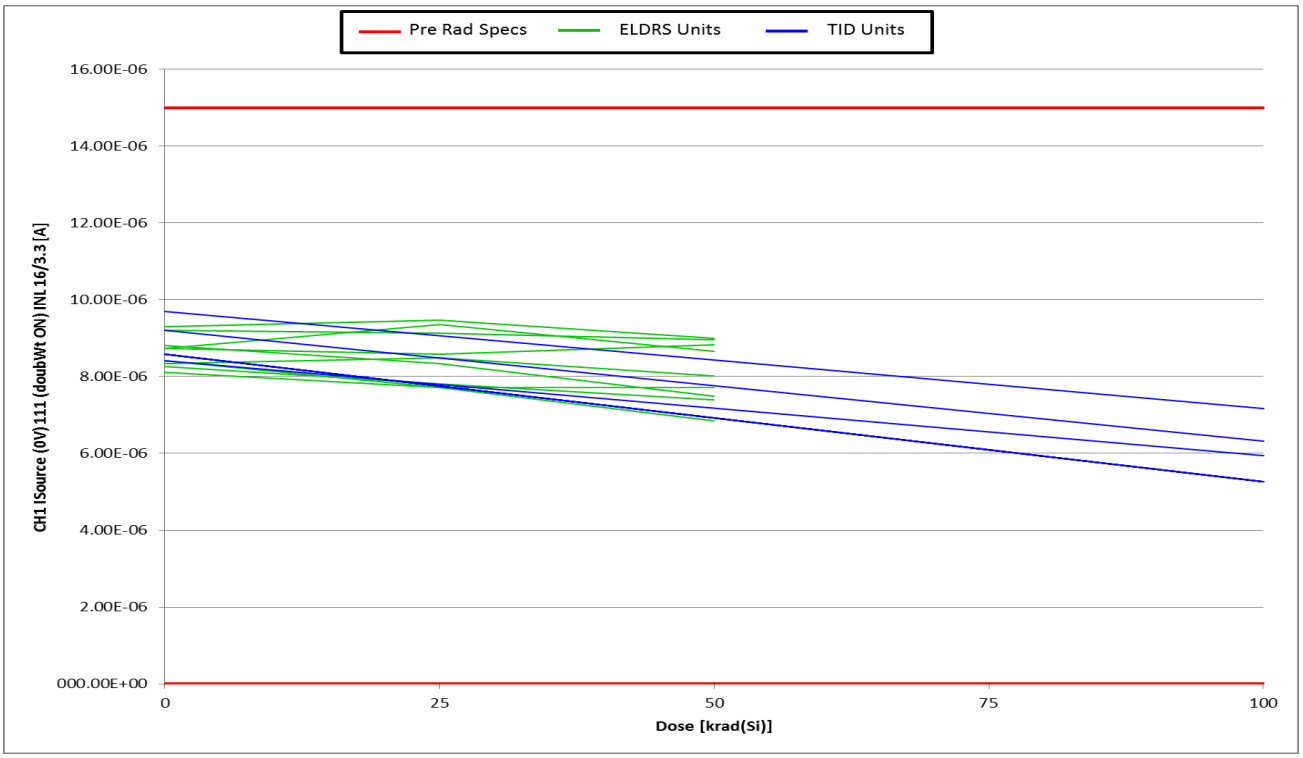
Programmable Current Source DNL (doubWt OFF) at VCC=16V



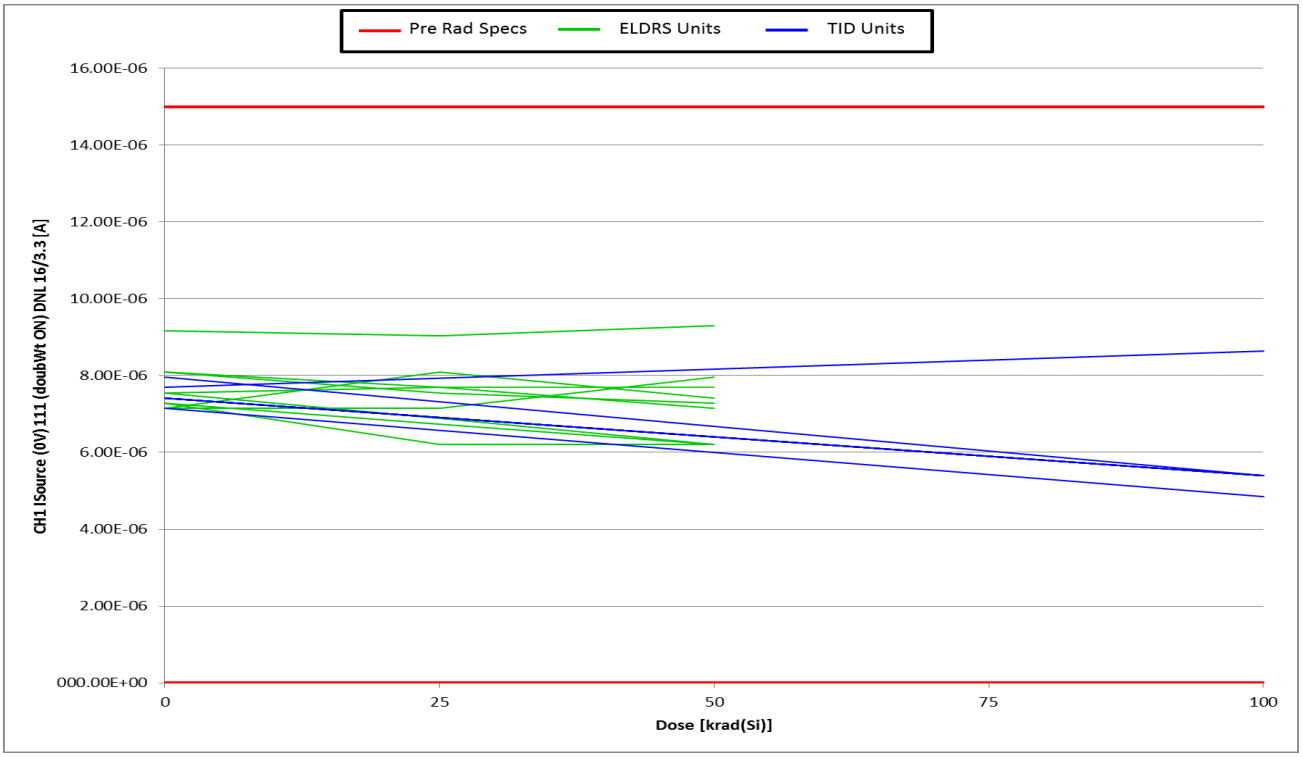
Programmable Current Source Full scale current (doubWt ON) at VCC=16V



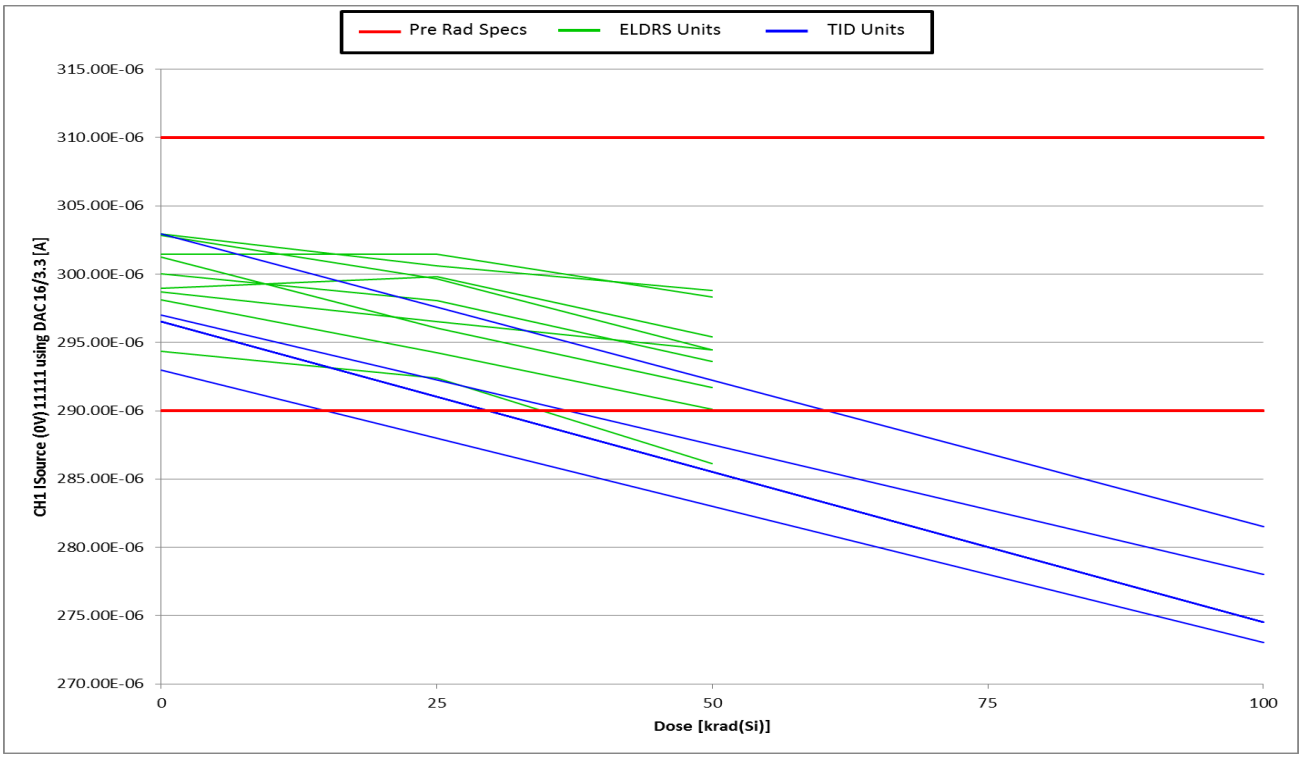
Programmable Current Source INL (doubWt ON) at VCC=16V



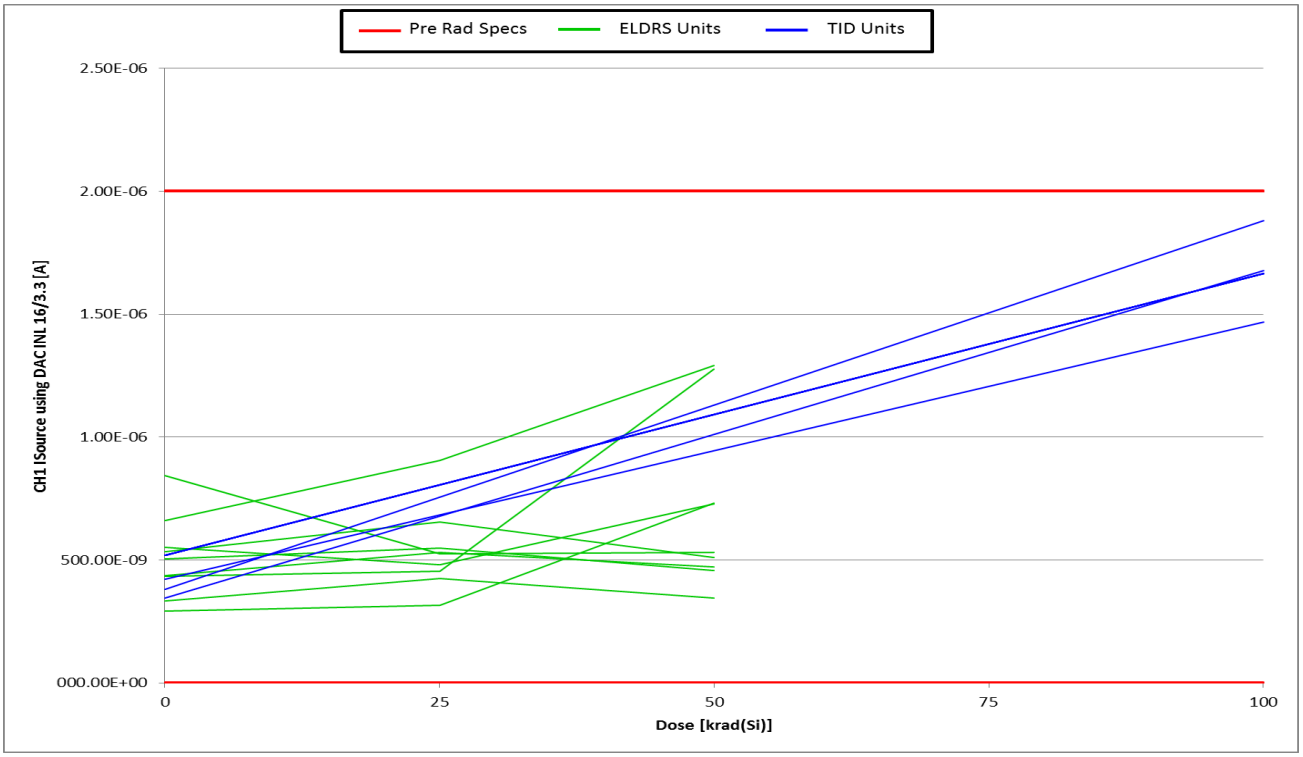
Programmable Current Source DNL (doubWt ON) at VCC=16V



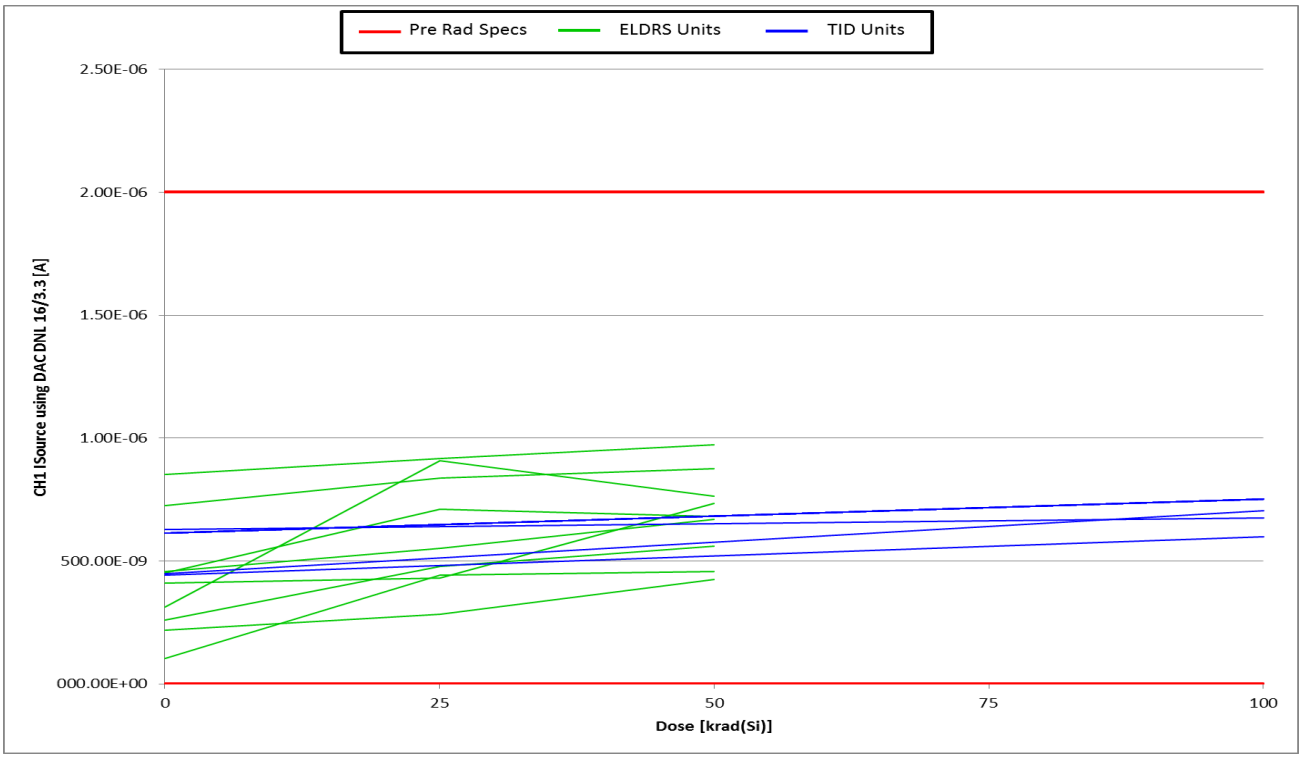
Programmable Current Source at DAC=31 at VCC=16V



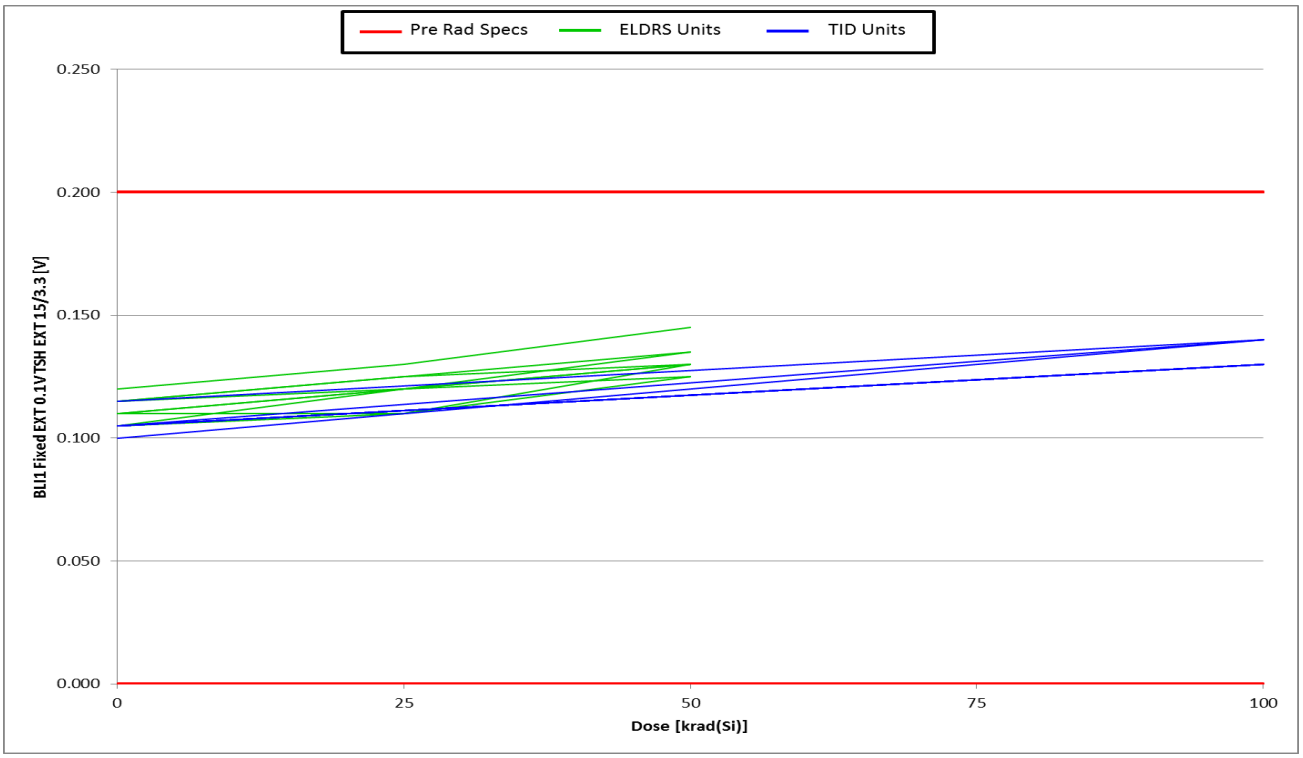
Programmable Current Source INL (DAC) at VCC=16V



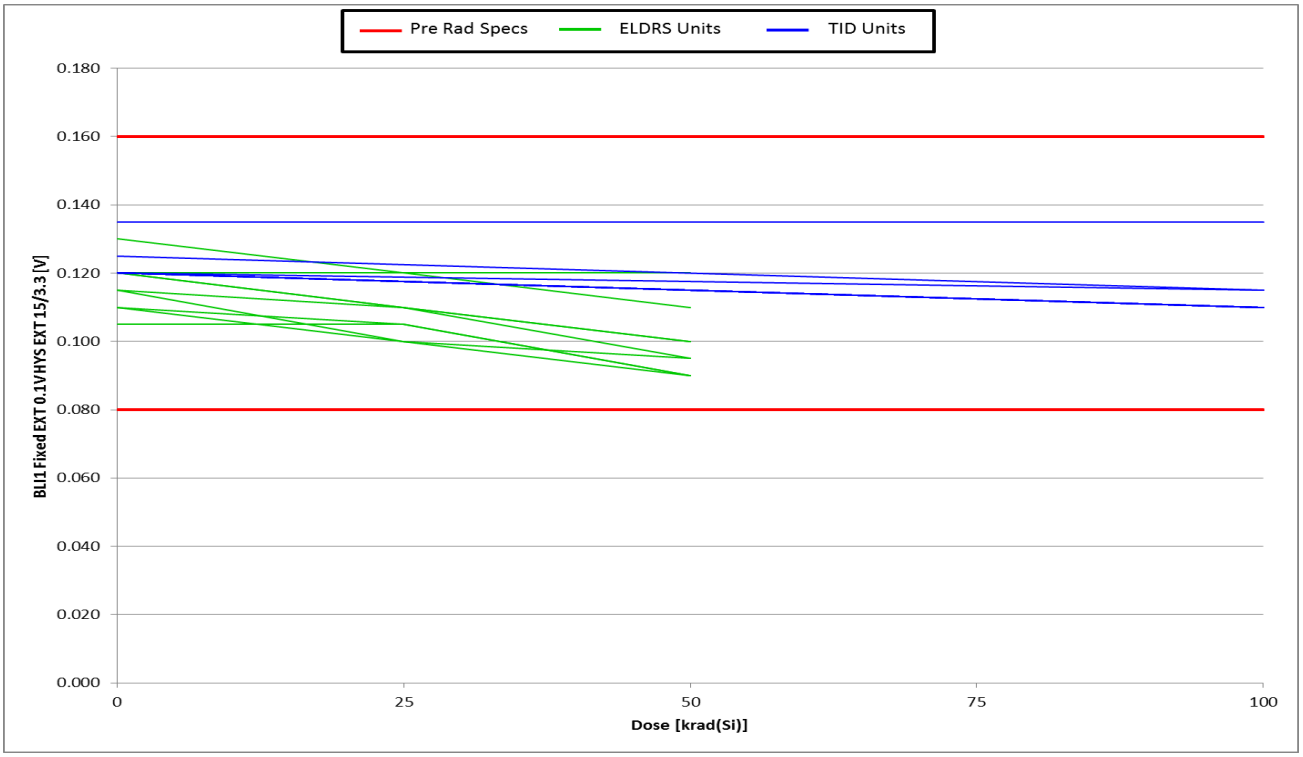
Programmable Current Source DNL (DAC) at VCC=16V



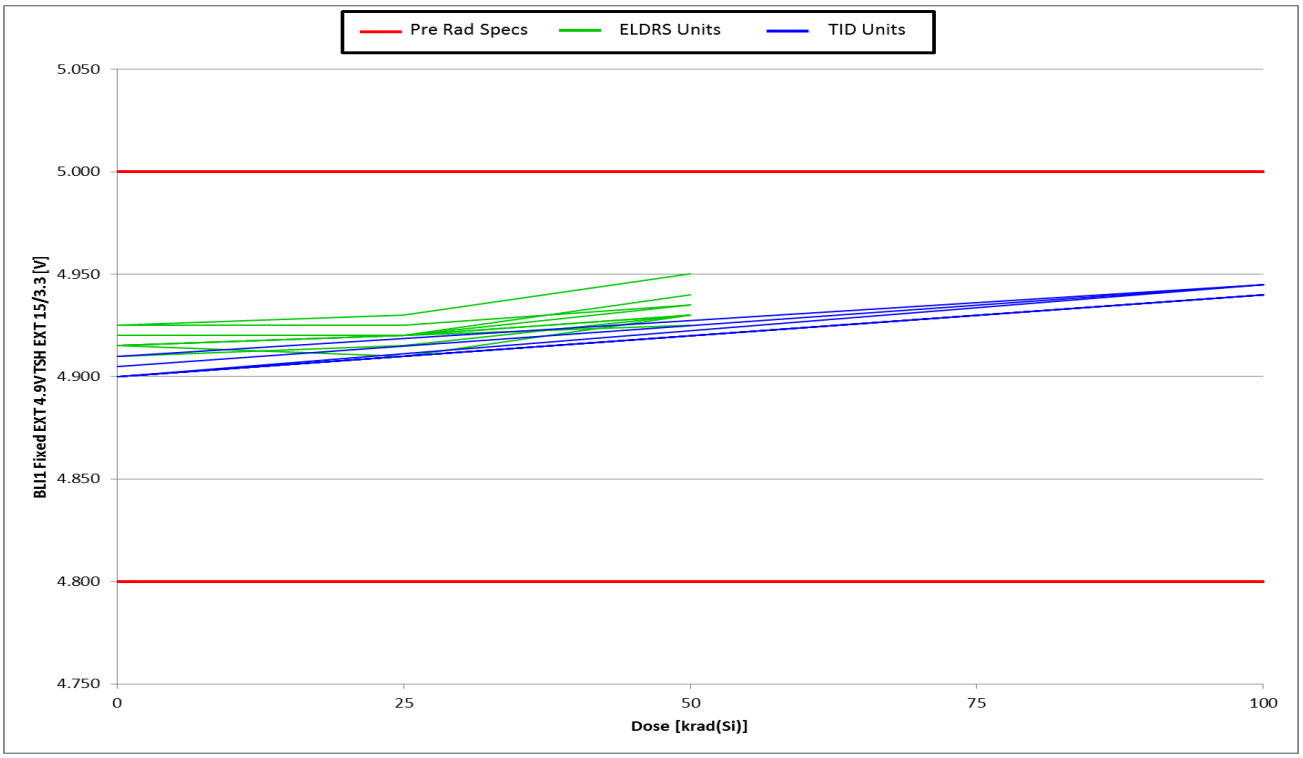
Fixed Threshold Bi-Level Inputs - Threshold – External 0.1V (Rising Voltage) at VCC=15V



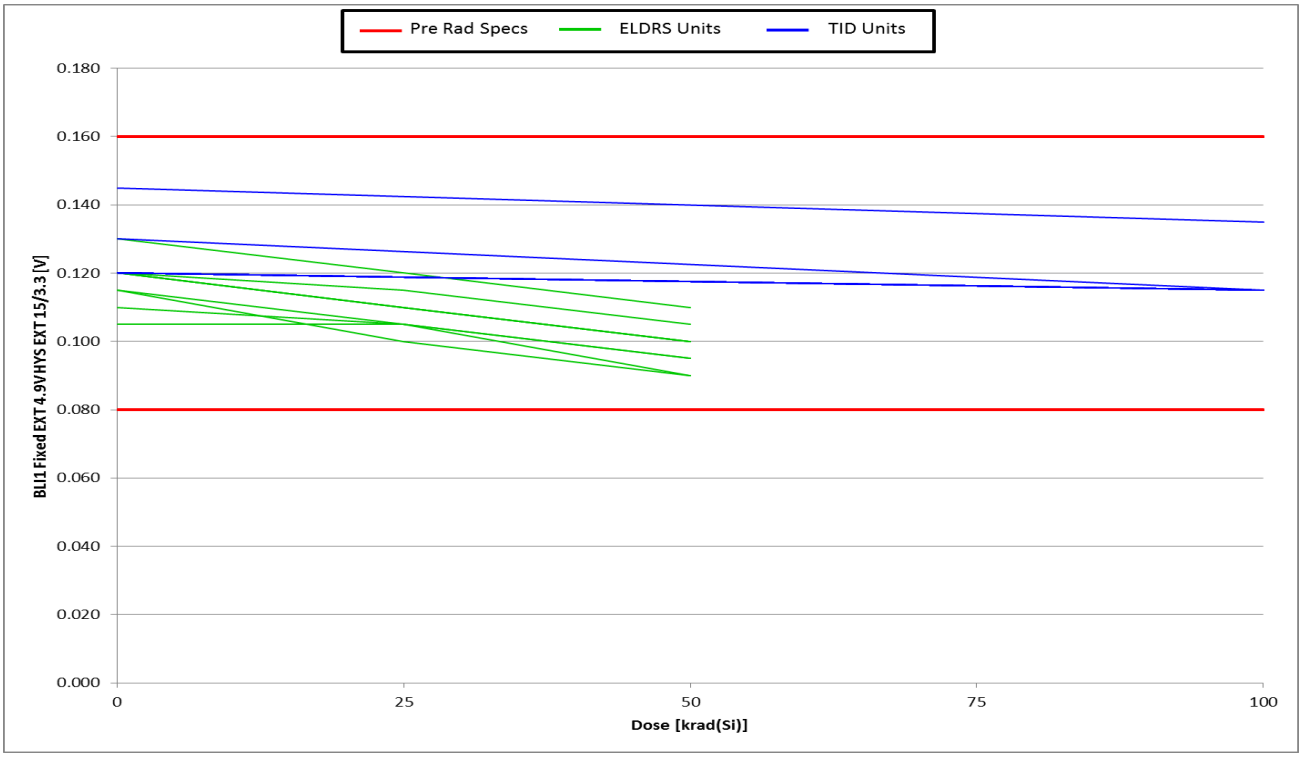
Fixed Threshold Bi-Level Inputs – Threshold Hysteresis – External 0.1V (Rising Voltage) at VCC=15V



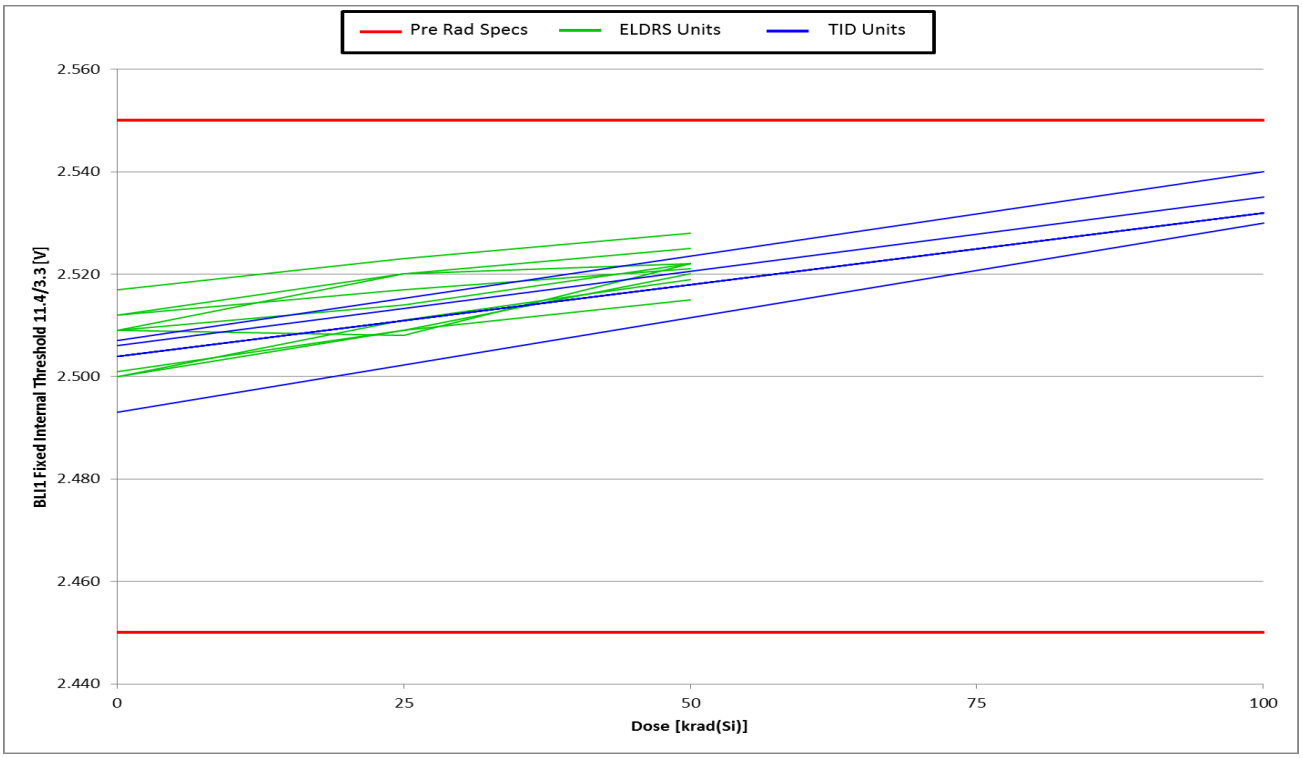
Fixed Threshold Bi-Level Inputs - Threshold – External 4.9V (Rising Voltage) at VCC=15V



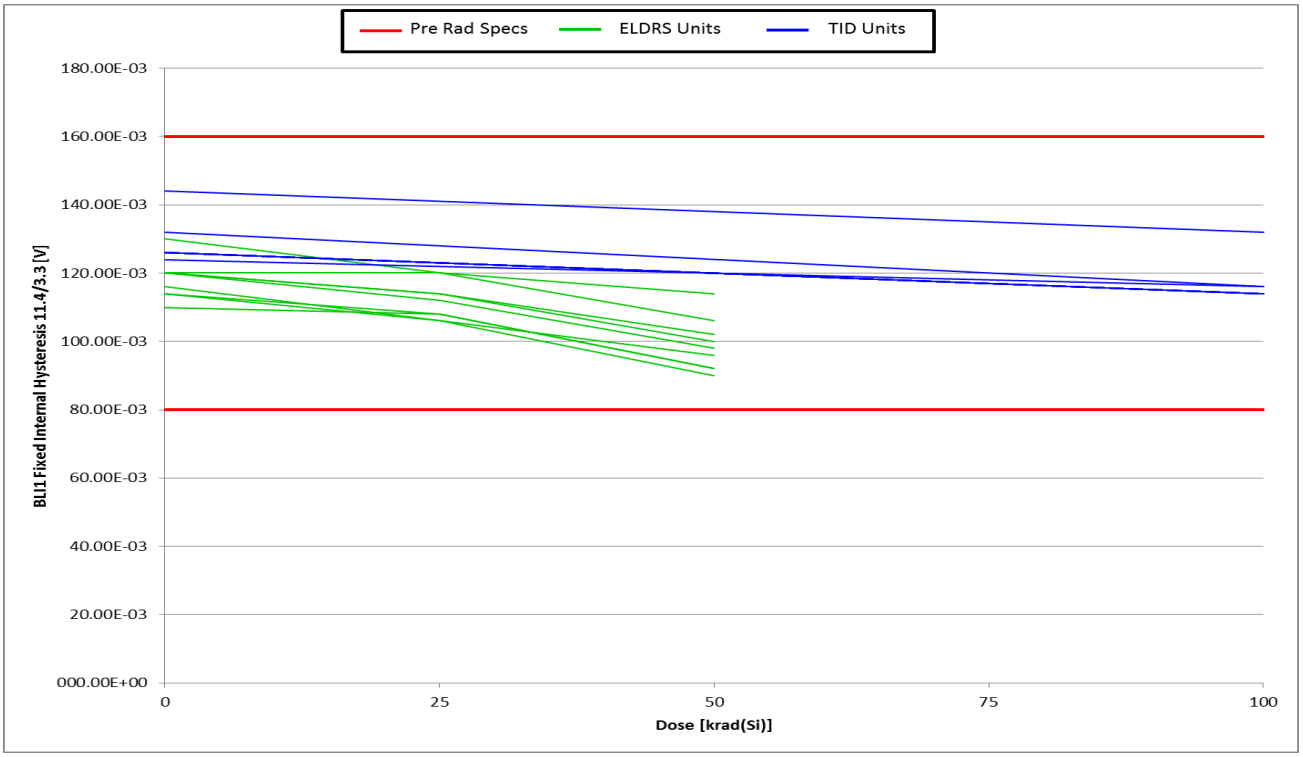
Fixed Threshold Bi-Level Inputs – Threshold Hysteresis – External 4.9V (Rising Voltage) at VCC=15V



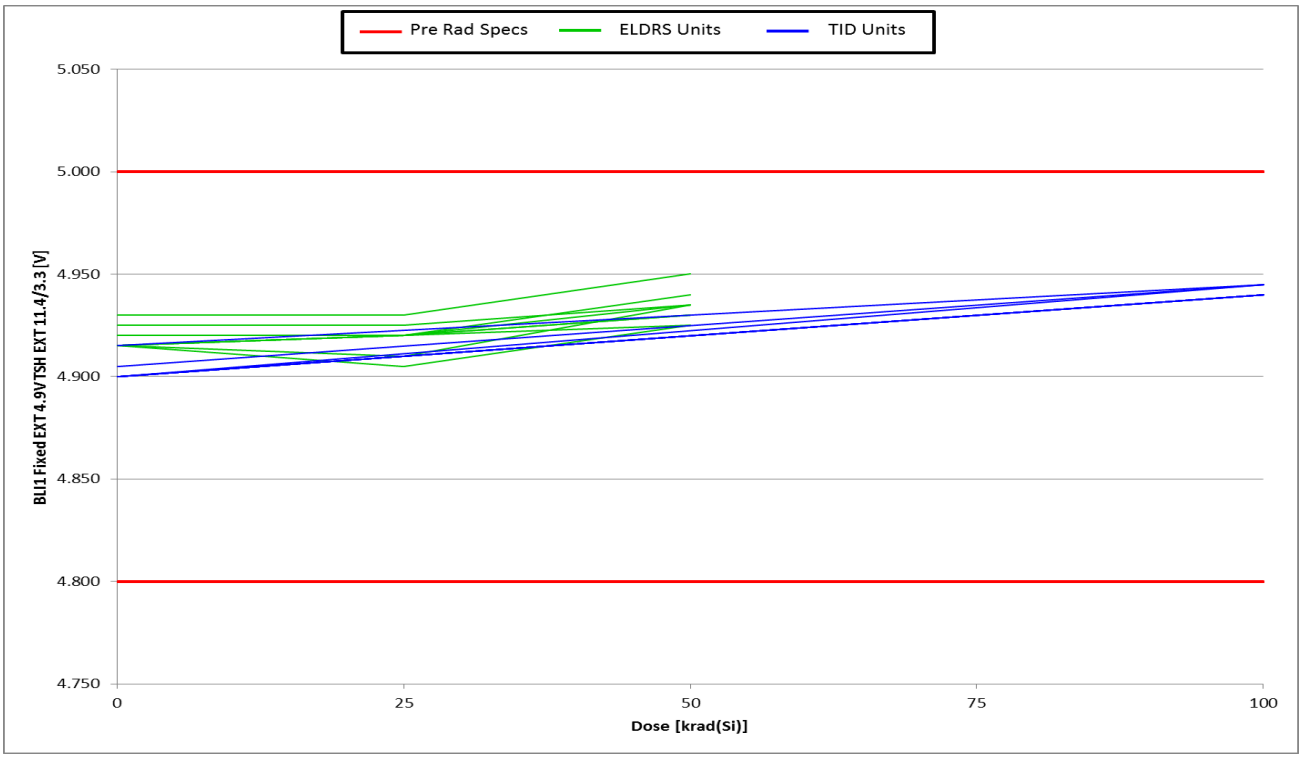
Fixed Threshold Bi-Level Inputs - Threshold – Internal (Rising Voltage) at VCC=11.4V



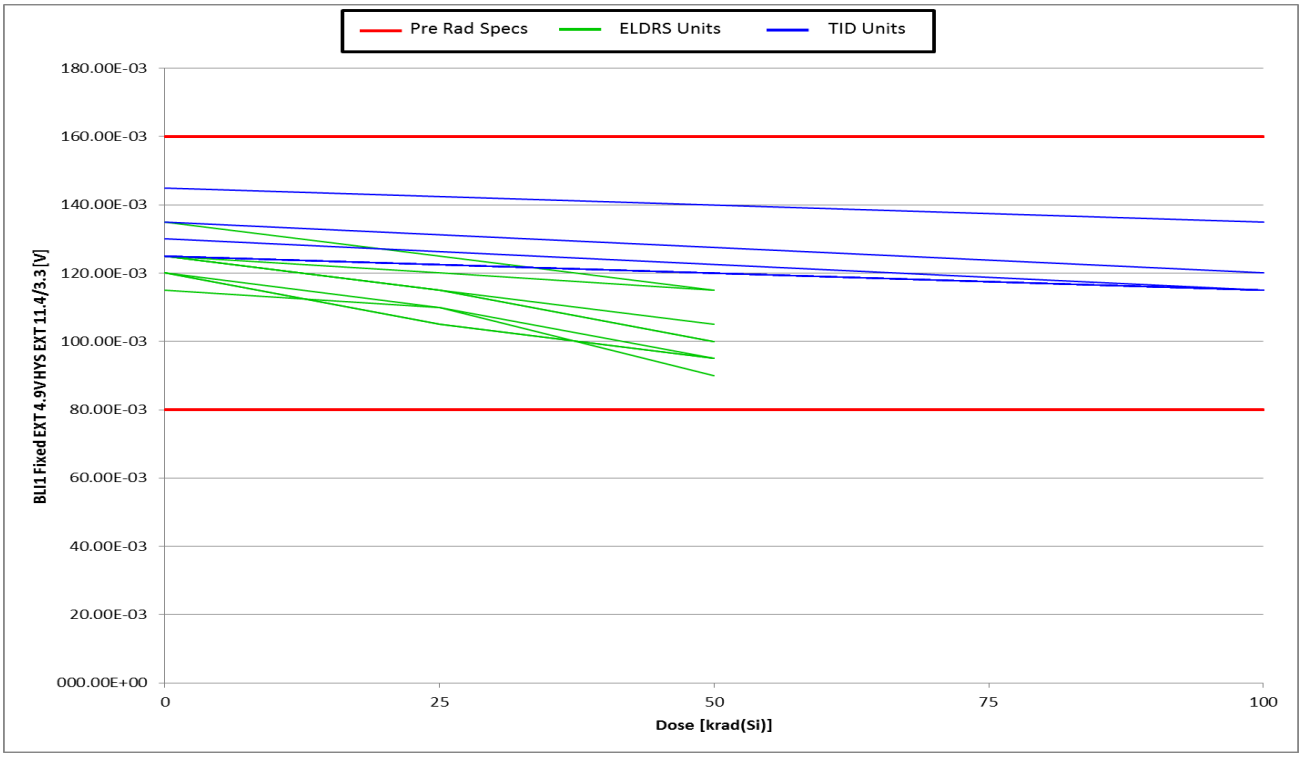
Fixed Threshold Bi-Level Inputs – Threshold Hysteresis – Internal (Rising Voltage) at VCC=11.4V



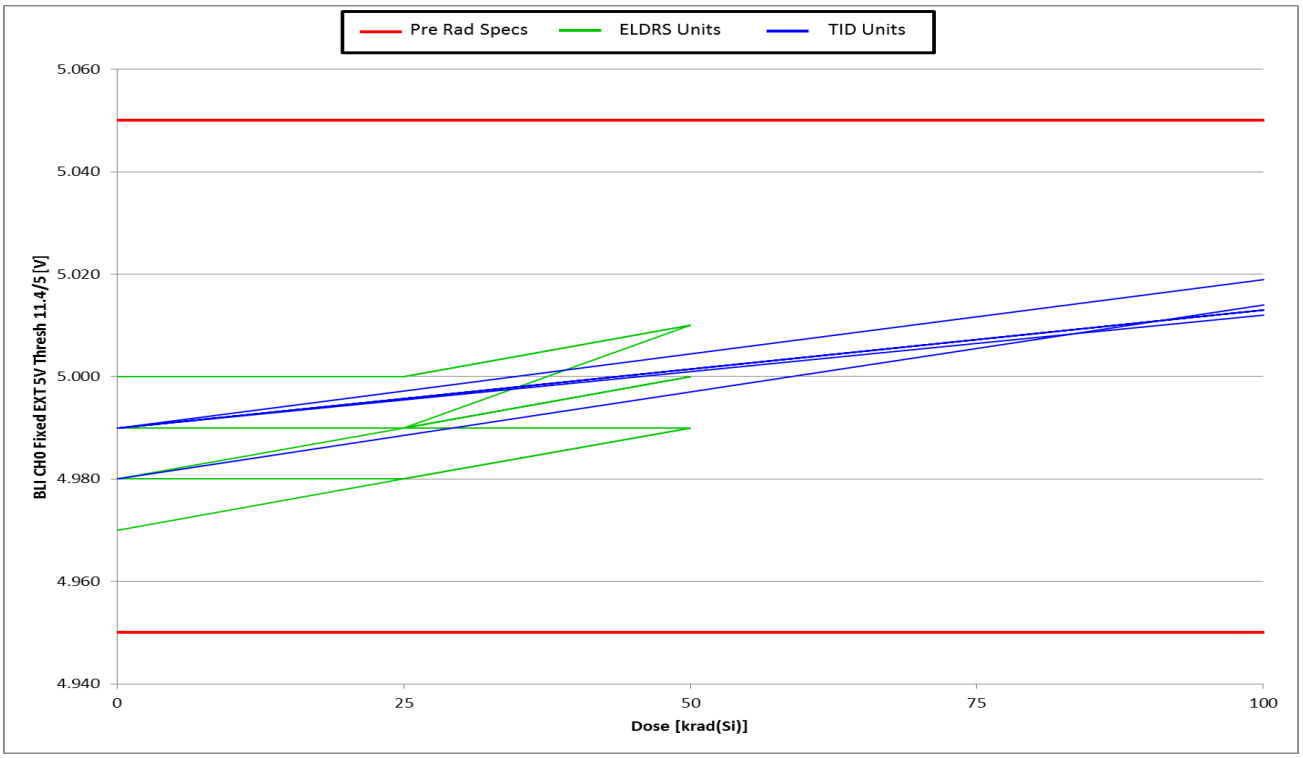
Fixed Threshold Bi-Level Inputs - Threshold – External 4.9V (Rising Voltage) at VCC=11.4V



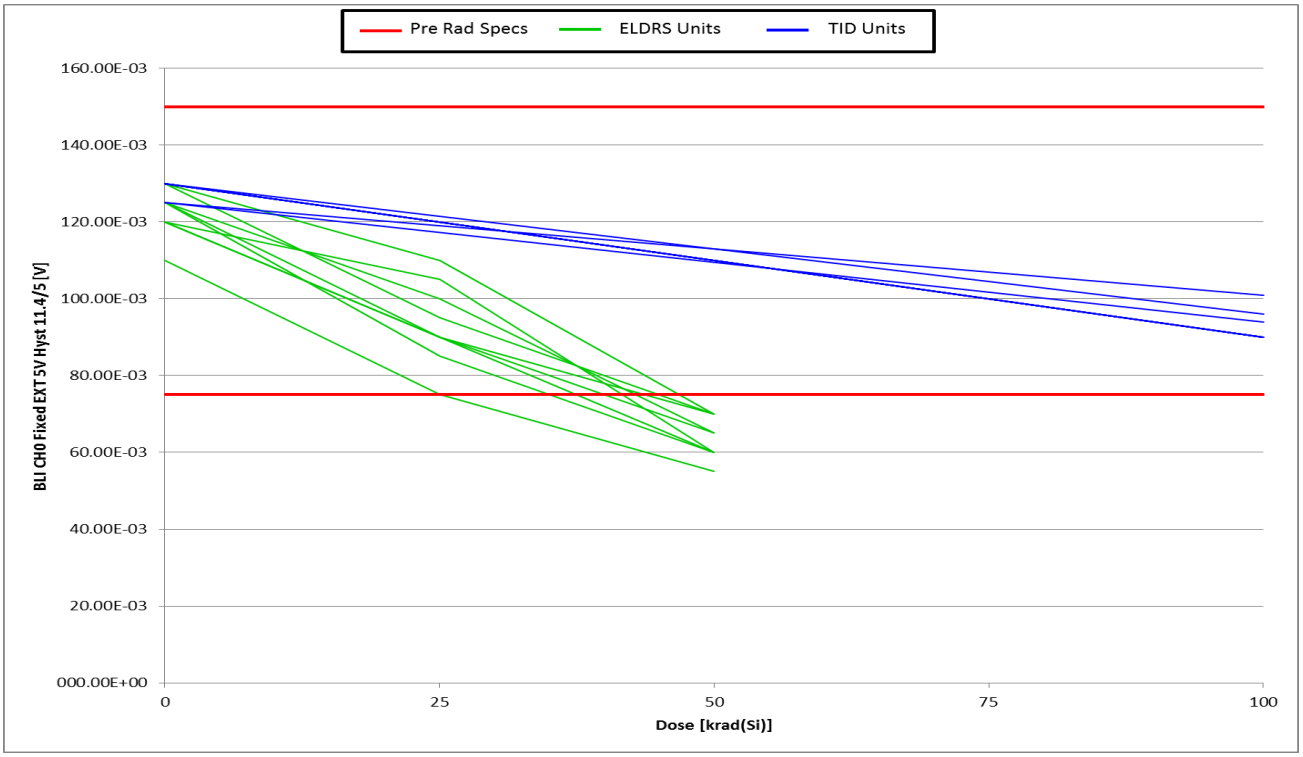
Fixed Threshold Bi-Level Inputs - Threshold Hysteresis – External 4.9V (Rising Voltage) at VCC=11.4V



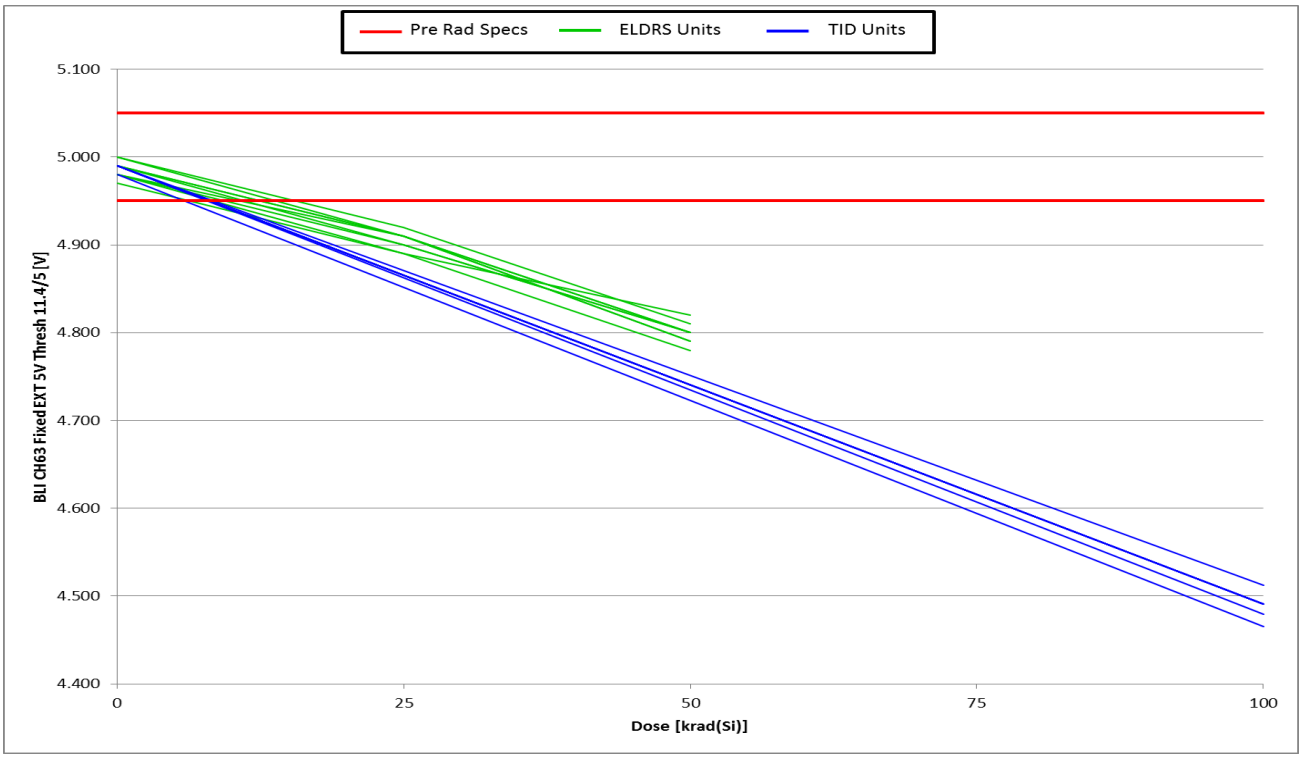
Adj threshold Bi-level MUX Threshold at DAC Max Output (If input >=0V during exposure) at VCC=11.4V



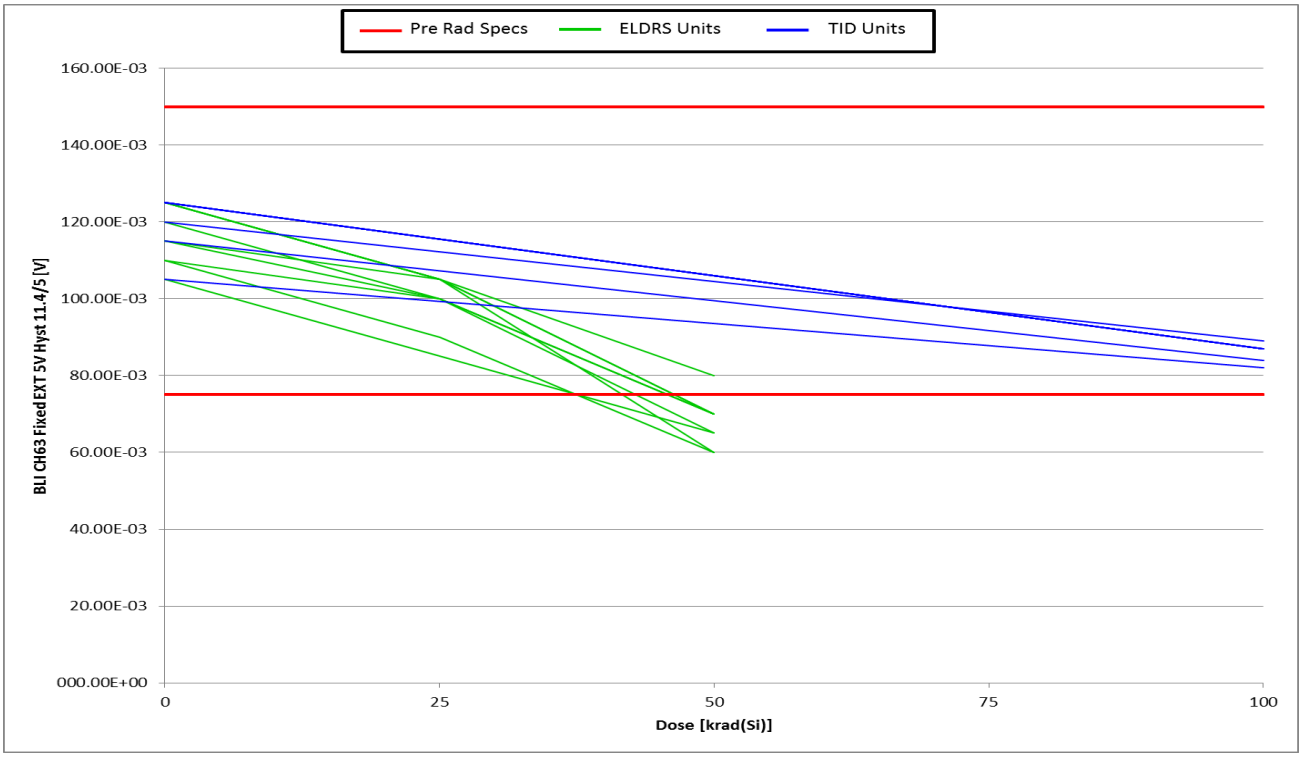
Adj threshold Bi-level MUX Hysteresis at DAC Max Output (If input >=0V during exposure) at VCC=11.4V



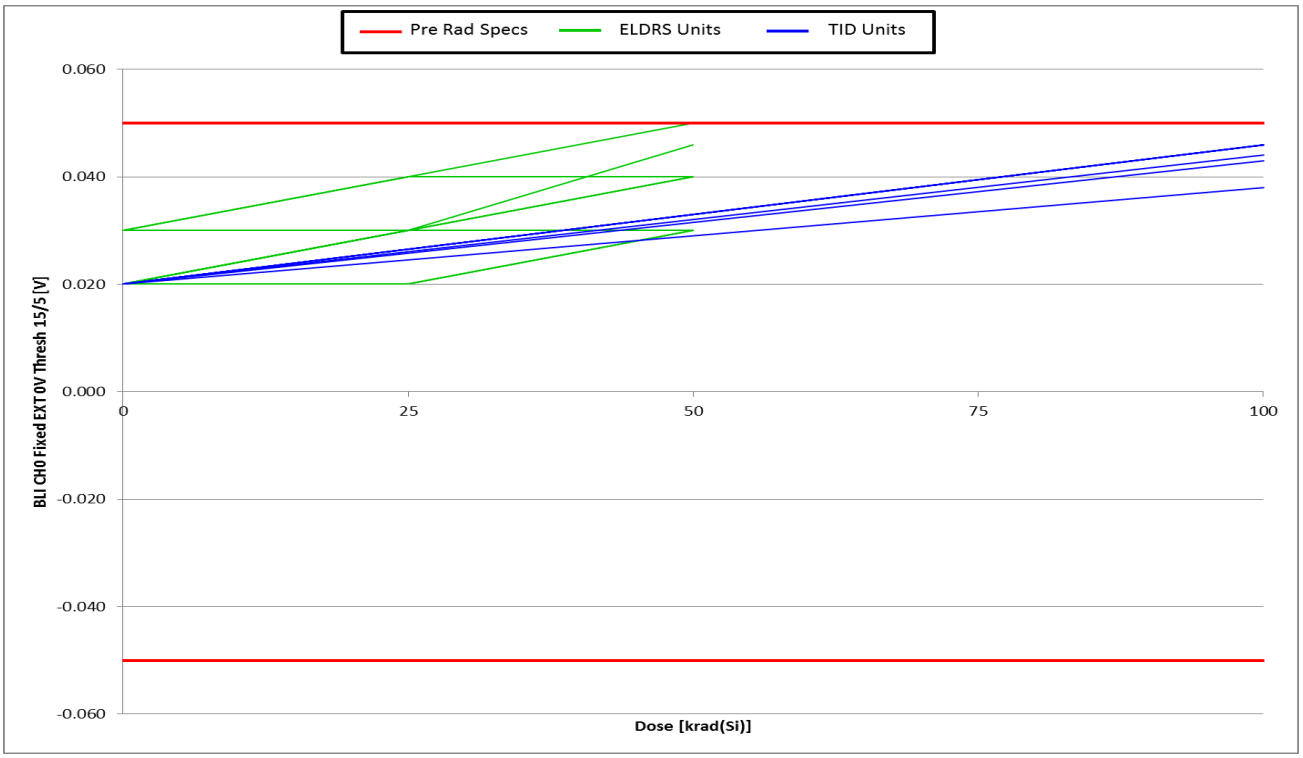
Adj threshold Bi-level MUX Threshold at DAC Max Output (If input = VEE/2 during exposure) at VCC=11.4V



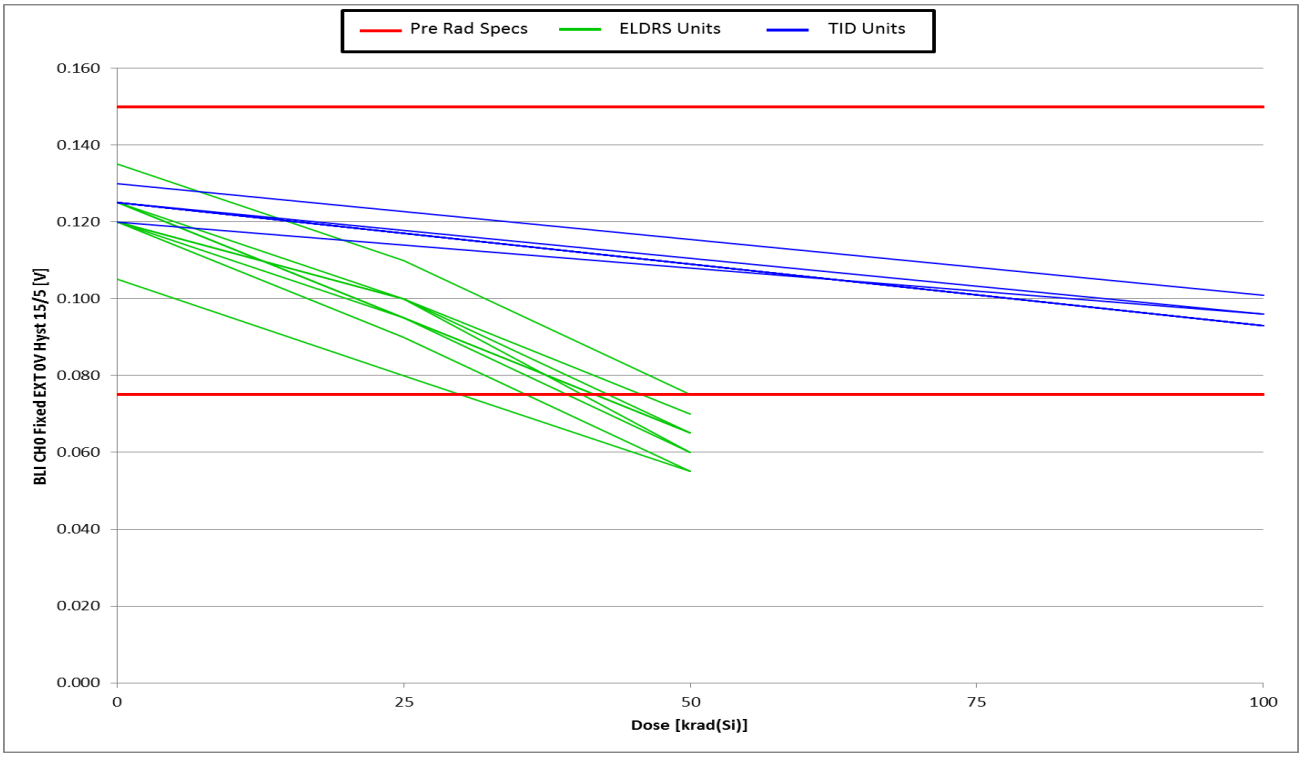
Adj threshold Bi-level MUX Hysteresis at DAC Max Output (If input = VEE/2 during exposure) at VCC=11.4V



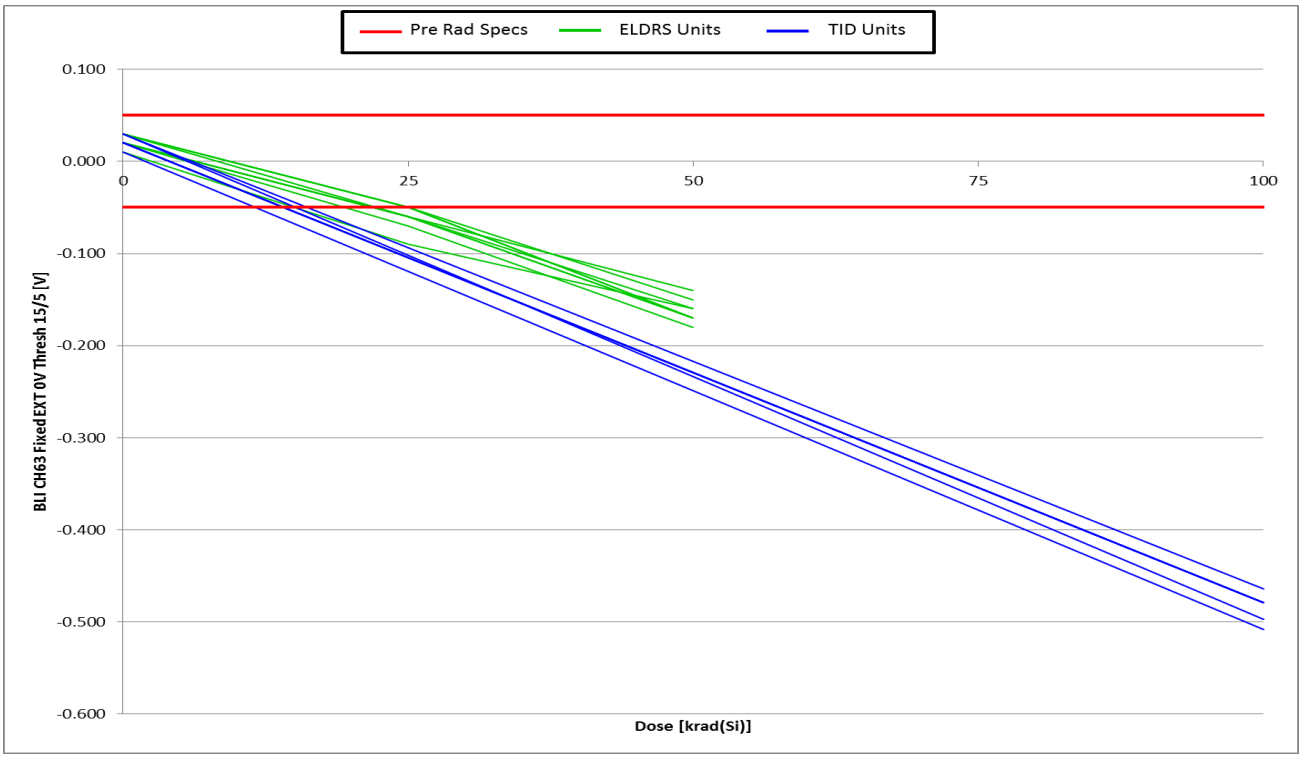
Adj threshold Bi-level MUX Threshold at DAC=0 Output (If input >=0V during exposure) at VCC=15V



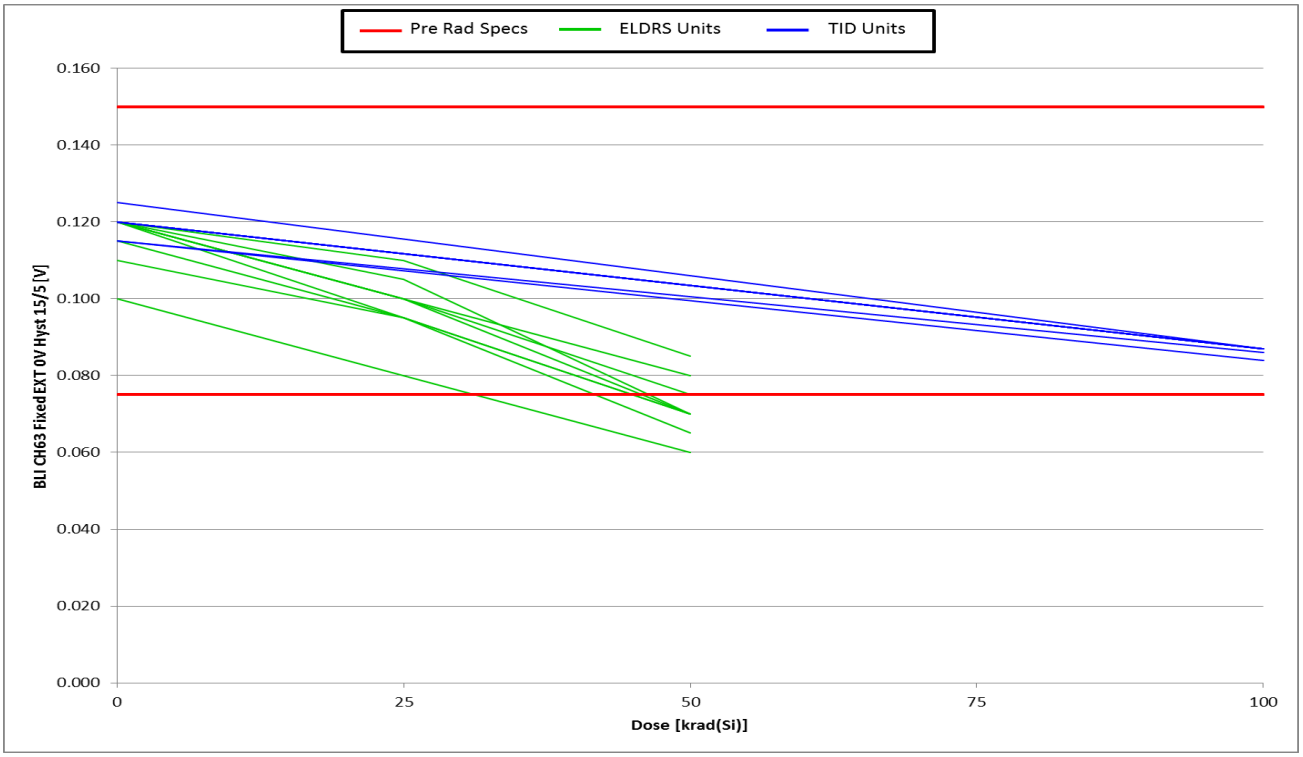
Adj threshold Bi-level MUX Hysteresis at DAC=0 Output (If input >=0V during exposure) at VCC=15V



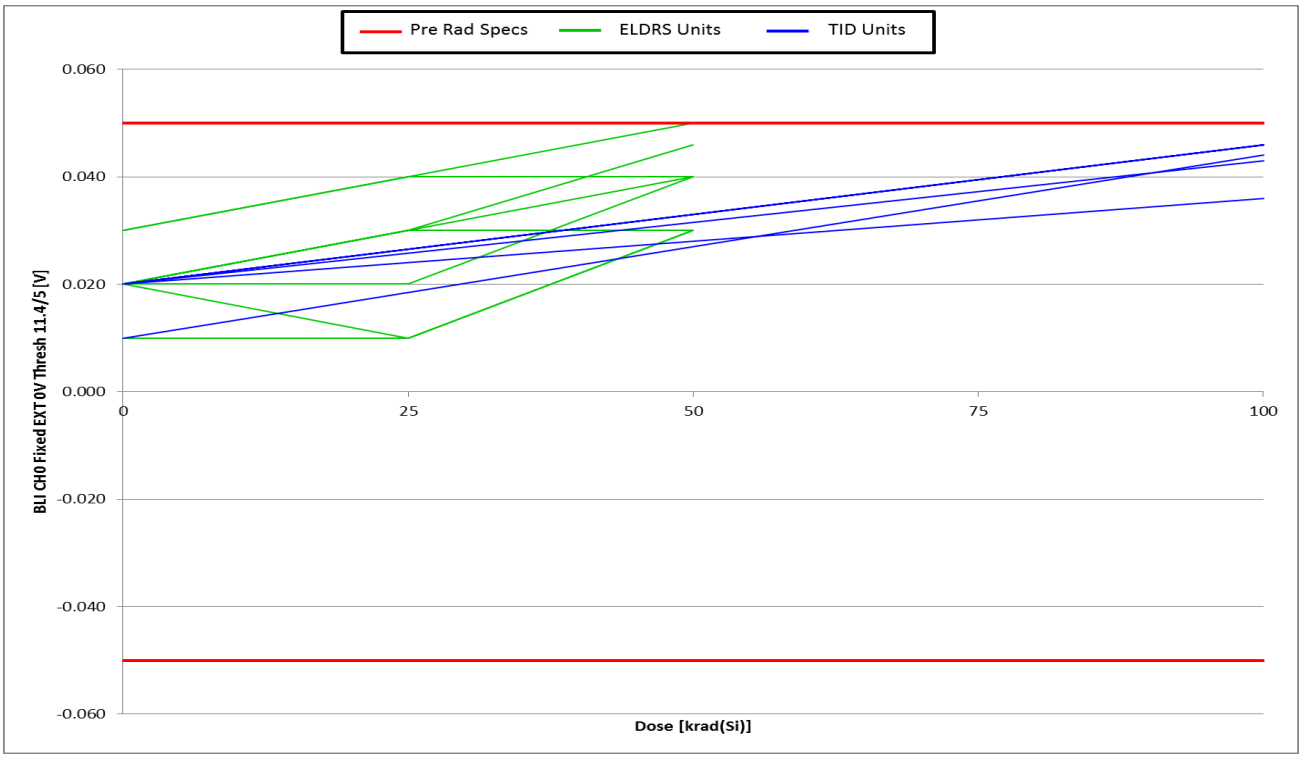
Adj threshold Bi-level MUX Threshold at DAC=0 Output (If input = VEE/2 during exposure) at VCC=15V



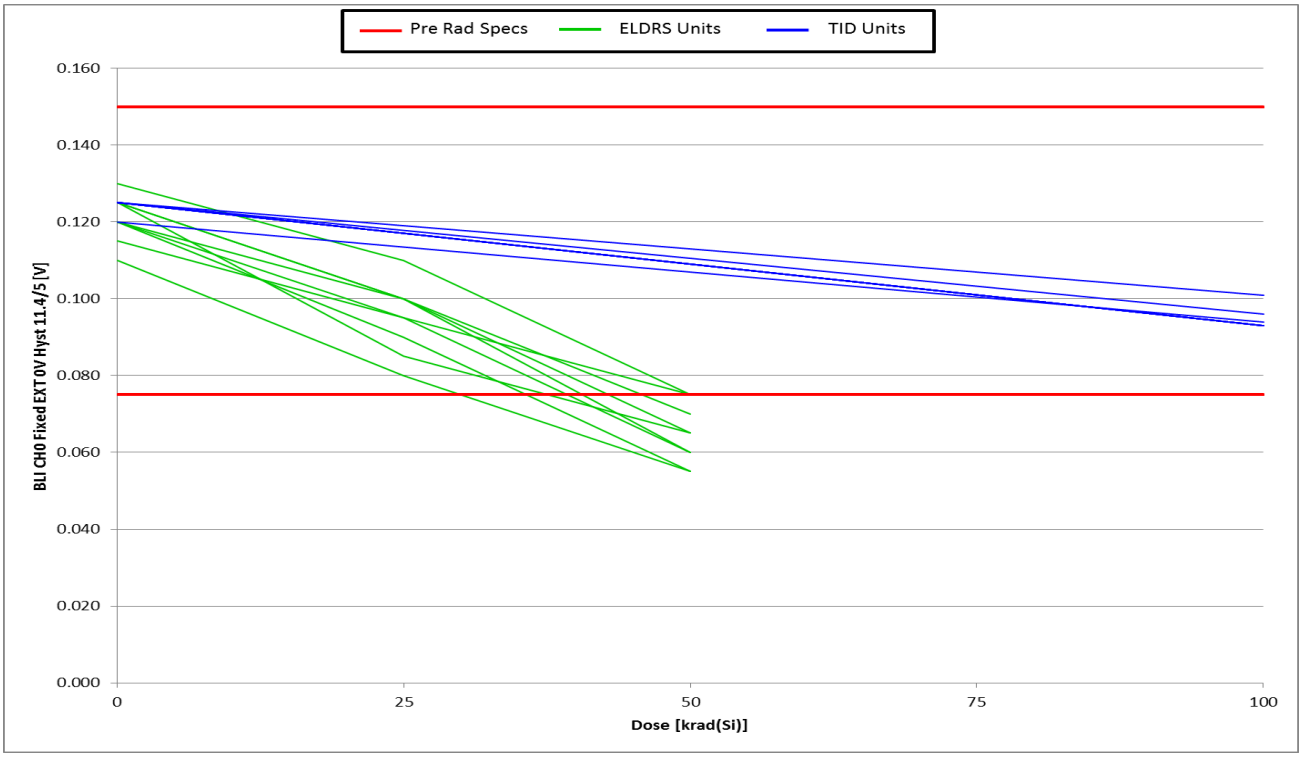
Adj threshold Bi-level MUX Hysteresis at DAC=0 Output (If input = VEE/2 during exposure) at VCC=15V



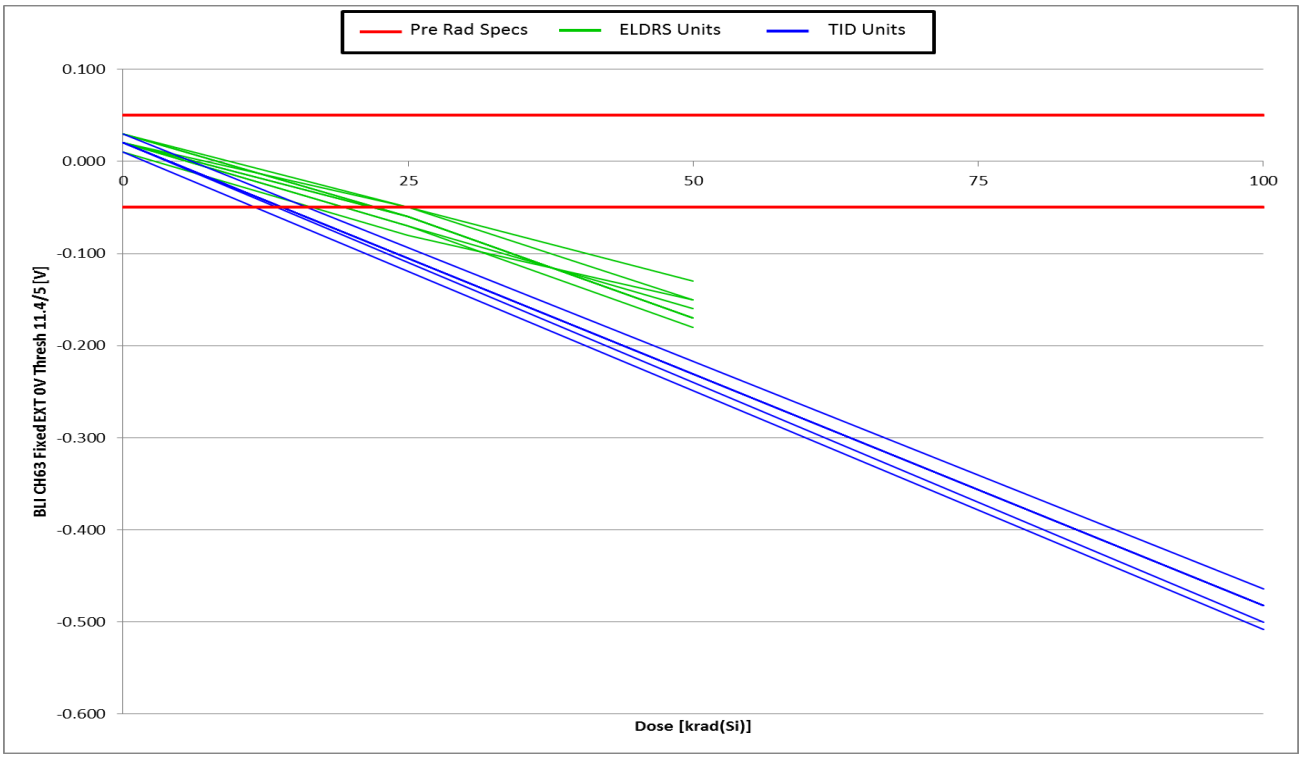
Adj threshold Bi-level MUX Threshold at DAC=0 Output (If input >=0V during exposure) at VCC=11.4V



Adj threshold Bi-level MUX Hysteresis at DAC=0 Output (If input >=0V during exposure) at VCC=11.4V



Adj threshold Bi-level MUX Threshold at DAC=0 Output (If input = VEE/2 during exposure) at VCC=11.4V



Adj threshold Bi-level MUX Hysteresis at DAC=0 Output (If input = VEE/2 during exposure) at VCC=11.4V