SmartTime for Libero SoC v11.8
SmartFusion2, IGLOO2, and RTG4
Timing Constraints Editor User Guide

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5-02-00679-1/01.17

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Timing Constraints Editor

The Timing Constraints Editor enables you to create, view, and edit timing constraints. This editor includes powerful visual dialogs that guide you toward capturing your timing requirements and timing exceptions quickly and correctly.

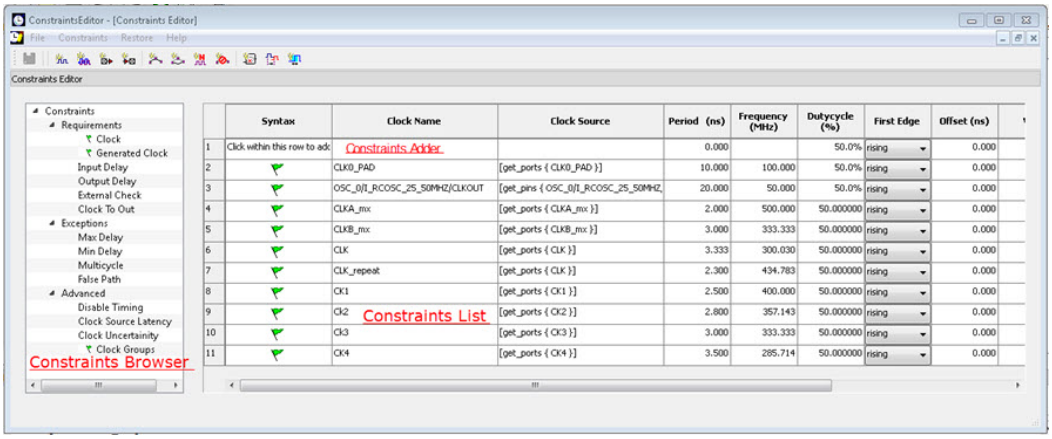


Figure 1 · Constraints Editor

The Constraints Editor window is divided into a Constraint Browser, Constraint List, and a Constraint Adder.

Constraints Browser

The Constraint Browser categorizes constraints based on three types of Constraints:

- **Requirements** – General constraints to meet the design's timing requirements and specifications. Examples are clock constraints and generated clock constraints.
- **Exceptions** – Constraints on certain timing paths for special considerations by SmartTime. Examples are false path constraints and multicycle path constraints.
- **Advanced** – Special timing constraints such as clock latency and clock groups

Constraints List

This is a spreadsheet-like list of the constraints with detailed values and parameters of the constraint displayed in individual cells. You may click on individual cells of the spreadsheet to change the values of the constraint parameters.

Constraints Adder

This is the first row of the spreadsheet-like constraint list. There are 2 ways of adding a constraint from this row. User can right click on the row, and select Add Constraint to add a constraint of the same type to the Constraint List. This method will invoke the specific add constraint dialog.

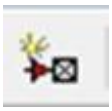
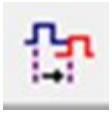
Alternatively, user can select a cell by clicking in it. Then follow by double-clicking and start typing text. This method of creating a constraint is targeted at the experienced user who knows the design well, and need not rely on the dialog box for guidance.

You can perform the following tasks in the Constraints View:

- Select a constraint type from the Constraint Browser and create or edit the constraint.
- Add a new constraint and check the syntax.
- Right-click a constraint in the Constraints List to edit or delete.
- Use the first row to create a constraint (as described above), and add it to the main table (list)

Constraint Icons

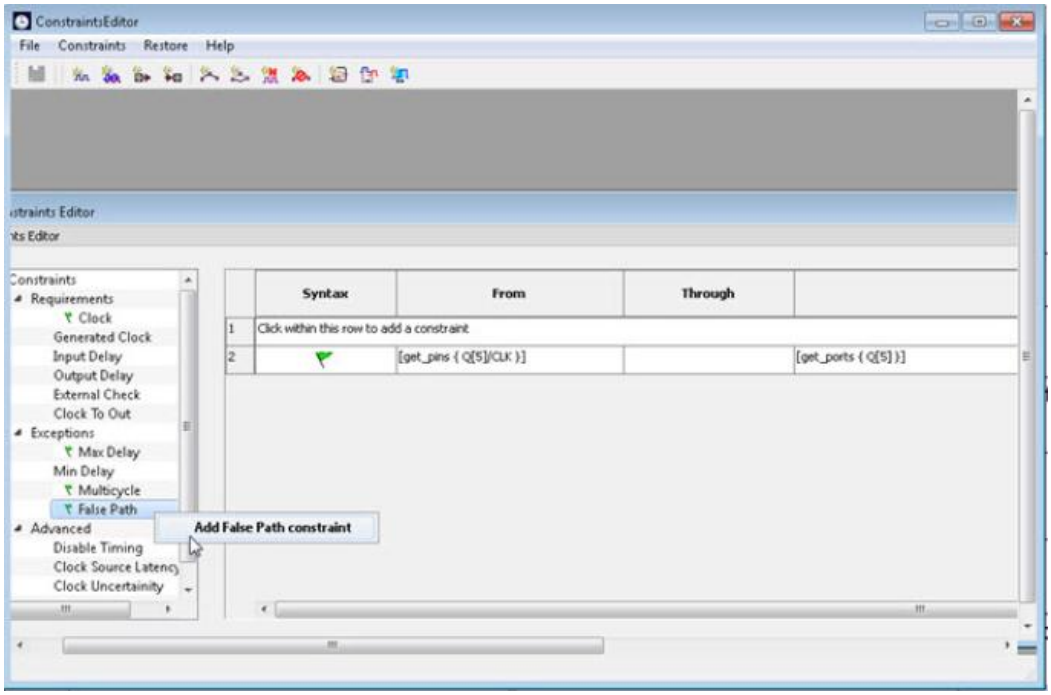
Across the top of the Constraint Editor is a list of icons you can click to add constraints. Tooltips are available to identify the constraints.

Icon	Name
	Add Clock Constraint
	Add Generated Clock Constraint
	Add Input Delay Constraint
	Add Output Delay Constraint
	Add Maximum Delay Constraint
	Add Minimum Delay Constraint
	Add Multicycle Path Constraint
	Add False Path Constraint
	Add Disable Timing Constraint
	Add Clock Source Latency
	Add Clock to Clock Uncertainty

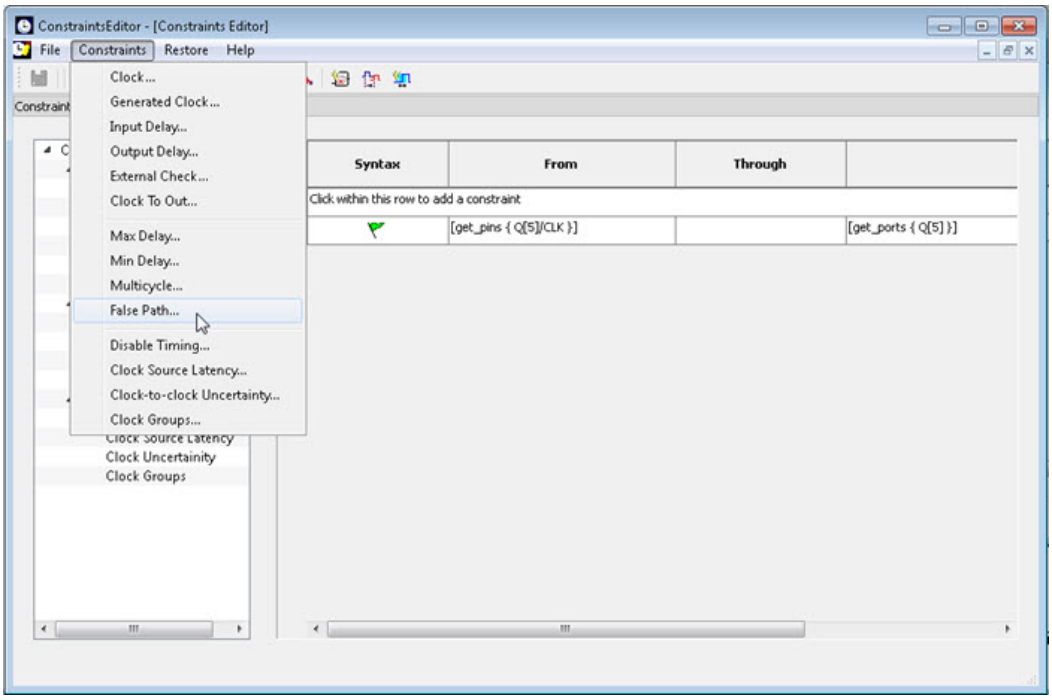
Adding Constraints

The Constraints Editor provides four ways to add Constraints. The Add Constraints dialog box appears when you add constraints in one of the following four ways:

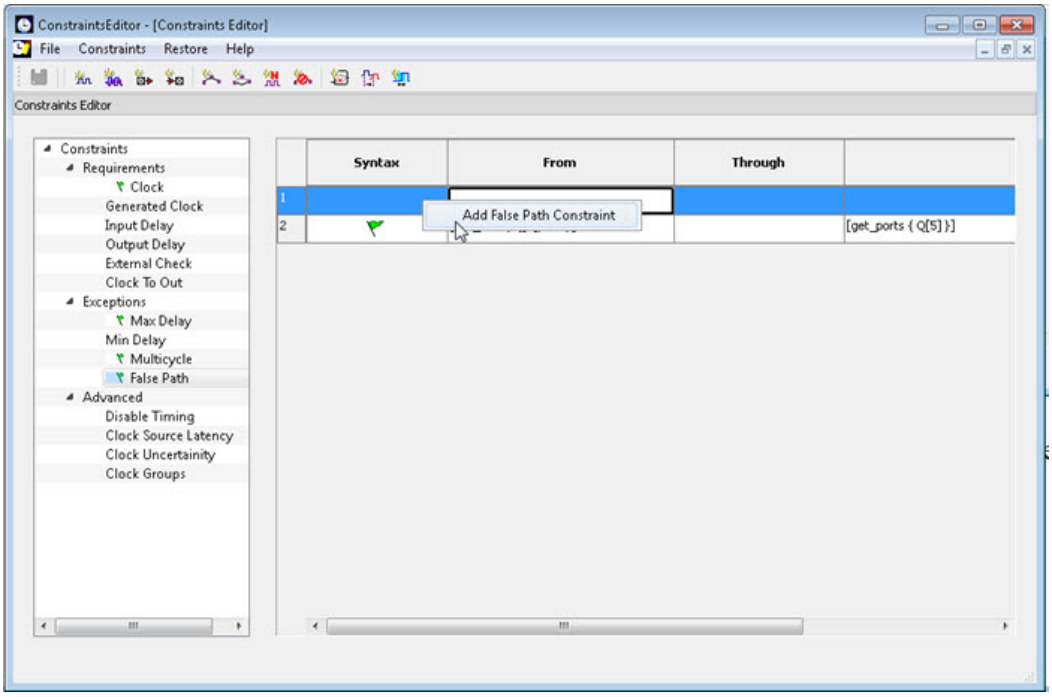
- Click the Add Constraint icon. Example: Click  to add False Path Constraints.
- From the Constraints Browser, choose the type of Constraints to add. Example: False Path



- Choose **False Path** from the Constraints drop-down menu (**Constraints > False Path**).



- Right-click the first row and choose **Add False Path Constraint**.



See Also

[Set Clock Constraints]

[Set Generated Clock Constraints]

[Set Input Delay Constraints]

[Set Output Delay Constraints]

[Set External Check Constraints]

Required Constraints

Set Clock Constraints

Adding a clock constraint is the most effective way to constrain and verify the timing behavior of a sequential design. Use clock constraints to meet your performance goals.

To set a clock constraint, open the Create Clock Constraint dialog box in one of the following four ways:

- From the Constraints Browser, choose **Clock**.
- Double-click the Add Clock Constraint icon  .
- Choose **Clock** from the Constraints drop-down menu (**Constraints > Clock**).
- Right-click the first row or any other row (if they exist) in the Clock Constraints Table and choose **Add Clock Constraint**.

The Create Clock Constraint dialog box appears.

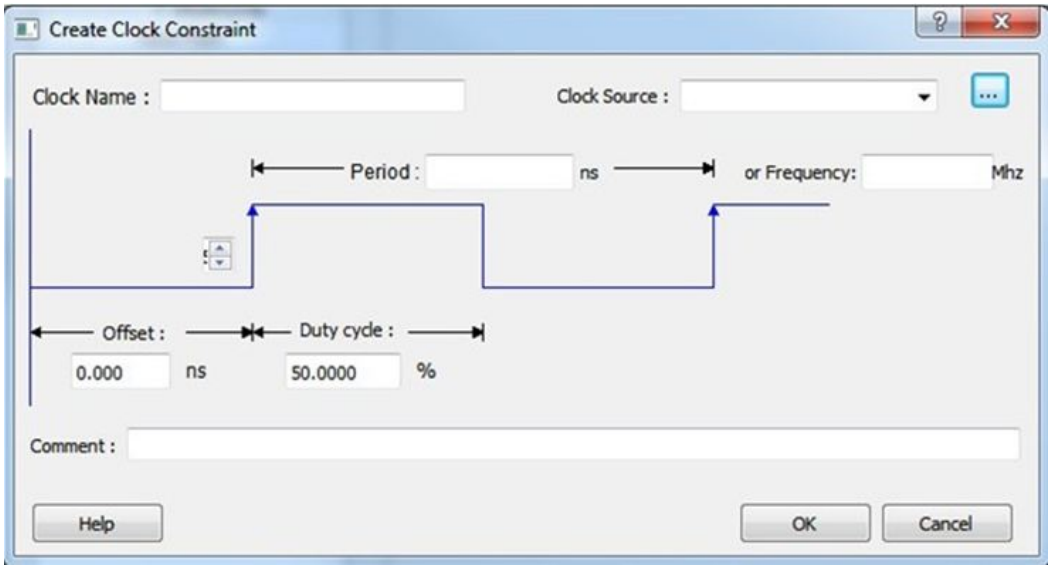


Figure 2 · Create Clock Constraint Dialog Box

Clock Name

Specifies the name of the clock constraint.

Clock Source

Select the pin to use as clock source. You can click the Browse button to display the Select Source Pins for Clock Constraint Dialog Box.

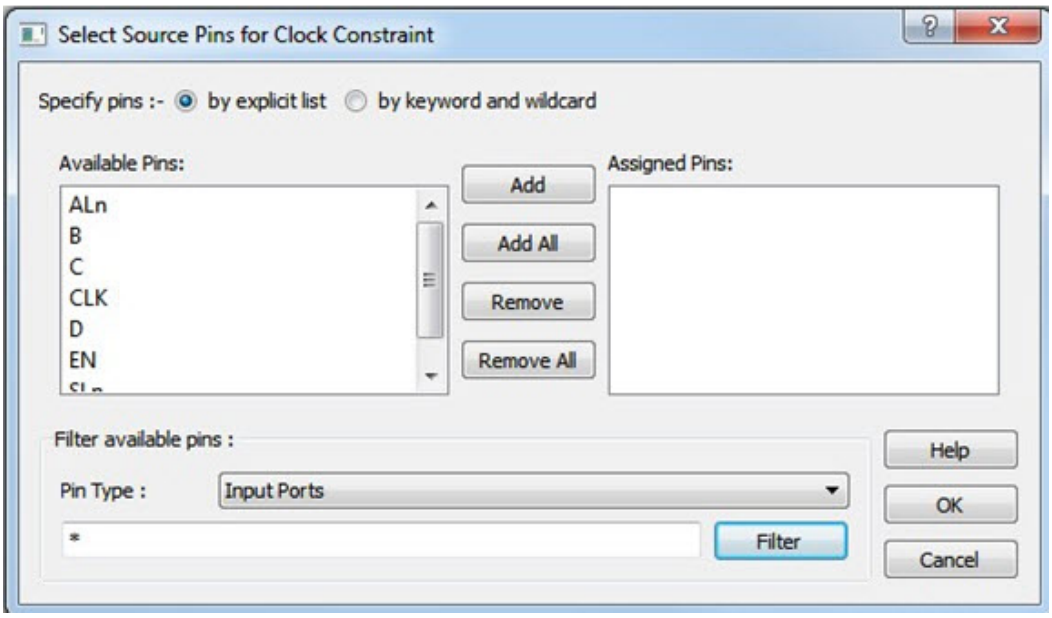


Figure 3 · Select Source Pin for Clock Constraint Dialog Box

The Pin Type options are:

- Input Ports
- All Pins
- All Nets

Use the Select Source Pin for Clock Constraint dialog box to display a list of source pins from which you can choose. By default, it displays the Input Ports of the design.

To choose other pin types in the design as clock source pins, click the drop-down and choose **Input Ports**, **All Pins**, or **All Nets**. To display a subset of the displayed clock source pins, you can create and apply a filter. The default filter is * (wild-card for all).

Click **OK** to save these dialog box settings.

Period/Frequency

Specifies the Period in nanoseconds (ns) or Frequency in MegaHertz (MHz). When you edit the period, the tool automatically updates the frequency value and vice versa. The frequency must be a positive real number. Accuracy is up to 3 decimal places.

Starting Clock Edge Selector

Click the Up or Down arrow to use the rising or falling edge as the starting edge for the created clock.

Offset

Indicates the shift (in nanoseconds) of the first clock edge with respect to instant zero common to all clocks in the design.

The offset value must be a positive real number. Accuracy is up to 2 decimal places. Default value is 0.

Duty Cycle

This number specifies the percentage of the overall period that the clock pulse is high. The duty cycle must be a positive real number. Accuracy is up to 4 decimal places. Default value is 50%.

Comment

Enter a single line of text that describes the clock constraints purpose.

See Also

create_clock (SDC)

Set Generated Clock Constraints

Use the generated clock constraint to define an internally generated clock for your design and verify its timing behavior. Use generated clock constraints and clock constraints to meet your performance goals.

To set a generated clock constraint, open the Create Generated Clock Constraint dialog box in one of the following four ways:

- From the Constraints Browser, choose **Generated Clock**.
- Double-click the Add Generated Clock Constraint icon  .
- Choose **Generated Clock** from the Constraints drop-down menu (**Constraints > Generated Clock**).
- Right-click any row in the Generated Clock Constraints Table and choose **Add Generated Clock Constraint**.

The Create Generated Clock Constraint dialog box appears.

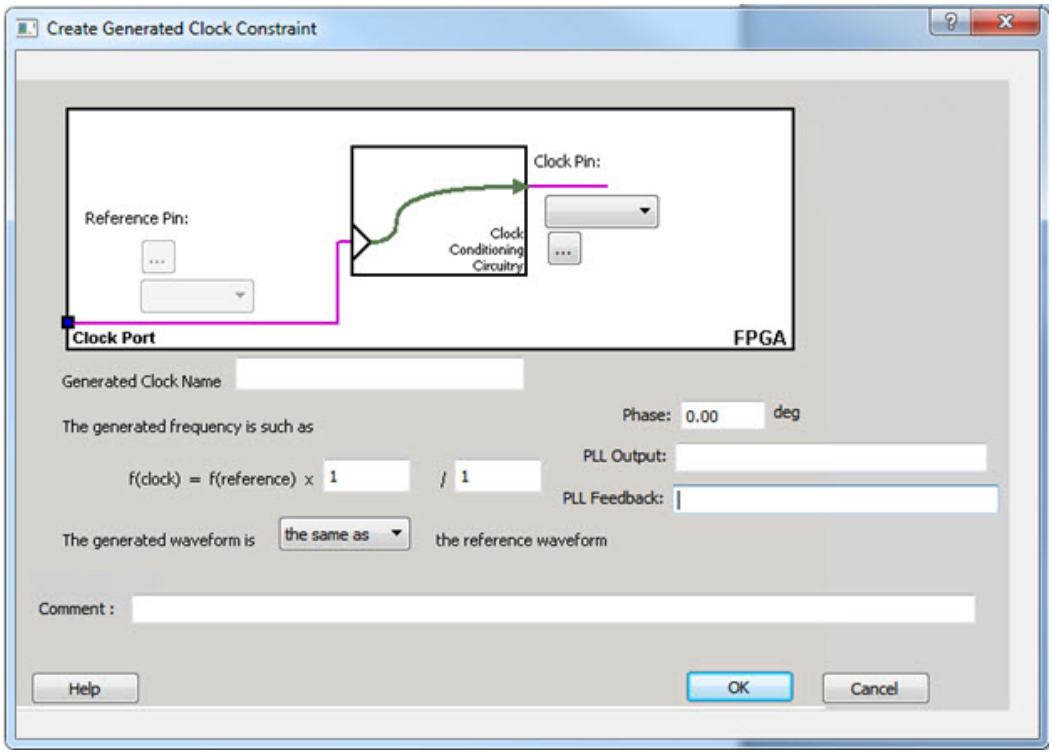


Figure 4 · Create Generated Clock Constraint Dialog Box

Clock Pin

Select a Clock Pin to use as the generated clock source. To display a list of the available generated clock source pins, click the Browse button. The Select Generated Clock Source dialog box appears.

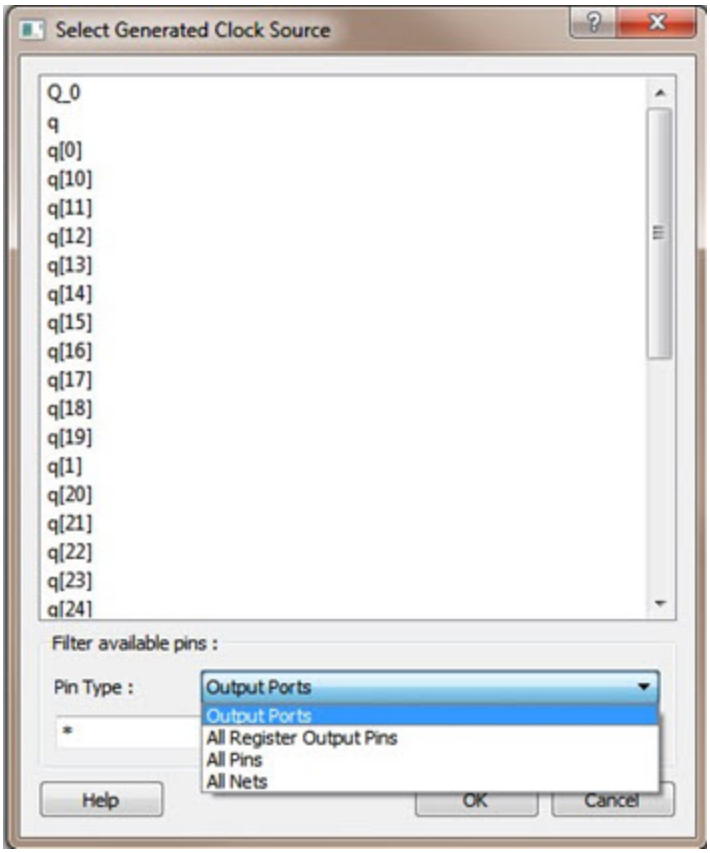


Figure 5 · Select Generated Clock Source Dialog Box

The Pin Type options for Generated Clock Source are:

- Output Ports
- All Register Output Pins
- All Pins
- All Nets

Click **OK** to save the dialog box settings.

Modify the Clock Name if necessary.

Reference Pin

Specify a Clock Reference. To display the list of available clock reference pins, click the Browse button. The Select Generated Clock Reference dialog box appears.

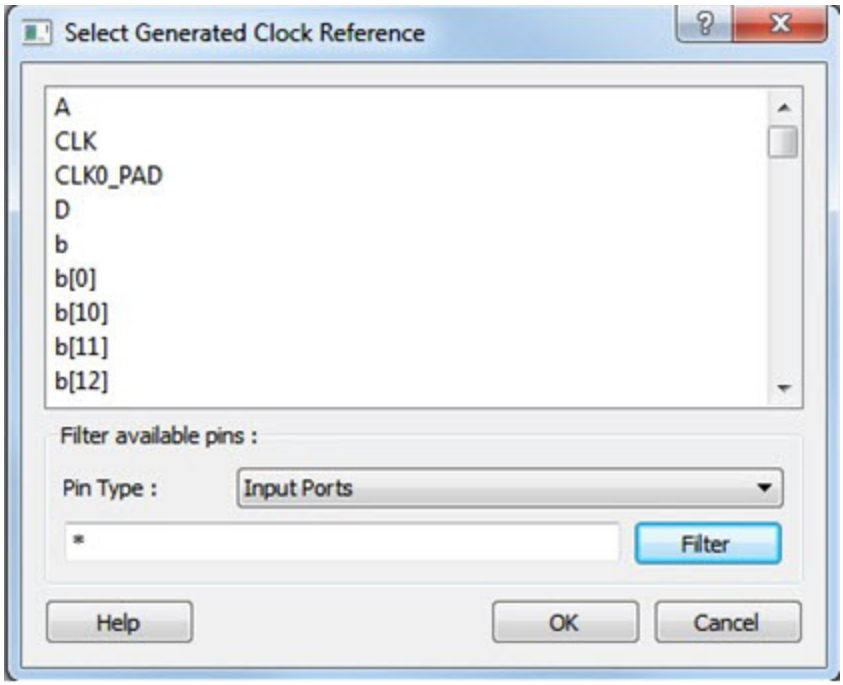


Figure 6 · Select Generated Clock Reference Dialog Box

The Pin Type options for Generated Clock Reference are:

- Input Ports
- All Pins

Click **OK** to save the dialog box settings.

Generated Clock Name

Specifies the name of the Generated clock constraint. This field is required for virtual clocks when no clock source is provided.

Generated Frequency

Specify the values to calculate the generated frequency: a multiplication factor and/or division factor (must be positive integers) is applied to the reference clock to compute the generated clock.

Generated Waveform

Specify whether the generated waveform is the same or inverted with respect to the reference waveform. Click **OK**.

Phase

This field is primarily used to report the information captured from the CCC configuration process, and when constraint is auto-generated. Meaningful phase values are: 0, 45, 90, 135, 180, 225, 270, and 315. This field is used to report the information captured from the CCC configuration process, and when the constraint is auto-generated.

PLL Output

This field refers to the CCC GL0/1/2/3 output that is fed back to the PLL (in the CCC). This field is primarily used to report the information captured from the CCC configuration process, and when constraint is auto-generated.

PLL Feedback

This field refers to the manner in which the GL/0/1/2/3 output signal of the CCC is connected to the PLL's FBCLK input. This field is primarily used to report the information captured from the CCC configuration process, and when constraint is auto-generated.

Comment

Enter a single line of text that describes the generated clock constraints purpose.

See Also

create_generated_clock (SDC)

Specifying Generated Clock Constraints

Select Generated Clock Source

Set an Input Delay Constraint

Use the input delay constraint to define the arrival time of an input relative to a clock.

To specify an input delay constraint, open the Add Input Delay Constraint dialog box in one of the following four ways:

- From the Constraints Browser, choose **Input Delay**.
- Double-click the Add Input Delay Constraint icon  .
- Choose **Input Delay** from the Constraints drop-down menu (**Constraints > Input Delay**).
- Right-click any row in the Input Delay Constraints Table and choose **Add Input Delay Constraint**.

The Add Input Delay Constraint dialog box appears.

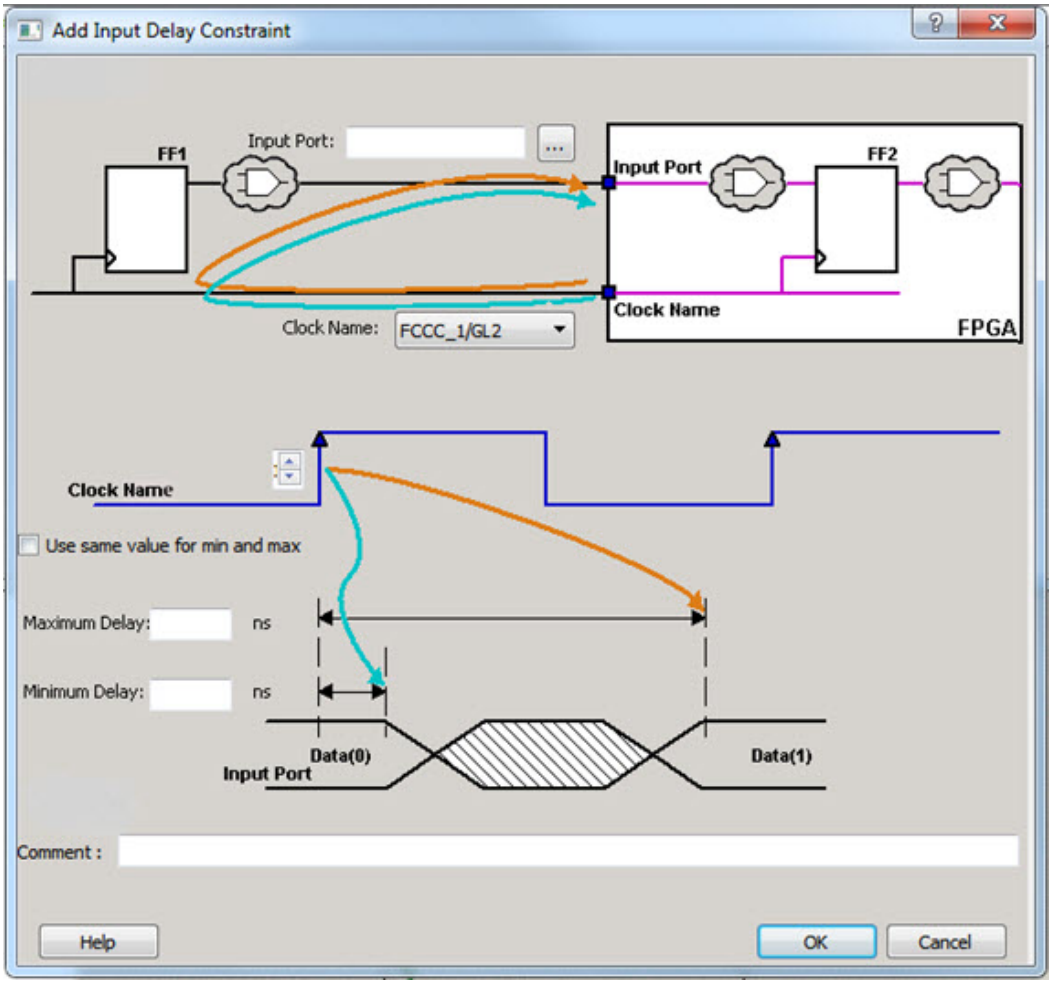


Figure 7 · Add Input Delay Constraint Dialog Box

The Input Delay Dialog Box enables you to enter an input delay constraint by specifying the timing budget outside the FPGA. You can enter the Maximum Delay, the Minimum Delay, or both.

Input Port

Specify the Input Port or click the browse button next to Input Port to display the Select Ports for Input Delay dialog box. You can select multiple input ports on which to apply the input delay constraint.

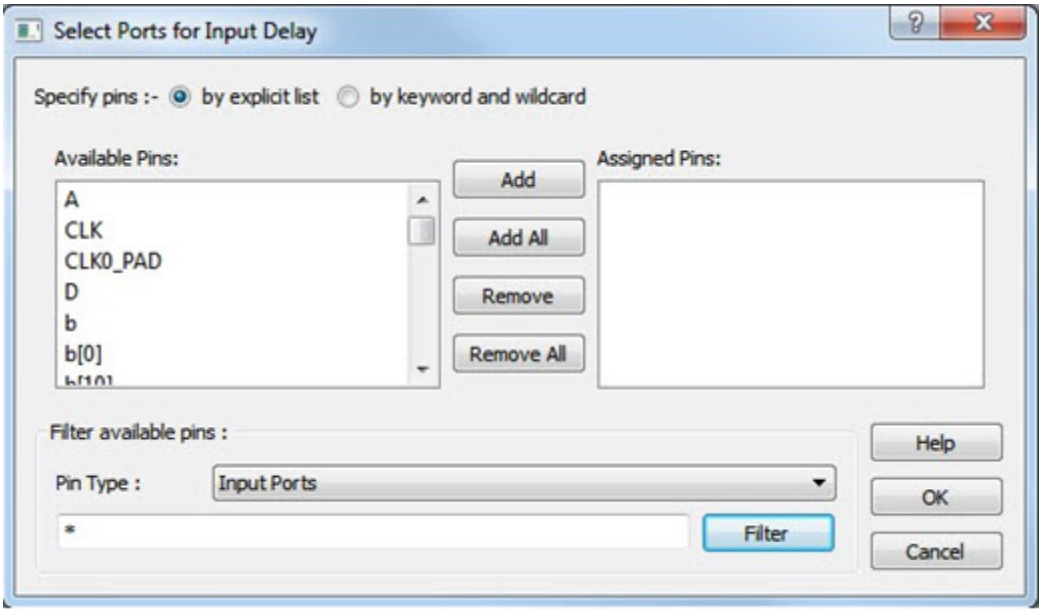


Figure 8 · Select Ports for Input Delay Dialog Box

There is only 1 Pin Type available for Input Delay: Input Ports.

Clock Name

Specifies the clock reference to which the specified input delay is based.

Clock edge

Select rising or falling as the launching edge of the clock.

Use same value for min and max

Specifies that the minimum input delay uses the same value as the maximum input delay.

Maximum Delay

Specifies that the delay refers to the longest path arriving at the specified input.

Minimum Delay

Specifies that the delay refers to the shortest path arriving at the specified input.

Comment

Enter a one-line comment for this constraint.

See Also

set_input_delay (SDC)

Set an Output Delay Constraint

Use the output delay constraints to define the output delay of an output relative to a clock.

To specify an output delay constraint, open the Add Output Delay Constraint Dialog box in one of the following four ways:

- From the Constraints Browser, choose **Output Delay**.
- Double-click the Add Output Delay Constraint icon  .
- Choose Output Delay from the Constraints drop-down menu (**Constraints > Output Delay**).

- Right-click any row in the Output Delay Constraints Table and choose **Add Output Delay Constraint**.

The Add Output Delay Constraint dialog box appears.

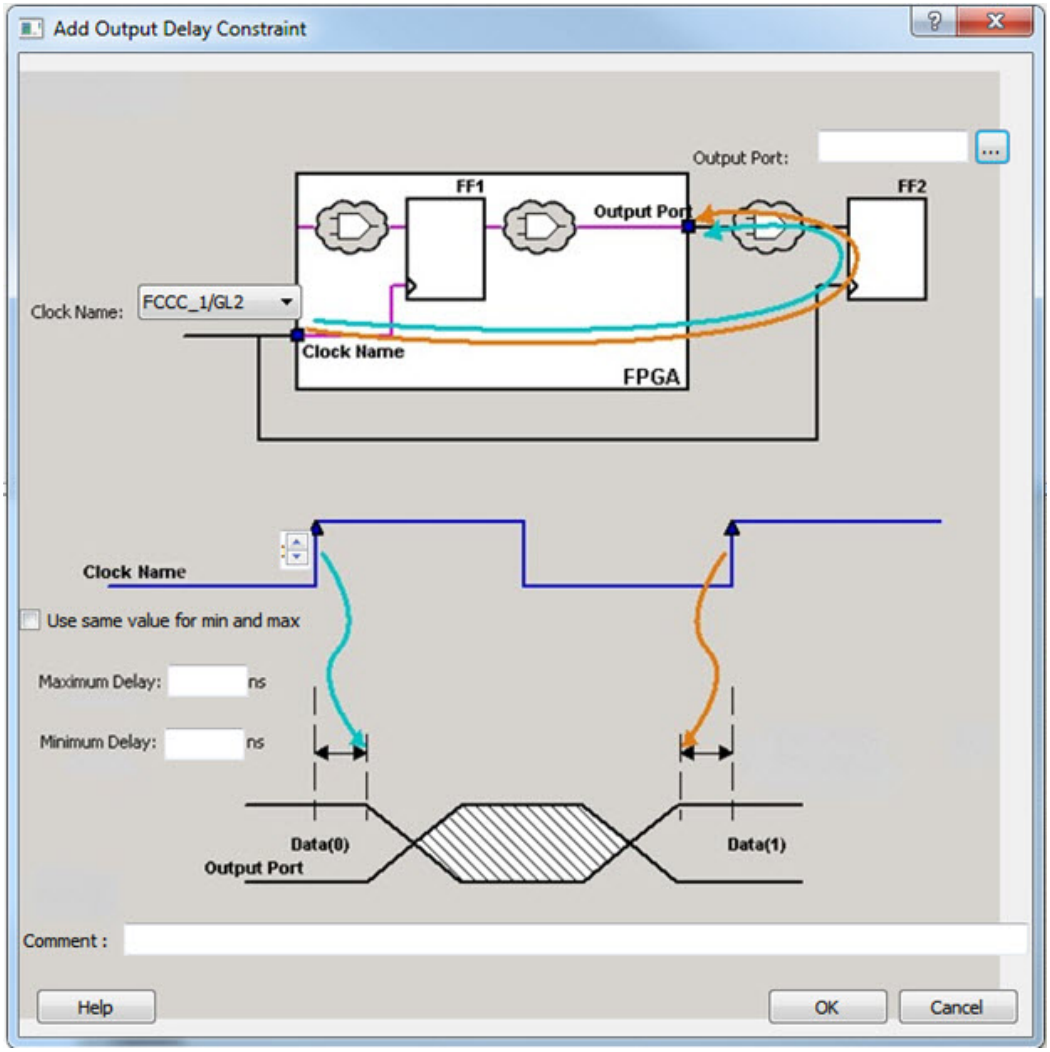


Figure 9 · Add Output Delay Constraint Dialog Box

The Output Delay dialog box enables you to enter an output delay constraint by specifying the timing budget outside the FPGA. You can enter the Maximum Delay, the Minimum Delay, or both.

Enter the name of the Output Port or click the browse button to display the Select Ports for Output Delay dialog box.

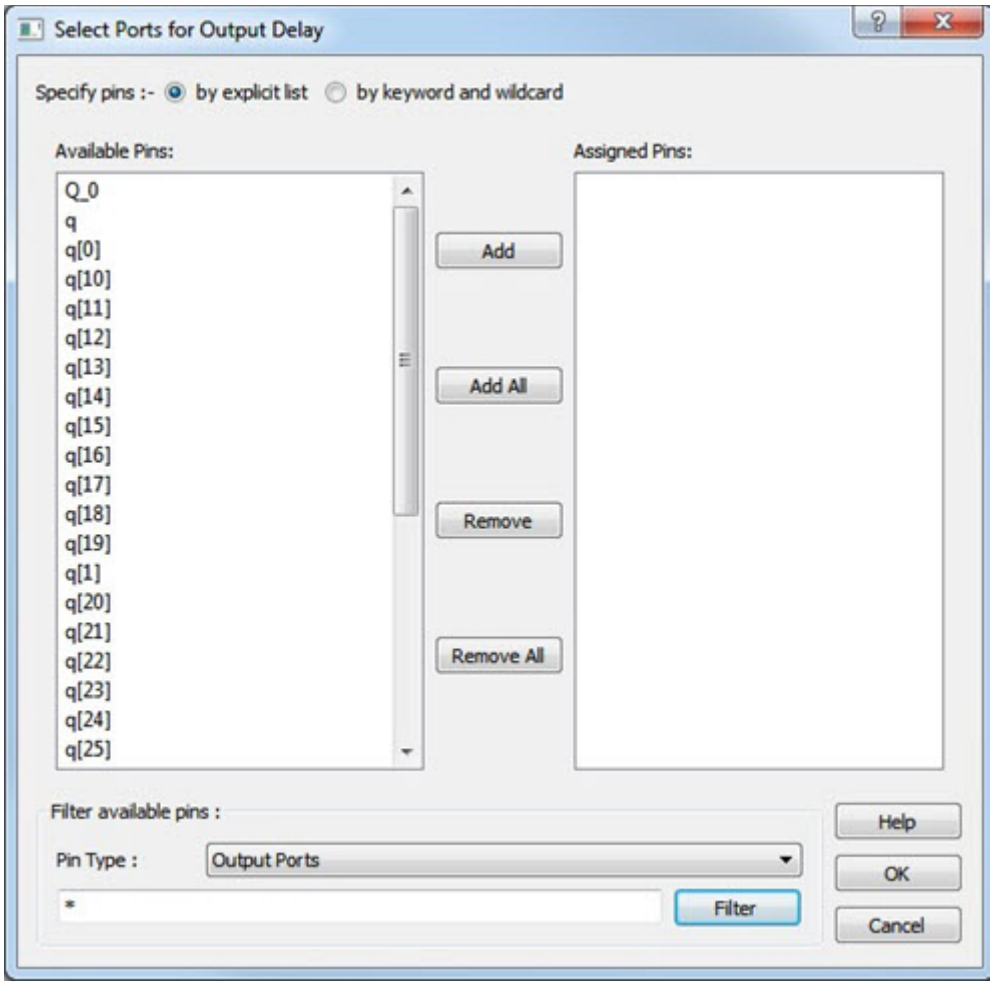


Figure 10 · Output Delay Dialog Box

There is only 1 Pin Type available for Output Delay: Output Ports

Output Port

Specifies a list of output ports in the current design to which the constraint is assigned. You can select multiple output ports to apply the output delay constraints.

Clock Name

Specifies the clock reference to which the specified output delay is related.

Clock edge Selector

Use the Up or Down arrow to select the rising or falling edge as the launching edge of the clock.

Use Same Value for Min and Max

Check this checkbox to use the same delay value for Min and Max delay.

Maximum Delay

Specifies the delay in nanoseconds for the longest path from the specified output to the captured edge. This represents a combinational path delay to a register outside the current design plus the library setup time.

Minimum Delay

Specifies the delay in nanoseconds for the shortest path from the specified output to the captured edge. This represents a combinational path delay to a register outside the current design plus the library hold time.

Comment

Enter a one-line comment for the constraint.

See Also

set_output_delay (SDC)

Set an External Check Constraint

Use the Add External Check Constraint to specify the timing budget inside the FPGA.

To specify an External Check constraint, open the Add External Check Constraint dialog box in one of the following three ways:

- From the Constraints Browser, choose **External Check**.
- Choose **External Check** from the Constraints drop-down menu (**Constraints > External Check**).
- Right-click any row in the External Check Constraints Table and choose **Add External Check Constraint**.

The Add External Check Constraint dialog box appears.

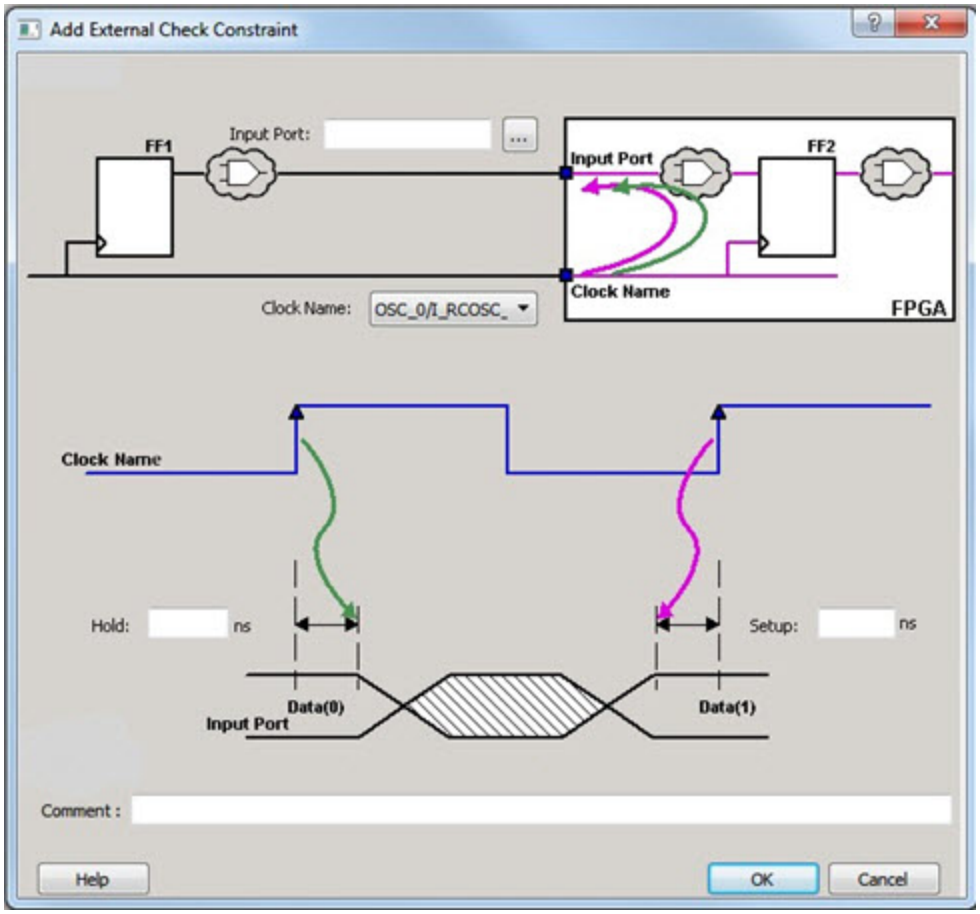


Figure 11 · Add External Check Constraint Dialog Box

Input Port

Specify the Input Port or click the browse button next to Input Port to display the Select Ports for External Check dialog box. You can select multiple input ports on which to apply the External Check constraint.

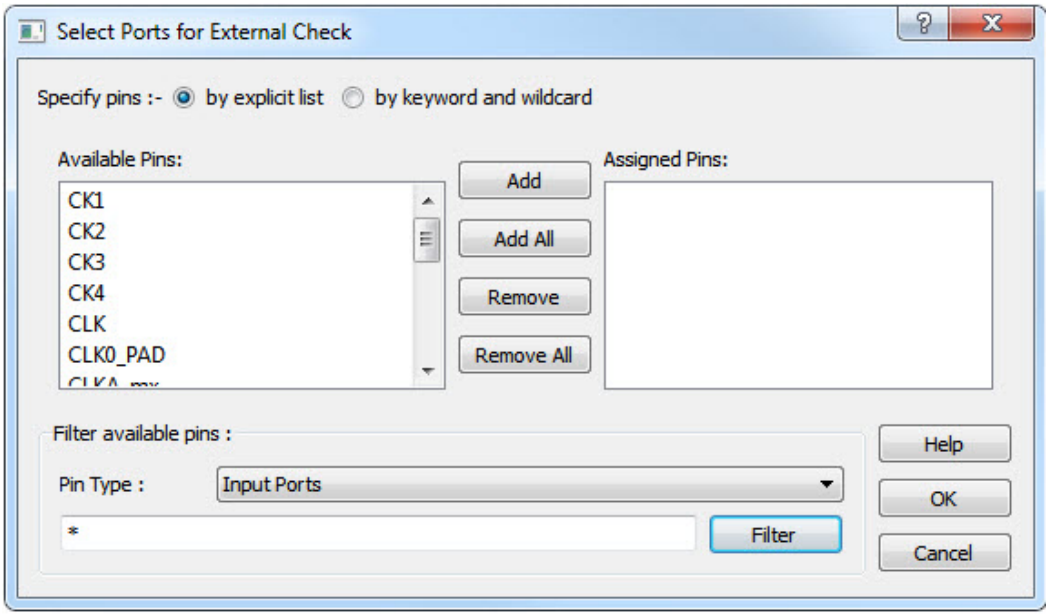


Figure 12 · Select Ports for External Check Dialog Box

Clock Name

Specifies the clock reference to which the specified External Check is related.

Hold

Specifies the external hold time requirement in nanoseconds for the specified input ports.

Setup

Specifies the external setup time requirement in nanoseconds for the specified input ports.

Comment

Enter a one-line comment for this constraint.

See Also

set_external_check

Set Clock To Out Constraint

Enter a clock to output constraint by specifying the timing budget inside the FPGA.

To specify a Clock to Out constraint, open the Add Clock to Out Constraint dialog box in one of the following three ways:

- From the Constraints Browser, choose **Clock to Out**.
- Choose **Clock to Out** from the Constraints drop-down menu (**Constraints > Clock to Out**).
- Right-click any row of the Clock To Out Constraints Table and choose **Add Clock to Out Constraint**.

The Add Clock To Out Constraint dialog box appears.

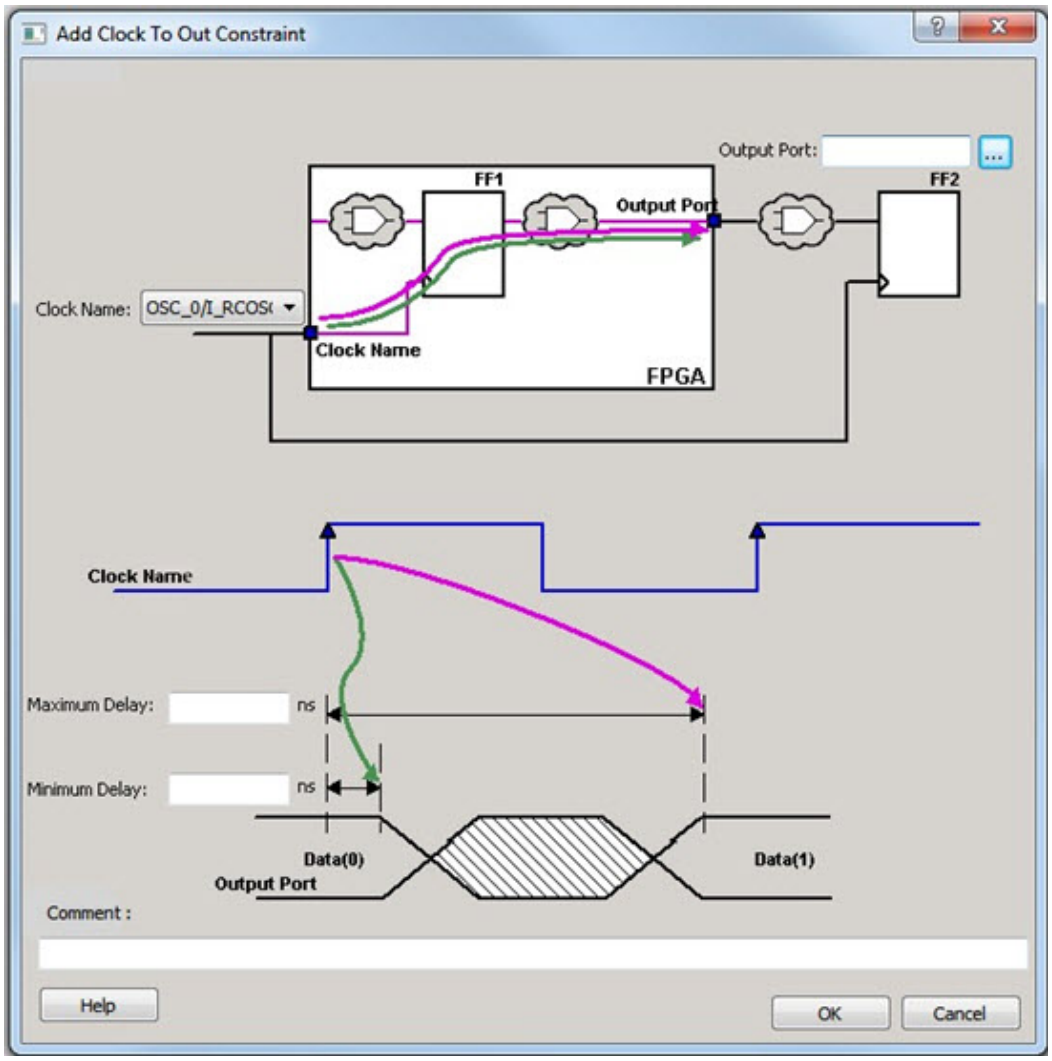


Figure 13 · Add Clock to Out Constraint Dialog Box

Specify the Output Port or click the browse button to display the Select Ports for Clock to Output dialog box. You can select multiple output ports on which to apply the Clock to Out constraint.

Click the browse button next to Output Port to open the Select Ports for Clock To Output dialog box.

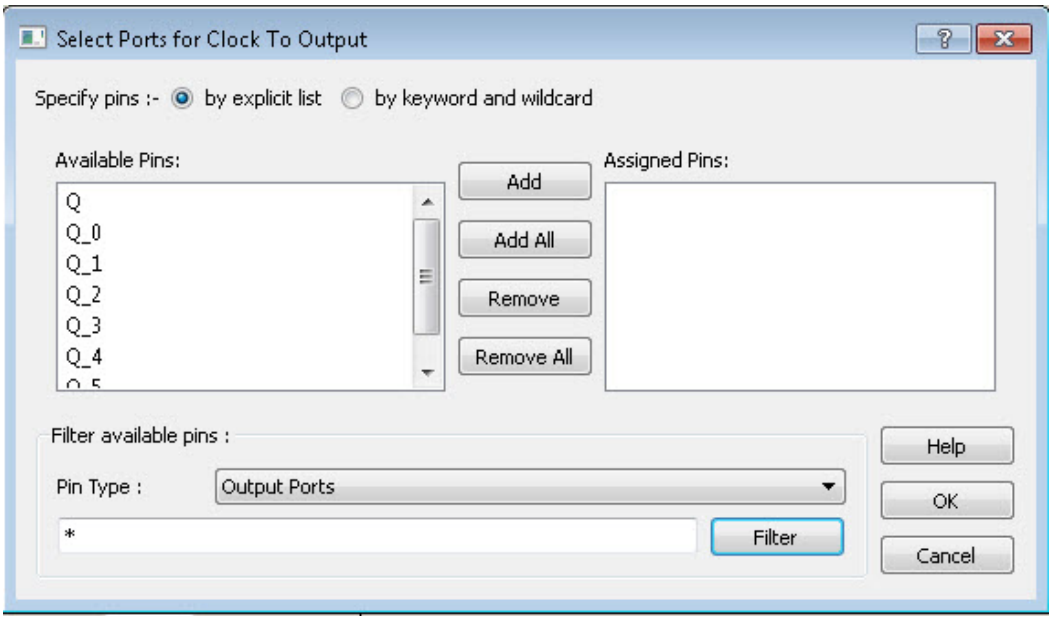


Figure 14 · Select Ports for Clock To Output Dialog Box

Clock Name

Specifies the clock reference to which the specified Clock to Out delay is related.

Maximum Delay

Specifies the delay in nanoseconds for the longest path from the specified output to the captured edge. This represents a combinational path delay to a register outside the current design plus the library setup time.

Minimum Delay

Specifies the delay in nanoseconds for the shortest path from the specified output to the captured edge. This represents a combinational path delay to a register outside the current design plus the library hold time.

Comment

Enter a one-line comment for this constraint.

See Also

set_clock_to_ouput

Exceptions

Set a Maximum Delay Constraint

Set the options in the Maximum Delay Constraint dialog box to relax or to tighten the original clock constraint requirement on specific paths.

SmartTime automatically derives the individual maximum delay targets from clock waveforms and port input or output delays. So the maximum delay constraint is a timing exception. This constraint overrides the default single cycle timing relationship for one or more timing paths. This constraint also overrides a multiple cycle path constraint.

Note: When the same timing path has more than one timing exception constraint, SmartTime honors the timing constraint with the highest precedence and ignores the other timing exceptions according to the order of precedence shown.

Timing Exception Constraints	Order of Precedence
set_disable_timing	1
set_false_path	2
set_maximum_delay/set_minimum_delay	3
set_multicycle_path	4

Note: The set_maximum_delay_constraint has a higher precedence over set_multicycle_path constraint and therefore the former overrides the latter when both constraints are set on the same timing path.

To set a Maximum Delay constraint, open the Set Maximum Delay Constraint Dialog box in one of the following four ways:

- From the Constraints Browser, choose **Max Delay**.
- Double-click the Add Max Delay Constraint icon  .
- Choose **Max Delay** from the Constraints drop-down menu (**Constraints > Max Delay**).
- From the Max Delay Constraints Table, right-click any row and choose **Add Maximum Delay Constraint**.

The Set Maximum Delay Constraint dialog box appears.

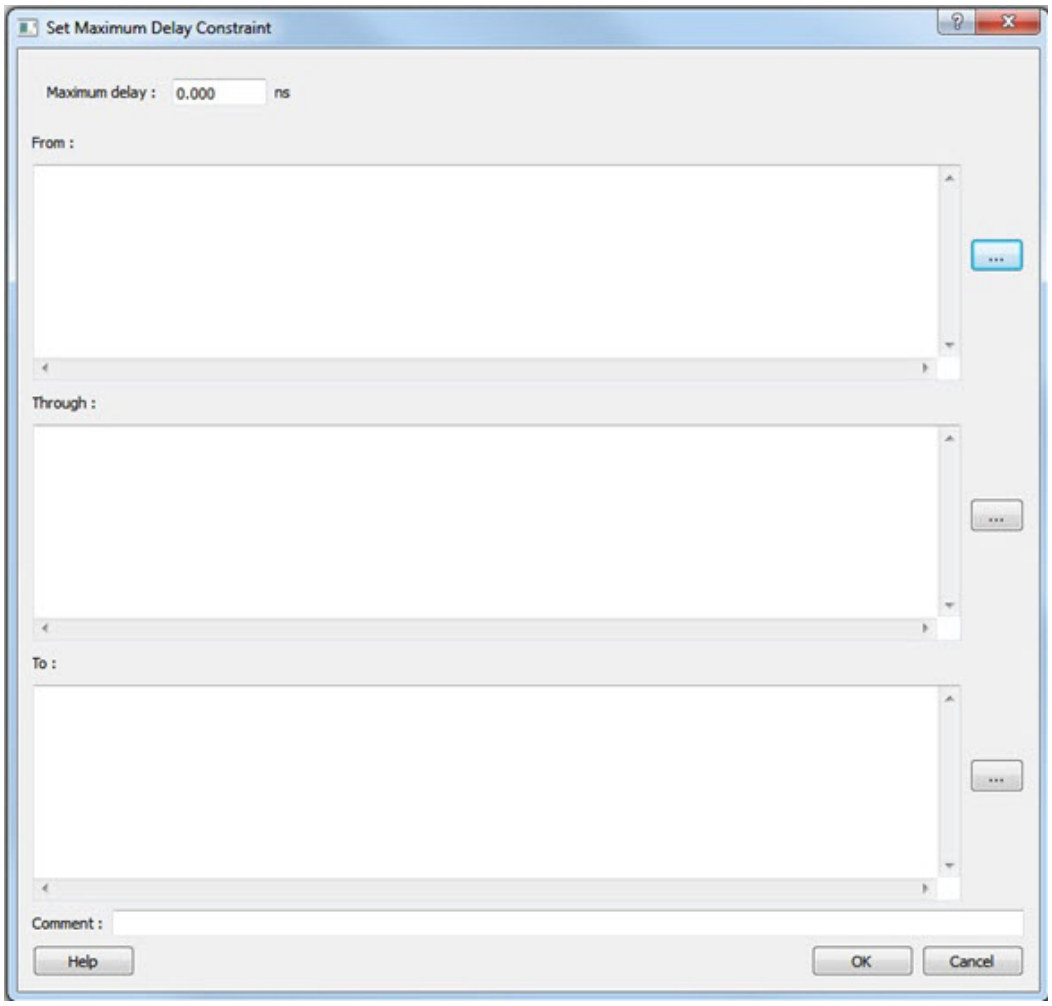


Figure 15 · Set Maximum Delay Constraint Dialog Box

Maximum Delay

Specifies a floating point number in nanoseconds that represents the required maximum delay value for specified paths.

If the path starting point is on a sequential device, SmartTime includes clock skew in the computed delay.

If the path starting point has an input delay specified, SmartTime adds that delay value to the path delay.

If the path ending point is on a sequential device, SmartTime includes clock skew and library setup time in the computed delay.

If the ending point has an output delay specified, SmartTime adds that delay to the path delay.

Source/From Pins

Specifies the starting points for max delay constraint path. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

To specify the Source pins(s), click on the Browse button to open the Select Source Pins for Max Delay Constraint dialog box.

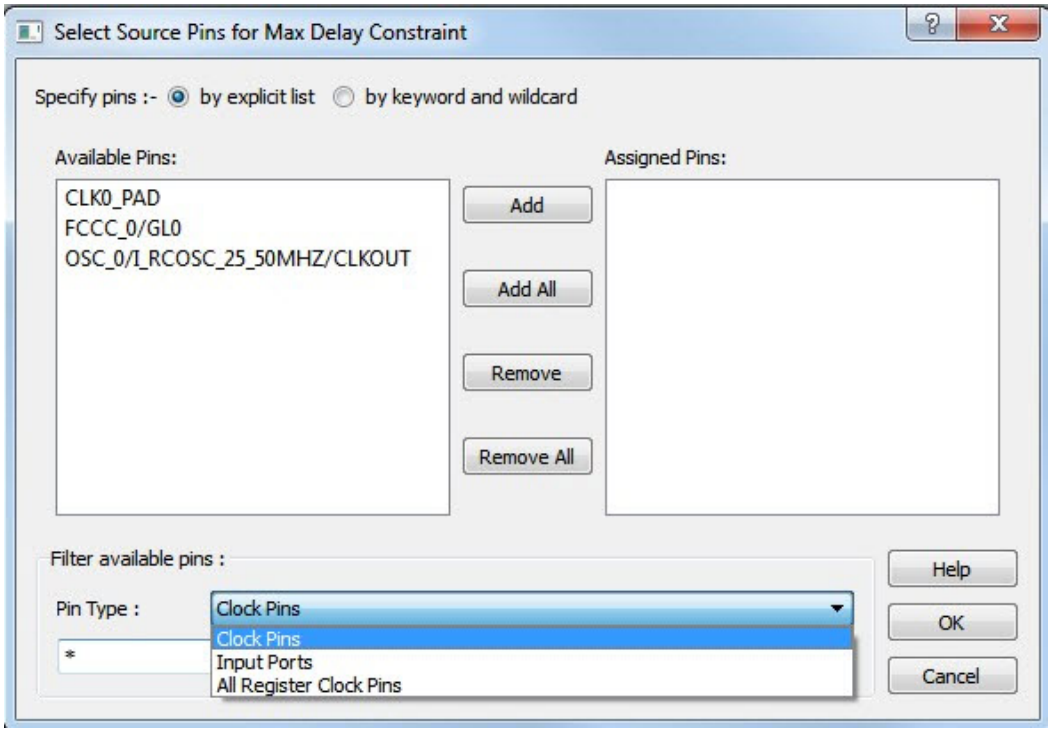


Figure 16 · Select Source Pins for Max Delay Constraint Dialog Box

The Pin Type options for Source Pins are:

- Clock Pins
- Input Ports
- All Register Clock Pins

Through Pins

Specifies the through pins in the specified path for the Maximum Delay constraint.

To specify the Through pin(s), click on the browse button next to the “Through” field to open the Select Through Pins for Max Delay Constraint dialog box.

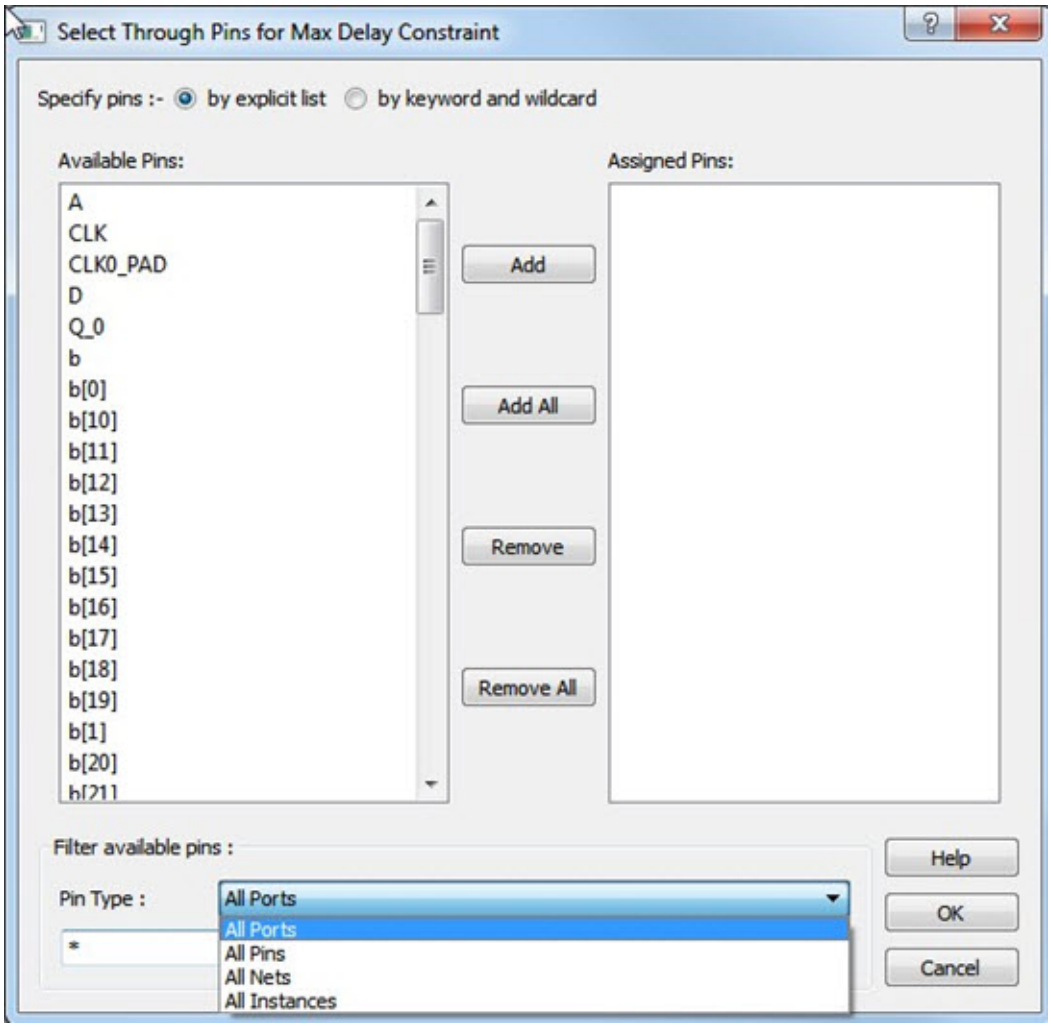


Figure 17 · Select Through Pins for Max Delay Constraint Dialog Box

The available Pin Type options are:

- All Ports
- All Pins
- All Nets
- All Instances

Destination/To Pins

Specifies the ending points for maximum delay constraint. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

To specify the Destination pin(s), click on the browse button next to the “To” field to open the Select Destination Pins for Max Delay Constraint dialog box.

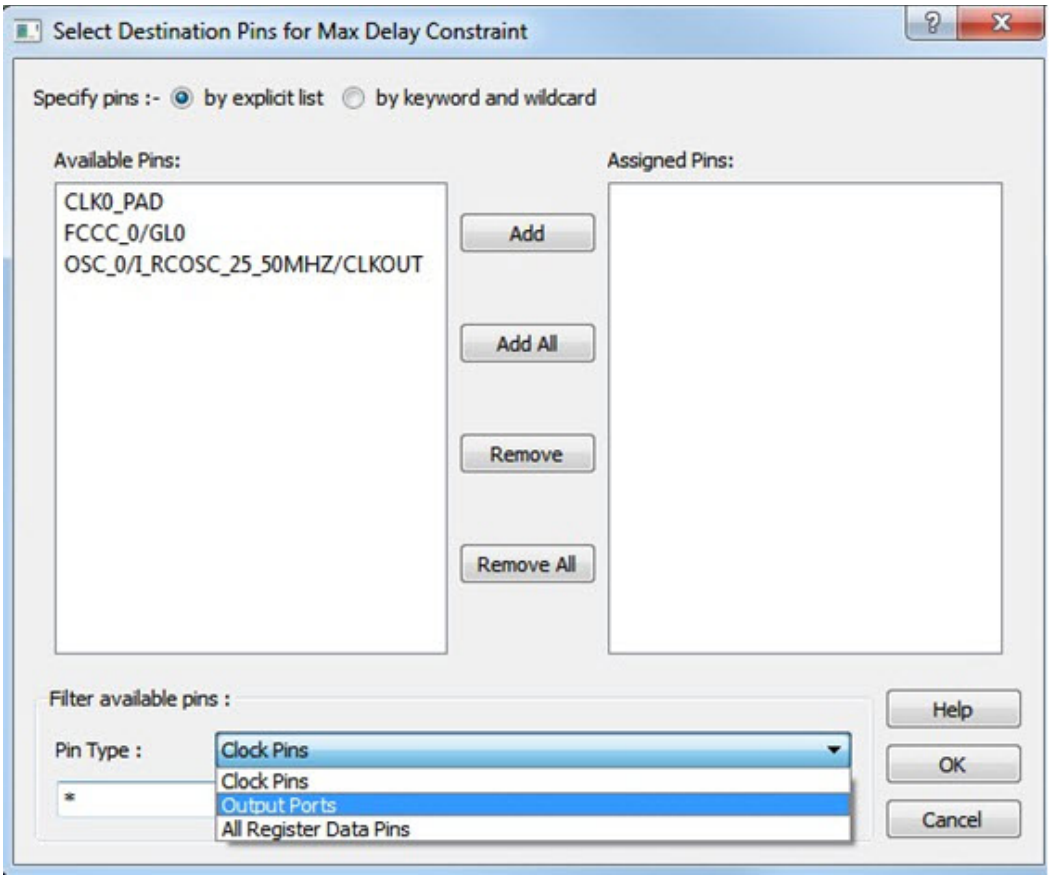


Figure 18 · Select Destination Pins for Max Delay Constraint Dialog Box

The available Pin Type options are:

- Clock Pins
- Output Ports
- All Register Data Pins

Comment

Enter a one-line comment for the constraint.

See Also

Timing Exceptions Overview

Set a Minimum Delay Constraint

Set the options in the Mimimum Delay Constraint dialog box to relax or to tighten the original clock constraint requirement on specific paths.

SmartTime automatically derives the individual minimum delay targets from clock waveforms and port input or output delays. So the minimum delay constraint is a timing exception. This constraint overrides the default single cycle timing relationship for one or more timing paths. This constraint also overrides a multiple cycle path constraint.

Note: When the same timing path has more than one timing exception constraint, SmartTime honors the timing constraint with the highest precedence and ignores the other timing exceptions according to the order of precedence shown.

Timing Exception Constraints	Order of Precedence
set_disable_timing	1
set_false_path	2
set_maximum_delay/set_minimum_delay	3
set_multicycle_path	4

Note: The set_maximum_delay_constraint has a higher precedence over set_multicycle_path constraint and therefore the former overrides the latter when both constraints are set on the same timing path.

To set a Minimum Delay constraint, open the Set Minimum Delay Constraint dialog box in one of the following four ways:

- From the Constraints Browser, choose Min Delay.
- Double-click the Add Min Delay Constraint icon  .
- Choose Min Delay from the Constraints drop-down menu (Constraints > Min Delay).
- Right click on any row in the Min Delay Constraints Table and select Add Minimum Delay Constraint.

The Set Minimum Delay Constraint dialog box appears.

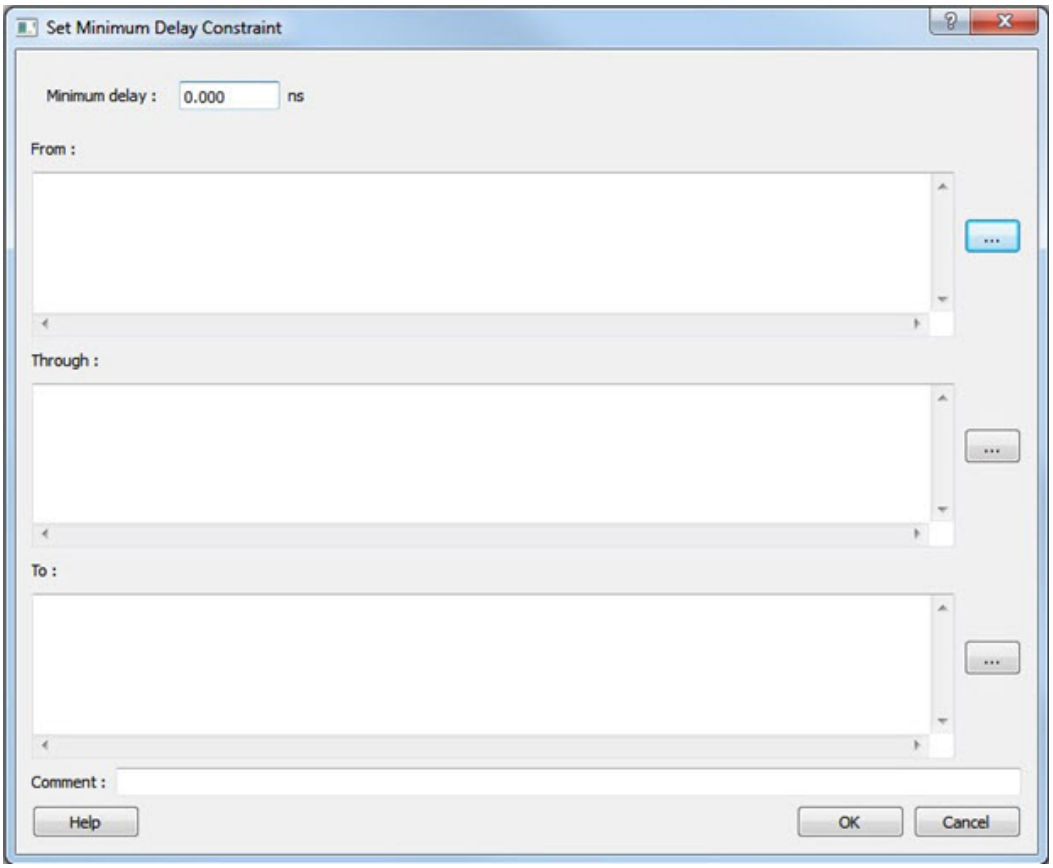


Figure 19 · Set Minimum Delay Constraint Dialog Box

Minimum Delay

Specifies a floating point number in nanoseconds that represents the required minimum delay value for specified paths.

If the path starting point is on a sequential device, SmartTime includes clock skew in the computed delay.

If the path starting point has an input delay specified, SmartTime adds that delay value to the path delay.

If the path ending point is on a sequential device, SmartTime includes clock skew and library setup time in the computed delay.

If the ending point has an output delay specified, SmartTime adds that delay to the path delay.

Source Pins/From

Specifies the starting point for minimum delay constraint. A valid timing starting point is a clock, a primary input, an input port, or a clock pin of a sequential cell.

Click the browse button next to the “From” field to open the Select Source Pins for Min Delay Constraint dialog box.

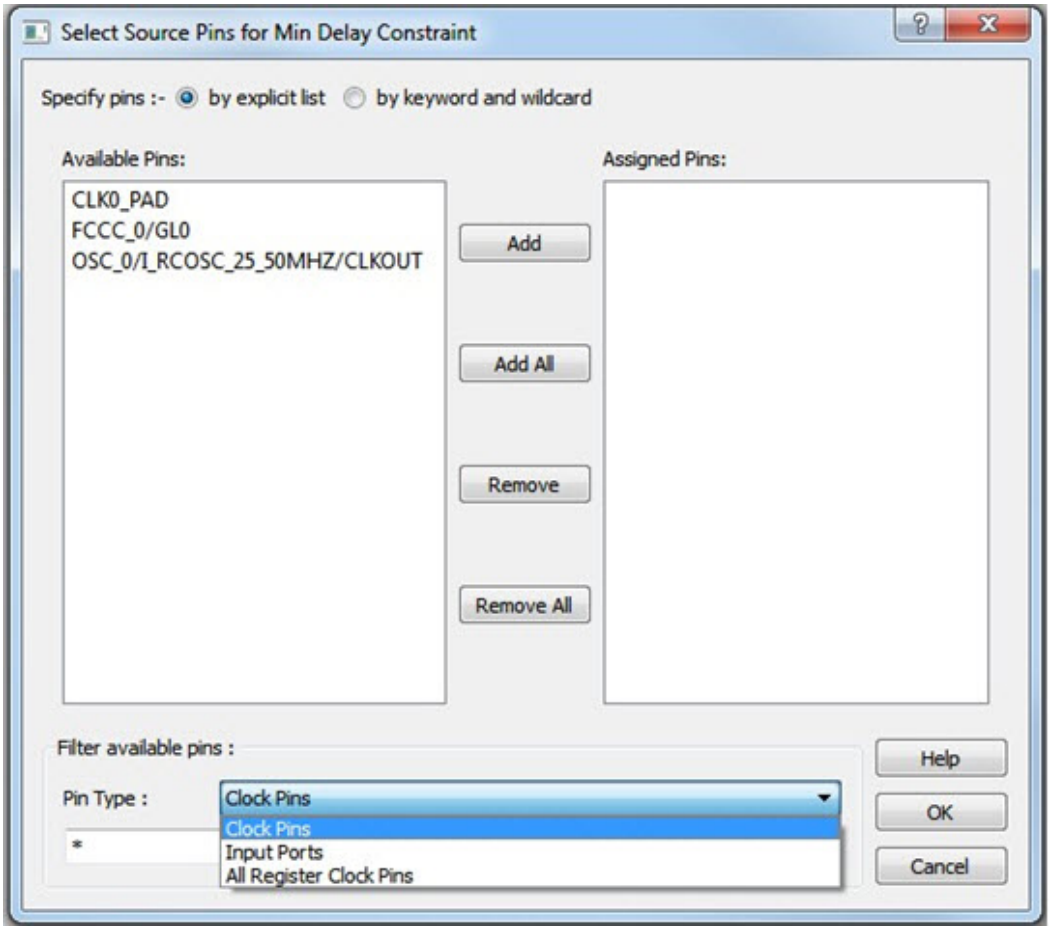


Figure 20 · Select Source Pins for Min Delay Constraint Dialog Box

The available Pin Type options are:

- Clock Pins
- Input Ports
- All Register Clock Pins

Through Pins

Specifies the through points for the Minimum Delay constraint.

Click the browse button next to the “Through” field to open the Select the Through Pins for Min Delay dialog box.

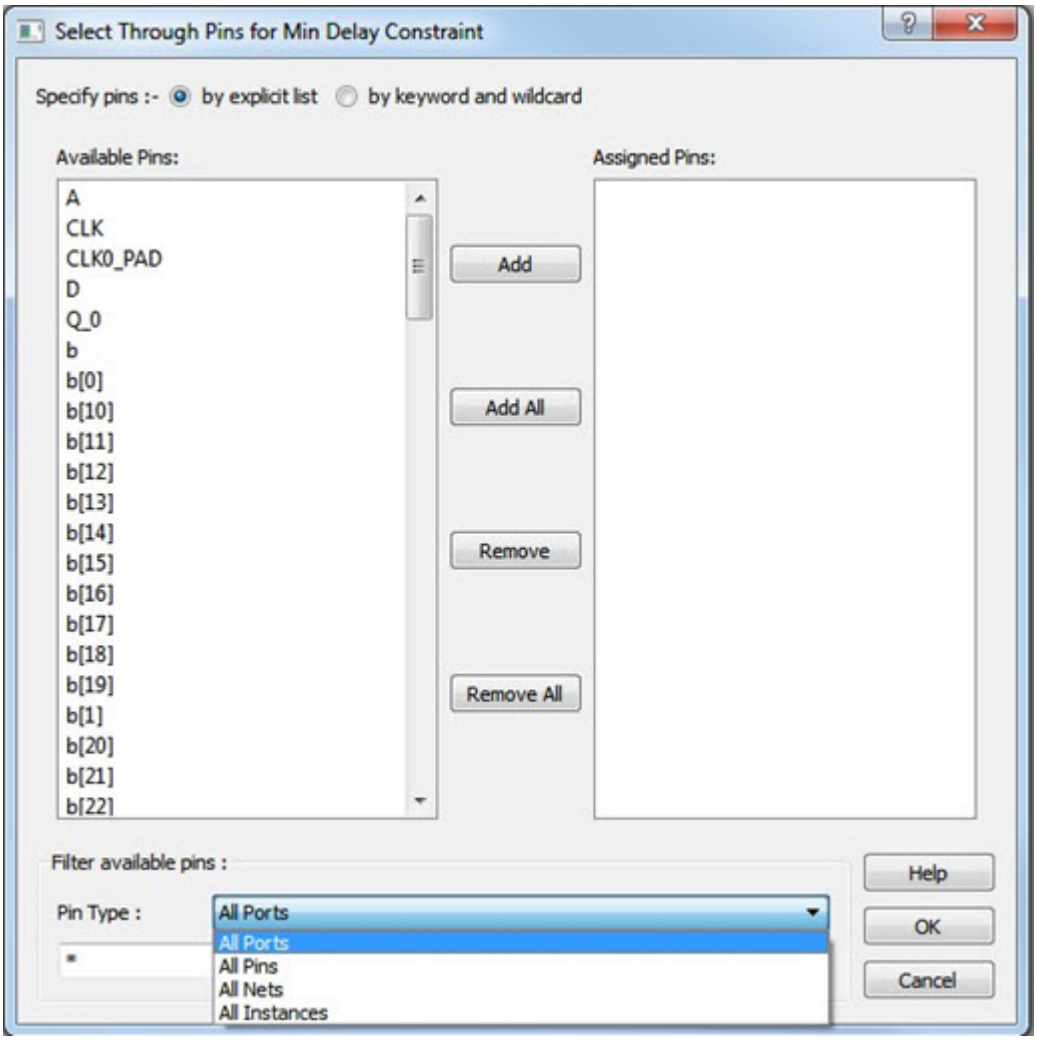


Figure 21 · Select the Through Pins for Min Delay Dialog Box

The available Pin Type options are:

- All Ports
- All Pins
- All Nets
- All Instances

Destination Pins

Specifies the ending points for minimum delay constraint. A valid timing ending point is a clock, a primary output, or a data pin of a sequential cell.

Click the browse button next to the “To” field to open the Select the Destination Pins for Min Delay Constraint dialog box.

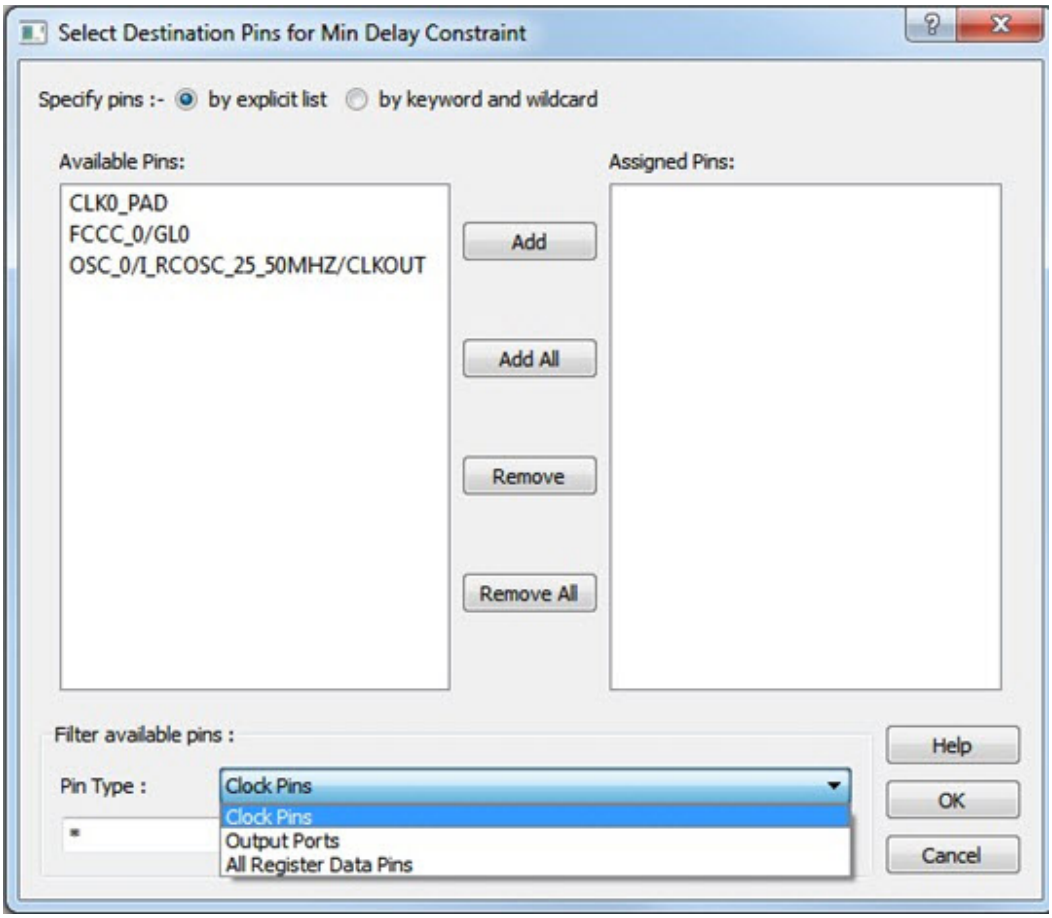


Figure 22 · Select the Destination Pins for Min Delay Constraint Dialog Box

The available Pin Type options are:

- Clock Pins
- Output Ports
- All Register Data Pins

Comment

Enter a one-line comment for the Constraint.

See Also

Timing Exceptions Overview

Specifying Minimum Delay Constraints

set_min_delay (SDC)

Set a Multicycle Constraint

Set the options in the Set Multicycle Constraint dialog box to specify paths that take multiple clock cycles in the current design.

Setting the multiple-cycle path constraint overrides the single-cycle timing relationships (the default) between sequential elements by specifying the number of cycles (two or more) that the data path must have for setup or hold checks.

Note: The false path information always takes precedence over multiple cycle path information. A specific maximum delay constraint overrides a general multiple cycle path constraint.

To set a multicycle constraint, open the Set Multicycle Constraint dialog box in one of the following four ways:

- From the Constraints Browser, choose **Multicycle**.
- Double-click the Add Multicycle Constraint icon  .
- Choose Multicycle from the Constraints drop-down menu (**Constraints > Multicycle**).
- Right-click any row in the Multicycle Constraints Table and choose **Add Multicycle Path Constraint**.

The Set Multicycle Constraint dialog box appears.

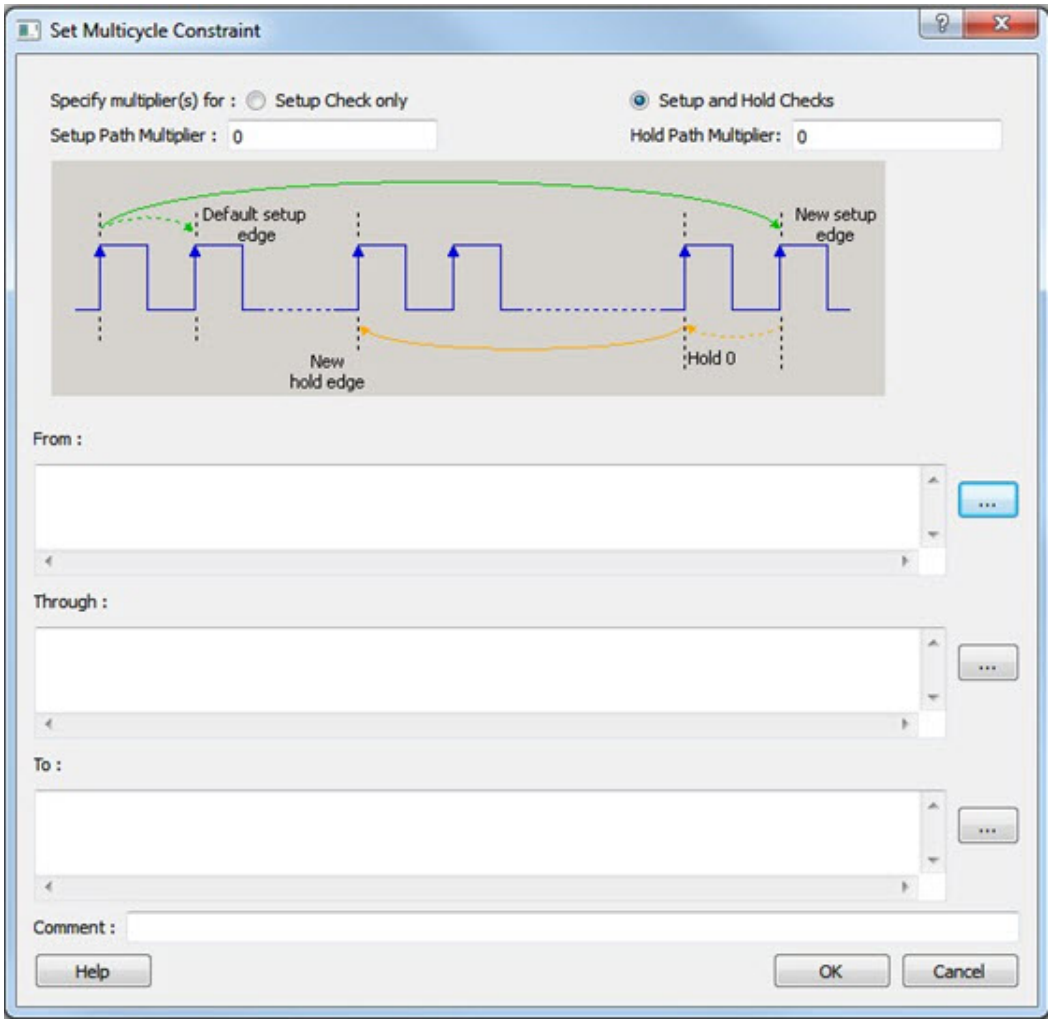


Figure 23 · Set Multicycle Constraint Dialog Box

Setup Check Only

Check this box to apply multiple clock cycle timing consideration for Setup Check only.

Setup and Hold Checks

Check this box to apply multiple clock cycle timing consideration for both Setup and Hold Checks.

Setup Path Multiplier

Specifies an integer value that represents the number of clock cycles (more than one) the data path must have for a setup check.

Hold Path Multiplier

Specifies an integer value that represents the number of clock cycles (more than one) the data path must have for a Hold check.

Source Pins/From Pins

Specifies the starting points for the multiple cycle path. A valid starting point is a clock, a primary input, an inout port, or the clock pin of a sequential cell.

Click the browse button next to the “From” field to open the Select Source Pins for Multicycle Constraint dialog box.

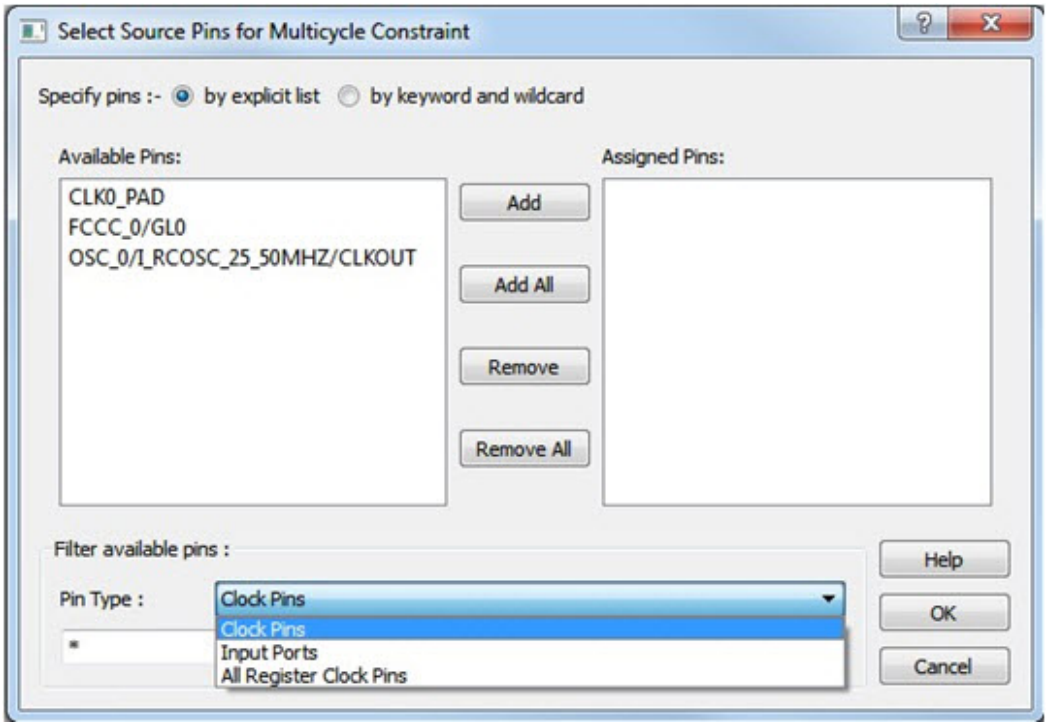


Figure 24 · Select Source Pins for Multicycle Constraint Dialog Box

The available Pin Type options are:

- Clock Pins
- Input Ports
- All Register Clock Pins

Through Pins

Click the browse button next to the “Through” field to open the Select Through Pins for Multicycle Constraint dialog box. The Select Through Pins for Multicycle Constraint dialog box appears.

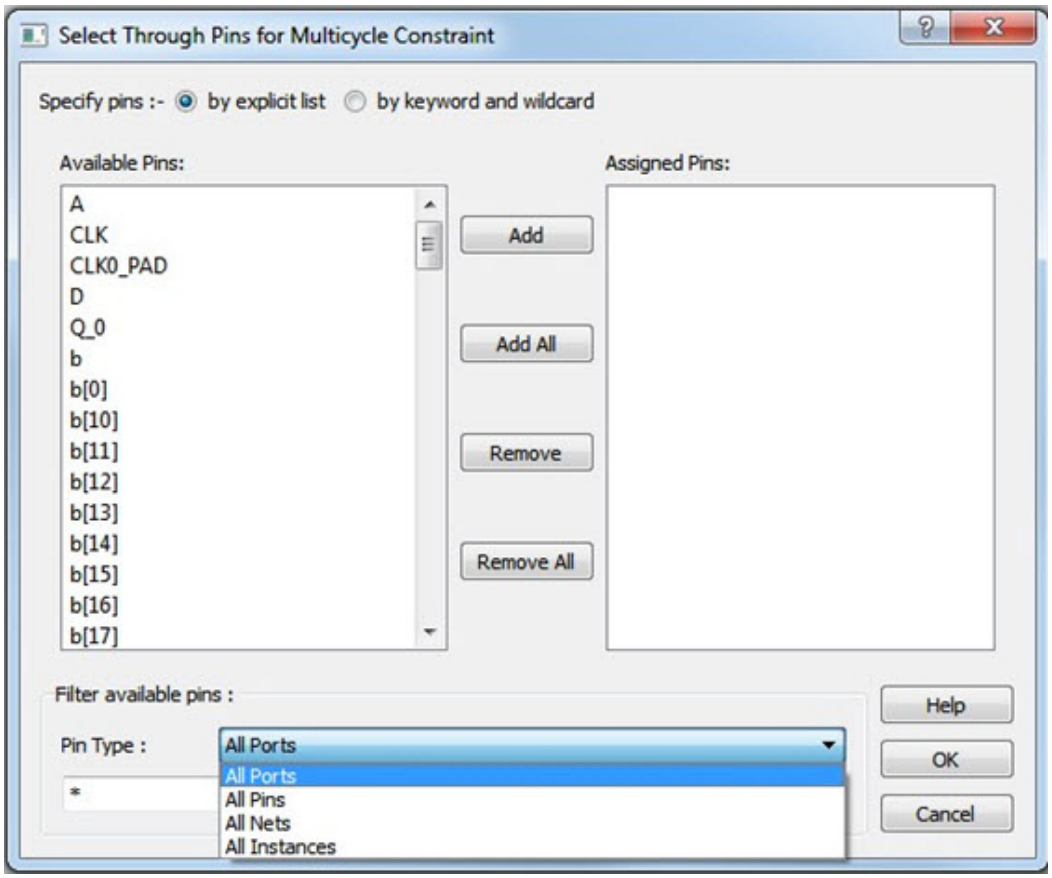


Figure 25 · Select Through Pins for Multicycle Constraint Dialog Box

The available Pin Type options are:

- All Ports
- All Pins
- All Nets
- • AllInstances

Destination/To Pins

Click the browse button next to the “To” field to open the Select Destination Pins for Multicycle Constraint dialog box.

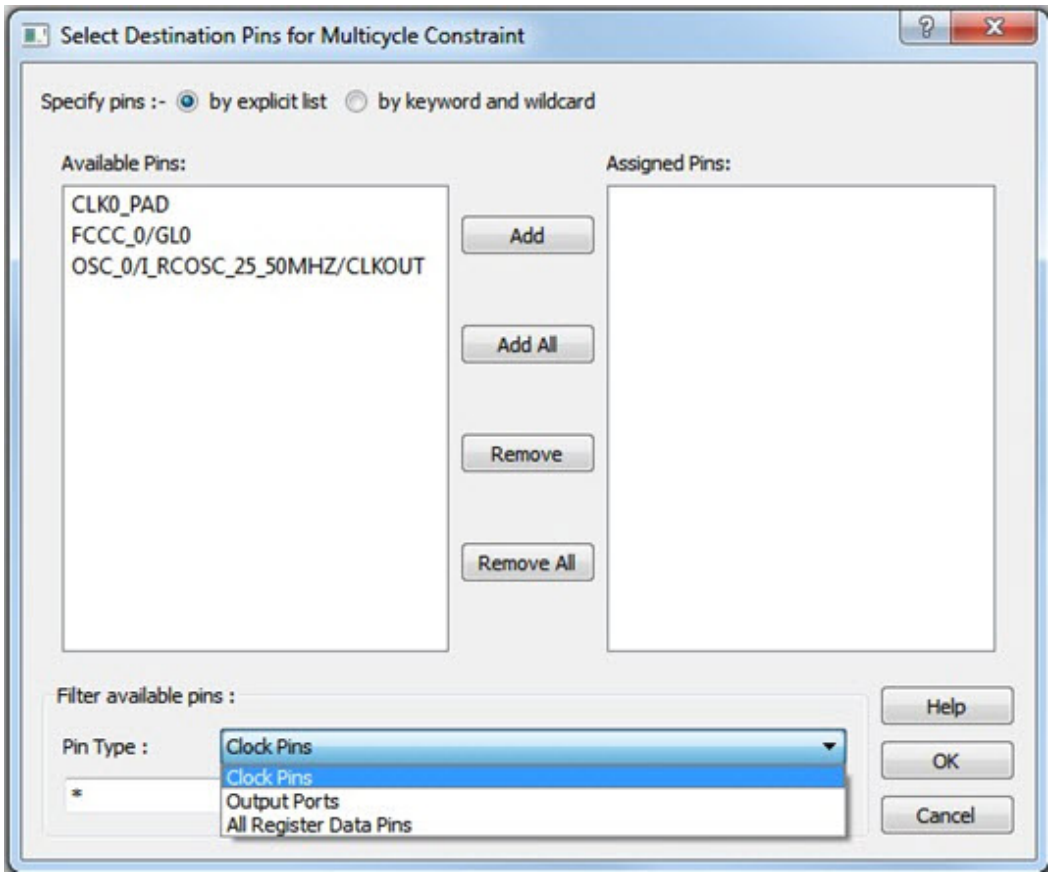


Figure 26 · Select Destination Pins for Multicycle Constraint Dialog Box

The available Pin Type options are:

- Clock Pins
- Output Ports
- All Register Data Pins

Comment

Enter a one-line comment for the constraint.

See Also

Specifying a Multicycle Constraint

set_multicycle_path (SDC)

Set a False Path Constraint

Set options in the Set False Path Constraint dialog box to define specific timing paths as false path.

This constraint removes timing requirements on these false paths so that they are not considered during the timing analysis. The path starting points are the input ports or register clock pins and path ending points are the register data pins or output ports. This constraint disables setup and hold checking for the specified paths.

Note: When the same timing path has more than one timing exception constraint, SmartTime honors the timing constraint with the highest precedence and ignores the other timing exceptions according to the order of precedence shown below.

Timing Exception Constraints	Order of Precedence
set_disable_timing	1
set_false_path	2
set_maximum_delay/set_minimum_delay	3
set_multicycle_path	4

Note: The set_false_path constraint has the second highest precedence and always overrides the set_multicycle_path constraints and set_maximum/minimum_delay constraints.

To set a false path constraint, open the Set False Path Constraint dialog box in one of the following four ways:

- From the Constraints Browser, choose **False Path**.
- Double-click the Add False Path Constraint icon  .
- Choose **False Path** from the Constraints drop-down menu (**Constraints > False Path**).
- Right-click any row in the False Path Constraints Table and choose **Add False Path Constraint**.

The Set False Path Constraint dialog box appears.

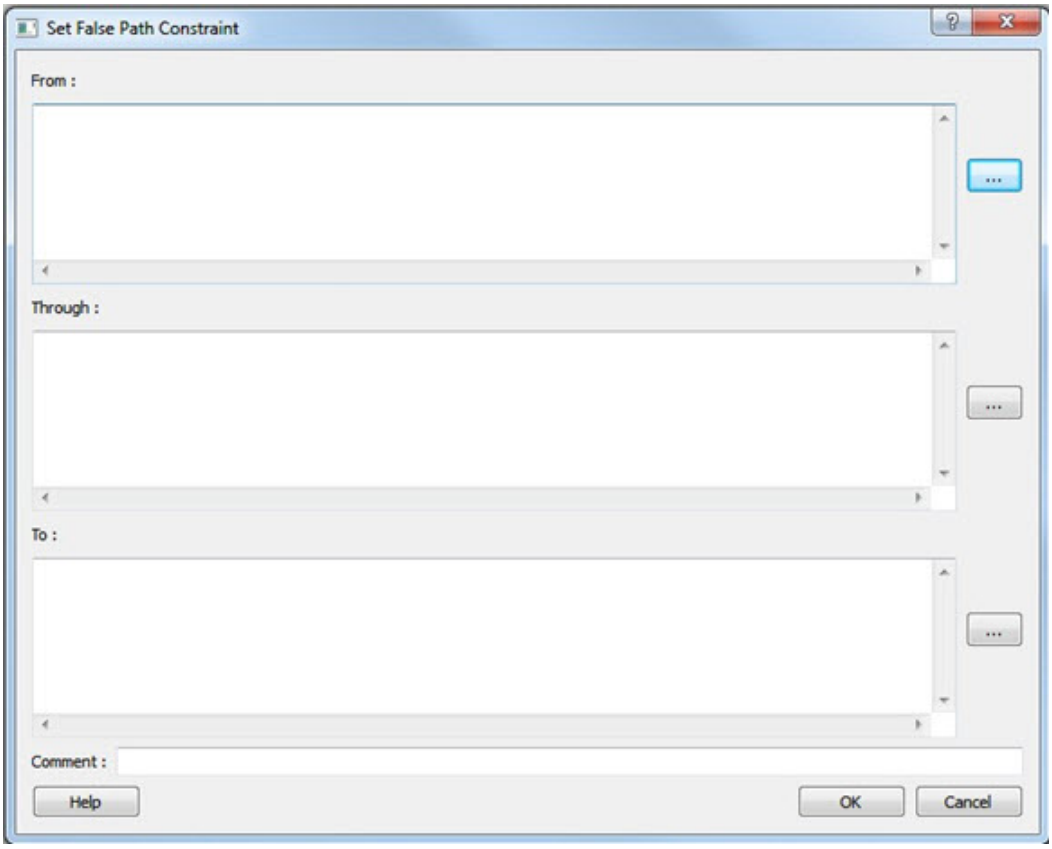


Figure 27 · Set False Path Constraint Dialog Box

Source/From Pins

To select the Source Pin(s), click the browse button next to the “From” field and open the Select Source Pins for False Path Constraint dialog box.

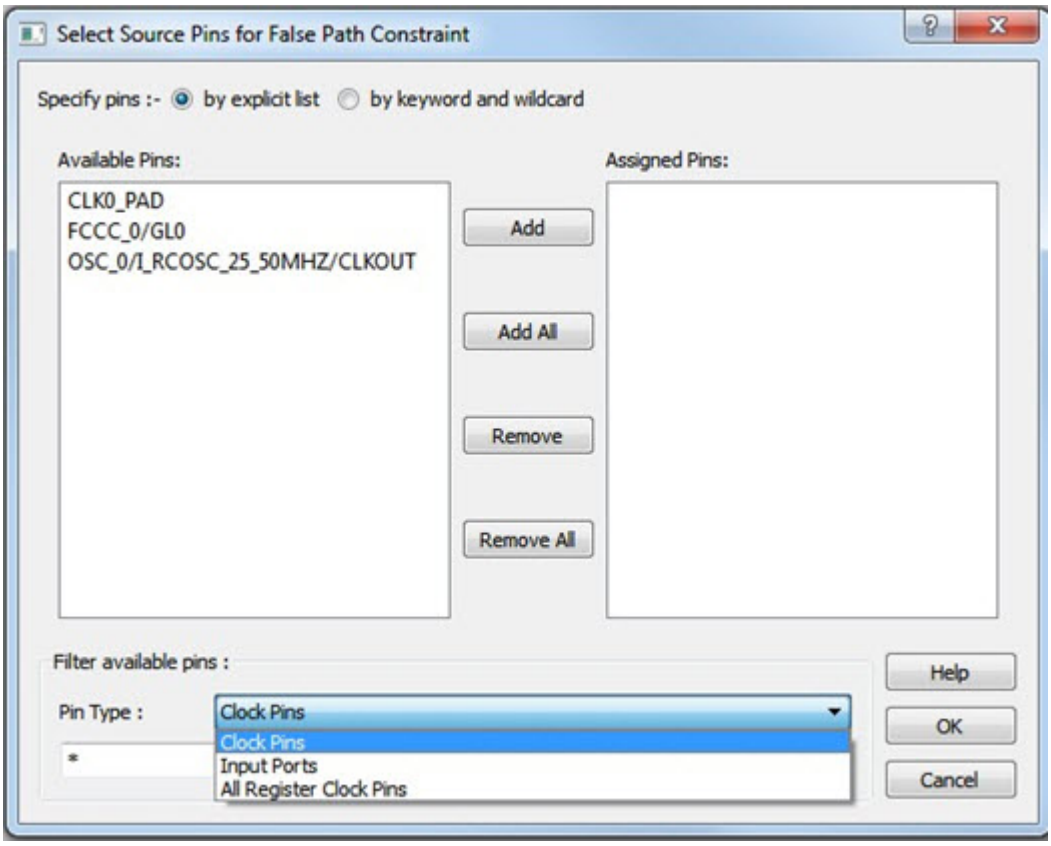


Figure 28 · Select Source Pins for False Path Constraint Dialog Box

The available options for Pin Type are:

- Clock Pins
- Input Ports
- All Register Clock Pins

Through Pins

Specifies a list of pins, ports, cells, or nets through which the false paths must pass.

To select the Through pin(s), click the browse button next to the “Through” field to open the Select Through Pins for False Path Constraint dialog box.

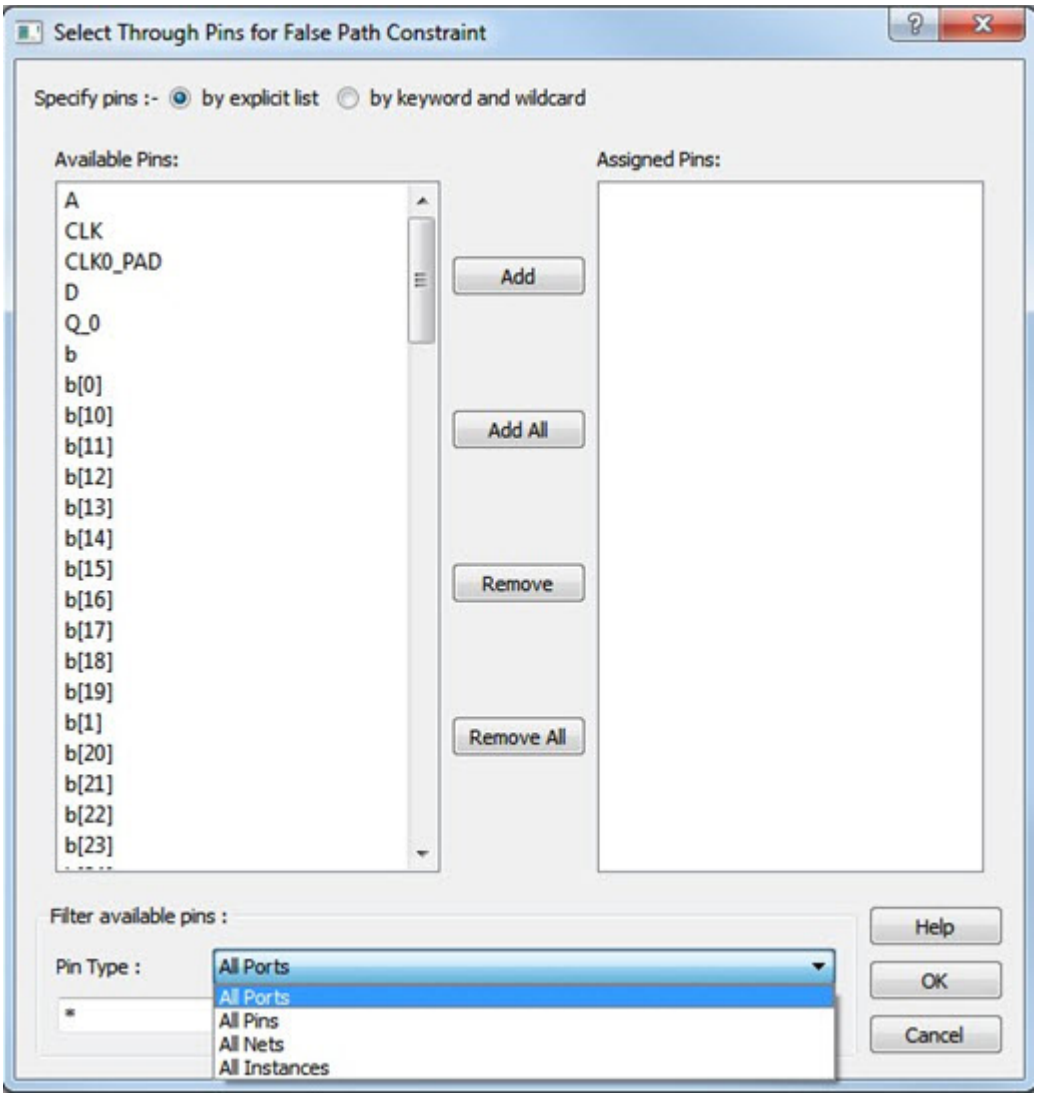


Figure 29 · Select Through Pins for False Path Constraint Dialog Box

The available options for Pin Type are:

- All Ports
- All Pins
- All Nets
- All Instances

Destination/To Pins

To select the Destination Pin(s), click the browse button next to the “To” field to open the Select Destination Pins for False Path Constraint dialog box.

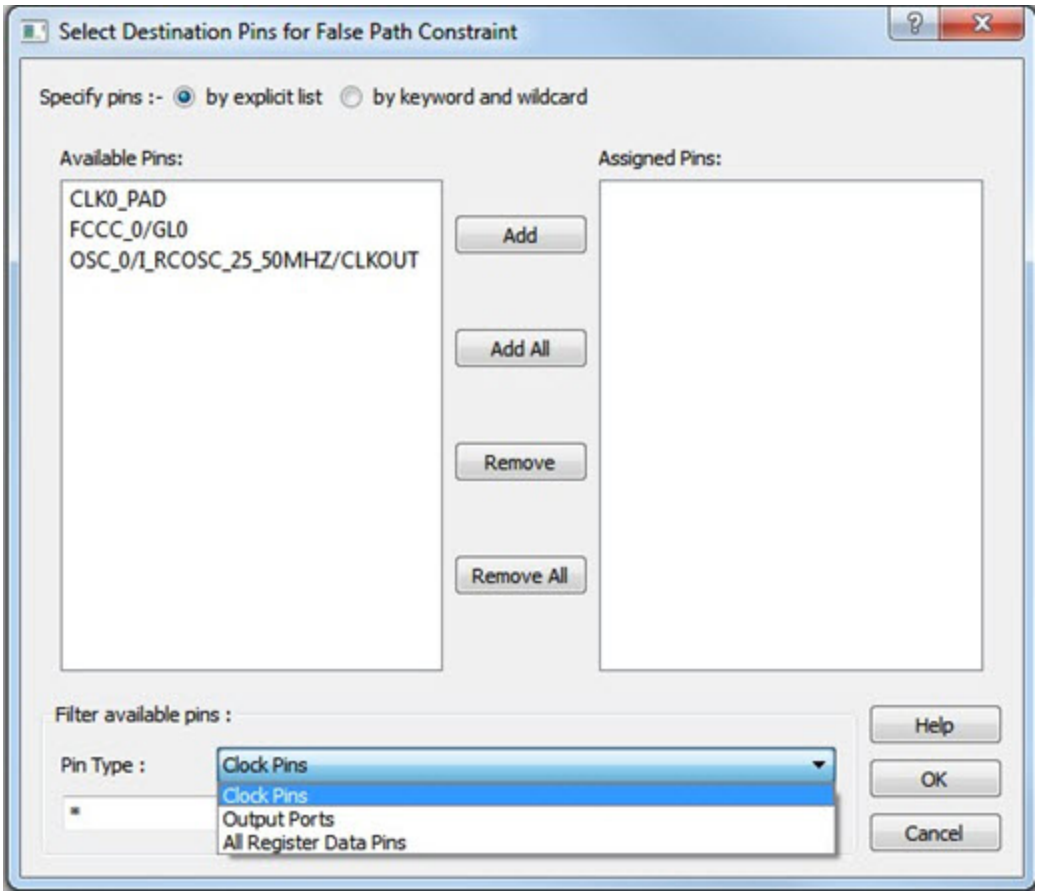


Figure 30 · Select Destination Pins for False Path Constraint Dialog Box

The available options for Pin Type are:

- Clock Pins
- Output Ports
- All Register Data Pins

Comment

Enter a one-line comment for the constraint.

See Also

Specifying False Path Constraints

set_false_path (SDC)

Advanced Constraints

Set a Disable Timing Constraint

Use disable timing constraint to specify the timing arcs to be disabled for timing consideration.

Note: This constraint is for the Place and Route tool and the Verify Timing tool. It is ignored by the Synthesis tool.

To specify a Disable Timing constraint, open the Set Constraint to Disable Timing Arcs dialog box in one of the following four ways:

- From the Constraints Browser, choose **Advanced > Disable Timing**.
- Double-click the Add Disable Timing Constraint icon  .
- Choose **Disable Timing** from the Constraints drop-down menu (**Constraints > Disable Timing**).
- Right-click any row in the Disable Timing Constraints Table and choose **Add Constraint to Disable Timing**.

The Set Constraint to Disable Timing Arcs dialog box appears.

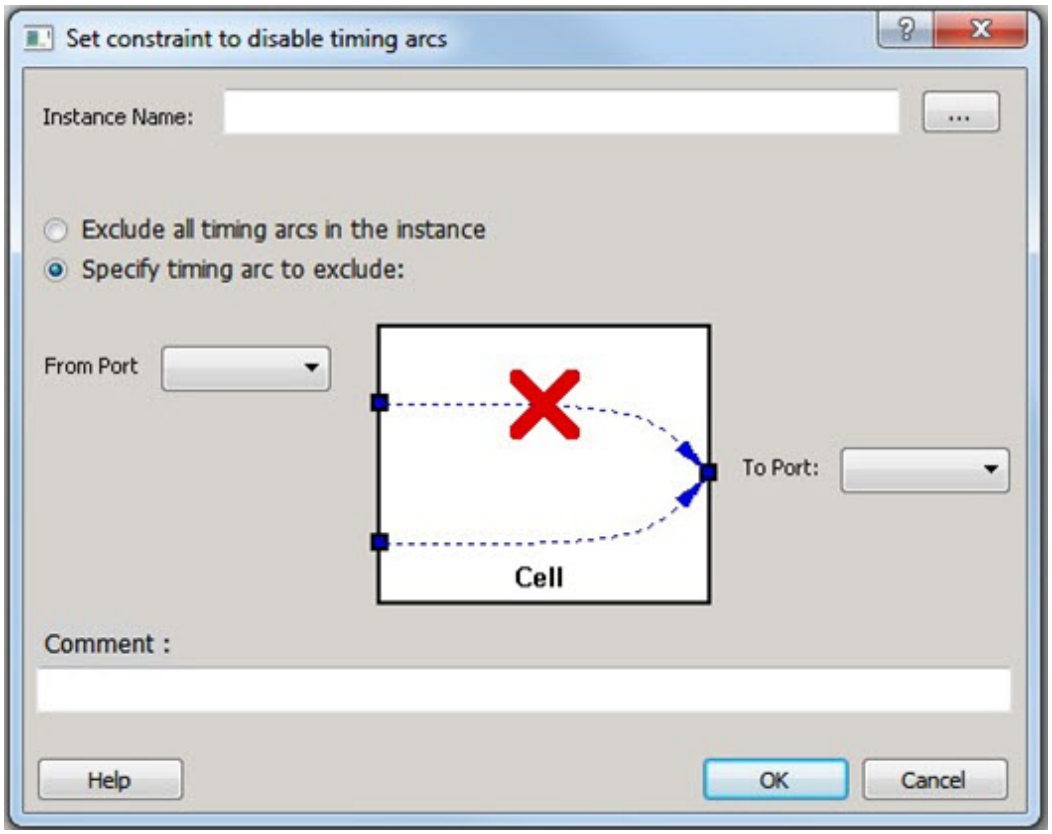


Figure 31 · Set Constraint to Disable Timing Arcs Dialog Box

Instance Name

Specifies the instance name for which the disable timing arc constraint will be created.

Click the browse button next to the Instance Name field to open the Select instance to constrain dialog box.

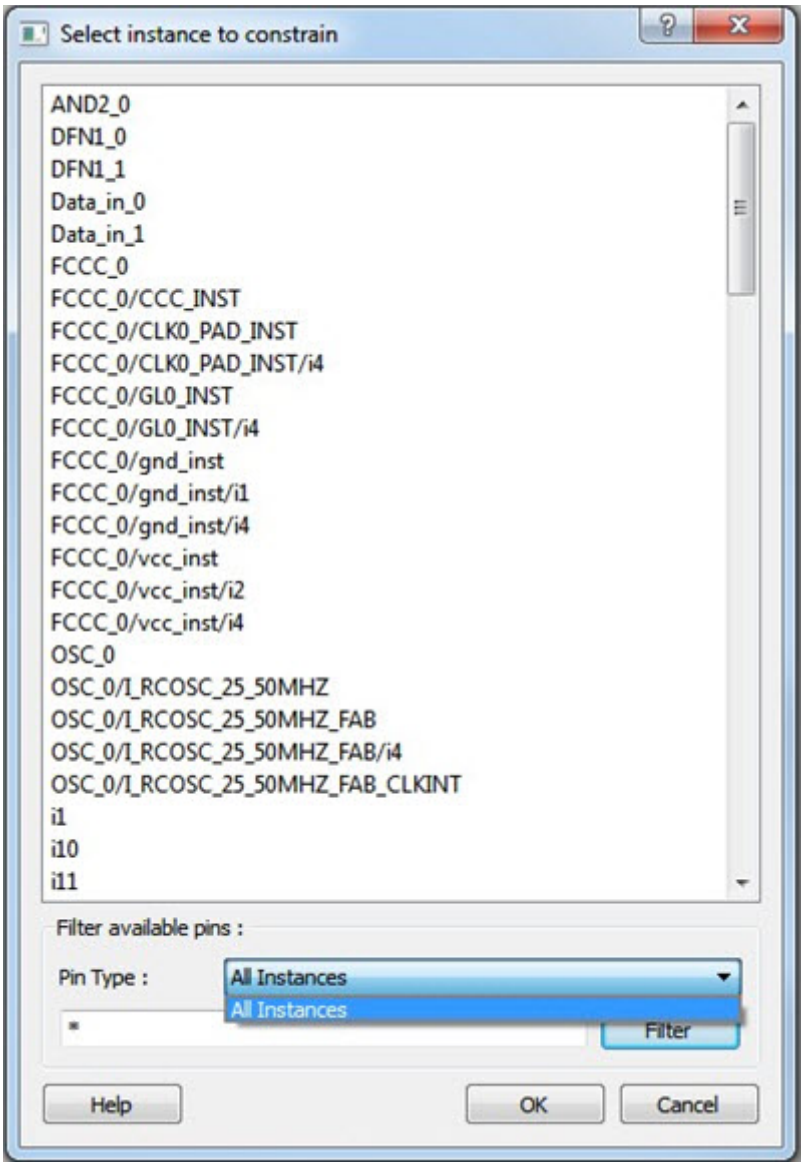


Figure 32 · Set Instance to Constrain Dialog Box

The Pin Type selection is limited to All Instances only.

Exclude All Timing Arcs in the Instance

This option enables you to exclude all timing arcs in the specified instance.

Specify Timing Arc to Exclude

This option enables you to specify the timing arc to exclude. In this case, you need to specify the from and to ports:

From Port

Specifies the starting point for the timing arc.

To Port

Specifies the ending point for the timing arc.

Comment

Enter a one-line comment for the constraint.

See Also

Specifying Disable Timing Constraint

Set Clock Source Latency Constraint

Use clock source latency constraint to specify the delay from the clock generation point to the clock definition point in the design.

Clock source latency defines the delay between an external clock source and the definition pin of a clock. It behaves much like an input delay constraint.

You can specify both an "early" delay and a "late" delay for this latency, providing an uncertainty which the timing analyzer can use for propagating through its calculations. Rising and falling edges of the same clock can have different latencies. If only one value is provided for the clock source latency, it is taken as the exact latency value, for both rising and falling edges.

To specify a Clock Source Latency constraint, open the Set Clock Source Latency Constraint dialog box in one of the following four ways:

- From the Constraints Browser, choose **Clock Source Latency**.
- Double-click the Clock Source Latency Constraint icon  .
- Choose **Clock Source Latency** from the Constraints drop-down menu (**Constraints > Advanced > Clock Source Latency**).
- Right-click any row of the Clock Latency Constraints Table and choose **Add Clock Source Latency**.

The Set Clock Source Latency Constraint dialog box appears.

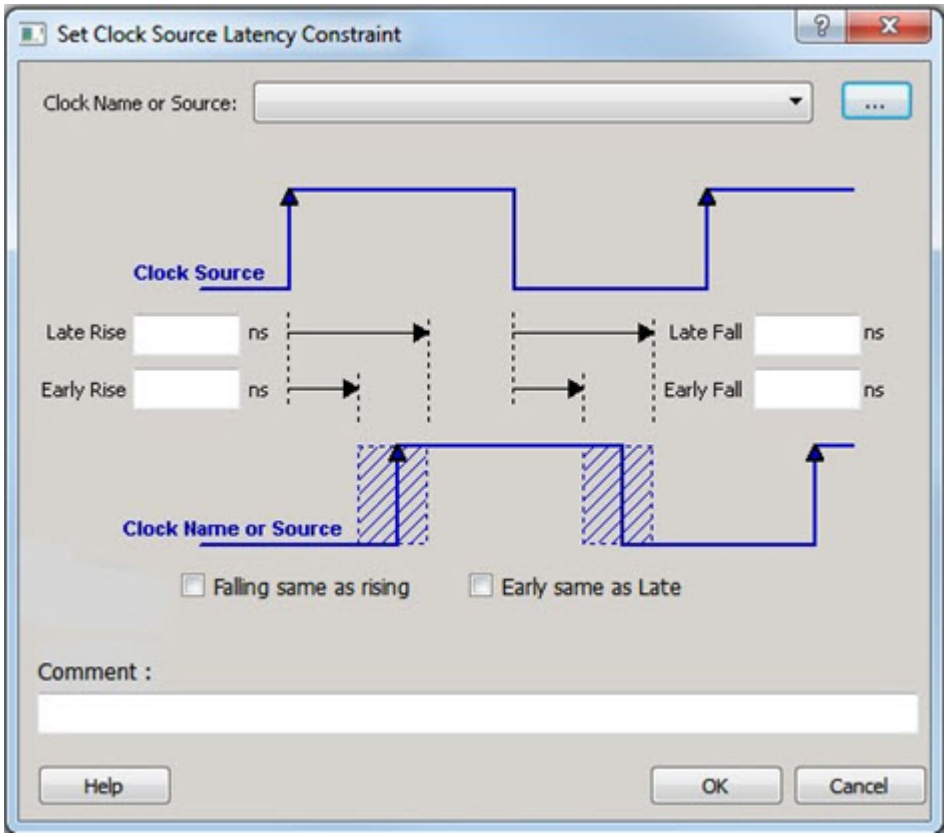


Figure 33 · Set Clock Source Latency Constraint Dialog Box

To select the Clock Source, click on the browser button to open the Choose the Clock Source Pin dialog box:

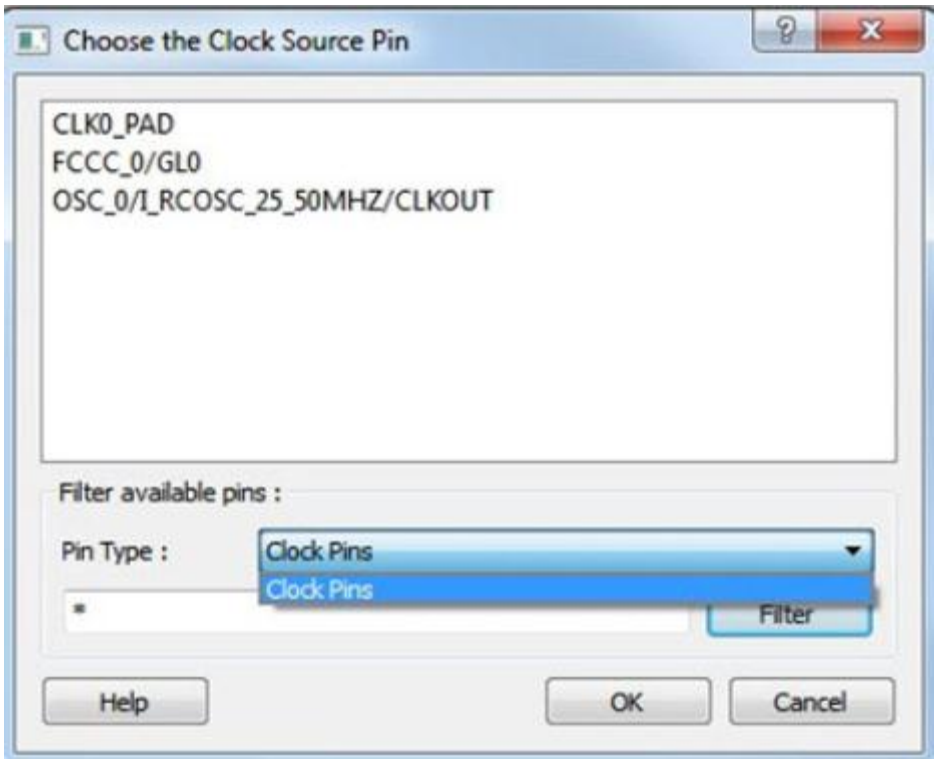


Figure 34 · Choose the Clock Source Pin Dialog Box

The only choice available for Pin Type is Clock Pins.

Late Rise

Specifies the largest possible latency, in nanoseconds, of the rising clock edge at the clock port or pin selected, with respect to its source. Negative values are acceptable, but may lead to overly optimistic analysis.

Early Rise

Specifies the smallest possible latency, in nanoseconds, of the rising clock edge at the clock port or pin selected, with respect to its source. Negative values are acceptable, but may lead to overly optimistic analysis.

Late Fall

Specifies the largest possible latency, in nanoseconds, of the falling clock edge at the clock port or pin selected, with respect to its source. Negative values are acceptable, but may lead to overly optimistic analysis.

Early Fall

Specifies the smallest possible latency, in nanoseconds, of the falling clock edge at the clock port or pin selected, with respect to its source. Negative values are acceptable, but may lead to overly optimistic analysis.

Clock Edges

Select the latency for the rising and falling edges:

Falling same as rising: Specifies that Rising and Falling clock edges have the same latency.

Early same as late: Specifies that the clock source latency should be considered as a single value, not a range from "early" to '"late".

Comment

Enter a one-line comment to describe the clock source latency.

See Also

Specifying Clock Constraints

Set Clock Latency Constraint

Set Clock-to-Clock Uncertainty Constraint

Use the clock-to-clock uncertainty constraint to model tracking jitter between two clocks in your design.

To specify a Clock-to-Clock Uncertainty constraint, open the Set Clock-to-Clock Uncertainty Constraint dialog box in one of the following four ways:

- From the Constraints Browser, choose **Clock Uncertainty**.
- Double-click the Clock-to-Clock Uncertainty icon  .
- Choose **Clock-to-Clock Uncertainty** from the Constraints drop-down menu (**Constraints > Advanced > Clock-to-Clock Uncertainty**).
- Right-click any row in the Clock Uncertainty Constraints Table and choose **Add Clock-to-Clock Uncertainty**.

The Set Clock-to-Clock Uncertainty Constraint dialog box appears.

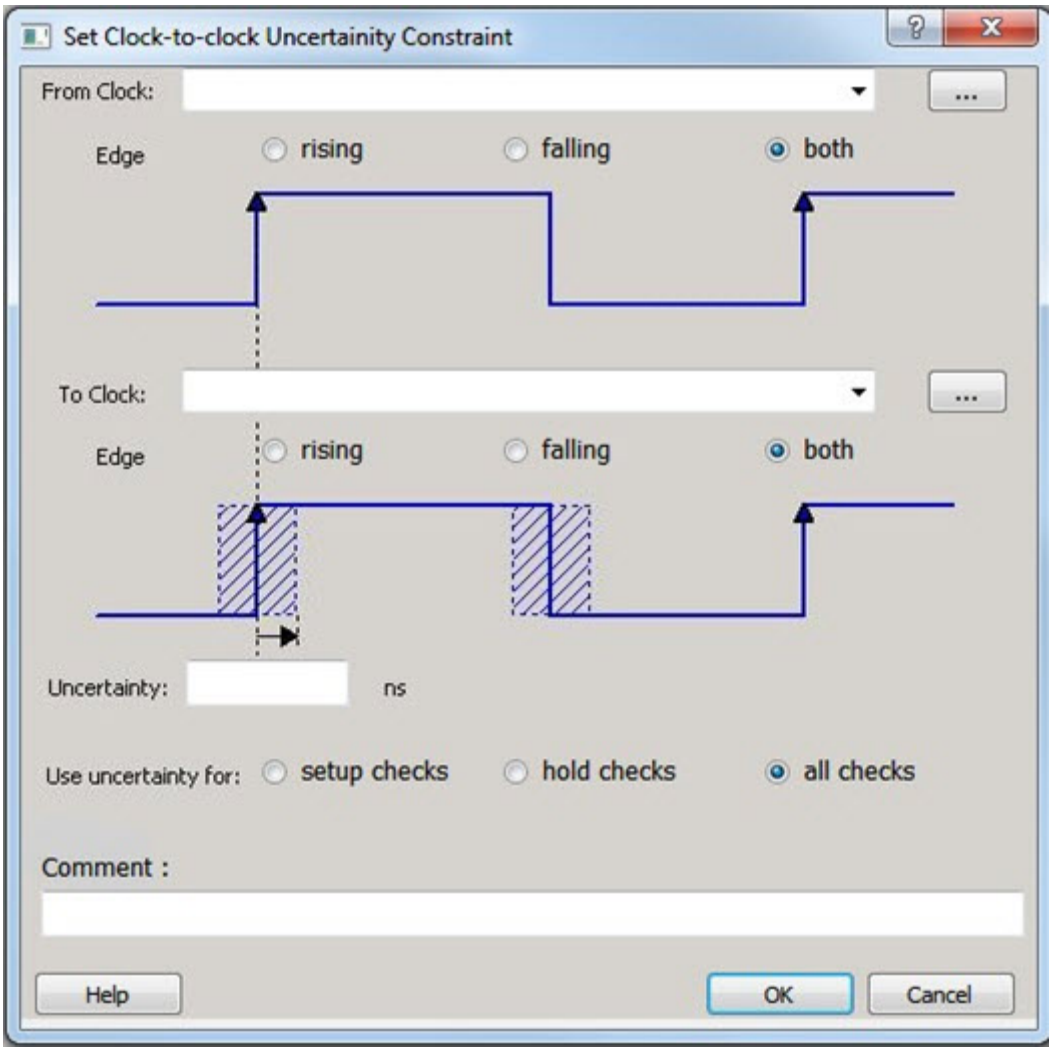


Figure 35 · Set Clock-to-Clock Uncertainty Dialog Box

From Clock

Specifies clock name as the uncertainty source.

To set the From Clock, click the browser button to open the Select Source Clock List for Clock-to-clock Uncertainty dialog box.

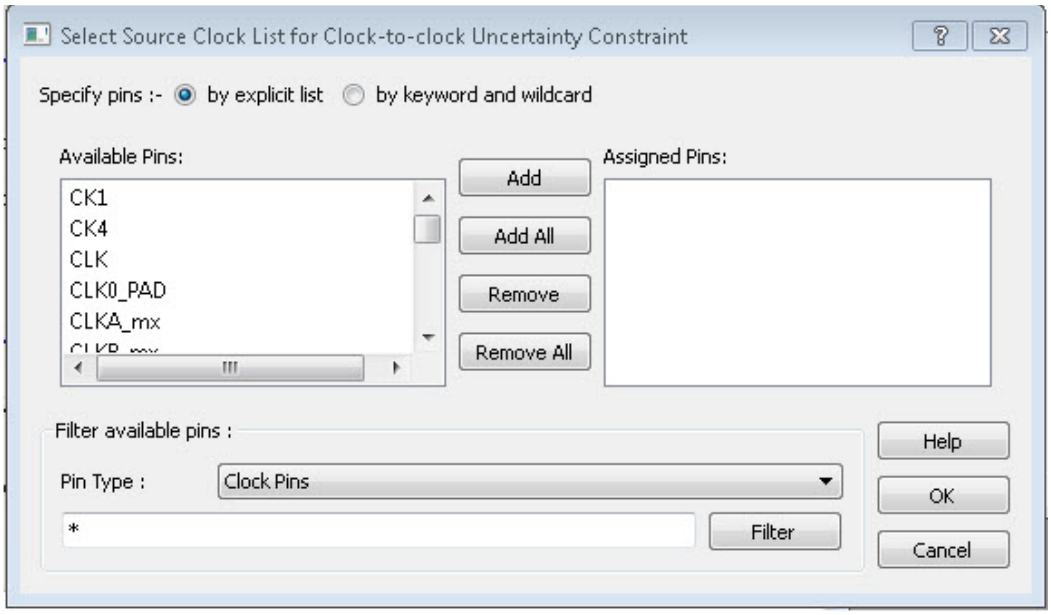


Figure 36 · Select Source Clock List for Clock-to-Clock Uncertainty Dialog Box

The Pin Type selection is for Clock Pins only.

Edge

This option enables you to select if the clock-to-clock uncertainty applies to rising, falling, or both edges.

To Clock

Specifies clock name as the uncertainty destination.

To set the To Clock, click the browser button to open the Select Destination Clock List for Clock-to-clock Uncertainty Constraint dialog box.

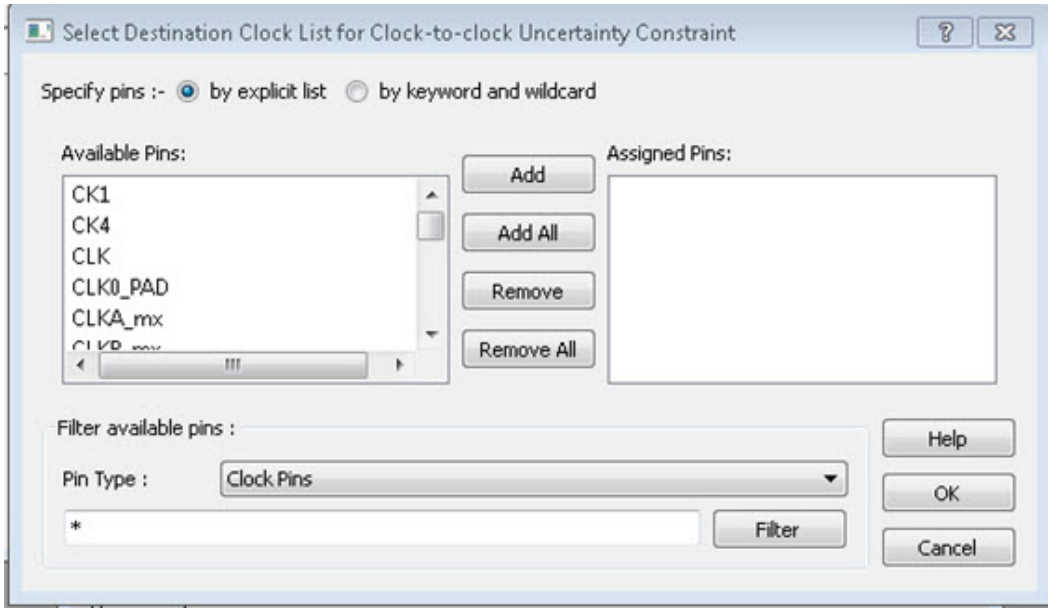


Figure 37 · Select Destination Clock List for Clock-to-Clock Uncertainty Constraint Dialog Box

Edge

This option enables you to select if the clock-to-clock uncertainty applies to rising, falling, or both edges.

Uncertainty

Enter the time in nanoseconds that represents the amount of variation between two clock edges.

Use Uncertainty For

This option enables you select whether the uncertainty constraint applies to setup, hold, or all checks.

Comment

Enter a single line of text that describes this constraint.

To set the Destination Clock, click the browser button to open the Select Destination Clock List for Clock-to-clock Uncertainty Constraint dialog box.

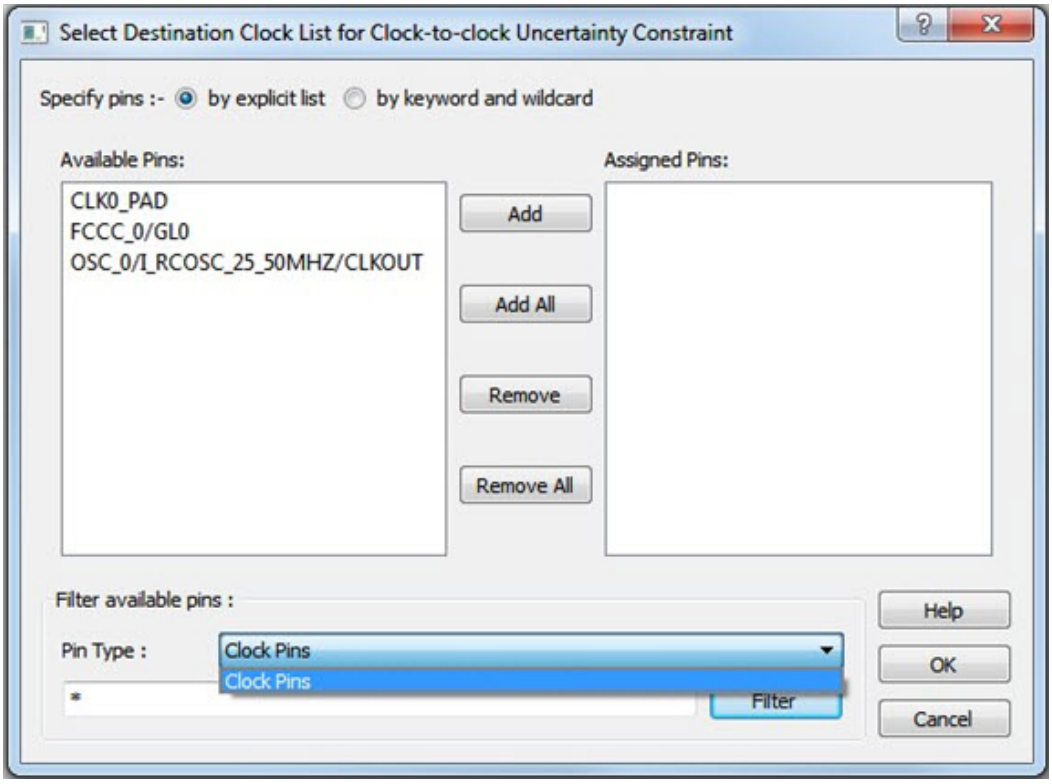


Figure 38 · Select Destination Clock List for Clock-to-Clock Uncertainty Dialog Box

The Pin Type selection is for Clock Pins only.

See Also

Specifying Disable Timing Constraints

set_clock_uncertainty

Set Clock Groups

To add or delete a Clock Group constraint, open the Add Clock Groups Constraint dialog box in one of three ways:

- Select **Clock Groups** from the Constraints drop-down menu (**Constraints > Clock Groups**).
- Double-click **Clock Groups** in the Constraints Browser.
- Right-click any row in the Clock Groups Constraints Table and choose **Add Clock Groups**.

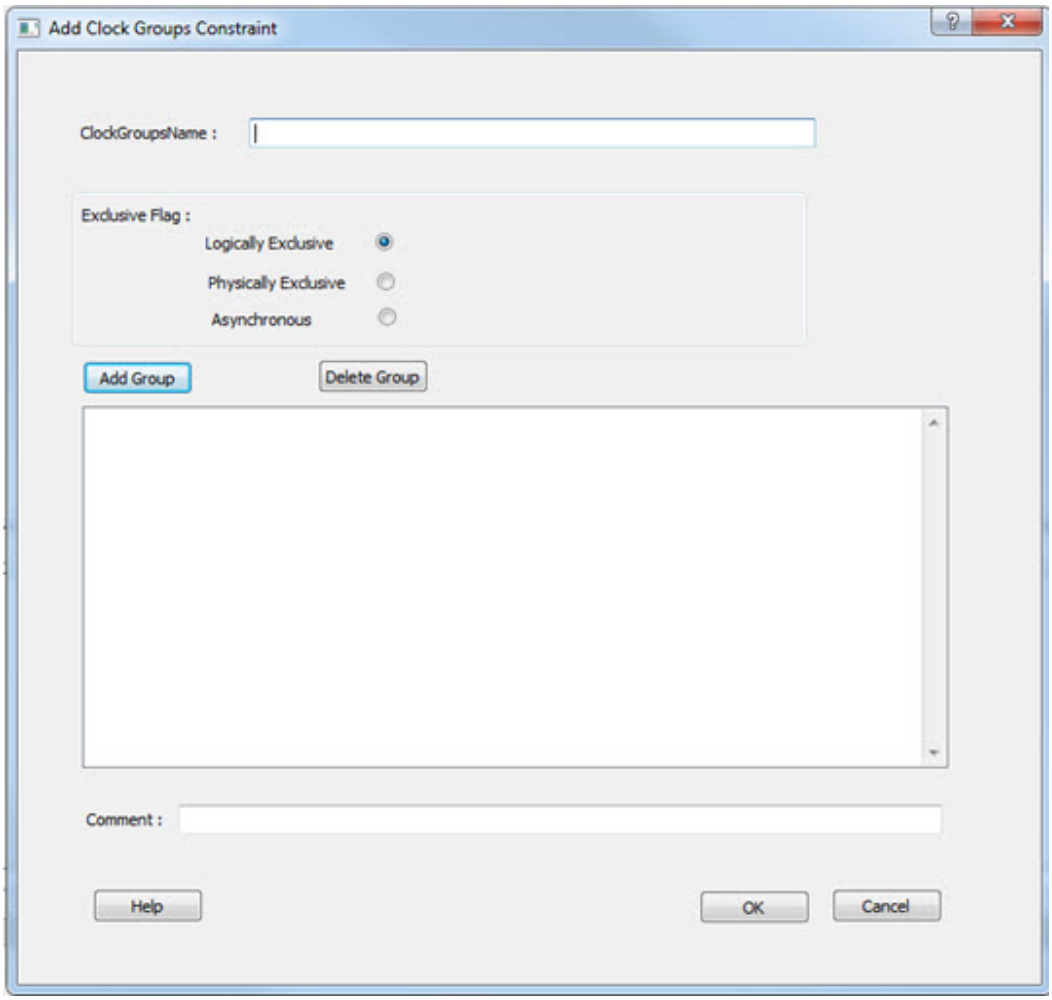


Figure 39 · Add Clock Group Constraints Dialog Box

ClockGroupsName – Enter a name for the Clock Groups to be added.

Exclusive Flag - Choose one of the three clock group attributes for the clock group:

- **Logically Exclusive** - Use this setting for clocks that can exist physically on the device at the same time but are logically exclusive (e.g., multiplexed clocks).
- **Physically Exclusive** - Use this setting for clocks that cannot exist physically on the device at the same time (e.g., multiple clocks defined on the same pin).
- **Asynchronous** – Use this setting when there are valid timing paths between the two clock groups but the two clocks do not have any frequency or phase relationship and therefore these timing paths can be excluded from timing analysis.

Add Group – Click **Add** to open a dialog to add clocks to a clock group. Select the clocks from the Available Pins list and click **Add** to move them to Assigned Pins list. Click **OK**.

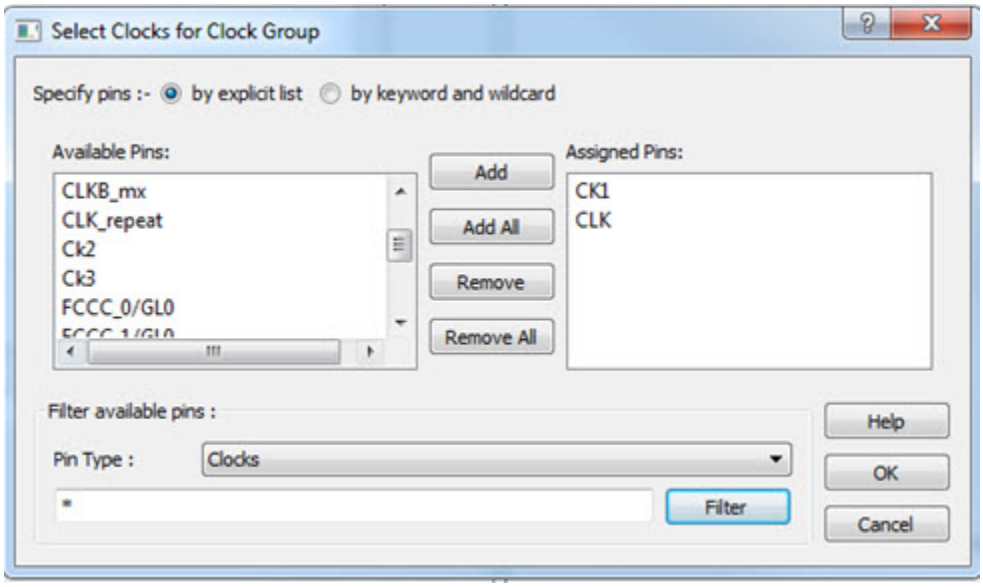


Figure 40 · Add Clocks For Clock Group Dialog Box

Delete Group – Delete the clocks from the Clock Group. Select the group of clock to be deleted and click **Delete Group**. This will delete the clock group.

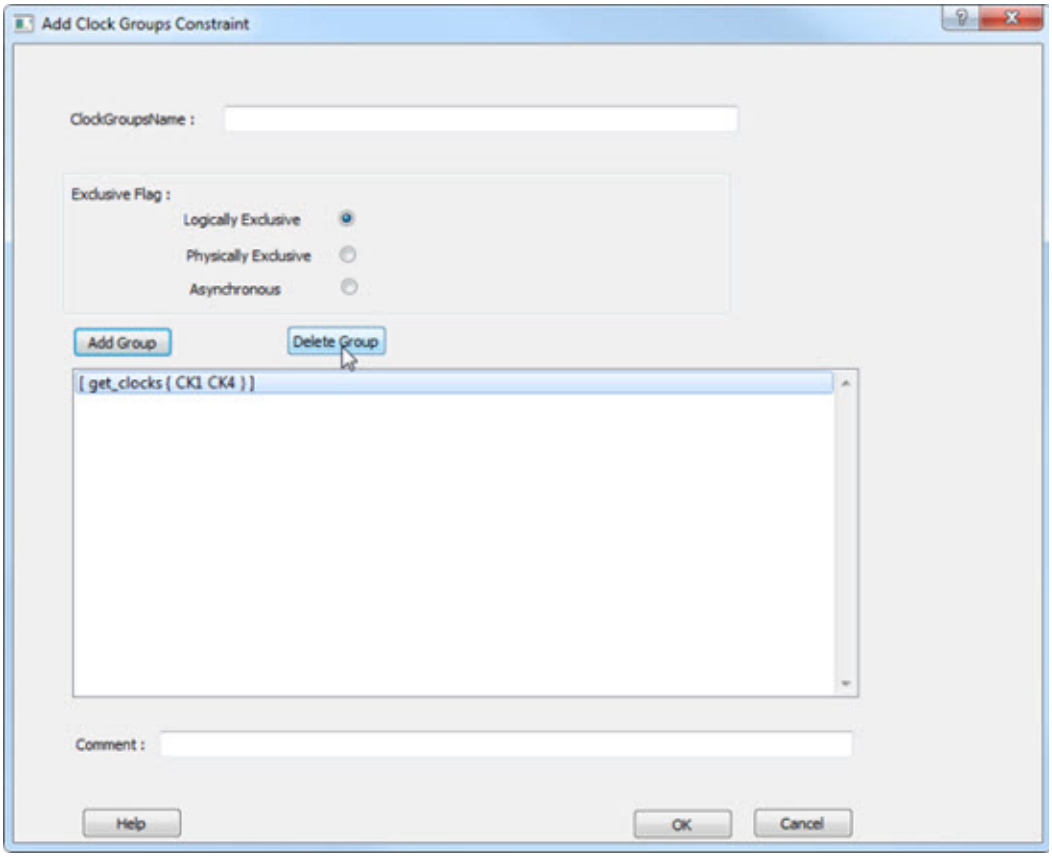


Figure 41 · Delete Group

See Also

set_clock_groups

list_clock_groups

remove_clock_groups

Select Destination Clock for Clock-to-clock Uncertainty Constraint Dialog Box

This dialog box opens when you select the browse button for Destination/To Clock for Clock-to-clock Uncertainty Constraints dialog box.

Use this dialog box to select Clock Pins:

- By explicit list
- By keyword and wildcard

To open the Select Destination Clock dialog box, double-click **Constraint > Advanced > Clock Uncertainty**. Click the browse button next to the To Clock field to select the Destination Clock Pin.

By Explicit List

This is the default. This mode stores the actual Clock Pin names. The following figure shows an example dialog box for Select Destination Clock.

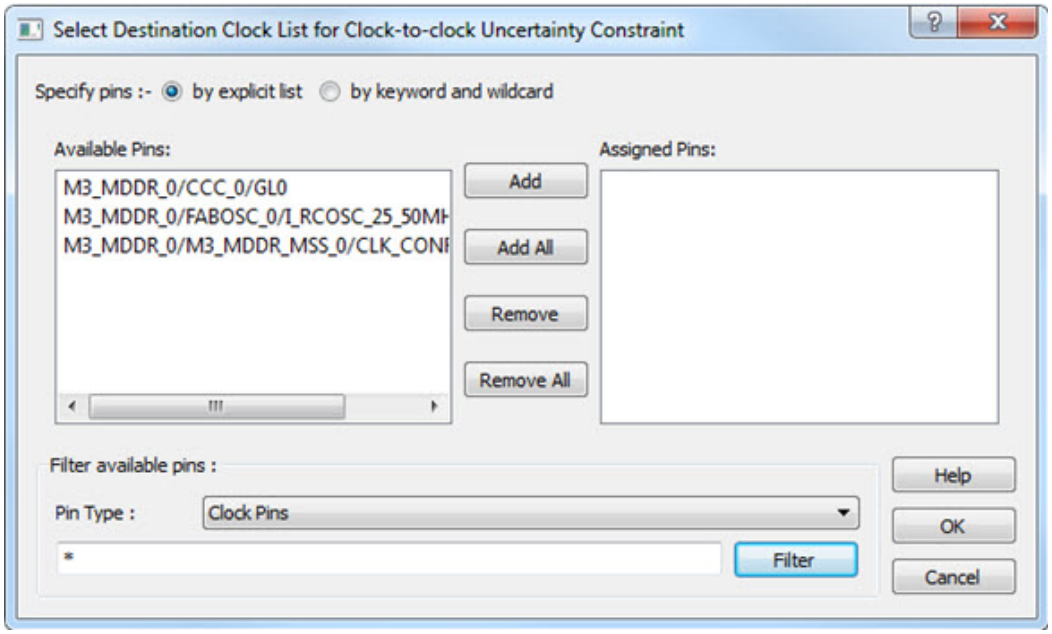


Figure 42 · Select Destination Clock Pins for Clock-to-Clock Uncertainty Dialog Box – by Explicit List

Available Pins

The list box displays the available Clock Pins. If you change the filter value, the list box shows the available pins based on the filter.

Use Add, Add All, to add Clock Pins from the Available Pins List or Remove, Remove All to delete Clock Pins from the Assigned Pins list.

Filter Available Pins

Pin type – Specifies the filter on the available Clock Pins.

Filter

Specifies the filter based on which the Available Pins list shows the Clock Pin names. The default is *, which is a wild-card match for all. You can specify any string value.

By Keyword and Wildcard

This mode stores the filter only. It does not store the actual pin names. The constraints created using this mode get exported with the SDC accessors (get_pins) and the wildcard filter.The following figure shows an example dialog box for Select Destination Clock Pins by keyword and the *CCC* filter.

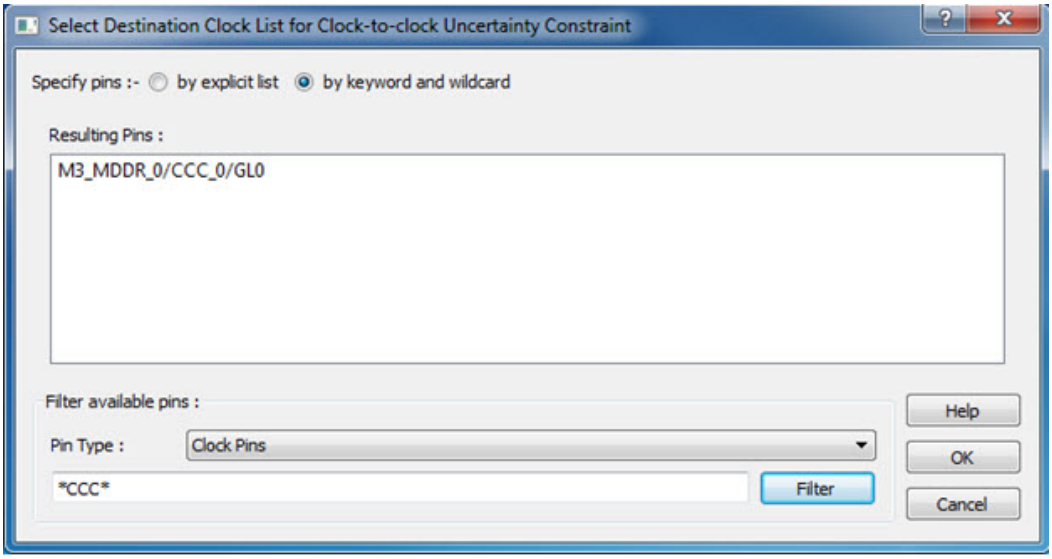


Figure 43 · Select Destination Clock Pins for Clock-to-Clock Uncertainty Dialog Box – By Keyword and Wildcard

Pin Type

Specifies the filter on the available pins. The only valid selection is Clock Pins.

Filter

Specifies the filter based on which the Available Pins list shows the pin names. The default is *, which is a wild-card match for all. You can specify any string value.

Resulting Pins

Displays pins from the available pins based on the filter.

Select Instance to Constrain Dialog Box

This dialog box appears when you click the browse button next to the Instance Name field in the Set Constraint to Disable Timing Arcs Dialog Box.

The list box displays the available Pins. If you change the filter value, the list box shows the available pins based on the filter.

Filter Available Pins

Pin type – Specifies the filter on the available Pin Types: All Instances is the only valid type.

Filter

Specifies the filter based on which the Available Pins list shows the Pin names. The default is *, which is a wild-card match for all. You can specify any string value.

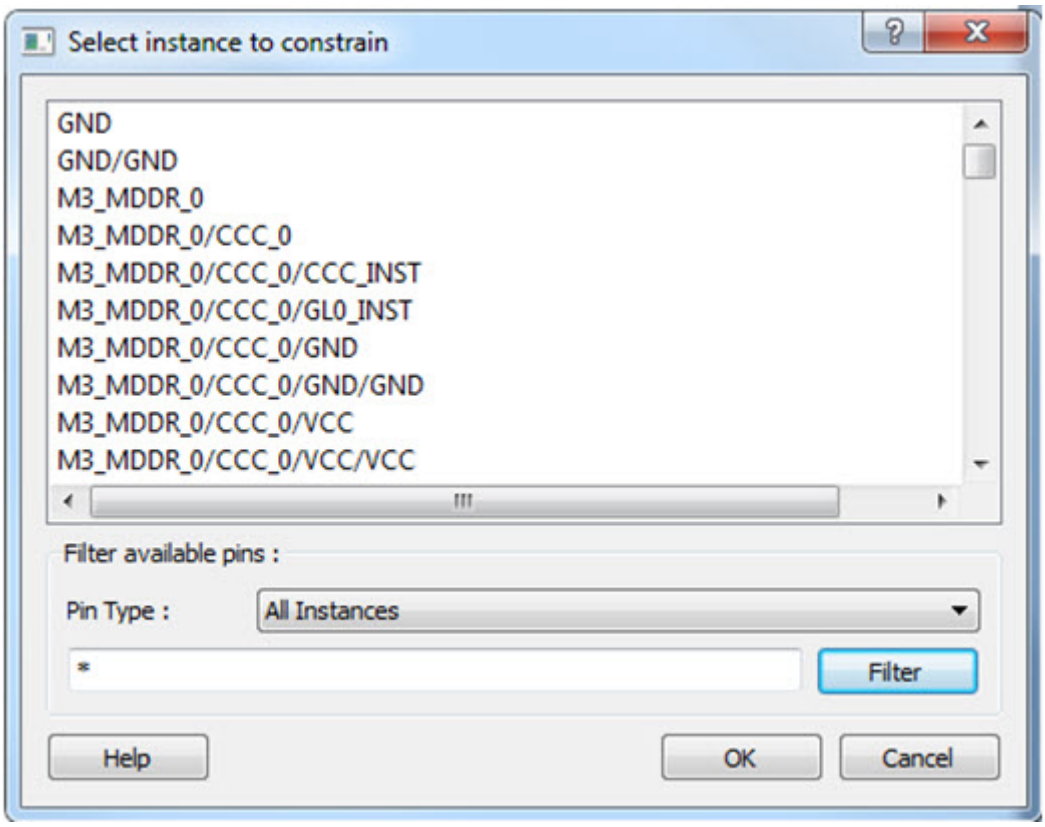


Figure 44 · Select Instance to Constrain Dialog Box

Select Generated Clock Reference Dialog Box

Use this dialog box to find and choose the generated clock reference pin from the list of available pins.

To open the Select Select Generated Clock Reference dialog box (shown below) from the Constraints Editor, open the Create Generated Clock Constraint Dialog Box dialog box and click the browse button for the Reference Pin.

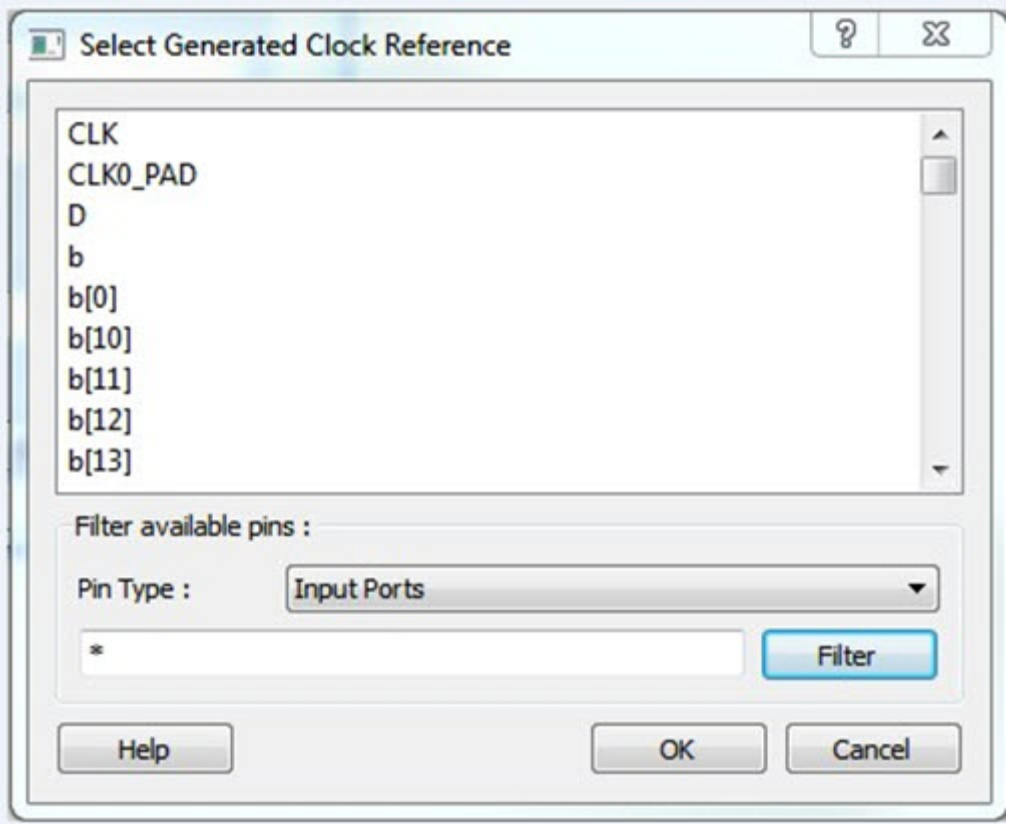


Figure 45 · Select Generated Clock Reference Dialog Box

Filter Available Pins

To identify any other pins in the design as the generated master pin, under **Filter available pins**, for Pin Type, select **Input Ports** or **All Pins**. You can also click filter the generated reference clock pin name in the displayed list. The default filter is *, which is a wild-card match for all.

See Also

Specifying Generated Clock Constraints

Select Generated Clock Source Dialog Box

Use this dialog box to find and choose the generated clock source from the list of available pins.

To open the Select Generated Clock Source dialog box (shown below) from the Constraints Editor, open the Create Generated Clock Constraint dialog box and click the browse button for the Clock Pin. The Selected Generated Clock Source dialog box appears.

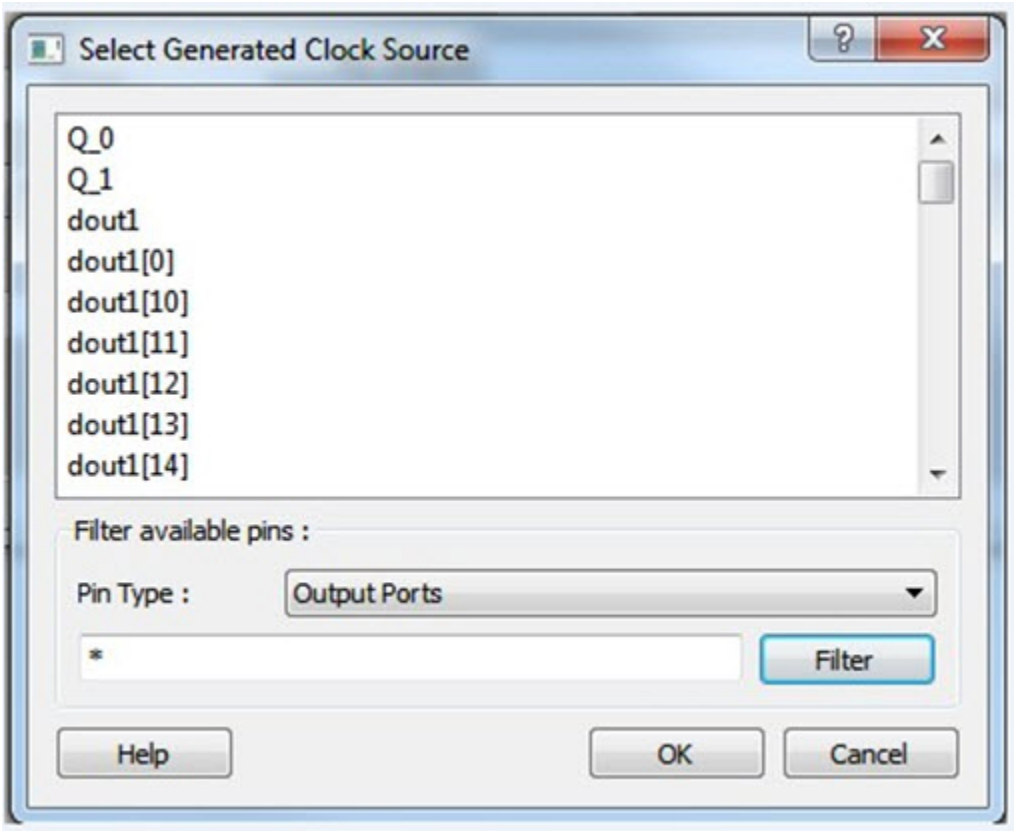


Figure 46 · Selected Generated Clock Source Dialog Box

Filter Available Pins

Explicit clock pins for the design is the default value. To identify any other pins in the design as the generated clock source pins, from the Pin Type pull-down list, select **All Ports**, **All Pins**, **All Nets**, or **All Register Output Pins**. You can also filter the generated clock source pin name in the displayed list. The default filter is *, which is a wild-card match for all.

See Also

Specifying Generated Clock Constraint

Select Ports Dialog Box

This dialog box appears when you click the browse button next to the Input Port field in the Set Input Delay Dialog Box or the Output Port field in the Set Output Delay Dialog Box. It also applies to the Set External Check & Set Clock To Output constraints.

The list box displays the available Pins. If you change the filter value, the list box shows the available pins based on the filter.

Use this dialog box to select the Input or Output Port:

- By explicit list
- By keyword and wildcard

By Explicit List

This is the default. This mode stores the actual Input/Out Port names. The following figure shows an example dialog box for the Select Input Port for Input Delay.

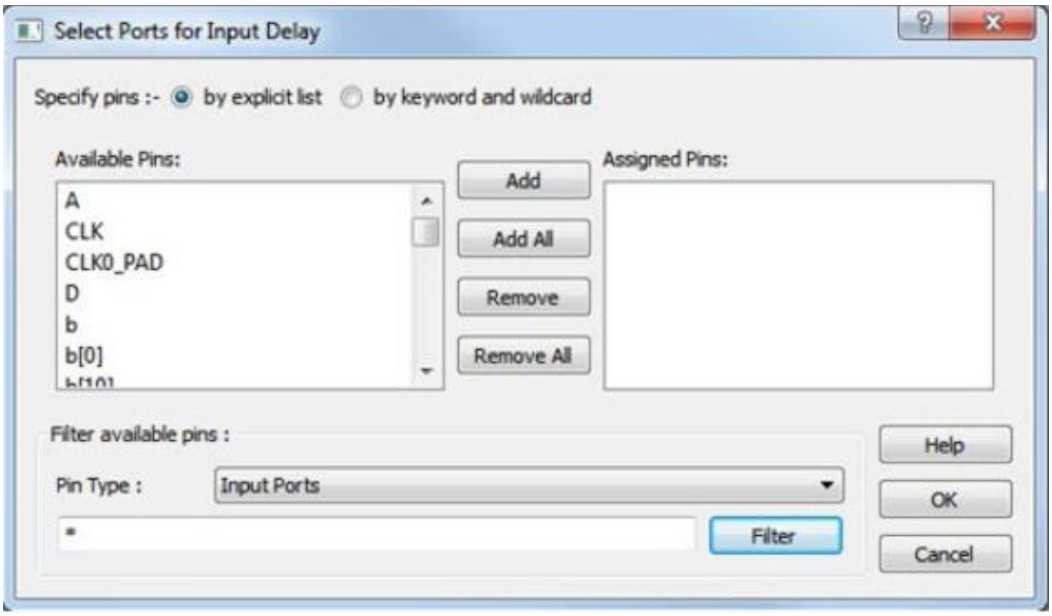


Figure 47 · Select Input Port for Input Delay Dialog Box

Available Pins

The list box displays the available Pins. If you change the filter value, the list box shows the available pins based on the filter.

Use **Add**, **Add All**, to add Pins from the Available Pins List or **Remove**, **Remove All** to delete Pins from the Assigned Pins list.

Filter Available Pins

Pin type – Specifies the filter on the available Pin Types: Input Port is the only valid type for Input Delay and Output Port is the only valid type for Output Delay.

Filter

Specifies the filter based on which the Available Pins list shows the Pin names. The default is *, which is a wild-card match for all. You can specify any string value.

By Keyword and Wildcard

This mode stores the filter only. It does not store the actual pin names. The constraints created using this mode get exported with the SDC accessors (get_ports) and the wildcard filter. The following figure shows an example dialog box for Select Output Ports by keyword and the *DM* filter.

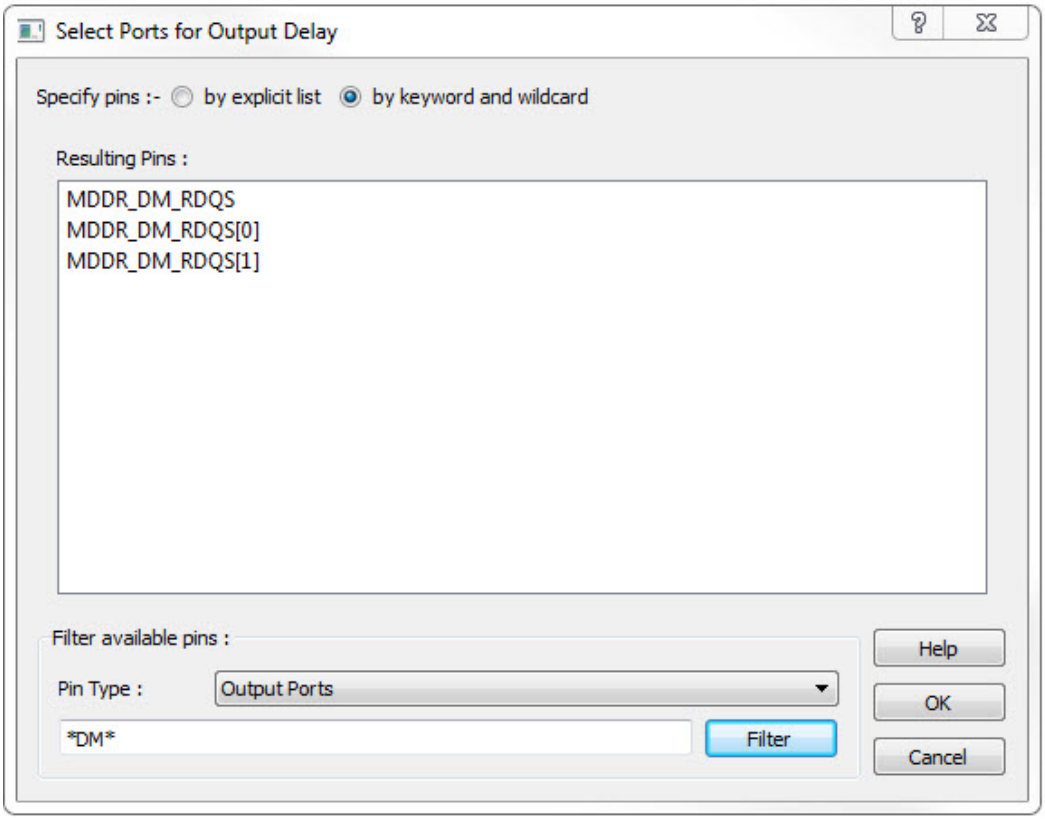


Figure 48 · Select Ports for Output Delay Dialog Box – By Keyword and Wildcard

Pin Type

Specifies the filter on the available pins. The valid values are Input Ports for Input Delay and Output Ports for Output Delay.

Filter

Specifies the filter based on which the Available Pins list shows the pin names. The default is *, which is a wild-card match for all. You can specify any string value.

Available Pins

Displays pins from the Pin Type based on the filter.

Select Source Clock for Clock-to-clock Uncertainty Constraint Dialog Box

This dialog box opens when you click the browse button for Source/From Clock for Clock-to-clock Uncertainty Constraints dialog box.

Use this dialog box to select Clock Pins:

- By explicit list
- By keyword and wildcard

To open the Select Source Clock dialog box, double-click **Constraint > Advanced > Clock Uncertainty**. Click the browse button to select the source.

By Explicit List

This is the default. This mode stores the actual Clock Pin names. The following figure shows an example dialog box for Select Source Clock List for Clock-to-Clock Uncertainty Constraint Dialog Box .

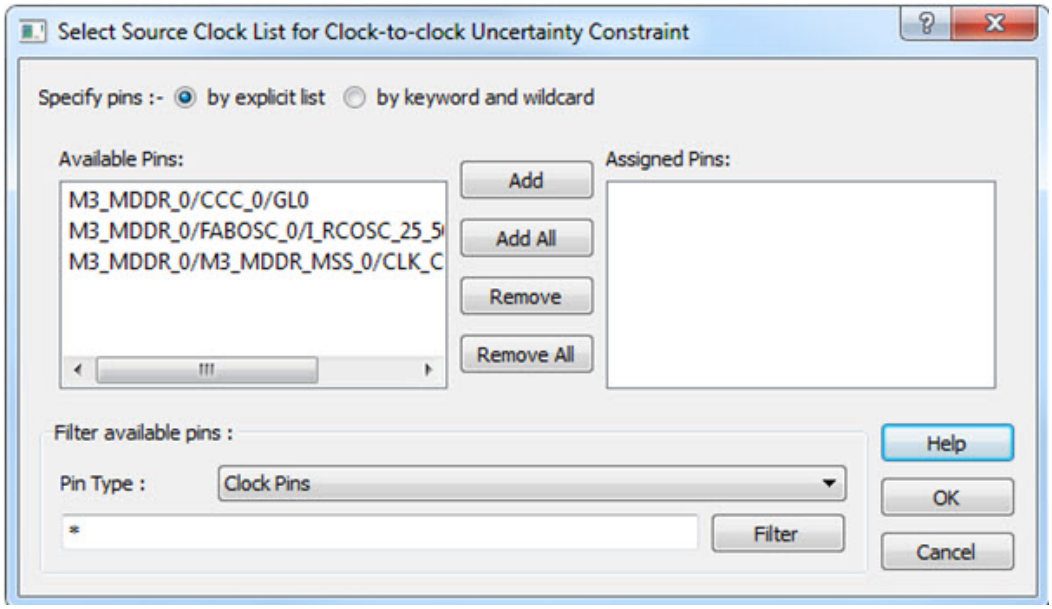


Figure 49 · Select Source Clock List for Clock-to-Clock Uncertainty Constraint Dialog Box – By Explicit List

Available Pins

The list box displays the available Clock Pins. If you change the filter value, the list box shows the available pins based on the filter.

Use Add, Add All, to add Clock Pins from the Available Pins List or Remove, Remove All to delete Clock Pins from the Assigned Pins list.

Filter Available Pins

Pin type – Specifies the filter on the available Clock Pins.

Filter

Specifies the filter based on which the Available Pins list shows the Clock Pin names. The default is *, which is a wild-card match for all. You can specify any string value.

By Keyword and Wildcard

This mode stores the filter only. It does not store the actual pin names. The constraints created using this mode get exported with the SDC accessors (get_pins) and the wildcard filter.The following figure shows an example dialog box for Select Source Clock Pins by keyword and the *CCC* filter.

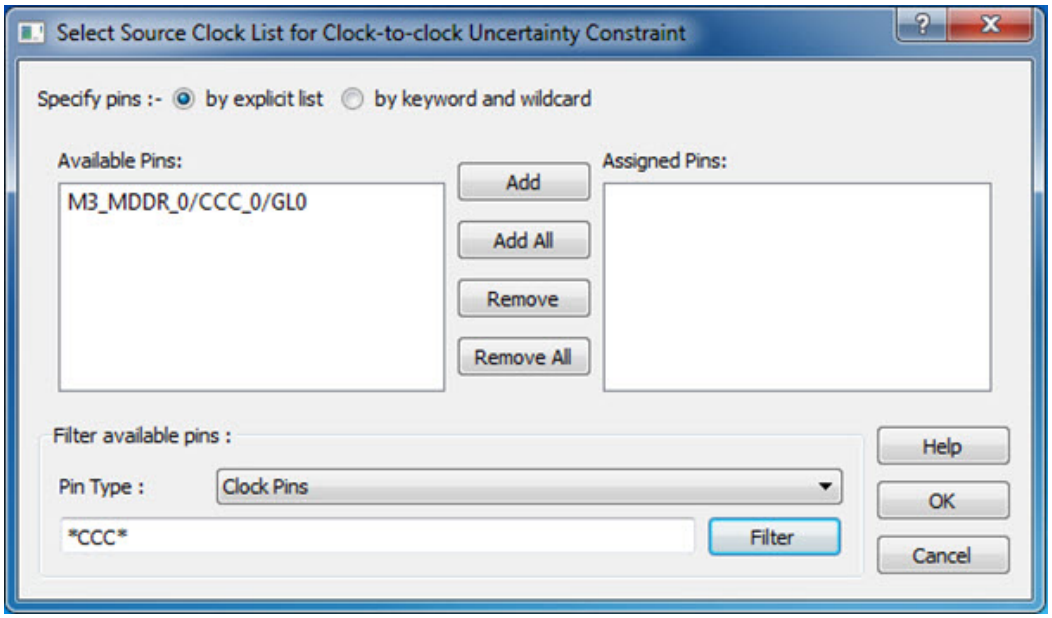


Figure 50 · Select Source Clock List for Clock-to-Clock Uncertainty Constraint Dialog Box – By Keyword and Wildcard

Pin Type

Specifies the filter on the available pins. The only valid selection is Clock Pins.

Filter

Specifies the filter based on which the Available Pins list shows the pin names. The default is *, which is a wild-card match for all. You can specify any string value.

Resulting Pins

Displays pins from the available pins based on the filter.

Select Source or Destination Pins for Constraint Dialog Box

This dialog box opens when you select the browse button for Source/From, Intermediate/Through and Destination/To pins for Timing Exception Constraints: False Path Constraints, Multicycle Path Constraints, and Maximum/Minimum Delay Constraints.

Use this dialog box to select pins or ports:

- By explicit list
- By keyword and wildcard

To open the Select Source or Destination Pins for Constraint dialog box from the Constraints Editor, choose **Constraint > Timing Exception Constraint Name**. Click the browse button to select the source.

By Explicit List

This is the default. This mode stores the actual pin names. The following figure shows an example dialog box for Select Source Pins for Multicycle Constraint (specify by explicit list).

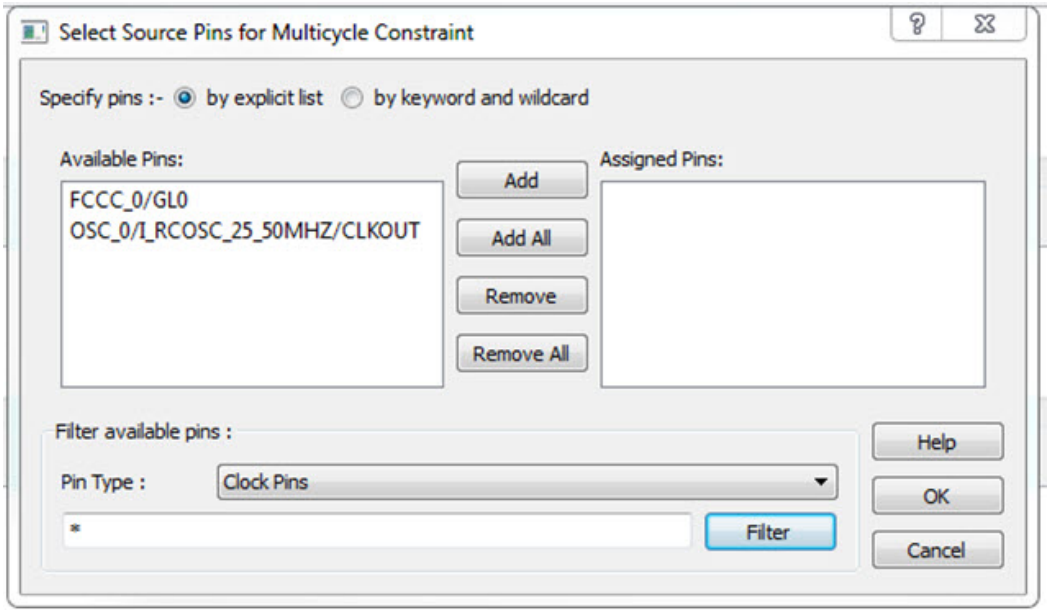


Figure 51 · Select Source Pins for Multicycle Constraint Dialog Box (specify by explicit list)

Available Pins

The list box displays the available pins. If you change the filter value, the list box shows the available pins based on the filter.

Click **Add**, **Add All**, **Remove**, and **Remove All** to add or delete pins from the Assigned Pins list.

Filter Available Pins

Pin Type – Specifies the filter on the available pins. You can specify Input Ports, Clock Pins, All Register Clock Pins.

Filter

Specifies the filter based on which the Available Pins list shows the pin names. The default is *, which is a wild-card match for all. You can specify any string value.

By Keyword and Wildcard

This mode stores the filter only. It does not store the actual pin names. The constraints created using this mode get exported with the SDC accessors (get_ports, get_pins, etc.) and the wildcard filter.The following figure shows an example dialog box for Select Source Pins for Multicycle Constraint (specified by keyword and wildcard).

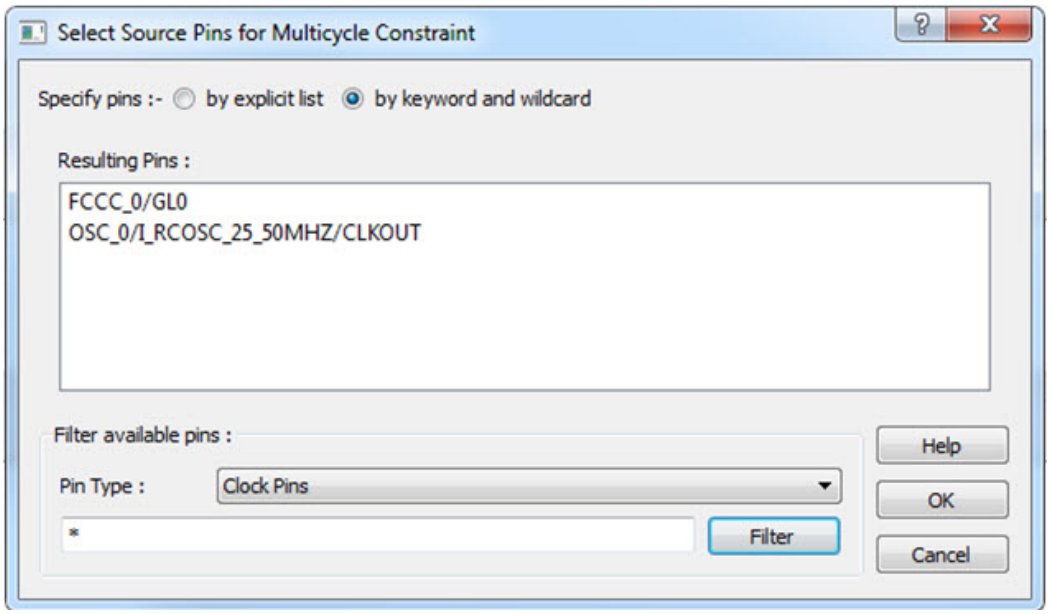


Figure 52 · Select Source Pins for Multicycle Constraint Dialog Box (specified by keyword and wildcard)

Pin Type

Specifies the filter on the available pins. The source pins can be Clock Pins, Input Ports, All Register Clock Pins. The default pin type is Clock Pins. The available Pin Type varies with Source Pins, Through Pins, and Destination Pins.

Filter

Specifies the filter based on which the Available Pins list shows the pin names. The default is *, which is a wild-card match for all. You can specify any string value.

Resulting Pins

Displays pins from the available pins based on the filter.

Select Source Pins for Clock Constraint Dialog Box

Use this dialog box to find and choose the clock source from the list of available pins.

To open the Select Source Pins for the Clock Constraint dialog box (shown below) from the Constraints Editor, click the browse button to the right of the Clock source field in the Create Clock Constraint dialog box.

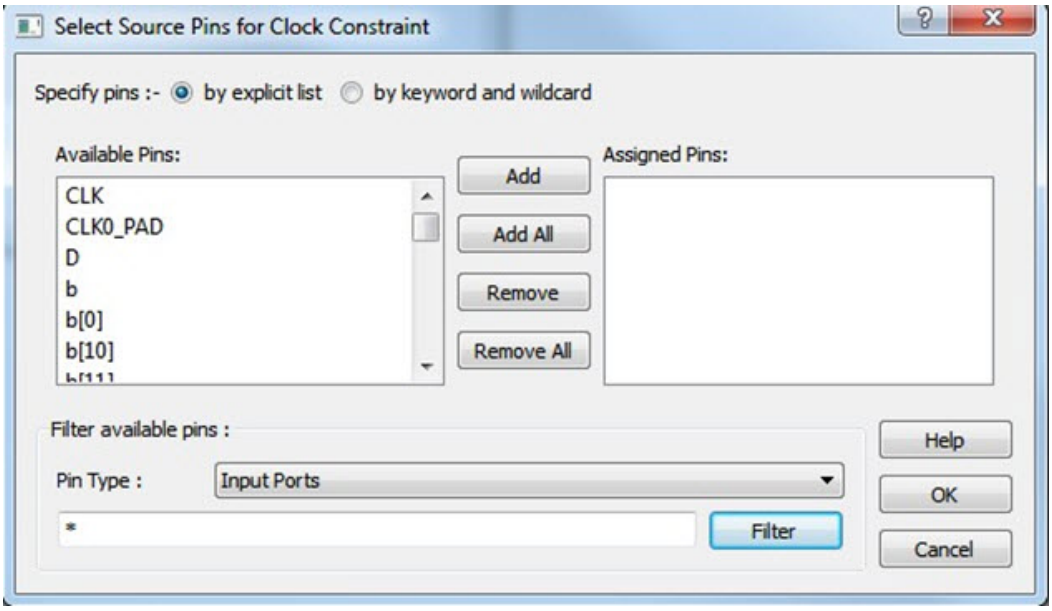


Figure 53 · Select Source Pins for Clock Constraint Dialog Box

Select a Pin

Displays all available pins.

Filter Available Objects

Explicit clock pins for the design is the default value. To identify any other pins in the design as clock pins, under **Filter available pins**, for Pin Type, select **Input Ports**, **All Pins**, or **All Nets**. You can also filter the clock source pin name in the displayed list. The default filter is *, which is a wild-card match for all.

See Also

Specifying Clock Constraints

Select Through Pins for Timing Exception Constraint Dialog Box

This dialog box opens when you select the Browse button for Intermediate/Through Pins for False Path, Multicycle Path, Min/Max Delay Constraints dialog box.

Use this dialog box to select the Intermediate Pin:

- By explicit list
- By keyword and wildcard

To open the Select Through Pins dialog box, double-click **Constraint > Exceptions > Max/Min Delay/False Path/Multicycle Path**. Click the browse button next to the To the Through field to select the Intermediate/Through Pin.

By Explicit List

This is the default. This mode stores the actual Intermediate/Through Pin names. The following figure shows an example dialog box for Select Through Pins for Multicycle Path Constraint.

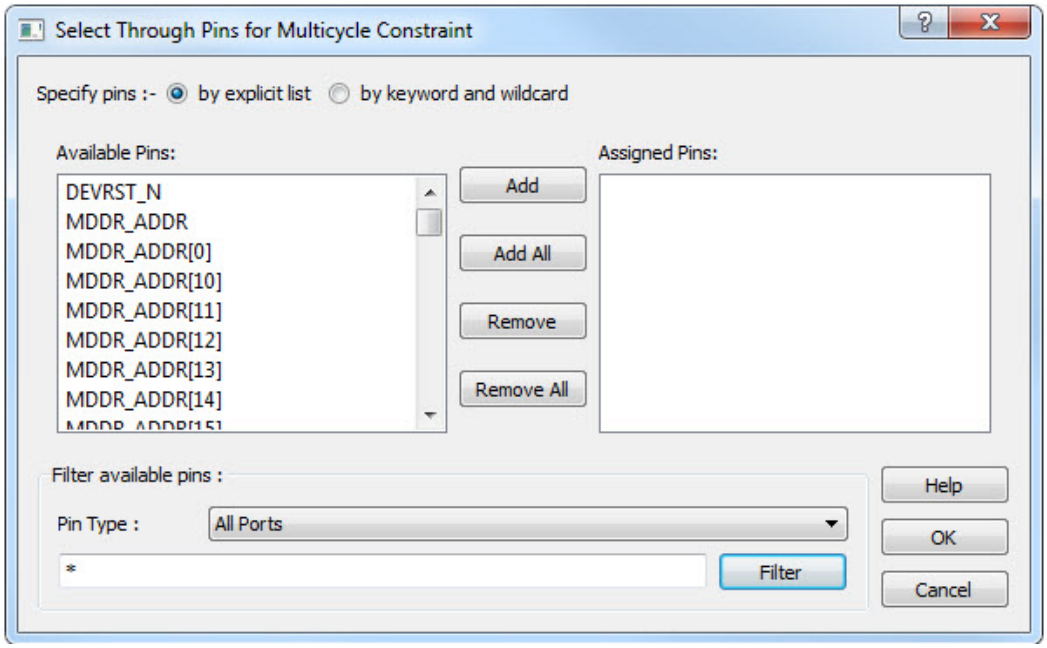


Figure 54 · Select Through Pins for Multicycle Path Constraint Dialog Box – By Explicit List

Available Pins

The list box displays the available Pins. If you change the filter value, the list box shows the available pins based on the filter.

Use **Add**, **Add All**, to add Pins from the Available Pins List or **Remove**, **Remove All** to delete Pins from the Assigned Pins list.

Filter Available Pins

Pin type – Specifies the filter on the available Pin Types: All Ports, All Nets, All Pins and All Instances.

Filter

Specifies the filter based on which the Available Pins list shows the Pin names. The default is *, which is a wild-card match for all. You can specify any string value.

By Keyword and Wildcard

This mode stores the filter only. It does not store the actual pin names. The constraints created using this mode get exported with the SDC accessors (get_pins) and the wildcard filter. The following figure shows an example dialog box for Select Through Pins by keyword and the *DM* filter.

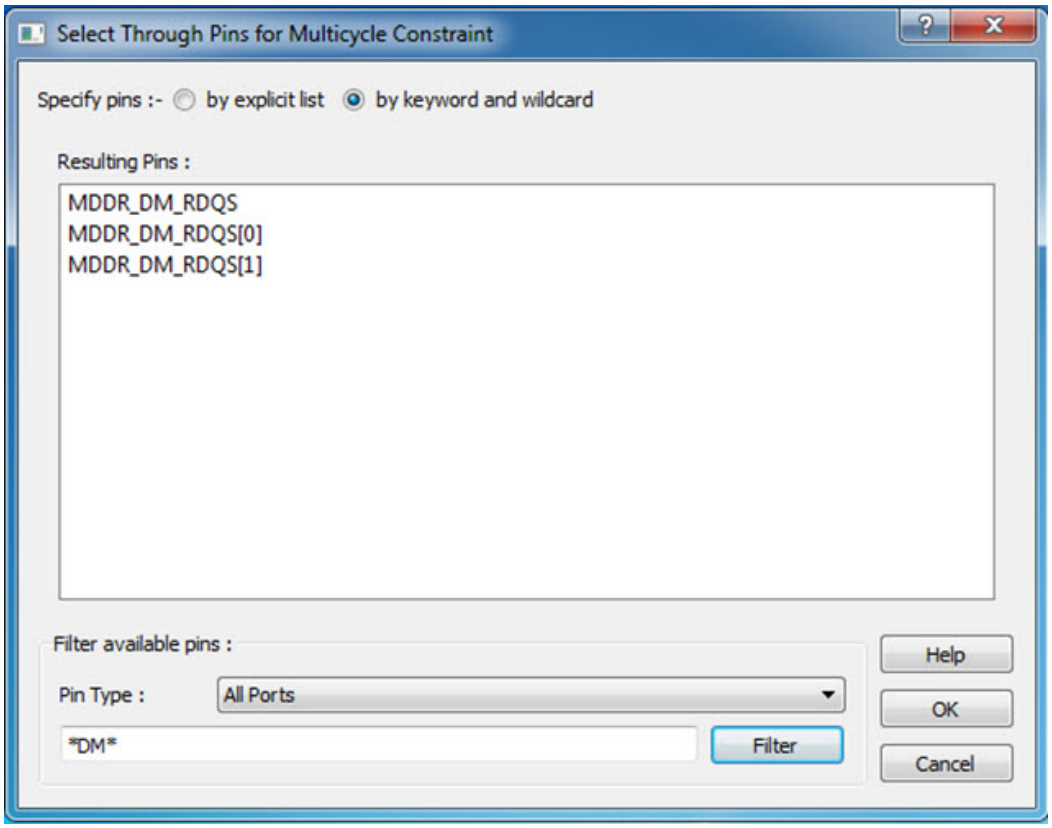


Figure 55 · Select Through Pins for Multicycle Path Constraint Dialog Box – By Keyword and Wilcard

Pin Type

Specifies the filter on the available pins. The valid values are All Ports, All Nets, All Pins and All Instances.

Filter

Specifies the filter based on which the Available Pins list shows the pin names. The default is *, which is a wild-card match for all. You can specify any string value.

Resulting Pins

Displays pins from the available pins based on the filter.

Referenced Topics

create_clock

SDC command; creates a clock and defines its characteristics.

```
create_clock -name name -period period_value [-waveform edge_list]  source
```

Arguments

`-name name`

Specifies the name of the clock constraint. This parameter is required for virtual clocks when no clock source is provided.

`-period period_value`

Specifies the clock period in nanoseconds. The value you specify is the minimum time over which the clock waveform repeats. The period_value must be greater than zero.

`-waveform edge_list`

Specifies the rise and fall times of the clock waveform in ns over a complete clock period. There must be exactly two transitions in the list, a rising transition followed by a falling transition. You can define a clock starting with a falling edge by providing an edge list where fall time is less than rise time. If you do not specify -waveform option, the tool creates a default waveform, with a rising edge at instant 0.0 ns and ©a falling edge at instant (period_value/2)ns.

source

Specifies the source of the clock constraint. The source can be ports or pins in the design. If you specify a clock constraint on a pin that already has a clock, the new clock replaces the existing one. Only one source is accepted. Wildcards are accepted as long as the resolution shows one port or pin.

Supported Families

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

Description

Creates a clock in the current design at the declared source and defines its period and waveform. The static timing analysis tool uses this information to propagate the waveform across the clock network to the clock pins of all sequential elements driven by this clock source.

The clock information is also used to compute the slacks in the specified clock domain that drive optimization tools such as place-and-route.

Exceptions

- None

Examples

The following example creates two clocks on ports CK1 and CK2 with a period of 6, a rising edge at 0, and a falling edge at 3:

```
create_clock -name {my_user_clock} -period 6 CK1
create_clock -name {my_other_user_clock} –period 6 –waveform {0 3} {CK2}
```

The following example creates a clock on port CK3 with a period of 7, a rising edge at 2, and a falling edge at 4:

```
create_clock –period 7 –waveform {2 4} [get_ports {CK3}]
```

Microsemi Implementation Specifics

- The -waveform in SDC accepts waveforms with multiple edges within a period. In Microsemi design implementation, only two waveforms are accepted.
- SDC accepts defining a clock on many sources using a single command. In Microsemi design implementation, only one source is accepted.
- The source argument in SDC create_clock command is optional. This is in conjunction with the -name argument in SDC to support the concept of virtual clocks. In Microsemi implementation, source is a mandatory argument as -name and virtual clocks concept is not supported.
- The -domain argument in the SDC create_clock command is not supported.

See Also

Constraint Support by Family

Constraint Entry Table

SDC Syntax Conventions

Clock Definition

Create Clock

Create a New Clock Constraint

create_generated_clock

SDC command; creates an internally generated clock and defines its characteristics.

```
create_generated_clock -name {name -source reference_pin [-divide_by divide_factor] [-
multiply_by multiply_factor] [-invert] source -pll_output pll_feedback_clock -pll_feedback
pll_feedback_input
```

Arguments

`-name` *name*

Specifies the name of the clock constraint. This parameter is required for virtual clocks when no clock source is provided.

`-source` *reference_pin*

Specifies the reference pin in the design from which the clock waveform is to be derived.

`-divide_by`*divide_factor*

Specifies the frequency division factor. For instance if the *divide_factor* is equal to 2, the generated clock period is twice the reference clock period.

`-multiply_by` *multiply_factor*

Specifies the frequency multiplication factor. For instance if the *multiply_factor* is equal to 2, the generated clock period is half the reference clock period.

`-invert`

Specifies that the generated clock waveform is inverted with respect to the reference clock.

`source`

Specifies the source of the clock constraint on internal pins of the design. If you specify a clock constraint on a pin that already has a clock, the new clock replaces the existing clock. Only one source is accepted. Wildcards are accepted as long as the resolution shows one pin.

`-pll_output` *pll_feedback_clock*

Specifies the output pin of the PLL which is used as the external feedback clock. This pin must drive the feedback input pin of the PLL specified using the –pll_feedback option. The PLL will align the rising edge of the reference input clock to the feedback clock. This is a mandatory argument if the PLL is operating in external feedback mode.

`-pll_feedback` *pll_feedback_input*

Specifies the feedback input pin of the PLL. This pin must be driven by the output pin of the PLL specified using the –pll_output option. The PLL will align the rising edge of the reference input clock to the external feedback clock. This is a mandatory argument if the PLL is operating in external feedback mode.

Supported Families

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

Description

Creates a generated clock in the current design at a declared source by defining its frequency with respect to the frequency at the reference pin. The static timing analysis tool uses this information to compute and propagate its waveform across the clock network to the clock pins of all sequential elements driven by this source.

The generated clock information is also used to compute the slacks in the specified clock domain that drive optimization tools such as place-and-route.

Examples

The following example creates a generated clock on pin U1/reg1:Q with a period twice as long as the period at the reference port CLK.

```
create_generated_clock -name {my_user_clock} –divide_by 2 –source [get_ports {CLK}]
U1/reg1/Q
```

The following example creates a generated clock at the primary output of myPLL with a period ¾ of the period at the reference pin clk.

```
create_generated_clock –divide_by 3 –multiply_by 4 -source clk [get_pins {myPLL/CLK1}]
```

The following example creates a generated clock named system_clk on the GL2 output pin of FCCC_0 with a period equal to half the period of the source clock. The constraint also identifies GL2 output pin as the external feedback clock source and CLK2 as the feedback input pin for FCCC_0.

```
create_generated_clock -name { system_clk } \
-multiply_by 2 \
-source { FCCC_0/CCC_INST/CLK3_PAD } \
-pll_output { FCCC_0/CCC_INST/GL2 } \
-pll_feedback { FCCC_0/CCC_INST/CLK2 } \
{ FCCC_0/CCC_INST/GL2 }
```

Microsemi Implementation Specifics

- SDC accepts either –multiply_by or –divide_by option. In Microsemi design implementation, both are accepted to accurately model the PLL behavior.
- SDC accepts defining a generated clock on many sources using a single command. In Microsemi design implementation, only one source is accepted.
- The -duty_cycle ,-edges and –edge_shift options in the SDC create_generated_clock command are not supported in Microsemi design implementation.

See Also

Constraint Support by Family

Constraint Entry Table

SDC Syntax Conventions

Create Generated Clock Constraint (SDC)

Specifying Generated Clock Constraints

Specifying a generated clock constraint enables you to define an internally generated clock for your design and verify its timing behavior. Use generated clock constraints and clock constraints to meet your performance goals.

To specify a generated clock constraint:

1. Open the Create Generated Clock Constraint dialog box using one of the following methods:
   - Click the  icon.
   - Right-click the **GeneratedClock** in the Constraint Browser and choose **Add Generated Clock**.
   - Double-click the Generated Clock Constraints grid. The Create Generated Clock Constraint dialog box appears (as shown below).

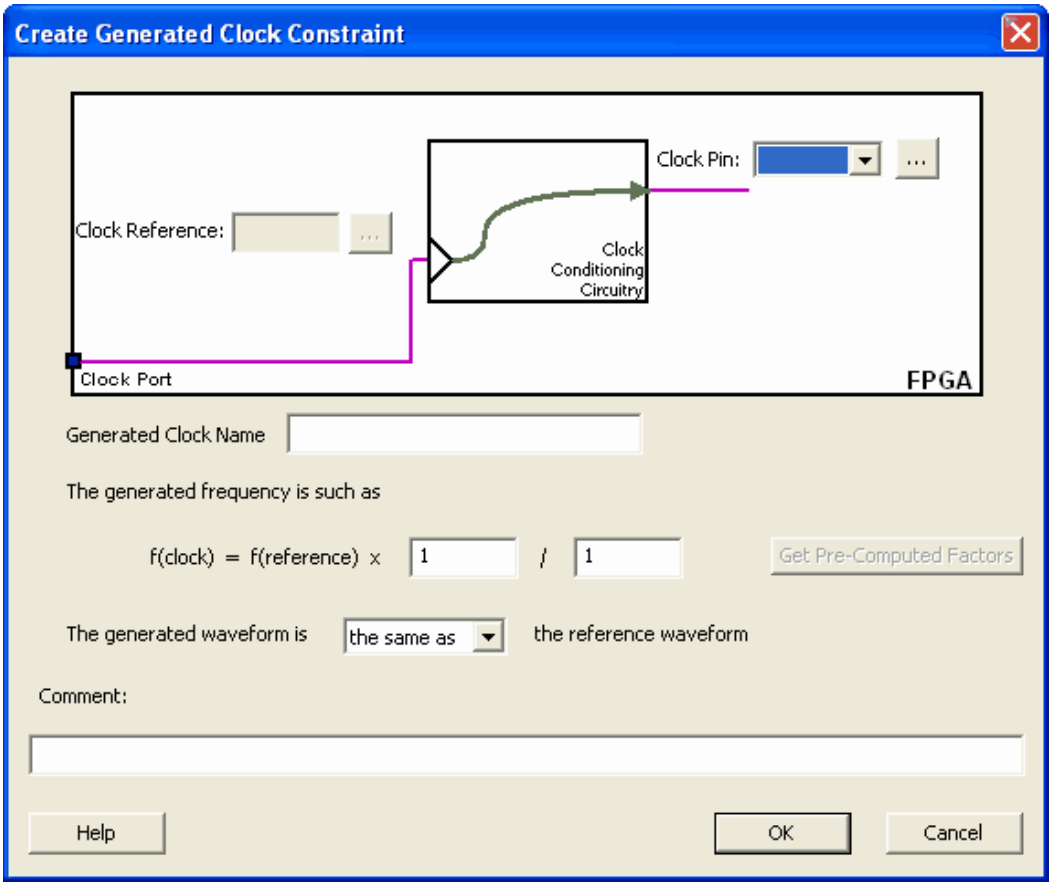


Figure 56 · Create Generated Clock Constraint

2. Select a **Clock Pin** to use as the generated clock source. To display a list of available generated clock source pins, click the **Browse** button. The Select Generated Clock Source dialog box appears (as shown below).

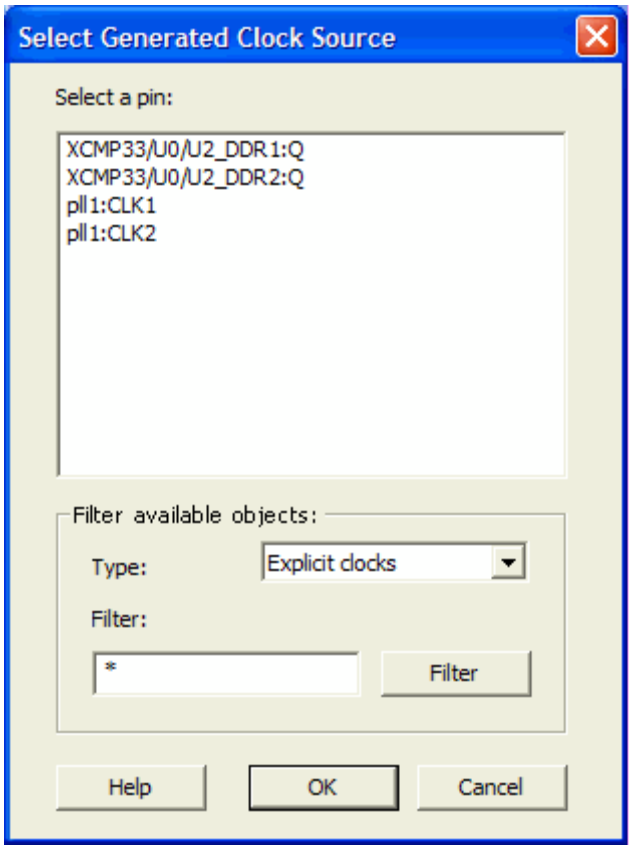


Figure 57 · Select Generated Clock Source Dialog Box

3. Modify the **Clock Name** if necessary.
4. Click **OK** to save these dialog box settings.
5. Specify a **Clock Reference**. To display a list of available clock reference pins, click the **Browse** button. The Select Generated Clock Reference dialog box appears.
5. Click **OK** to save this dialog box settings.
6. Specify the values to calculate the generated frequency: a multiplication factor and/or a division factor (both positive integers).
7. Specify the first edge of the generated waveform either same as or inverted with respect to the reference waveform.
8. Click **OK**. The new constraint appears in the Constraints List.

Tip: From the **File** menu, choose **Save**to save the newly created constraint in the database.

See Also

Design Constraint Guide: Clock

Design Constraint Guide: Create a Clock

Create Clock Constraint Dialog Box

Select Generated Clock Source Dialog Box

Use this dialog box to find and choose the generated clock source from the list of available pins.

To open the Select Generated Clock Source dialog box (shown below) from the SmartTime Constraints Editor, open the Create Generated Clock Constraint dialog box and click the **Browse** button for the **Clock Pin**.

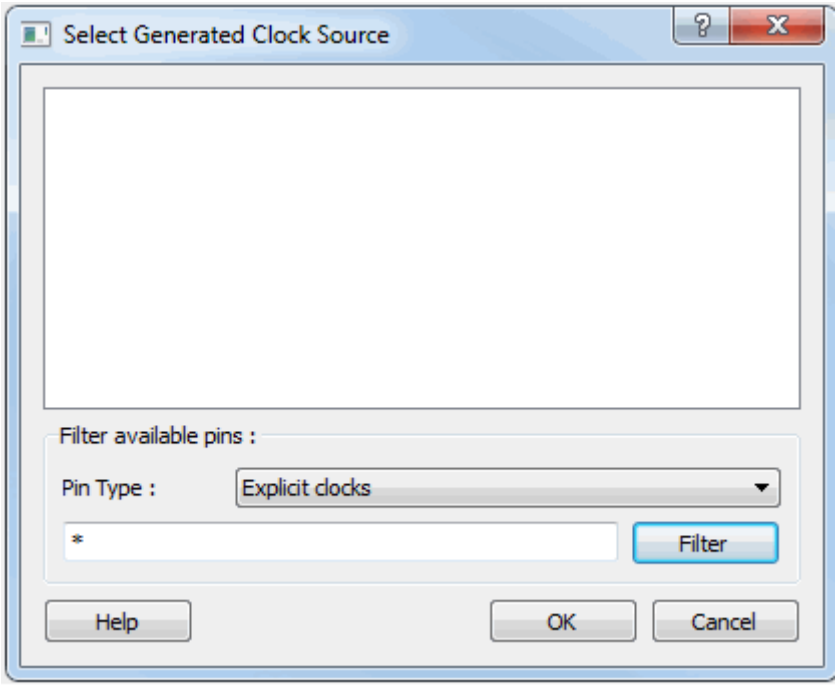


Figure 58 · Select Generated Clock Source Dialog Box

Filter Available Pins

Explicit clock pins for the design is the default value. To identify any other pins in the design as the generated clock source pins, from the **Pin Type** pull-down list, select **Explicit clocks**, **Potential clocks**, **All Ports**, **All Pins**, **All Nets**, **Pins on clock network**, or **Nets in clock network**. You can also use the **Filter** to filter the generated clock source pin name in the displayed list.

See Also

Specifying generated clock constraint (SDC)

set_input_delay

SDC command; defines the arrival time of an input relative to a clock.

```
set_input_delay delay_value -clock clock_ref [-max] [-min] [-clock_fall] input_list
```

Arguments

`delay_value`

Specifies the arrival time in nanoseconds that represents the amount of time for which the signal is available at the specified input after a clock edge.

`-clock clock_ref`

Specifies the clock reference to which the specified input delay is related. This is a mandatory argument. If you do not specify -max or -min options, the tool assumes the maximum and minimum input delays to be equal.

`-max`

Specifies that delay_value refers to the longest path arriving at the specified input. If you do not specify -max or -min options, the tool assumes maximum and minimum input delays to be equal.

`-min`

Specifies that delay_value refers to the shortest path arriving at the specified input. If you do not specify -max or -min options, the tool assumes maximum and minimum input delays to be equal.

`-clock_fall`

Specifies that the delay is relative to the falling edge of the clock reference. The default is the rising edge.

`input_list`

Provides a list of input ports in the current design to which delay_value is assigned. If you need to specify more than one object, enclose the objects in braces ({}).

Supported Families

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion and IGLOOe, except ProASIC3 nano and ProASIC3L

Description

The set_input_delay command sets input path delays on input ports relative to a clock edge. This usually represents a combinational path delay from the clock pin of a register external to the current design. For in/out (bidirectional) ports, you can specify the path delays for both input and output modes. The tool adds input delay to path delay for paths starting at primary inputs.

A clock is a singleton that represents the name of a defined clock constraint. This can be:

- a single port name used as source for a clock constraint
- a single pin name used as source for a clock constraint; for instance reg1:CLK. This name can be hierarchical (for instance toplevel/block1/reg2:CLK)
- an object accessor that will refer to one clock: [get_clocks {clk}]

Examples

The following example sets an input delay of 1.2ns for port data1 relative to the rising edge of CLK1:

```
set_input_delay 1.2 -clock [get_clocks CLK1] [get_ports data1]
```

The following example sets a different maximum and minimum input delay for port IN1 relative to the falling edge of CLK2:

```
set_input_delay 1.0 -clock_fall -clock CLK2 –min {IN1}
set_input_delay 1.4 -clock_fall -clock CLK2 –max {IN1}
```

Microsemi Implementation Specifics

In SDC, the -clock is an optional argument that allows you to set input delay for combinational designs. Microsemi Implementation currently requires this argument.

See Also

Constraint Support by Family

Constraint Entry Table

SDC Syntax Conventions

Set Input Delay

set_output_delay

SDC command; defines the output delay of an output relative to a clock.

```
set_output_delay delay_value -clock clock_ref [–max] [–min] [–clock_fall] output_list
```

Arguments

`delay_value`

Specifies the amount of time before a clock edge for which the signal is required. This represents a combinational path delay to a register outside the current design plus the library setup time (for maximum output delay) or hold time (for minimum output delay).

`-clock` *`clock_ref`*

Specifies the clock reference to which the specified output delay is related. This is a mandatory argument. If you do not specify -max or -min options, the tool assumes the maximum and minimum input delays to be equal.

`-max`

Specifies that delay_value refers to the longest path from the specified output. If you do not specify -max or -min options, the tool assumes the maximum and minimum output delays to be equal.

`-min`

Specifies that delay_value refers to the shortest path from the specified output. If you do not specify -max or -min options, the tool assumes the maximum and minimum output delays to be equal.

`-clock_fall`

Specifies that the delay is relative to the falling edge of the clock reference. The default is the rising edge.

`output_list`

Provides a list of output ports in the current design to which delay_value is assigned. If you need to specify more than one object, enclose the objects in braces ({}).

Supported Families

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

Description

The set_output_delay command sets output path delays on output ports relative to a clock edge. Output ports have no output delay unless you specify it. For in/out (bidirectional) ports, you can specify the path delays for both input and output modes. The tool adds output delay to path delay for paths ending at primary outputs.

Examples

The following example sets an output delay of 1.2ns for port OUT1 relative to the rising edge of CLK1:

```
set_output_delay 1.2 -clock [get_clocks CLK1] [get_ports OUT1]
```

The following example sets a different maximum and minimum output delay for port OUT1 relative to the falling edge of CLK2:

```
set_output_delay 1.0 -clock_fall -clock CLK2 –min {OUT1}
set_output_delay 1.4 -clock_fall -clock CLK2 –max {OUT1}
```

Microsemi Implementation Specifics

- In SDC, the -clock is an optional argument that allows you to set the output delay for combinational designs. Microsemi Implementation currently requires this option.

See Also

Constraint Support by Family

Constraint Entry Table

SDC Syntax Conventions

Set Output Delay

set_clock_to_output

SDC command; defines the timing budget available inside the FPGA for an output relative to a clock.

```
set_clock_to_output delay_value -clock clock_ref [–max] [–min] output_list
```

Arguments

delay_value

Specifies the clock to output delay in nanoseconds. This time represents the amount of time available inside the FPGA between the active clock edge and the data change at the output port.

`-clock` *clock_ref*

Specifies the reference clock to which the specified clock to output is related. This is a mandatory argument.

`-max`

Specifies that *delay_value* refers to the maximum clock to output at the specified output. If you do not specify –max or –min options, the tool assumes maximum and minimum clock to output delays to be equal.

`-min`

Specifies that *delay_value* refers to the minimum clock to output at the specified output. If you do not specify –max or –min options, the tool assumes maximum and minimum clock to output delays to be equal.

output_list

Provides a list of output ports in the current design to which delay_value is assigned. If you need to specify more than one object, enclose the objects in braces ({}).

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Timing Exceptions Overview

Use timing exceptions to overwrite the default behavior of the design path. Timing exceptions include:

- Setting multicycle constraint to specify paths that (by design) will take more than one cycle.
- Setting a false path constraint to identify paths that must not be included in the timing analysis or the optimization flow.
- Setting a maximum delay constraint on specific paths to relax or to tighten the original clock constraint requirement.

See Also

Specifying a Maximum Delay Constraint

Specifying a Minimum Delay Constraint

Specifying a Multicycle Constraint

Specifying a False Path Constraint

Changing Output Port Capacitance

Specifying a Minimum Delay Constraint

You set options in the Set Minimum Delay Constraint dialog box to relax or to tighten the original clock constraint requirement on specific paths.

To specify Min delay constraints:

1. Open the Set Minimum Delay Constraint dialog box using one of the following methods:
   - Click the  icon in the Constraints Editor.
   - From the Constraints Editor, right-click the Constraints Menu and choose **Min delay**.

The Set Minimum Delay Constraint dialog box appears (as shown below).

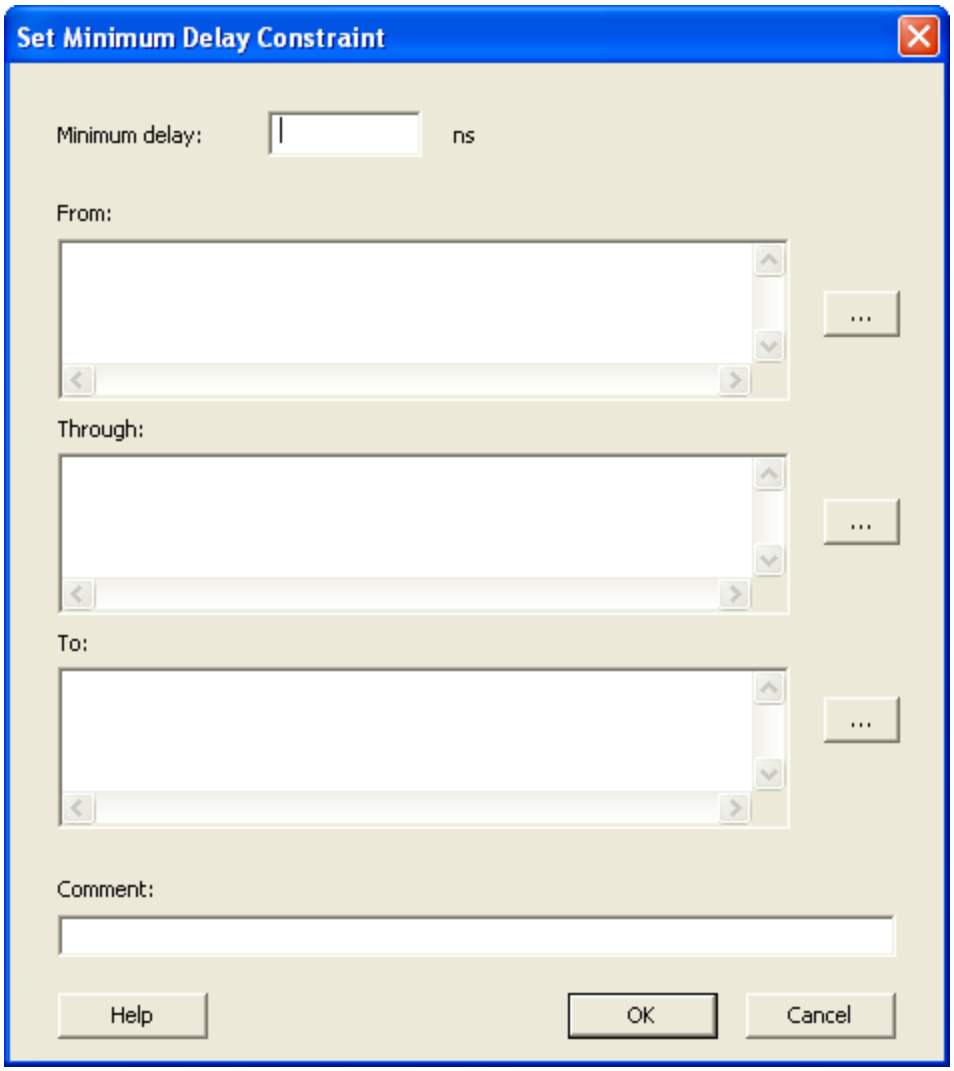


Figure 59 · Set Minimum Delay Constraint Dialog Box

2. Specify the delay in the **Minimum delay** field.
3. Specify the **From** pin(s). Click the **Browse** button next to **From** to open the Select Source Pins for Min Delay Constraint dialog box (as shown below).

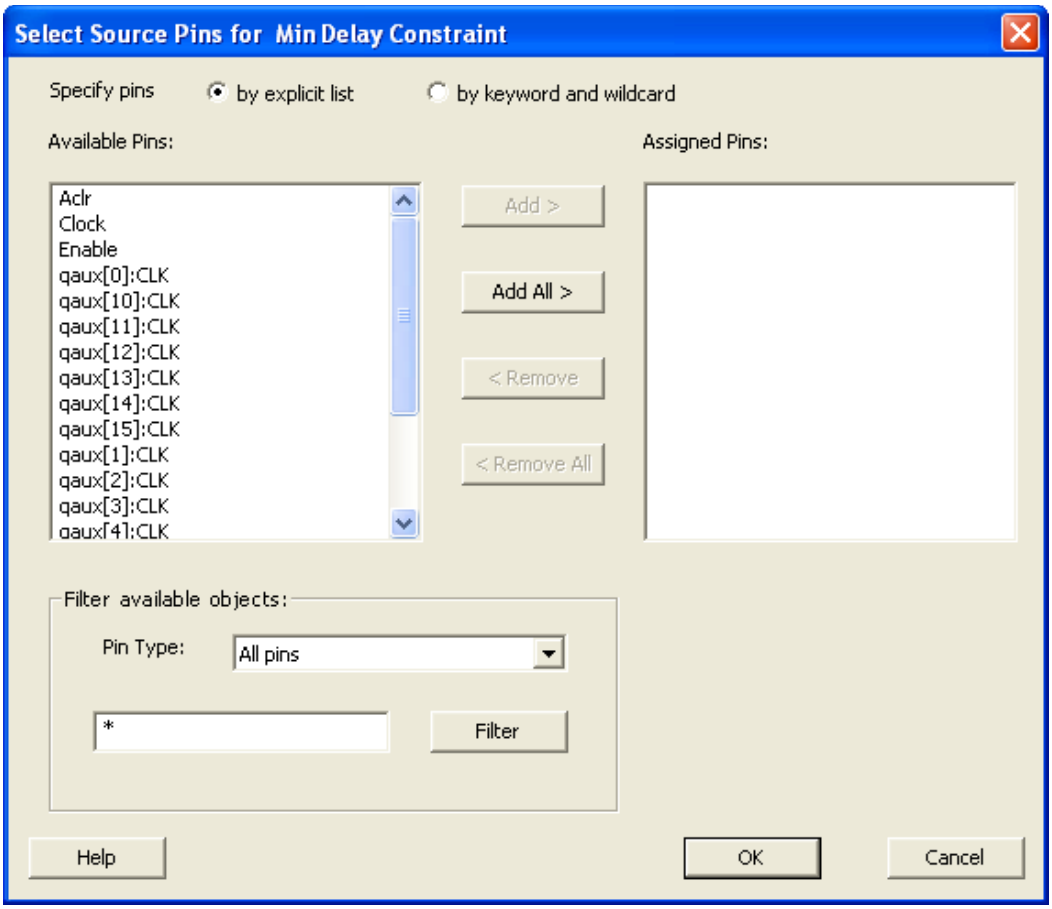


Figure 60 · Select Source Pins for Min Delay Constraint

4. Select **by explicit list**. (Alternatively, you can select **by keyword and wildcard**.)
5. Select the input pin(s) from the **Available Pins** list. You can also use **Filter available objects** to narrow the pin list. You can select multiple ports in this window.
6. Click **Add** or **Add All**. The input pin(s) move from the **Available Pins** list to the **Assigned Pins** list.
7. Click **OK**. The Set Minimum Delay Constraint dialog box displays the updated **From** pin(s) list.
8. Click the **Browse** button for **Through** and **To** and add the appropriate pin(s). The displayed list shows the pins reachable from the previously selected pin(s) list.
9. Enter comments in the **Comment** section.
10. Click **OK**.

SmartTime adds the minimum delay constraints to the Constraints List in the SmartTime Constraints Editor.

See Also

Timing Exceptions Overview

Set Maximum Delay Constraint dialog box

Specifying Maximum Delay Constraint

Specifying Multicycle Constraint

Specifying False Path Constraint

Changing Output Port Capacitance

set_min_delay

SDC command; specifies the minimum delay for the timing paths.

```
set_min_delay delay_value [-from from_list] [-to to_list]
```

Arguments

delay_value

Specifies a floating point number in nanoseconds that represents the required minimum delay value for specified paths.

- If the path starting point is on a sequential device, the tool includes clock skew in the computed delay.
- If the path starting point has an input delay specified, the tool adds that delay value to the path delay.
- If the path ending point is on a sequential device, the tool includes clock skew and library setup time in the computed delay.
- If the ending point has an output delay specified, the tool adds that delay to the path delay.

`-from` *from_list*

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

`-to` *to_list*

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

Supported Families

SmartFusion2, IGLOO2, RTG4, SmartFusion, IGLOO, ProASIC3, Fusion

Description

This command specifies the required minimum delay for timing paths in the current design. The path length for any startpoint in from_list to any endpoint in to_list must be less than delay_value.

The tool automatically derives the individual minimum delay targets from clock waveforms and port input or output delays. For more information, refer to the create_clock, set_input_delay, and set_output_delay commands.

The minimum delay constraint is a timing exception. This constraint overrides the default single cycle timing relationship for one or more timing paths. This constraint also overrides a multicycle path constraint.

Examples

The following example sets a minimum delay by constraining all paths from ff1a:CLK or ff1b:CLK to ff2e:D with a delay less than 5 ns:

```
set_min_delay 5 -from {ff1a:CLK ff1b:CLK} -to {ff2e:D}
```

The following example sets a minimum delay by constraining all paths to output ports whose names start by “out” with a delay less than 3.8 ns:

```
set_min_delay 3.8 -to [get_ports out*]
```

Microsemi Implementation Specifics

The –through option in the set_min_delay SDC command is not supported.

See Also

Constraint Support by Family

Constraint Entry Table

SDC Syntax Conventions

Set Multicycle Path

Families Supported

The following table shows which families support this constraint and which file formats and tools you can use to enter or modify it:

Families	SDC	SmartTime	Constraints Editor
RTG4	X	X [1]	X[2]
IGLOO2	X	X [1]	X[2]
SmartFusion2	X	X [1]	X[2]
IGLOO	X	X	
SmartFusion	X	X	
Fusion	X	X	
ProASIC3	X	X	

1 For Libero SoC Design Flow (Classic Constraint Flow)

2 For Libero SoC Design Flow (Enhanced Constraint Flow) - SmartFusion2, IGLOO2, RTG4

Purpose

Use this constraint to identify paths in the design that take multiple clock cycles.

You can set multicycle path constraints in an SDC file, which you can either create yourself or generate with Synthesis tools, at the same time you import the netlist. Alternatively, you can set multicycle paths using the GUI tools in the Designer software when you implement your design.

Tools /How to Enter

You can use one or more of the following commands or GUI tools to set multicycle paths constraints:

- SDC – set_multicycle_path
- SmartTime – Specifying Input Delay Constraint

See Also

Constraint Entry

`set_multicycle_paths` (SDC)

Specifying Input Delay Constraint

Specifying a Multicycle Constraint

You set options in the Set Multicycle Constraint dialog box to specify paths that take multiple clock cycles in the current design.

To specify multicycle constraints:

1. Add the constraint in the Editable Constraints Grid or open the Set Multicycle Constraint dialog box using one of the following methods:
   - From the SmartTime Constraints Editor, choose **Constraint > MultiCycle**.
   - Click the  icon.
   - Right-click the **Multicycle** option in the Constraint Browser and select **Add Multicycle Path Constraint**.

The Set Multicycle Constraint dialog box appears (as shown below).

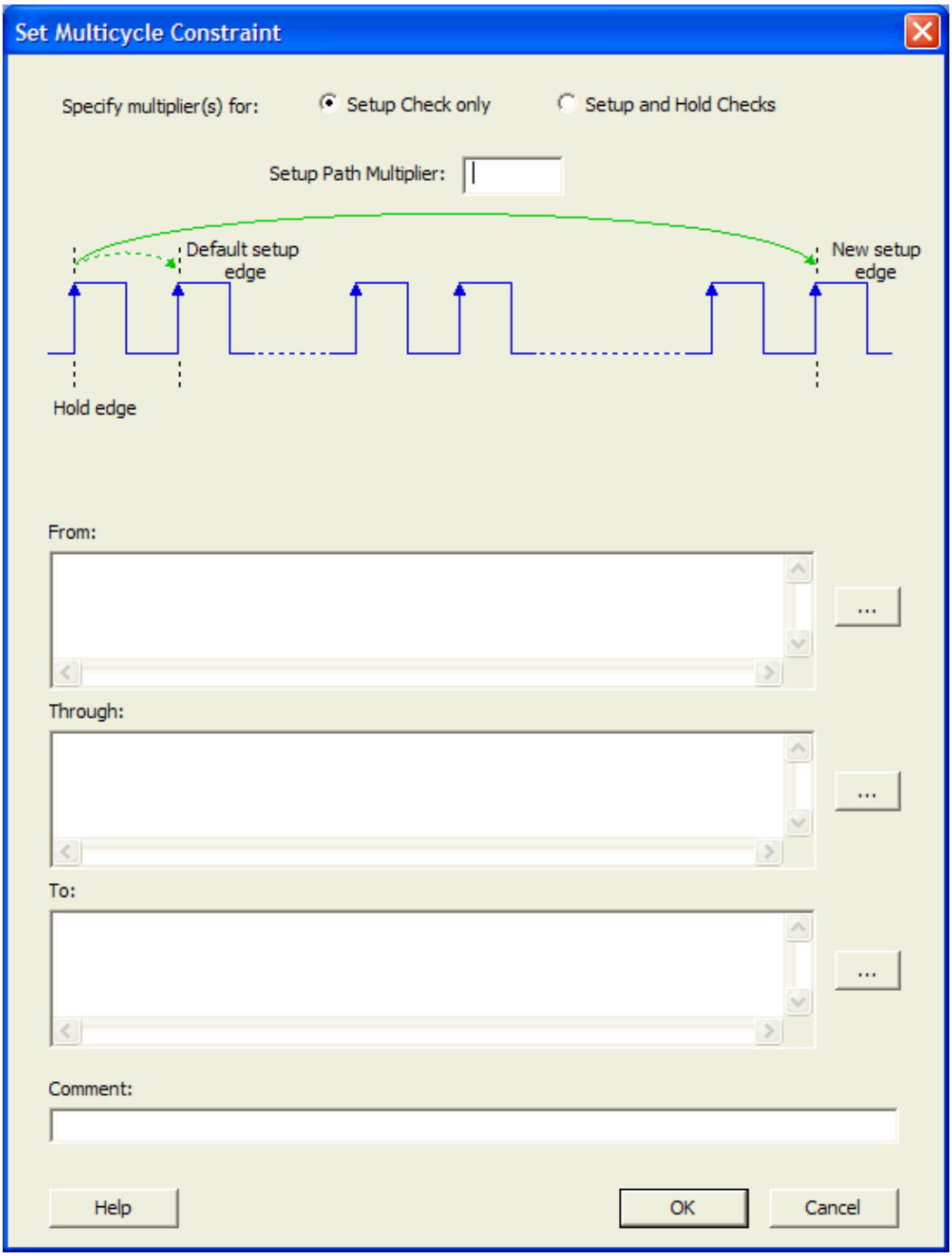


Figure 61 · Set Multicycle Constraint Dialog Box

2. Specify the number of cycles in the **Setup Path Multiplier**.
3. Specify the **From** pin(s). Click the **Browse** button next to **From** to open the Select Source Pins for Constraint dialog box (as shown below).

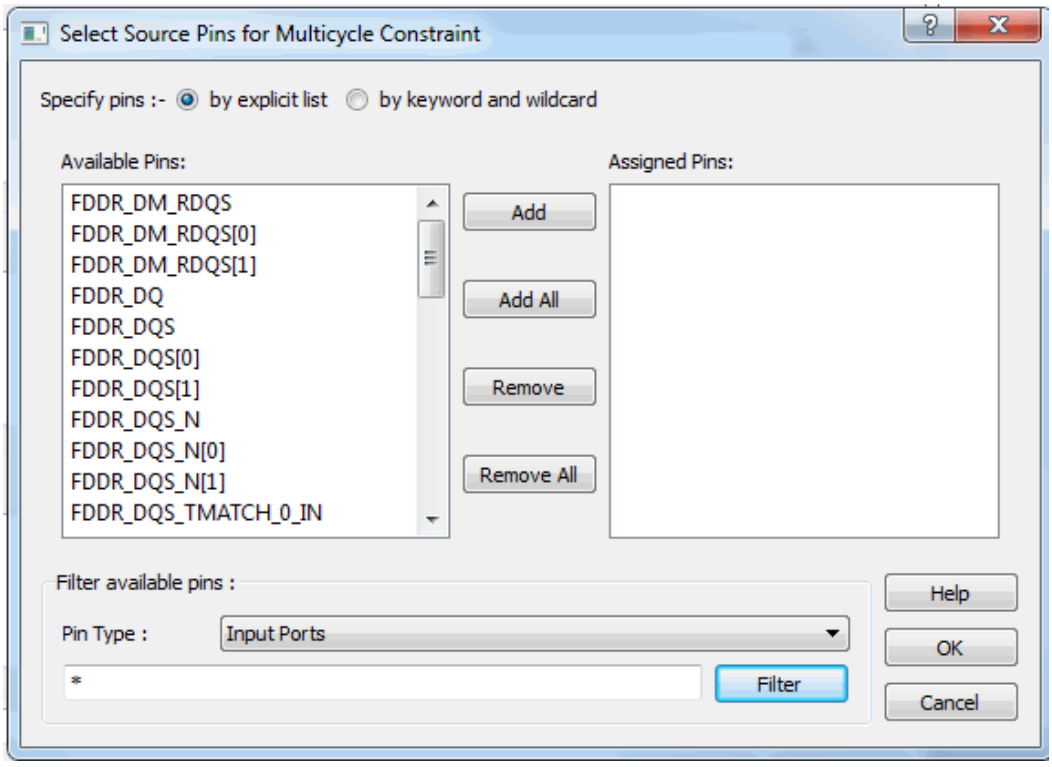


Figure 62 · Select Source Pins for Multicycle Constraint

4. Select **by explicit list**. (Alternatively, you can select **by keyword and wildcard**. For details, refer to the Select Source or Destination Pins for Constraint Dialog Box.)
5. Select the input pin(s) from the **Available Pin** list. You can use **Filter available objects** to narrow the pin list. You can select multiple ports in this window.
6. Click **Add** or **Add All** to move theinput pin(s) move from the **Available pins** list to the **Assigned Pins** list.
7. Click **OK**.

The Set Multicycle Constraint dialog box displays the updated representation of the **From** pin(s) (as shown below).

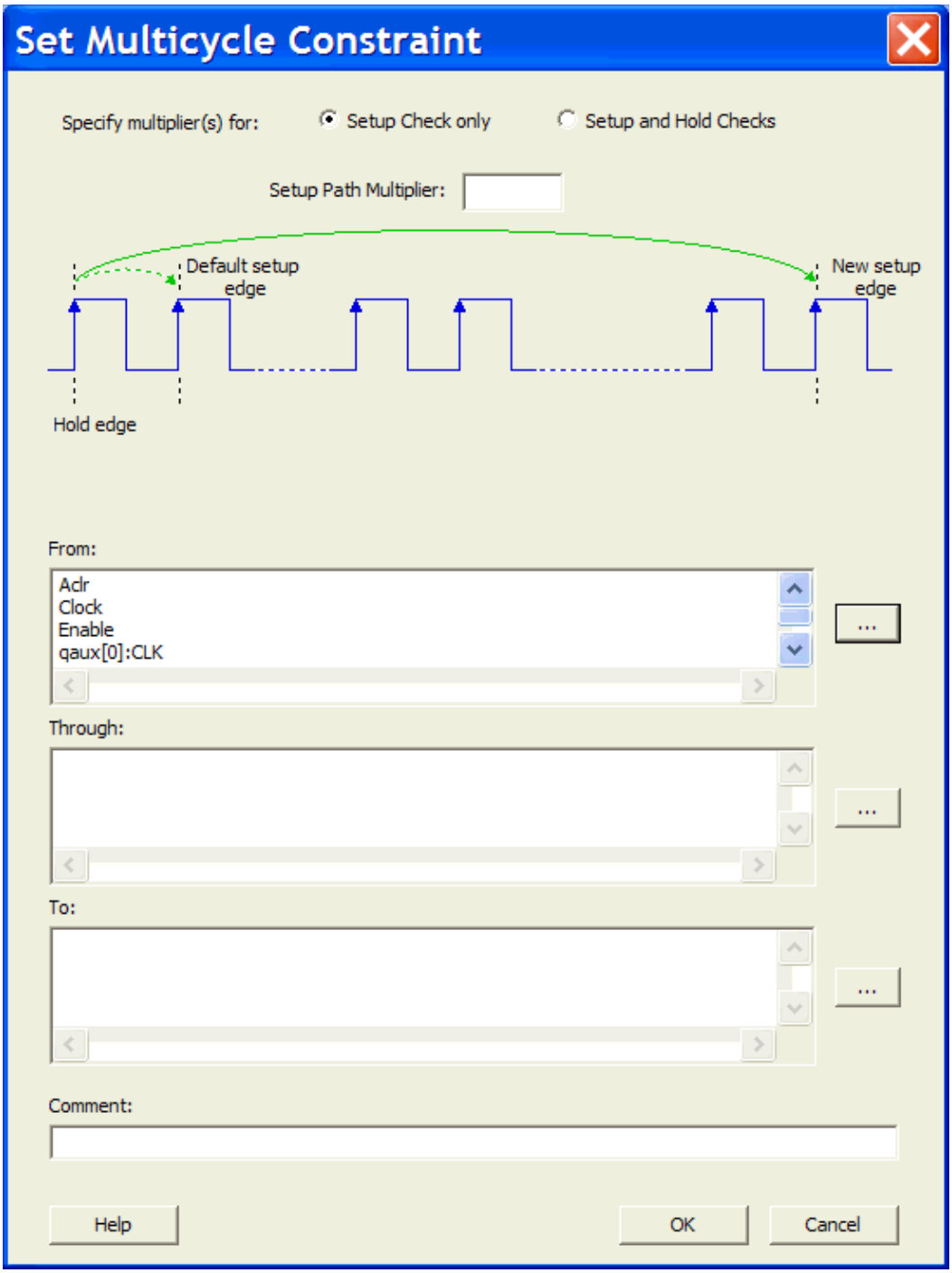


Figure 63 · Set Multicycle Constraint Dialog Box

8. Click the browse button for **Through** and **To** and add the appropriate pins. The displayed list shows the pins reachable from the previously selected pin(s) list.
9. Enter comments in the **Comment** section.
10. Click **OK**. SmartTime adds the multicycle constraints to the Constraints List in the SmartTime Constraints Editor.

See Also

Set Multicycle Constraint Dialog Box

Specifying a False Path Constraint

You set options in the Set False Path Constraint dialog box to define specific timing paths as false.

To specify False Path constraints:

1. Add the constraint in the Editable Constraints Grid or open the Set False Path Constraint dialog box. You can do this by using one of the following methods:
   - From the SmartTime **Constraints** menu, choose **False Path**.
   - Click the  icon.
   - Right-click **False Path** in the Constraint Browser and choose **Add False Path Constraint**.

   The Set False Path Constraint dialog box appears (as shown below).

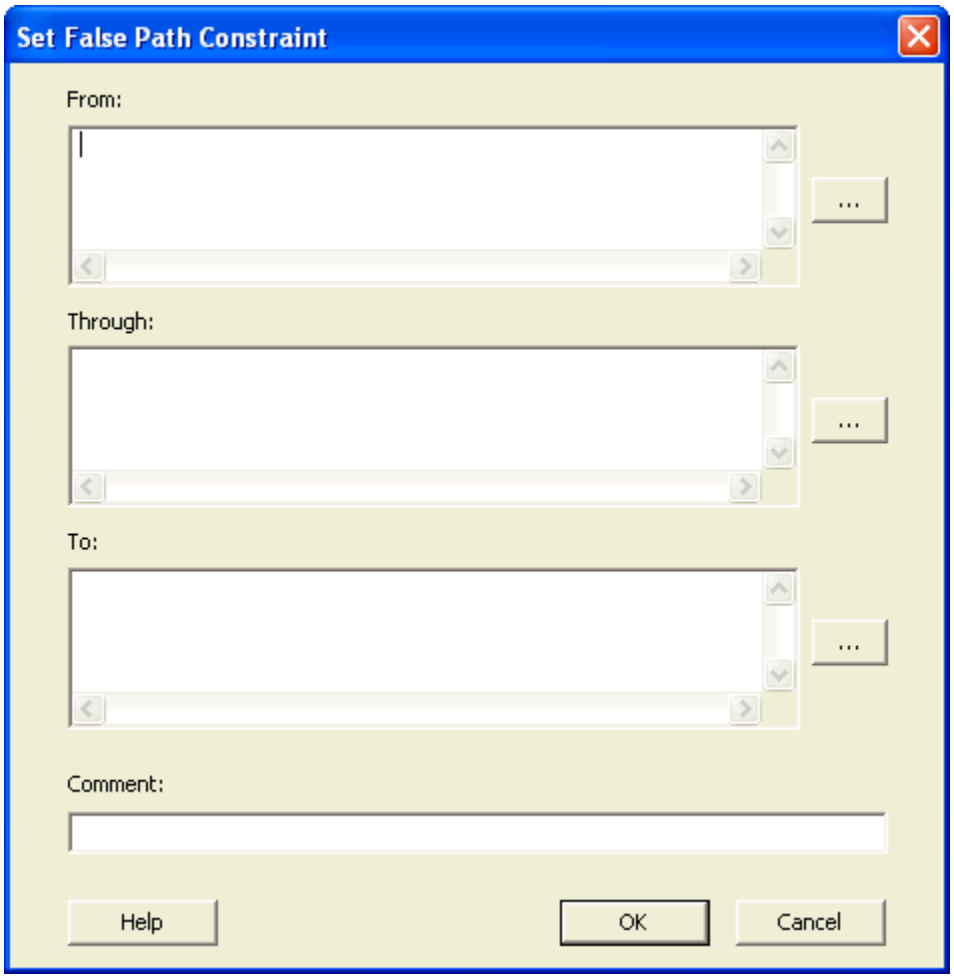


Figure 64 · Set False Path Constraint Dialog Box

2. Specify the **From** pin(s). Click the **Browse** button next to **From** to open the Select Source Pins for False Path Constraint dialog box (as shown below).

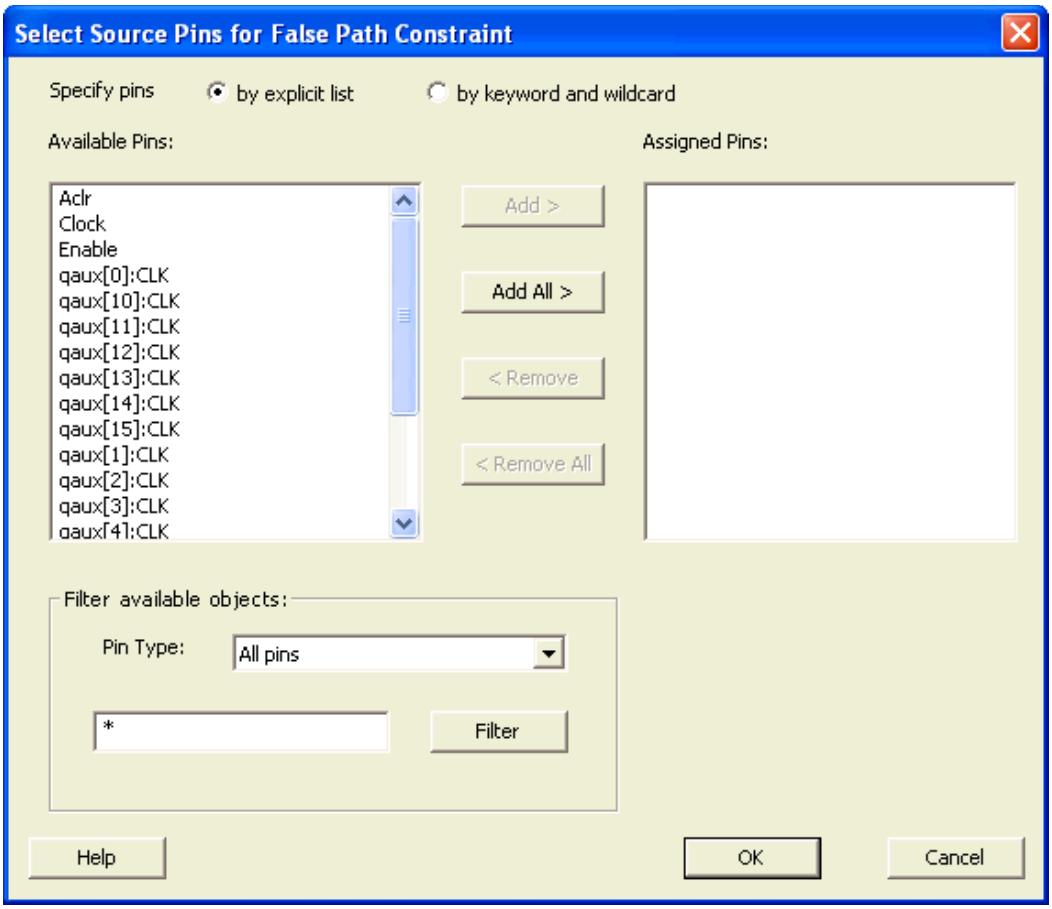


Figure 65 · Select Source Pins for False Path Constraint Dialog Box

3. Select **by explicit list**. (Alternatively, you can select **by keyword and wildcard**. For details, refer to Select Source or Destination Pins for Constraint Dialog Box.)
4. Select the input pin(s) from the **Available Pin** list. You can use **Filter available objects** to narrow the pin list. You can select multiple ports in this window.
5. Click **Add** or **Add All.** The input pin(s) move from the **Available Pins** list to the **Assigned Pins** list.
6. Click **OK**.

The Set False Path Constraint dialog box displays the updated representation of the **From** pin(s).

7. Click the **Browse** button for **Through** and **To** and add the appropriate pin(s). The displayed list shows the pins reachable from the previously selected pin(s) list.
8. Enter comments in the **Comment** section.
9. Click **OK**.

SmartTime adds the False Path constraints to the Constraints List in the SmartTime Constraints Editor.

See Also

Set False Path Constraint Dialog Box

Set False Path

Families Supported

The following table shows which families support this constraint and which file formats and tools you can use to enter or modify it:

Families	SDC	SmartTime	Constraints Editor
RTG4	X	X [1]	X[2]
IGLOO2	X	X [1]	X[2]
SmartFusion2	X	X [1]	X[2]
IGLOO	X	X	
SmartFusion	X	X	
Fusion	X	X	
ProASIC3	X	X	

1 For Libero SoC Design Flow (Classic Constraint Flow)

2 For Libero SoC Design Flow (Enhanced Constraint Flow) - SmartFusion2, IGLOO2, RTG4

Purpose

Use this constraint to identify paths in the design that should be disregarded during timing analysis and timing optimization.

By definition, false paths are paths that cannot be sensitized under any input vector pair. Therefore, including false paths in timing calculation may lead to unrealistic results. For accurate static timing analysis, it is important to identify the false paths.

You can set false paths constraints in an SDC file, which you can either create yourself or generate with Synthesis tools, at the same time you import the netlist. Alternatively, you can set false paths using the GUI tools in the Designer software when you implement your design.

Tools /How to Enter

You can use one or more of the following commands or GUI tools to set false paths:

- SDC – set_false_path
- SmartTime - Specifying False Path Constraint

See Also

Constraint Entry

set_false_path (SDC)

Breaks Tab

Specifying False Path Constraint

Specifying Disable Timing Constraint

Use disable timing constraint to specify the timing arcs being disabled.

To specify the disable timing constraint:

1. Add the constraint in the Editable Constraints Grid or open the Set Constraint to Disable Timing Arcs Dialog Box using one of the following methods:
   - From the SmartTime Constraints Editor, choose **Constraints > Disable Timing.**
   - Click the  icon in the Constraints Editor.
   - In the Constraints Editor, right-click **Disable Timing** and choose **Add Constraints** to disable timing ..
2. Select an instance from your design.
3. Select whether you want to exclude all timing arcs in the instance or if you want to specify the timing arc to exclude. If you selected specify timing arc to exclude, select a from and to port for the timing arc.
4. Enter any comments to be attached to the constraint.
5. Click **OK**. The new constraint appears in the constraints list.

   Note: When you choose Save from the File menu, SmartTime saves the newly-created constraint in the database.

See Also

Set Constraint to Disable Timing Arcs Dialog Box

Specifying Clock Constraints

Specifying clock constraints is the most effective way to constrain and verify the timing behavior of a sequential design. Use clock constraints to meet your performance goals.

To specify a clock constraint:

1. Add the constraint in the editable constraints grid or open the Create Clock Constraint dialog box using one of the following methods:
   - Click the  icon in the Constraints Editor.
   - Right-click the **Clock** in the Constraint Browser and choose **Add Clock Constraint**.
   - Double-click **Clock** in the Constraint Browser.

The Create Clock Constraint dialog box appears (as shown below).

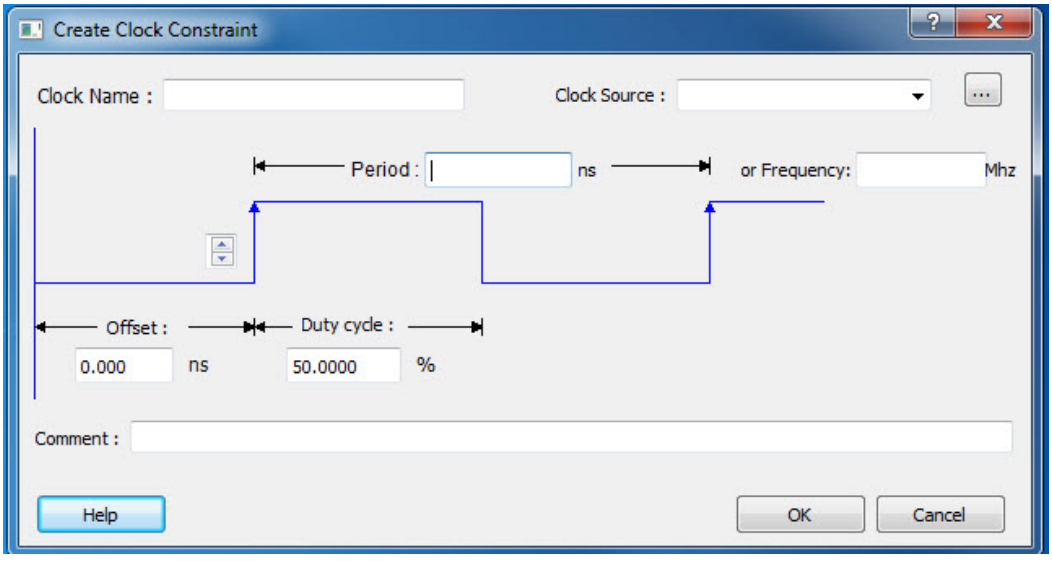


Figure 66 · Create Clock Constraint Dialog Box

2. Select the pin to use as the clock source. You can click the **Browse** button to display the Select Source Pins for Clock Constraint Dialog Box (as shown below).

   Note: Do not select a source pin when you specify a virtual clock. Virtual clocks can be used to define a clock outside the FPGA that it is used to synchronize I/Os.

   Use the Choose the Clock Source Pin dialog box to display a list of source pins from which you can choose. By default, it displays the explicit clock sources of the design. To choose other pins in the design as clock source pins, select **Filter available objects - Pin Type** as **Explicit clocks**, **Potential clocks**, **All Ports**, **All Pins**, **All Nets**, **Pins on clock network**, or **Nets in clock network**. To display a subset of the displayed clock source pins, you can create and apply a filter.

   Multiple source pins can be specified for the same clock when a single clock is entering the FPGA using multiple inputs with different delays.

   Click **OK** to save these dialog box settings.
3. Specify the **Period** in nanoseconds (ns) or **Frequency** in megahertz (MHz).
4. Modify the **Clock Name**. The name of the first clock source is provided as default.
5. Modify the **Duty cycle**, if needed.
6. Modify the **Offset** of the clock, if needed.
7. Modify the first edge direction of the clock, if needed.
8. Click **OK**. The new constraint appears in the Constraints List.

   Note: When you choose File > Save, SmartTime saves the newly created constraint in the database.

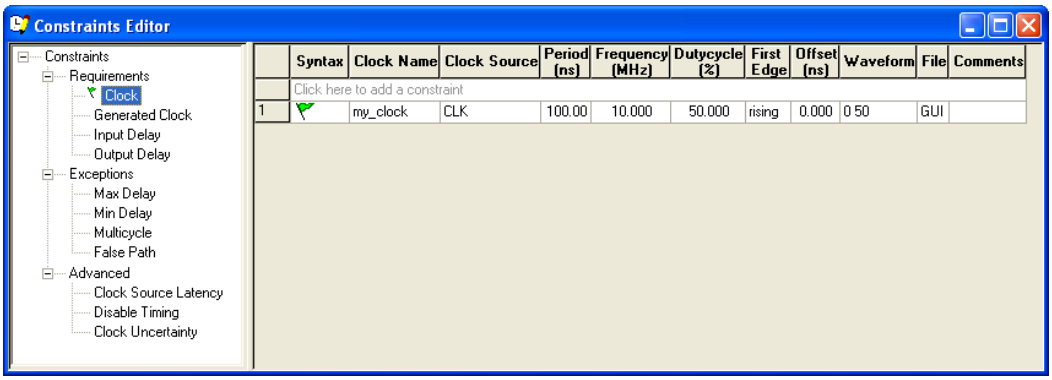


Figure 67 · SmartTime Timing Constraint View

See Also

Clock definition

Create a Clock

Create Clock Constraint Dialog Box

set_clock_uncertainty

Tcl command; specifies a clock-to-clock uncertainty between two clocks (from and to) and returns the ID of the created constraint if the command succeeded.

```
set_clock_uncertainty uncertainty -from | -rise_from | -fall_from from_clock_list -to | -
rise_to | -fall_to to_clock_list -setup {value} -hold {value}
```

Arguments

uncertainty

Specifies the time in nanoseconds that represents the amount of variation between two clock edges.

`-from`

Specifies that the clock-to-clock uncertainty applies to both rising and falling edges of the source clock list. Only one of the `-from`, `-rise_from`, or `-fall_from` arguments can be specified for the constraint to be valid.

`-rise_from`

Specifies that the clock-to-clock uncertainty applies only to rising edges of the source clock list. Only one of the `-from`, `-rise_from`, or `-fall_from` arguments can be specified for the constraint to be valid.

`-fall_from`

Specifies that the clock-to-clock uncertainty applies only to falling edges of the source clock list. Only one of the `-from`, `-rise_from`, or `-fall_from` arguments can be specified for the constraint to be valid.

`from_clock_list`

Specifies the list of clock names as the uncertainty source.

`-to`

Specifies that the clock-to-clock uncertainty applies to both rising and falling edges of the destination clock list. Only one of the `-to`, `-rise_to` , or `-fall_to` arguments can be specified for the constraint to be valid.

`-rise_to`

Specifies that the clock-to-clock uncertainty applies only to rising edges of the destination clock list. Only one of the `-to`, `-rise_to` , or `-fall_to` arguments can be specified for the constraint to be valid.

`-fall_to`

Specifies that the clock-to-clock uncertainty applies only to falling edges of the destination clock list. Only one of the `-to`, `-rise_to` , or `-fall_to` arguments can be specified for the constraint to be valid.

`to_clock_list`

Specifies the list of clock names as the uncertainty destination.

`-setup`

Specifies that the uncertainty applies only to setup checks. If none or both `-setup` and `-hold` are present, the uncertainty applies to both setup and hold checks.

`-hold`

Specifies that the uncertainty applies only to hold checks. If none or both `-setup` and `-hold` are present, the uncertainty applies to both setup and hold checks.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Description

The set_clock_uncertainty command sets the timing uncertainty between two clock waveforms or maximum clock skew. Timing between clocks have no uncertainty unless you specify it.

Examples

```
set_clock_uncertainty 10 -from Clk1 -to Clk2
set_clock_uncertainty 0 -from Clk1 -fall_to { Clk2 Clk3 } -setup
set_clock_uncertainty 4.3 -fall_from { Clk1 Clk2 } -rise_to *
set_clock_uncertainty 0.1 -rise_from [ get_clocks { Clk1 Clk2 } ] -fall_to { Clk3 Clk4 }
-setup
set_clock_uncertainty 5 -rise_from Clk1 -to [ get_clocks {*} ]
```

See Also

`create_clock`

`create_generated_clock`

`remove_clock_uncertainty`

Designer Tcl Command Reference

set_clock_groups

set_clock_groups is an SDC command which disables timing analysis between the specified clock groups. No paths are reported between the clock groups in both directions. Paths between clocks in the same group continue to be reported.

```
set_clock_groups [-name name]
                 [-physically_exclusive | -logically_exclusive | -asynchronous]
                 [-comment comment_string]
                 -group clock_list
```

Note: If you use the same name and the same exclusive flag of a previously defined clock group to create a new clock group, the previous clock group is removed and a new one is created in its place.

Arguments

`-name name`

Name given to the clock group. Optional.

`-physically_exclusive`

Specifies that the clock groups are physically exclusive with respect to each other. Examples are multiple clocks feeding a register clock pin. The exclusive flags are all mutually exclusive. Only one can be specified.

`-logically_exclusive`

Specifies that the clocks groups are logically exclusive with respect to each other. Examples are clocks passing through a mux.

`-asynchronous`

Specifies that the clock groups are asynchronous with respect to each other, as there is no phase relationship between them. The exclusive flags are all mutually exclusive. Only one can be specified.

Note: The exclusive flags for the arguments above are all mutually exclusive. Only one can be specified.

`-group clock_list`

Specifies a list of clocks. There can any number of groups specified in the set_clock_groups command.

Supported Families

SmartFusion2, IGLOO2, RTG4

Example

```
set_clock_groups –name mygroup3 –physically_exclusive \
–group [get_clocks clk_1] –group [get_clocks clk_2]
```

See Also

list_clock_groups

remove_clock_groups

set_false_path

Tcl command; identifies paths that are considered false and excluded from the timing analysis in the current timing scenario.

```
set_false_path [-from from_list] [-through through_list] [-to to_list]
```

Arguments

`-from from_list`

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

`-through` *`through_list`*

Specifies a list of pins, ports, cells, or nets through which the disabled paths must pass.

`-to` *`to_list`*

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Description

The `set_false_path` command identifies specific timing paths as being false. The false timing paths are paths that do not propagate logic level changes. This constraint removes timing requirements on these false paths so that they are not considered during the timing analysis. The path starting points are the input ports or register clock pins, and the path ending points are the register data pins or output ports. This constraint disables setup and hold checking for the specified paths.

The false path information always takes precedence over multiple cycle path information and overrides maximum delay constraints. If more than one object is specified within one -through option, the path can pass through any objects.

You must specify at least one of the `–from`, `-to`, or `–through` arguments for this constraint to be valid.

Examples

The following example specifies all paths from clock pins of the registers in clock domain clk1 to data pins of a specific register in clock domain clk2 as false paths:

```
set_false_path –from [get_clocks {clk1}] –to reg_2:D
```

The following example specifies all paths through the pin U0/U1:Y to be false:

```
set_false_path -through U0/U1:Y
```

See Also

Tcl Command Documentation Conventions

Designer Tcl Command Reference

set_max_delay

Tcl command; specifies the maximum delay for the timing paths in the current scenario.

```
set_max_delay delay_value [-from from_list] [-to to_list] [-through through_list]
```

Arguments

`delay_value`

Specifies a floating point number in nanoseconds that represents the required maximum delay value for specified paths.

- If the path starting point is on a sequential device, the tool includes clock skew in the computed delay.
- If the path starting point has an input delay specified, the tool adds that delay value to the path delay.
- If the path ending point is on a sequential device, the tool includes clock skew and library setup time in the computed delay.
- If the ending point has an output delay specified, the tool adds that delay to the path delay.

`-from` *`from_list`*

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

`-to` *`to_list`*

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

`-through` *`through_list`*

Specifies a list of pins, ports, cells, or nets through which the timing paths must pass.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Description

This command specifies the required maximum delay for timing paths in the current design. The path length for any startpoint in from_list to any endpoint in to_list must be less than delay_value.

The timing engine automatically derives the individual maximum delay targets from clock waveforms and port input or output delays.

The maximum delay constraint is a timing exception. This constraint overrides the default single cycle timing relationship for one or more timing paths. This constraint also overrides a multicycle path constraint.

You must specify at least one of the `–from`, `-to`, or `–through` arguments for this constraint to be valid.

Examples

The following example sets a maximum delay by constraining all paths from ff1a:CLK or ff1b:CLK to ff2e:D with a delay less than 5 ns:

```
set_max_delay 5 -from {ff1a:CLK ff1b:CLK} -to {ff2e:D}
```

The following example sets a maximum delay by constraining all paths to output ports whose names start by “out” with a delay less than 3.8 ns:

```
set_max_delay 3.8 -to [get_ports out*]
```

See Also

`set_min_delay`

`remove_max_delay`

Tcl Command Documentation Conventions

Designer Tcl Command Reference

set_multicycle_path

Tcl command; defines a path that takes multiple clock cycles in the current scenario.

```
set_multicycle_path ncycles [-setup] [-hold] [-from from_list[–through through_list[-to
to_list
```

Arguments

`ncycles`

Specifies an integer value that represents a number of cycles the data path must have for setup or hold check. The value is relative to the starting point or ending point clock, before data is required at the ending point.

`-setup`

Optional. Applies the cycle value for the setup check only. This option does not affect the hold check. The default hold check will be applied unless you have specified another set_multicycle_path command for the hold value.

`-hold`

Optional. Applies the cycle value for the hold check only. This option does not affect the setup check.

Note: If you do not specify "-setup" or "-hold", the cycle value is applied to the setup check and the default hold check is performed (*ncycles* -1).

`-from` *`from_list`*

Specifies a list of timing path starting points. A valid timing starting point is a clock, a primary input, an inout port, or a clock pin of a sequential cell.

`-through` *`through_list`*

Specifies a list of pins or ports through which the multiple cycle paths must pass.

`-to` *`to_list`*

Specifies a list of timing path ending points. A valid timing ending point is a clock, a primary output, an inout port, or a data pin of a sequential cell.

Supported Families

See the Tcl Commands and Supported Families table for the list of families that support this command.

Description

Setting multiple cycle paths constraint overrides the single cycle timing relationships between sequential elements by specifying the number of cycles that the data path must have for setup or hold checks. If you change the multiplier, it affects both the setup and hold checks.

False path information always takes precedence over multiple cycle path information. A specific maximum delay constraint overrides a general multiple cycle path constraint.

If you specify more than one object within one -through option, the path passes through any of the objects.

You must specify at least one of the `–from`, `-to`, or `–through` arguments for this constraint to be valid.

Exceptions

Multiple priority management is not supported in Microsemi SoC designs. All multiple cycle path constraints are handled with the same priority.

Examples

The following example sets all paths between reg1 and reg2 to 3 cycles for setup check. Hold check is measured at the previous edge of the clock at reg2.

```
set_multicycle_path 3 -from [get_pins {reg1}] –to [get_pins {reg2}]
```

The following example specifies that four cycles are needed for setup check on all paths starting at the registers in the clock domain ck1. Hold check is further specified with two cycles instead of the three cycles that would have been applied otherwise.

```
set_multicycle_path 4 -setup -from [get_clocks {ck1}]
set_multicycle_path 2 -hold -from [get_clocks {ck1}]
```

See Also

`remove_multicycle_path`

Tcl Command Documentation Conventions

Designer Tcl Command Reference

remove_clock_groups

This Tcl command removes a clock group by name or by ID.

```
remove_clock_groups [-id id# | –name groupname] \
[-physically_exclusive | -logically_exclusive | -asynchronous]
```

Note: The exclusive flag is not needed when removing a clock group by ID.

Arguments

`-id id#`

Specifies the clock group by the ID.

`-name groupname`

Specifies the clock group by name (to be always followed by the exclusive flag).

`[-physically_exclusive | -logically_exclusive | - asynchronous]`

Supported Families

SmartFusion2, IGLOO2, RTG4

Example

Removal by group name

```
remove_clock_groups –name mygroup3 –physically_exclusive
```

Removal by goup ID

```
remove_clock_groups –id 12
```

See Also

set_clock_groups

list_clock_groups

list_clock_groups

This Tcl command lists all existing clock groups in the design.

```
list_clock_groups
```

Arguments

None

Supported Families

SmartFusion2, IGLOO2, RTG4

Example

```
list_clock_groups
```

See Also

set_clock_groups

remove_clock_groups