IGLOO2 FPGA CoreTSE MAC 1000 Base-T Loopback Demo – Libero SoC v11.6

DG0633 Demo Guide

September 2015

Microsemi

Revision History

Date	Revision	Change
25 September 2015	1	First release

Confidentiality Status

This is a non-confidential document.

Table of Contents

Preface . . . 4
About this document . . . 4
Intended Audience . . . 4
References . . . 4
Microsemi Publications . . . 4

IGLOO2 FPGA CoreTSE IP 1000 Base-T Loopback Demo Design . . . 5
Introduction . . . 5
Design Requirements . . . 6
Demo Design . . . 6
Introduction . . . 6
Demo Design Features . . . 7
Demo Design Description . . . 8
Simulating the Design . . . 9
Simulation . . . 9
Setting Up the Demo Design . . . 12
Programming the Demo Design . . . 12
Connecting IGLOO2 Evaluation Kit Board to Host PC . . . 14
Running the Demo Design with Cat Karat and Wireshark on the Hardware . . . 15

Appendix: Running the Demo Design using Spirent Test Center . . . 18

A List of Changes . . . 20

B Product Support . . . 21
Customer Service . . . 21
Customer Technical Support Center . . . 21
Technical Support . . . 21
Website . . . 21
Contacting the Customer Technical Support Center . . . 21
Email . . . 21
My Cases . . . 22
Outside the U.S. . . . 22
ITAR Technical Support . . . 22

Preface

About this document

This demo is for IGLOO®2 field programmable gate array (FPGA) devices. It provides instructions on how to use the reference design.

Intended Audience

The following designers using the IGLOO2 devices:

- FPGA designers
- System-level designers

References

The following references are used in this document:

- *UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide*
- *UG0447: SmartFusion2 and IGLOO2 FPGA High Speed Serial Interfaces User Guide*

Microsemi Publications

Refer to the following web page for a complete and up-to-date listing of IGLOO2 device documentation:
http://www.microsemi.com/products/fpga-soc/fpga/igloo2docs

IGLOO2 FPGA CoreTSE IP 1000 Base-T Loopback Demo Design

Introduction

This demo design provides an Ethernet solution for the IGLOO2 FPGA and implements a CoreTSE IP-based 1000Base-T loopback design on the IGLOO2 Evaluation Kit.

Microsemi® Core triple-speed Ethernet (CoreTSE) media access controller (MAC) IP is a configurable soft intellectual property (IP) core that complies with the IEEE 802.3 standard. The CoreTSE IP core enables system designers to implement a broad range of Ethernet designs, from low-cost 10/100 Ethernet to higher-performance 1 gigabit ports. The CoreTSE IP core is suited for use in networking equipment such as switches, routers, and data acquisition systems. CoreTSE is also available in a version that works with SmartFusion®2 system-on-chip (SoC) FPGA family.

The CoreTSE IP has the following interfaces:

- 10/100/1000 Mbps Ethernet MAC with a gigabit media independent interface (GMII) and ten bit interface (TBI) to support serial gigabit media independent interface (SGMII), 1000BASE-T, and 1000BASE-X
- GMII or TBI physical layer interface connects to Ethernet PHY
- MAC data path interface
- Advanced peripheral bus (APB) slave interface for MAC configuration registers and status counter access

The CoreTSE IP Ethernet MAC can be configured as GMII or TBI for Ethernet network at 10/100/1000 Mbps data transfer rates (line speeds).

The CoreTSE IP core is available in two different versions:

- CoreTSE_AHB: Uses AHB interface for both the transmit and receive paths. This IP works for SmartFusion2 SoC FPGA.
- CoreTSE (Non-AMBA): Uses direct access to the MAC with a streaming packet interface. This IP works for IGLOO2 FPGA and SmartFusion2 SoC FPGA.

CoreTSE and CoreTSE_AHB are identical to MSS hard Ethernet MAC in SmartFusion2 with respect to the supported features, register configuration, and register addresses. Multiple CoreTSE IPs can be used in IGLOO2 to achieve Ethernet solutions. CoreTSE can be used in SmartFusion2 devices along with MSS Ethernet MAC to support multiple Ethernet interfaces. For more information about CoreTSE IP, refer to the *CoreTSE Handbook*.

For more information about Ethernet applications, refer to the *AC423: SmartFusion2/IGLOO2 Ethernet Application Note*.

Note: CoreTSE IP requires license for using in Libero® SoC design. For license request, send an email to soc_marketing@microsemi.com.

Design Requirements

Table 1 lists the design requirements for running the demo.

Table 1 • **Design Requirements**

Design Requirements	Description
Hardware Requirements	
IGLOO2 Evaluation Kit • 12 V adapter	Rev D or later
Host PC or Laptop (12 GB RAM)	Windows 64-bit Operating System
Spirent Test Center (Optional)	–
Software Requirements	
Libero SoC	v11.6
FlashPro Programming Software	v11.6
Cat Karat Packet Generator Software	Provided with design files
Wireshark Software	Provided with design files
IP Requirements	
CoreTSE IP	License provided on request

Demo Design

Introduction

The demo design files are available for download from the following path:
http://soc.microsemi.com/download/rsc/?f=m2gl_dg0633_liberov11p6_df

The demo design files include:

- Libero project
- Programming files
- Source files
- Readme.txt file

Refer to the `Readme.txt` file for the complete directory structure.

Figure 1 shows the top-level structure of the design files.

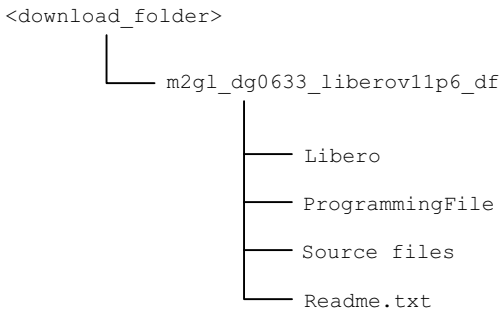


Figure 1 • **Demo Design Files Top-level Structure**

Figure 2 shows the demo design block diagram.

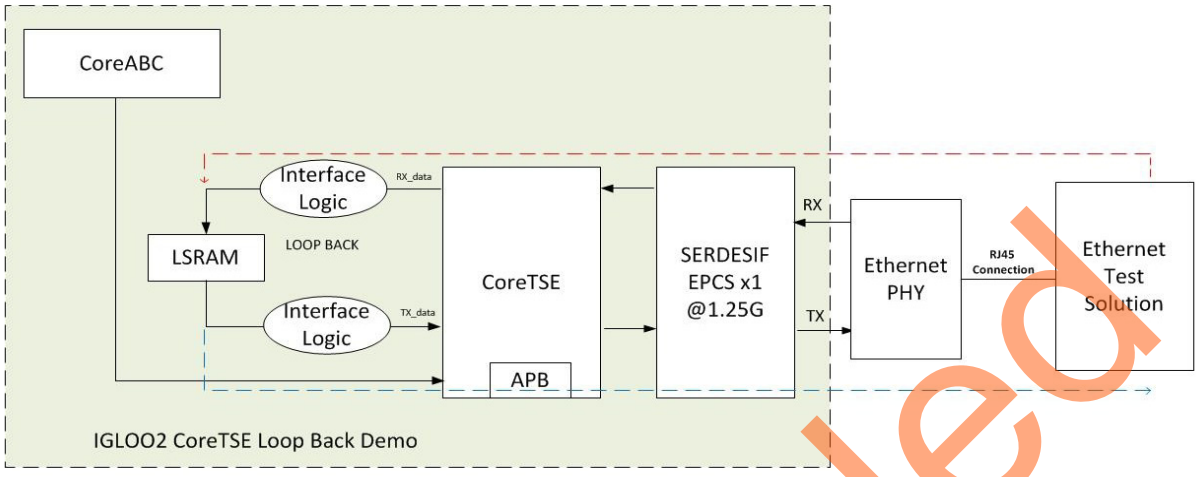


Figure 2 • **IGLOO2 CoreTSEIP 1000 Base-T Loop back Demo**

In this demo design CoreTSE IP is instantiated in the FPGA fabric and connected to the on-board Ethernet PHY using high-speed serial interface (SERDES_IF).

In Figure 2, the dotted arrow in red shows the transfer of Ethernet packet from the host PC to the internal LSRAM and the dotted arrow in blue shows the retransmission of packet from LSRAM to the host.

Demo Design Features

The demo design performs Ethernet loopback using CoreTSE in TBI 1000Base-T on hardware and also in simulation.

Following are the demo design features:

- Simulation model for CoreTSE loopback design.
- CoreTSE loopback design on IGLOO2 Evaluation Kit.

The following section explains the initialization and configuration of CoreTSE, SERDES_IF, and the loopback mechanism.

CoreTSE IP MAC Initialization

The CoreTSE IP MAC is configured in TBI mode. The CoreABC soft-core is used to initialize the CoreTSE MAC in 1000 Base-T and on-board Ethernet PHY.

Note: CoreABC is a Microsemi RISC processor that is implemented in logic gates. CoreABC IP is available in the Libero SoC software IP tools catalog.

High-Speed Serial Interface Configuration

The high-speed SERDES_IF is configured in the external physical coding sub layer (EPCS) mode lane 3 in the Libero GUI and is connected between CoreTSE MAC and on-board Ethernet PHY.

Ethernet Packet Loopback

The following Ethernet loopback mechanism is used in this demo:

Ethernet Packet Reception

The CoreTSE IP MAC receives the Ethernet packet from on-board Ethernet PHY through high-speed SERDES_IF.

The CoreTSE IP receive (RX) path is connected to LSRAM through the receive interface logic. This interface logic is implemented in Verilog RTL and is used to keep the packet on to LSRAM memory.

Ethernet Packet Transmission

To loop back the Ethernet packet, the interface logic implemented in Verilog RTL reads the Ethernet packet data from LSRAM memory and keeps it on CoreTSE transmit (TX) path.

CoreTSE MAC transmits the Ethernet packet to on-board Ethernet PHY through high-speed SERDES.

Ethernet Test Solution

There are many ways to evaluate the CoreTSE 1000 Base-T loopbackdemo on the IGLOO2 Evaluation Board.

Solution 1

- The Cat Karat packet generator software installed on the host PC is used to transmit the Ethernet packet through RJ45 Ethernet copper cable.
- The Wireshark packet receiver software installed on the host PC captures the Ethernet packet (loopback) through RJ45 Ethernet copper cable.

Solution 2

- Spirent test center,or an equivalent solution can be used to test the CoreTSE loopback demo. For more information, refer to Appendix: Running the Demo Design using Spirent Test Center.

Demo Design Description

This demo design is implemented by configuring the CoreTSE for the TBI mode. Figure 3 shows the Libero SoC hardware implementation for this demo design.

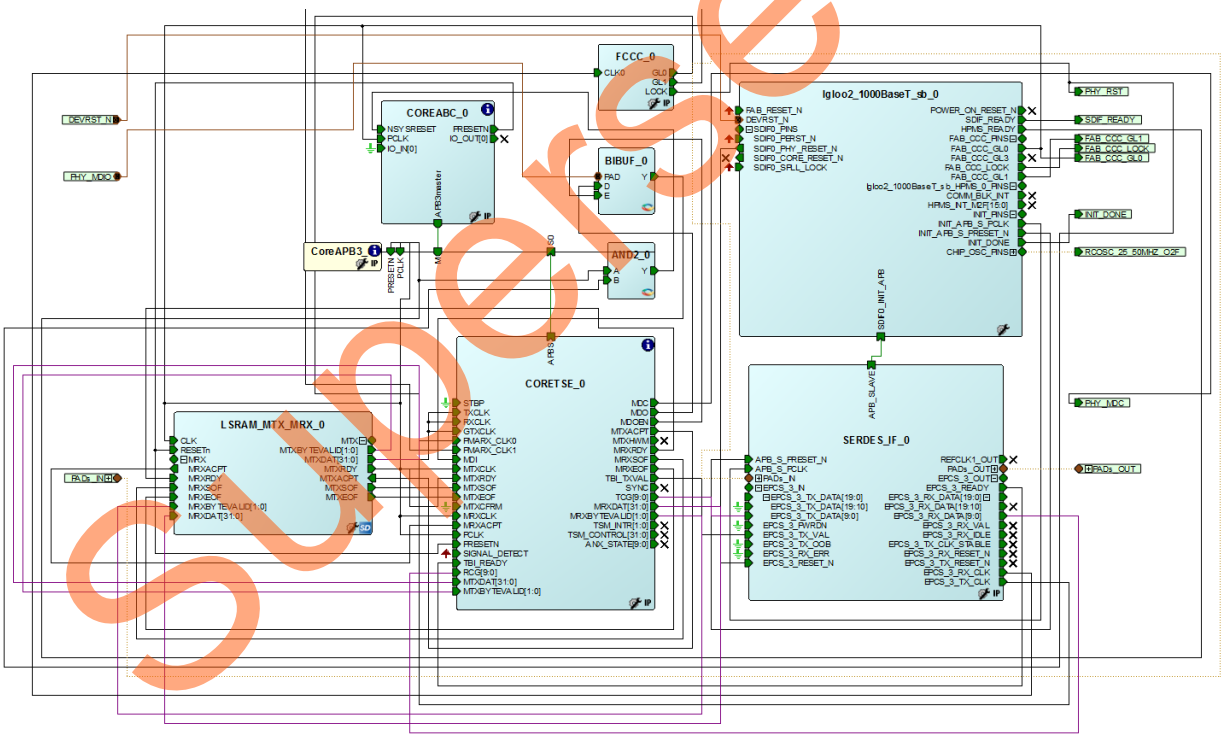


Figure 3 • **Libero SmartDesign**

Libero hardware project uses the following resources:

- CoreTSE MAC IP core
- CoreABC to configure CoreTSE MAC and on-board Ethernet PHY
- LSRAM interface logic uses TPSRAM, receives and transmits logic implemented in Verilog RTL
- High-speed serial interface (SERDES_IF) configured for EPCS lane 3 mode

Simulating the Design

The testbench design is created for CoreTSE loopback demo. The testbench transmits the Ethernet packet to CoreTSE loopback demo design and receives the loopback Ethernet packet from the CoreTSE loopback demo design.

Simulation

For simulation, the Ethernet packet is defined in a text file: (*\\m2gl_dg0633_liberov11p6_df\Libero\Simulation\CoreTSE_1000BaseT_Demo\simulation\packetfile.txt)*.

The Raw Ethernet Packet frame is:
010203040506070809 0a0b0c0d0e55555555555555555555555551b1c1d1e1f202122232425262728292a2b2c2d2e2f303132333435363738393a3b3c3d3e3f40.

Testbench reads the Ethernet packet from the text file and puts the Ethernet packet on to the high-speed SERDES_IF of CoreTSE loopback design.

The loopback packet is received by the testbench and displayed on the ModelSim transcript window.

Figure 4 and Figure 5 show the Libero SmartDesign to simulate the CoreTSE loopback demo design. The simulation testbench has the following Libero components:

- CoreTSE MAC IP core
- High-speed SERDES_IF
- Testbench with packet transmit and packet receive logic

The testbench smart design module reads the Ethernet packet from the `packetfile.txt` file and sends it to the IGLOO2 CoreTSE IP loopback design through high-speed serial interface. The loopback Ethernet packet is received by the testbench through high-speed serial interface. ModelSim displays the received Ethernet packet on the transcript window. This completes the Ethernet packet loopback simulation.

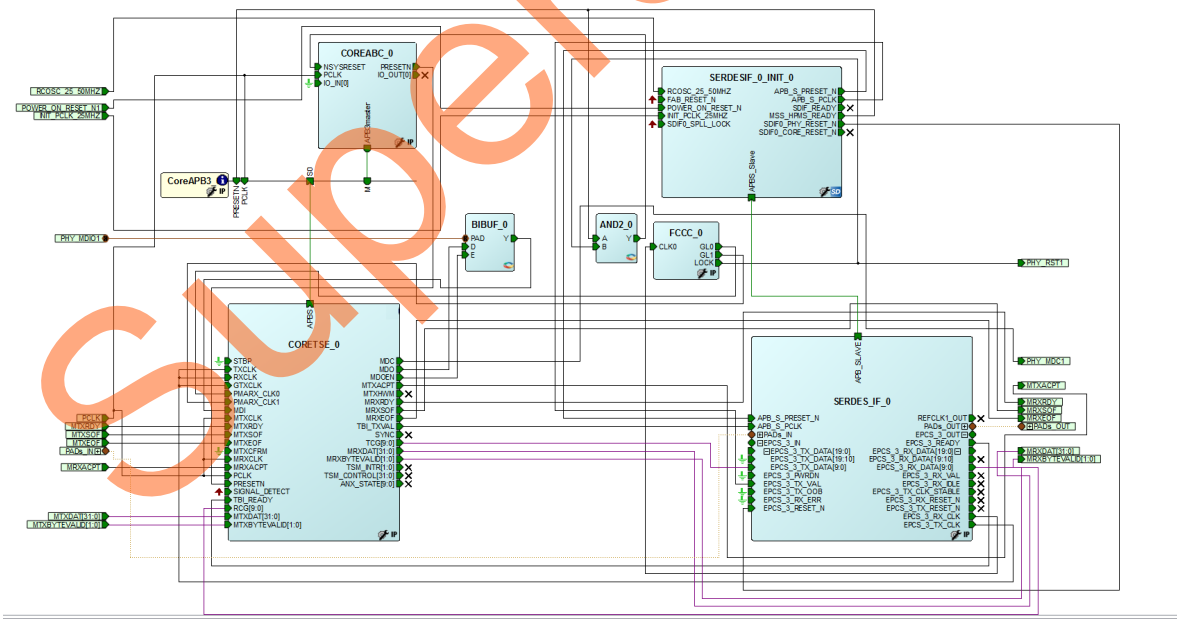


Figure 4 • **SmartDesign for Simulation**

The Libero SmartDesign top module contains the CoreTSE loopback design and the testbench module.

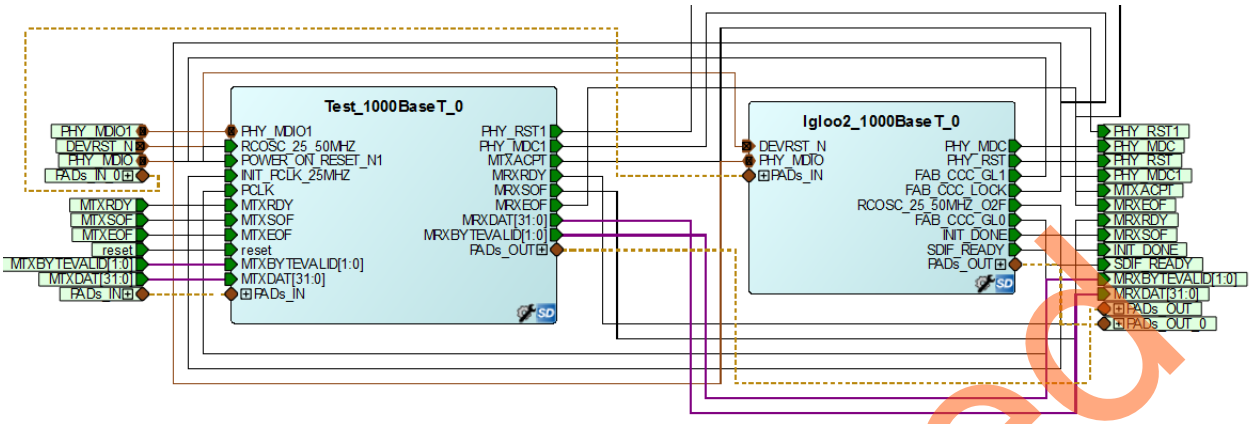


Figure 5 • **Libero SmartDesign Top Module**

The following steps describe how to simulate the demo:

1. Open the Libero project from the following design files: *\\m2gl_dg0633_liberov11p6_df\Libero\Simulation\CoreTSE_1000BaseT_Demo\CoreTSE_1000BaseT_Demo.prjx*.
2. In the **Design Flow** tab, under **Verify Pre-Synthesized Design,** double-click **Simulate**.

   ModelSim runs the design for 160 µs.
   Figure 6 shows the received Ethernet packet information displayed on the **ModelSim Transcript** window.

Figure 6 • **ModelSim Transcript Messages**

Figure 7 and Figure 8 show the **Waveform** window. The highlighted portion shows the transmitted and received Ethernet packets.

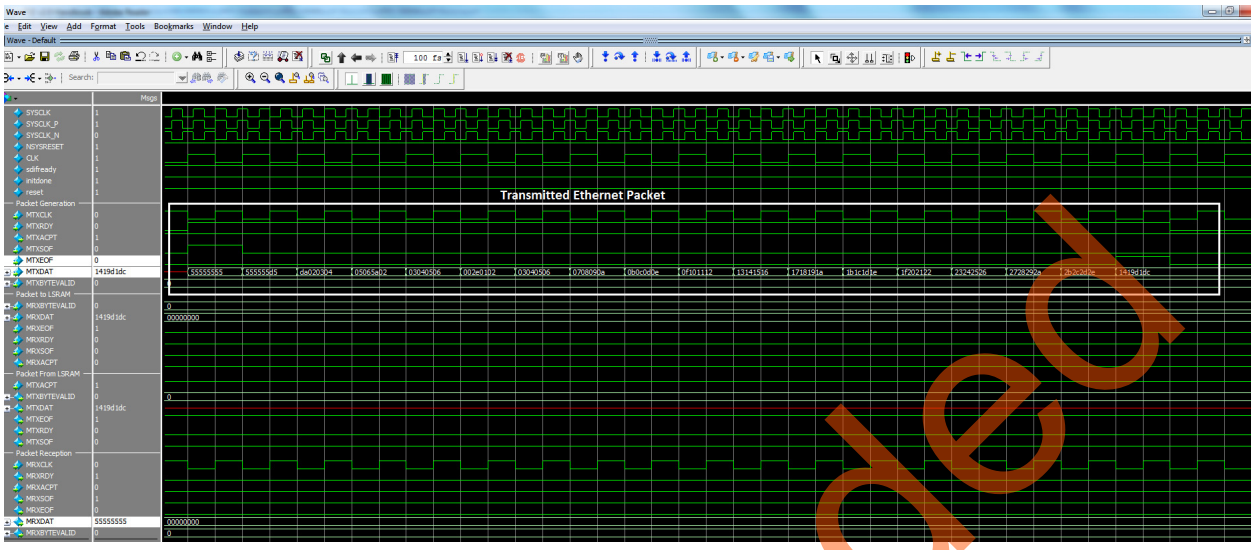


Figure 7 • **Simulation Window-Transmitted Ethernet Packet**

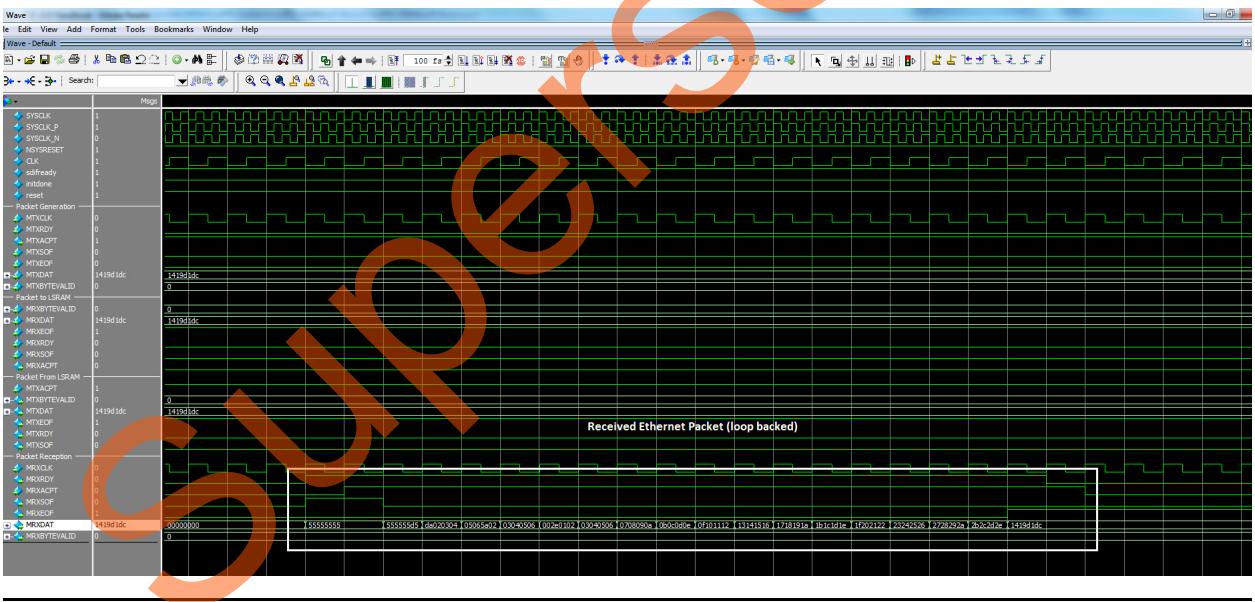


Figure 8 • **Simulation Window-Received Ethernet Packet**

Setting Up the Demo Design

The following steps describe how to setup the demo:

1. Connect the jumpers to the IGLOO2 FPGA Evaluation Kit board as shown in Table 2.
2. Connect the power supply to the J6 connector and switch it ON.
3. Connect the FlashPro4 Programmer to the J5 connector on the IGLOO2 FPGA Evaluation Kit board.

   Caution: Ensure that the power supply switch SW7 is switched off while connecting the jumpers to the IGLOO2 FPGA Evaluation Kit.

Table 2 • **IGLOO2 FPGA Evaluation Kit Jumper Settings**

Jumper	Pin (from)	Pin (to)	Comments
J22	1	2	Default
J23	1	2	Default
J24	1	2	Default
J8	1	2	Default
J3	1	2	Default

Programming the Demo Design

The following steps describe how to program the demo design:

1. Download the demo design from the following path:
   http://soc.microsemi.com/download/rsc/?f=m2gl_dg0633_liberov11p6_df
2. Switch ON the power supply switch, **SW7**.
3. Launch the **FlashPro** software.
4. Click **New Project**.
5. In the **New Project** window, enter the project name as **CoreTSE_Demo**.
6. Click **Browse** and navigate to the location where the project needs to be saved.
7. Select **Single device** as Programming mode.

8. Click **OK** to save the project.

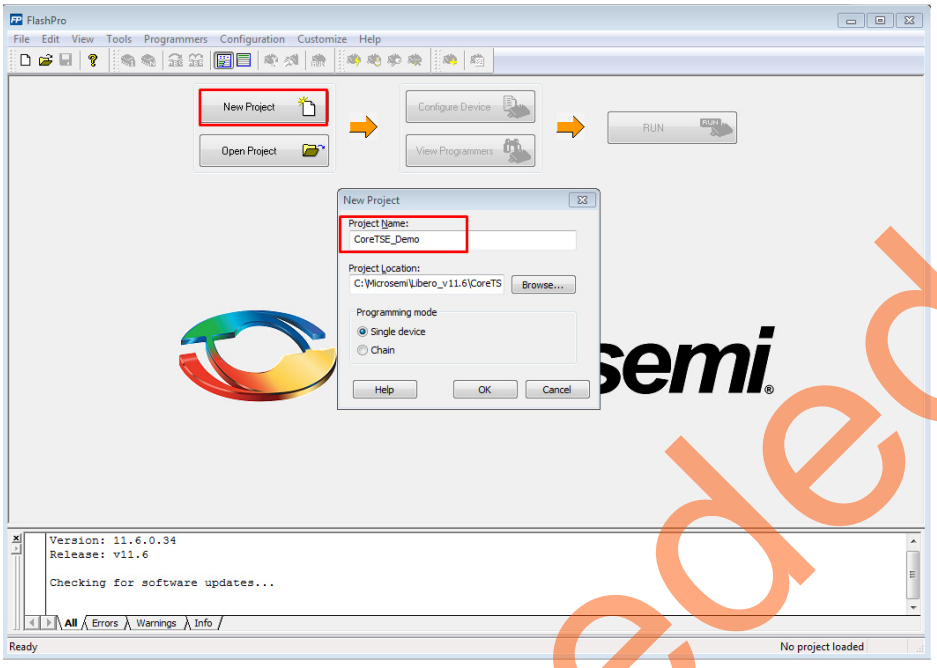


Figure 9 • **FlashPro New Project**

9. Click **Configure Device**.

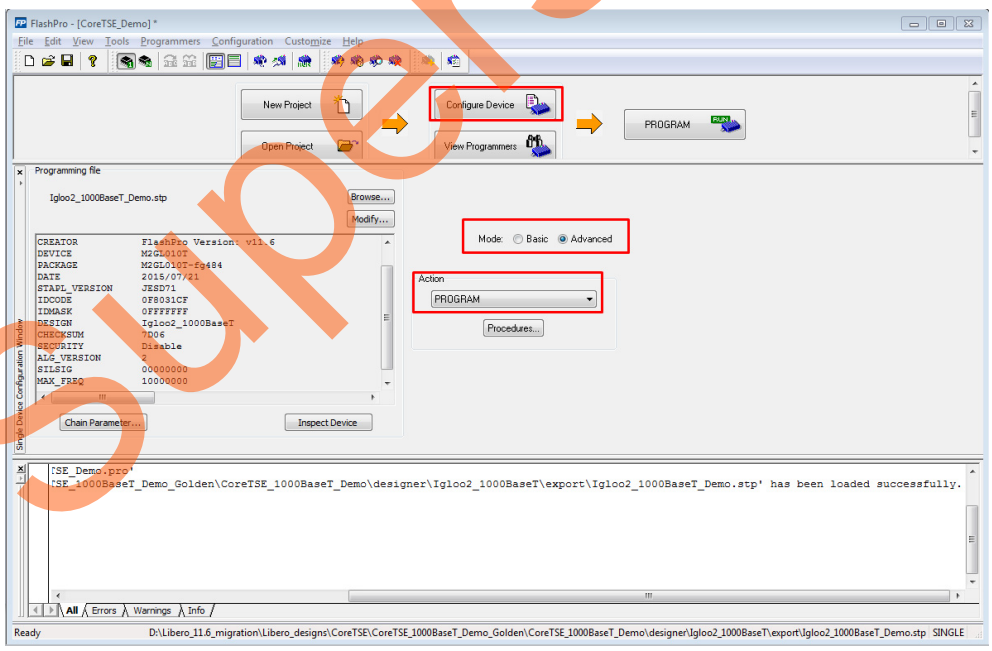


Figure 10 • **FlashPro Project Configuration**

10. Click **Browse** and navigate to the location where the `Igloo2_1000BaseT_Demo.stp` file is located and select the file. The default location is:

    <download_folder>\ m2gl_dg0633_liberov11p6_df\ProgrammingFile

11. Select **Advanced** as Mode and **PROGRAM** as Action.
12. Click **PROGRAM** to start programming the device. Wait until the programmer status is changed to **RUN PASSED**.

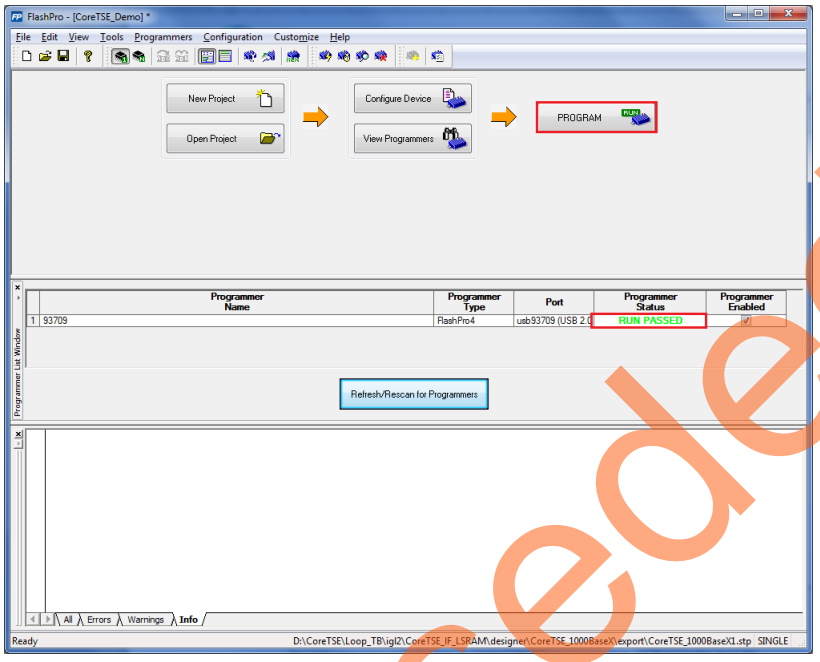


Figure 11 • **FlashPro Programming Passed**

Connecting IGLOO2 Evaluation Kit Board to Host PC

The following steps describe how to connect the IGLOO2 Evaluation Kit Board to the host PC:

1. After successful programming, switch OFF the IGLOO2 Evaluation Kit Board.
2. Connect the host PC to the J13 connector on the IGLOO2 Evaluation Kit using the RJ45 cable.

Figure 12 shows the IGLOO2 Evaluation Kit board setup.

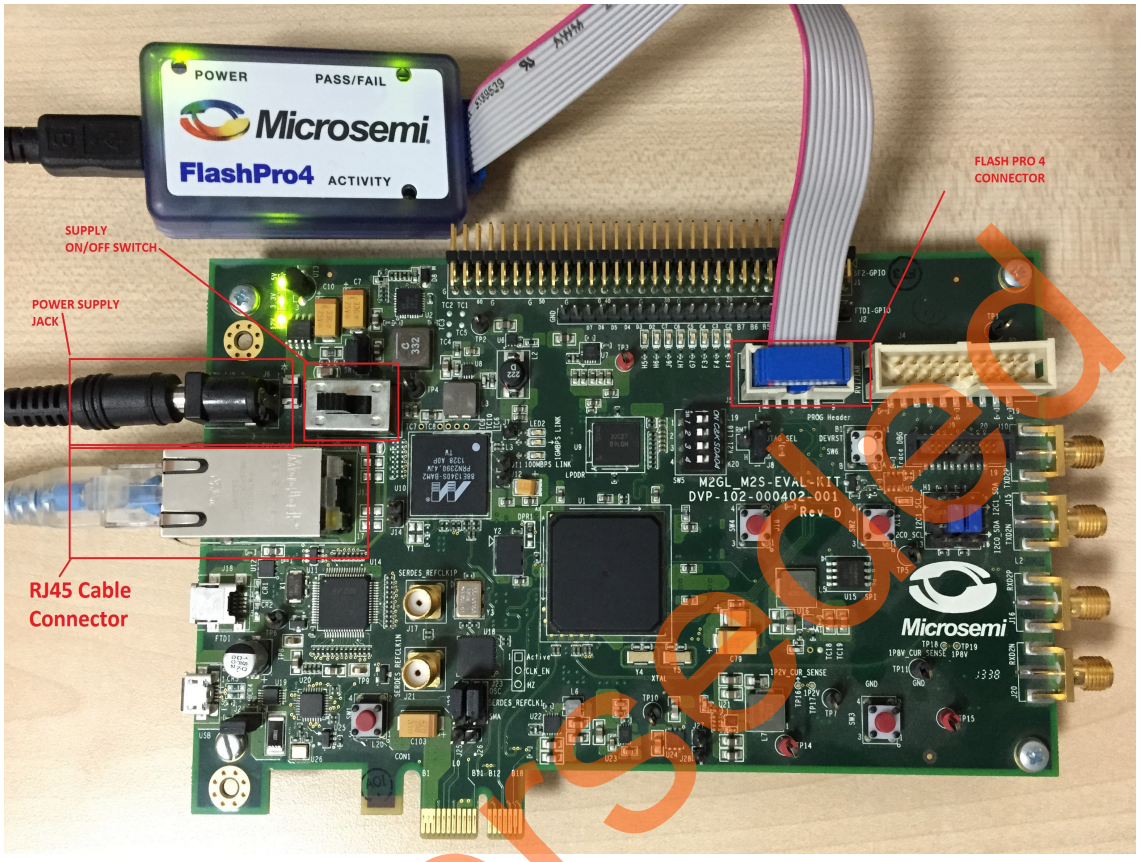


Figure 12 • **IGLOO2 Evaluation Kit Setup**

Running the Demo Design with Cat Karat and Wireshark on the Hardware

The following steps describe how to run the demo design:

1. Switch ON the power supply switch SW7.
2. Install the Cat Karat packet software and Wireshark software on the host PC from the source files. (*<download folder>\ m2gl_dg0633_liberov11p6_df \Source files*)

3. On the host PC, open the Wireshark network analyzer. Select **Start** as shown in Figure 13.

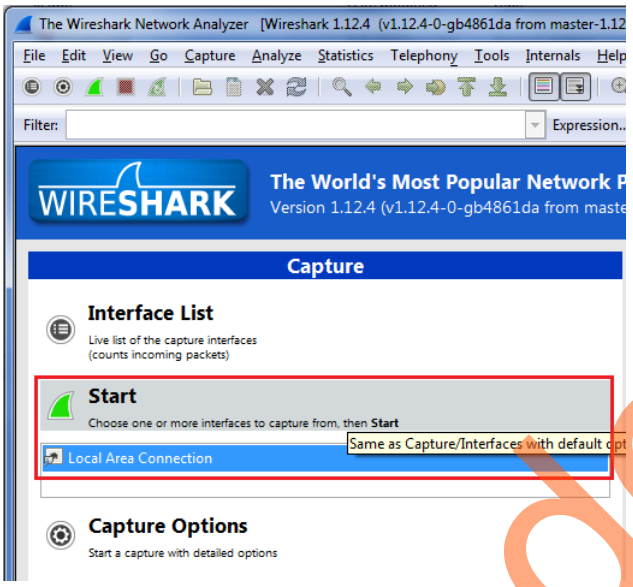


Figure 13 • **Wireshark Network Analyzer**

4. On the host PC, open the Cat Karat software as shown in Figure 14.

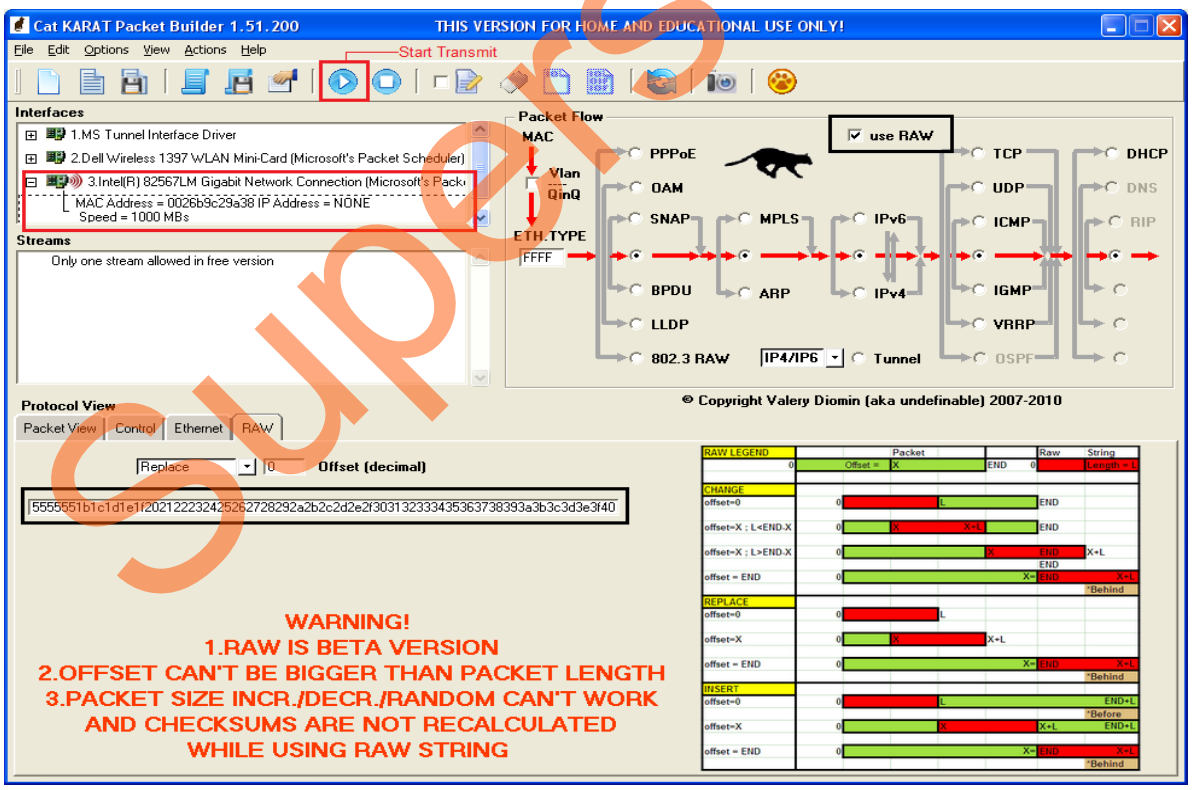


Figure 14 • **Cat Karat Packet Generate Window**

5. Under **Protocol View**, click the **Control** tab and enter the value 1 for **Packets per Burst** as shown in Figure 15.

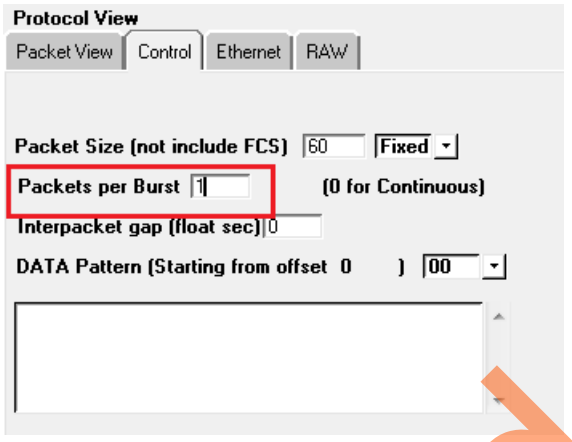


Figure 15 • **Packet Flow Control**

6. Under **Packet Flow,** click **use RAW** as shown in Figure 14.
7. Under **Protocol View**, select the **RAW** tab and copy and paste the Ethernet net packet from the source files (*<download folder>\ m2gl_dg0633_liberov11p6_df \Source files\Raw_frame.txt*) as shown in Figure 14.
8. Under **Interfaces,** select the Ethernet connection to the IGLOO2 Evaluation Board.
9. Select **Start Transmit** from the menu as shown in Figure 14, to transmit the packet.
10. In the Wireshark software window, double-click Ethernet-II, as shown in Figure 16. The transmitted and received Ethernet packets are displayed.

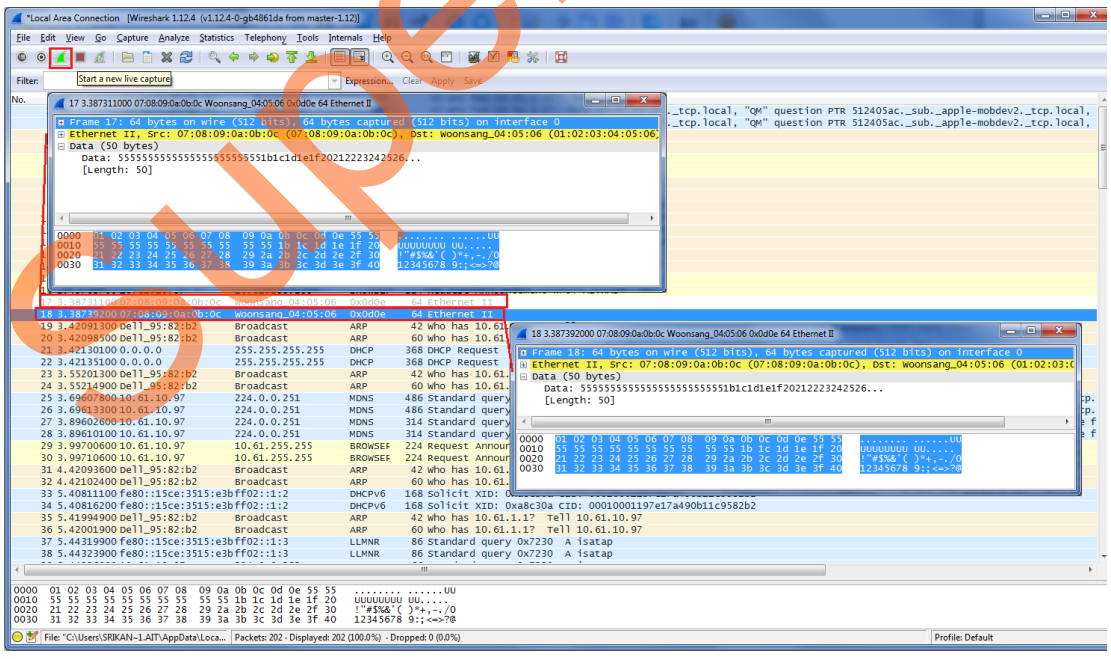


Figure 16 • **Wireshark Software Window**

Appendix: Running the Demo Design using Spirent Test Center

The following steps describe how to run the CoreTSE IP loopback demo using Spirent test center:

1. Connect the IGLOO2 Evaluation Kit to the slot 1 Ethernet port on the Spirent test equipment using the RJ45 cable.
2. In the host PC, open the Spirent test center configurator.
3. Add **port** (Ethernet) in Spirent test center as shown in Figure 1.

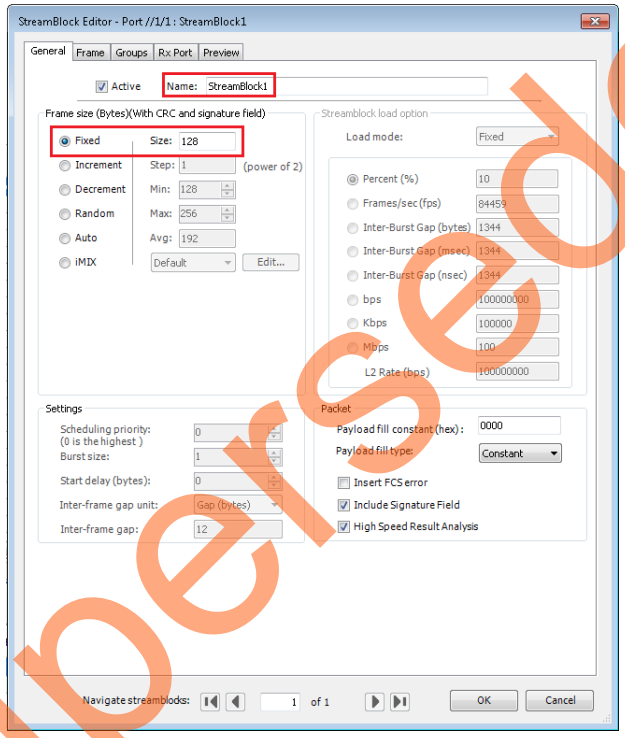


***Figure 1* • Spirent Test Center Stream Block – General Tab**

4. Select **Traffic generator** under **Port**, add packet information in stream block editor, and click **OK** as shown in Figure 2.

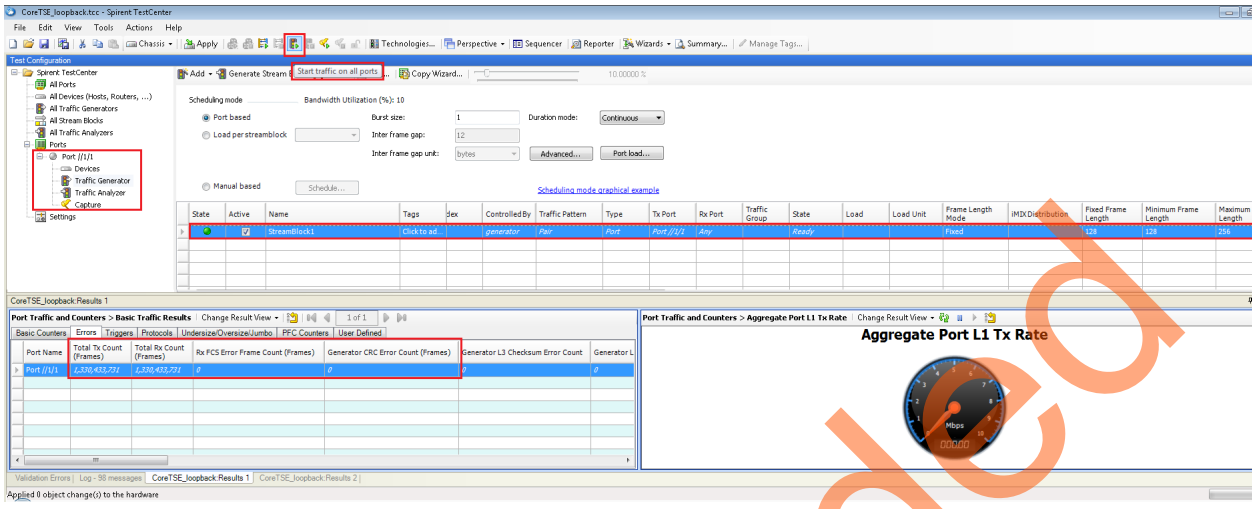


***Figure 2* • Spirent Test Center**

5. Click **Start traffic on all ports** as shown in Figure 2. Ethernet packets are transmitted and received on port1 through the RJ45 cable.
6. Observe the Total TX, RX, RX FCS, and CRC error counts.

   Figure 3 shows the total TX, RX, RX FCS, and CRC error count information in Spirent test center. 0 indicates no loss in the packet transmission and reception.

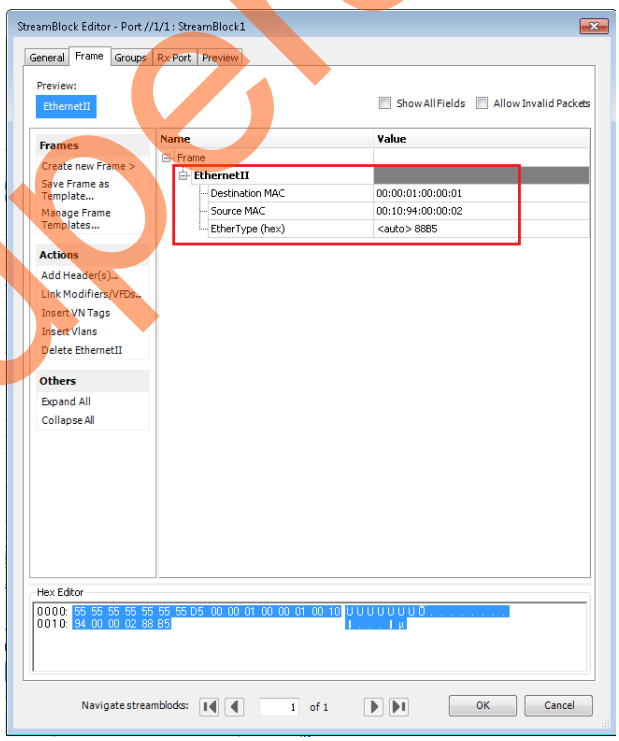


***Figure 3* • Spirent Test Center Stream Block – Frame Tab**

A – List of Changes

The following table shows important changes made in this document for each revision.

Revision*	Changes	Page
Revision 1 (September 2015)	Initial release	N/A

*Note: *The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.*

B – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

For Microsemi SoC Products Support, visit

http://www.microsemi.com/products/fpga-soc/designsupport/fpga-soc-support

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

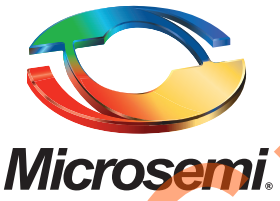
Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office.Visit About Us for sales office listings and corporate contacts.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.



Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 3,600 employees globally. Learn more at **www.microsemi.com**.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

50200633-1/09-15