Limiting Surge Current During SmartFusion2/IGLOO2 Device Reset Operation

Table of Contents

Purpose

After device power-up, if the application asserts the DEVRST_N pin and there are no decoupling capacitors on the board, additional surge current on VDD may be observed during assertion of DEVRST_N or during a digest check operation. This application note describes how to minimize additional surge current during SmartFusion2/IGLOO2 device reset operation. Note that this additional surge current does not occur during device power-up and is applicable only when DEVRST_N is asserted.

Introduction

SmartFusion2/IGLOO2 device reset can be activated either directly through an external DEVRST_N pin, or indirectly through the Tamper macro IP. When the device reset is asserted, the system controller immediately puts the field programmable gate array (FPGA) core in inactive state. During this operation, depending on the board design layout and decoupling capacitors used, there may be additional surge current on the VDD power rail. The additional surge current has no effect on device reliability.

This surge current is for a very short duration and is normally handled by bulk decoupling capacitors on the power plane in a typical system. For guidelines on proper board design using SmartFusion2/IGLOO2 devices, see *AC393: Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs Application Note*.

In cases where Microsemi-recommended board design guidelines cannot be implemented for decoupling capacitors for VDD (due to limited board spacing or other reasons), there is a possibility of higher than expected surge current during device reset. This application note provides a method to limit surge current using the Flash*Freeze feature of SmartFusion2/IGLOO2 devices.

Table 1 provides the characterized surge current data for VDD during DEVRST_N assertion. This data represents the worst case condition with no decoupling capacitors on the board.

Table 1 • Surge Current on VDD during DEVRST_N Assertion (No decoupling capacitors on board)

Device	Width of Surge at 50% of Pulse (uS)	Surge Current on VDD			Units
		0°C to 85°C	-40°C to 100°C	-55°C to 125°C	
M2S005/M2GL005	2	0.5	0.6	0.6	A
M2S010/M2GL010	3	0.9	0.9	0.9	A
M2S025/M2GL025	6	1.7	1.7	1.7	A
M2S050/M2GL050	12	3.2	3.2	3.2	A
M2S060/M2GL060	12	3.2	3.2	3.2	A
M2S090/M2GL090	22	4.4	4.6	4.6	A
M2S150/M2GL150	42	7.0	7.3	7.3	A

However, Table 1 surge current data does not represent a typical system. To illustrate this, surge current during device reset was measured at room temperature separately for the M2S090 security evaluation kit and the M2S150 advanced development kit. These kits have decoupling capacitors as per Microsemi-recommended board design guidelines. Table 2 shows the observed surge currents on the M2S090 security evaluation kit and the M2S150 advanced development kit. These surge current values are within acceptable limits.

Table 2 • M2S090 and M2S150 Surge Current During DEVRST_N Assertion (With recommended decoupling capacitors on board)

Kits	Width of Surge at 50% of Pulse	Surge Current
M2S090 Security Evaluation Kit	5 us	150 mA
M2S150 Advanced Development Kit	40 us	1.5 A

Note: "Appendix: Observed Surge Currents in Evaluation and Development Kits" on page 12 shows the screen shots of the observed surge current.

The digest check system service performs on-chip non-volatile memory (NVM) data integrity check on SmartFusion2 devices. The digest check using system services may also cause additional surge current on VDD. For more information on Digest Check Service, refer to *UG0450: SmartFusion2 SoC and IGLOO2 FPGA System Controller User Guide*.

Table 3 lists surge current data for VDD during digest check using system services. To limit the surge current during digest check, follow the Microsemi-recommended board design guidelines.

Table 3 • Surge Current on VDD during Digest Check using System Services (No decoupling capacitors on board)

Device	Width of Surge at 50% of Pulse (uS)	Surge Current on VDD			Units
		0°C to 85°C	-40°C to 100°C	-55°C to 125°C	
M2S005/M2GL005	12	0.2	0.2	0.2	A
M2S010/M2GL010	12	0.5	0.5	0.5	A
M2S025/M2GL025	13	0.6	0.6	0.6	A
M2S050/M2GL050	13	0.9	0.9	0.9	A
M2S060/M2GL060	13	0.9	0.9	0.9	A
M2S090/M2GL090	20	1.0	1.0	1.0	A
M2S150/M2GL150	26	1.0	1.0	1.0	A

References

Following are the references:

- *UG0444: SmartFusion2 and IGLOO2 Low Power Design User Guide*
- *AC393: Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs Application Note*
- *UG0331: SmartFusion2 Microcontroller Subsystem User Guide*
- *UG0450: SmartFusion2 SoC and IGLOO2 FPGA System Controller User Guide*

Design Requirements

Table 4 lists the design requirements.

Table 4 • **Design Requirements**

Design Requirements	Description
Hardware Requirements	
SmartFusion2 Security Evaluation Kit: • 12 V adapter • FlashPro4 programmer • USB A to Mini-B cable	Rev D or later
Host PC or Laptop	Any 64-bit Windows Operating System
Software Requirements	
Libero® System-on-Chip (SoC)	v11.7
SoftConsole	v3.4SP1
Host PC Drivers	*USB Drivers*

Limiting Surge Current using Flash*Freeze Feature

If the board is severely space constrained with virtually no decoupling capacitors, placing the device in Flash*Freeze mode before asserting DEVRST_N prevents surge currents from occurring.

SmartFusion2/IGLOO2 FPGAs offer the Flash*Freeze technology for implementing low-power solutions. The Flash*Freeze mode is an ultra-low power static mode. The Flash*Freeze technology enables easy entry and exit from ultra-low power static mode while retaining SRAM content, I/O state, and register data, thereby dramatically reducing power.

Initiating the Flash*Freeze ultra-low power mode feature and then issuing an active low pulse to DEVRST_N pin to reset the device prevents high surge currents. To disable the function of FPGA core logic, a standard practice followed in Microsemi flash-based FPGAs is to switch the ground supply of the FPGA to VDD rather than switching VDD to ground. Setting the power switches this way offers technological advantages in terms of programming. This method also eliminates the need to have power switches on both the power and ground connections.

As a result, the peak current can be high for a short duration during the device reset. Using the Flash*Freeze feature, the FPGA core logic is disabled in a controlled manner, thereby avoiding any surge current increase.

SmartFusion2 Devices

To limit surge current during device reset in SmartFusion2 devices, the active low pulse to DEVRST_N pin can be generated using the Cortex®-M3 processor after initiating the Flash*Freeze feature, as shown in Figure 1.

In the sample design provided in this application note, a microcontroller subsystem (MSS) general purpose I/O (GPIO) is routed to DEVRST_N pin. The Cortex-M3 processor drives the GPIO to activate and assert a device reset, as shown in Figure 1.

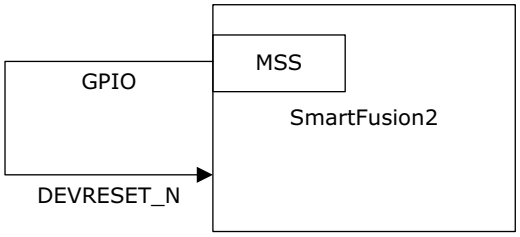

***Figure 1* • Top-Level Block Diagram to Reset a SmartFusion2 Device**

IGLOO2 Devices

To limit surge current during device reset in IGLOO2 devices, the active low pulse to DEVRST_N can be generated using an external microcontroller after initiating the Flash*Freeze feature, as shown in Figure 2.

To reset IGLOO2 devices:

1. Initiate the Flash*Freeze feature by sending the Flash*Freeze command to the CoreSystemServices IP using an external microcontroller.
2. Monitor the Flash*Freeze start signal for 1, using the external microcontroller (expose the IGLOO2 FLASH_FREEZE macro signal, Flash*Freeze start, to an I/O, and configure that I/O to store the last value during Flash*Freeze using the I/O editor).
3. Drive active low pulse to DEVRST_N from the external microcontroller.

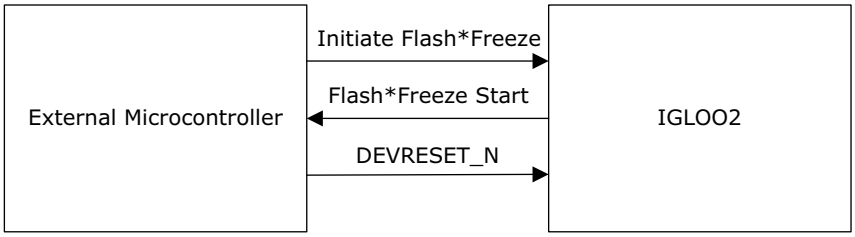

***Figure 2* • Top-Level Block Diagram to Reset SmartFusion2/IGLOO2 Devices**

Note:

1. Another option for IGLOO2 is to migrate to the corresponding SmartFusion2 device. SmartFusion2 and IGLOO2 devices are pin compatible with each other. No board changes are required to swap between the devices.
2. This implementation can also be followed for SmartFusion2 devices.

Design Implementation

SmartFusion2 Hardware Implementation

The hardware implementation involves configuring the MSS, fabric, clocks, and oscillator using System Builder.

1. In the **System Builder - Peripherals** window, select **MM_UART_1** and **MSS_GPIO** check boxes.

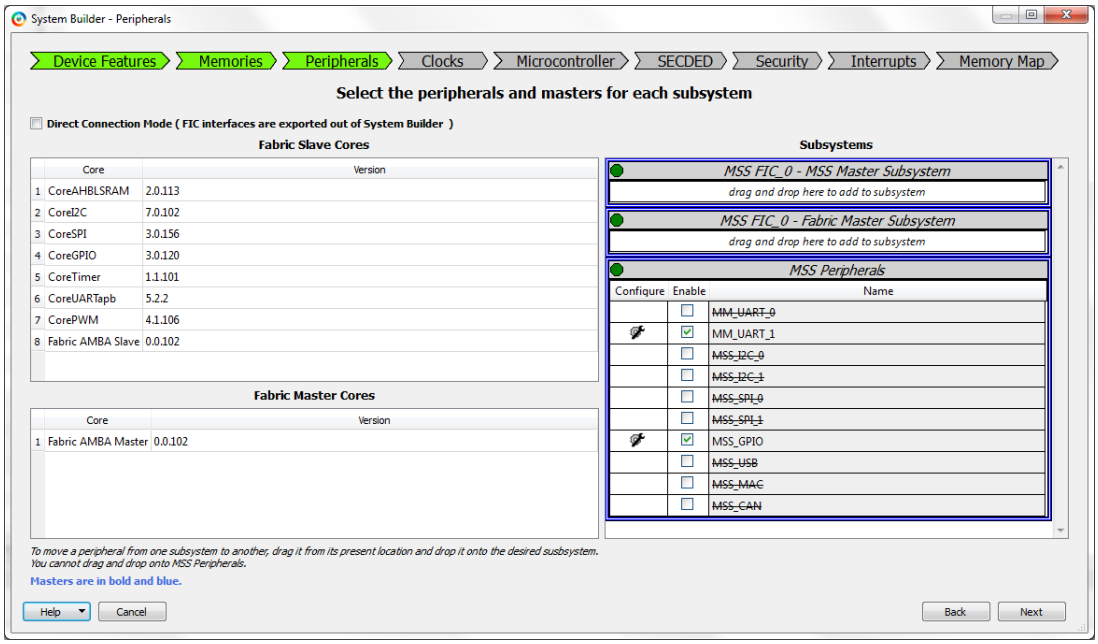

***Figure 3* • Peripherals Selection Using System Builder**

2. Select **GPIO_0** as an **Output** under **GPIO Assignment**. The GPIO must be configured as input or output package pin I/Os and not routed to fabric. Ensure that the reset state of these I/Os are high.

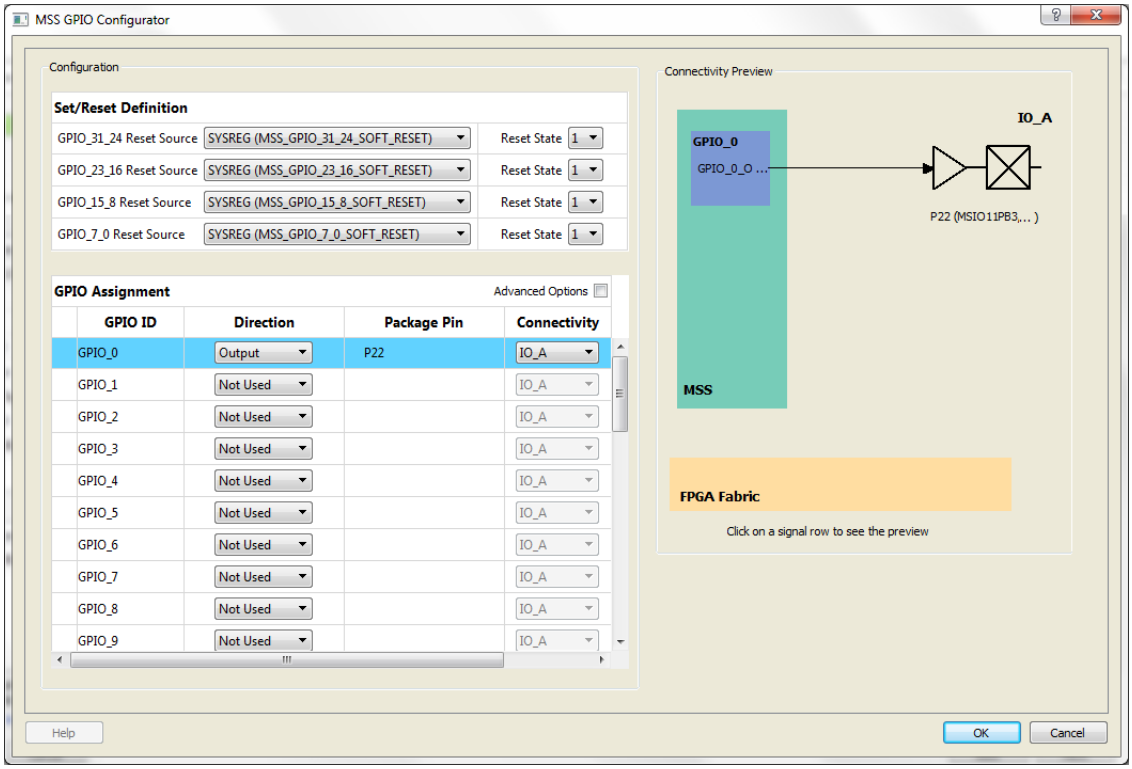

Figure 4 • **MSS GPIO Configuration**

3. Select the **On-chip 25/50 MHz RC Oscillator** from the list under **System Clock** in the **System Builder - Clocks** window.

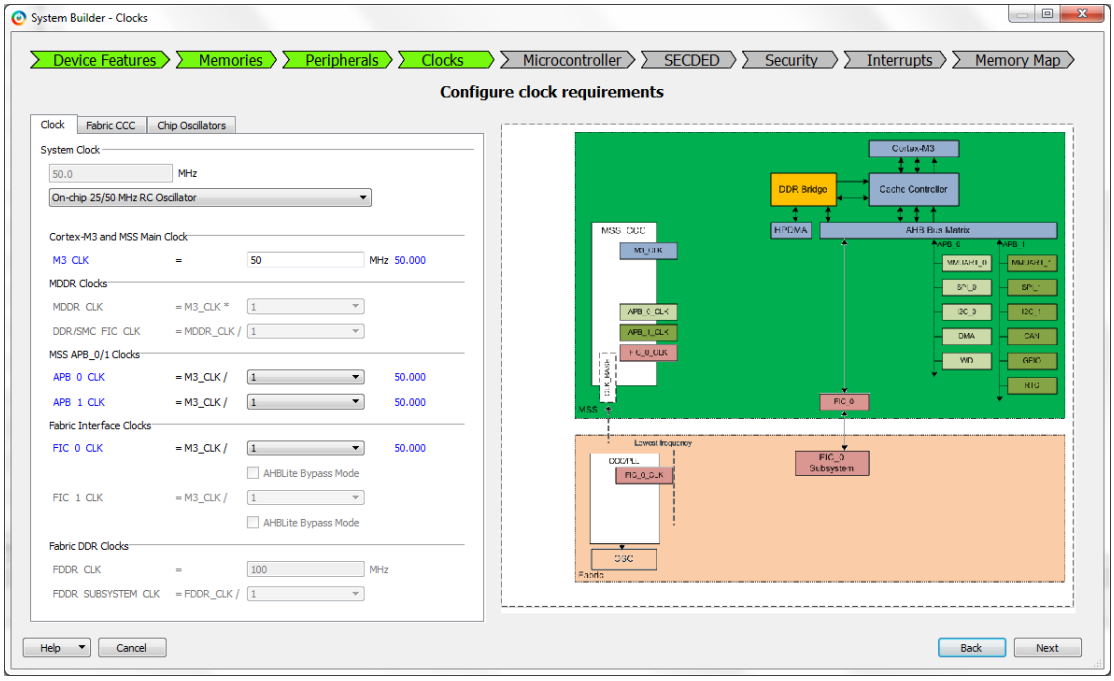

***Figure 5* • Clock Configuration**

For more information about how to generate a complete system builder component for SmartFusion2 devices, see the *SmartFusion2 System Builder User Guide*. Figure 6 shows the top-level SmartDesign of the application.

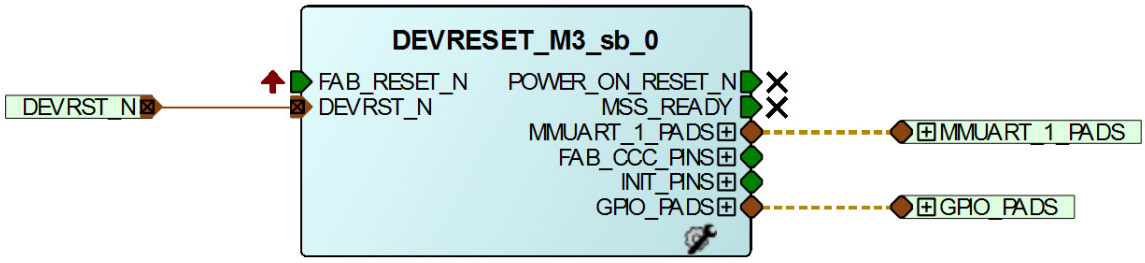

***Figure 6* • Top-Level SmartDesign**

4. Under **Compile > Configure Flash*Freeze** option of Libero, set the **MSS Clock Source** in the **Flash*Freeze Hardware Settings** to **On-Chip 50 MHz RC Oscillator**. This is the MSS clock base when the part goes into Flash*Freeze mode.

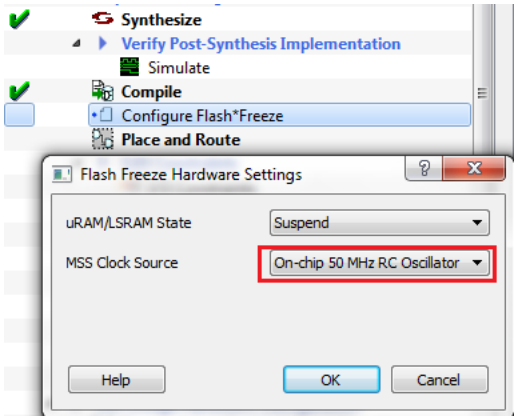

***Figure 7* • Flash*Freeze Hardware Settings**

5. In the **I/O Editor**, make the GPIO_0 signals and MMUART_1 signals available in Flash*Freeze mode, as shown in Figure 8. Also, set the **Resistor Pull** to **Up** for GPIO_0_OUT.

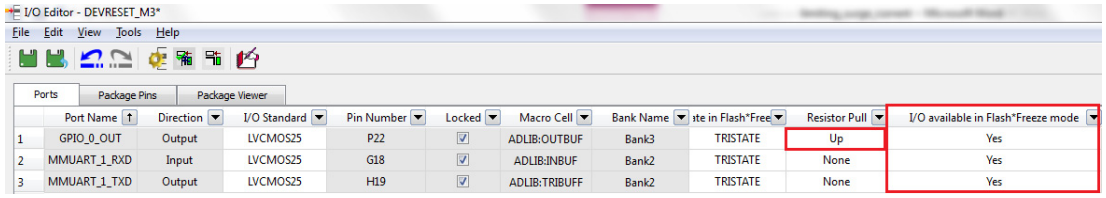

***Figure 8* • I/O Editor**

6. Ensure that the latest firmware cores are exported from Libero. In the sample design, the following versions of the firmware are used:

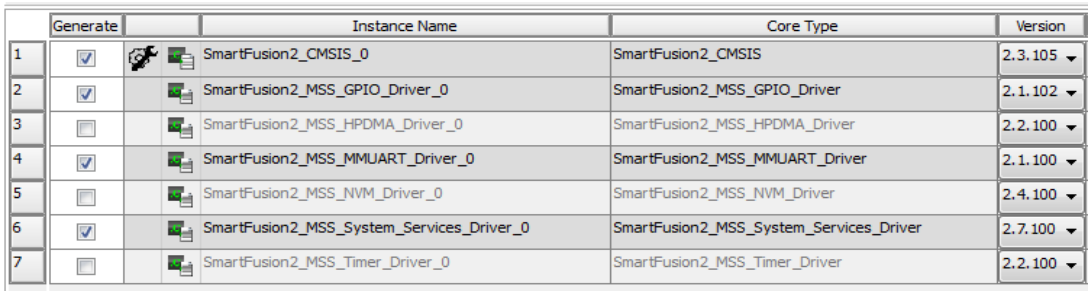

***Figure 9* • Firmware Versions**

SmartFusion2 Software Implementation

The software sequentially performs the following operations:

1. Initializes UART and GPIO
2. Waits for the command from UART
3. Requests the system controller to put the device in Flash*Freeze mode. The fabric is set in Flash*Freeze power down mode using the command:

   ```
   MSS_SYS_flash_freeze(MSS_SYS_FPGA_POWER_DOWN);
   ```

4. Drives GPIO_0 to 0 to reset the device

Validation Results

The device reset is controlled through MSS_UART in the sample design. The command sent through MSS_UART is detected by the Cortex-M3 processor, which then drives the GPIO to 0. Driving the GPIO to 0 causes the device to be reset because on board this GPIO is connected to DEVRESET_N pin of SmartFusion2 SoC FPGA.

Figure 10 shows the results of the device reset in the sample design and no surge current is observed during the SmartFusion2 device reset.

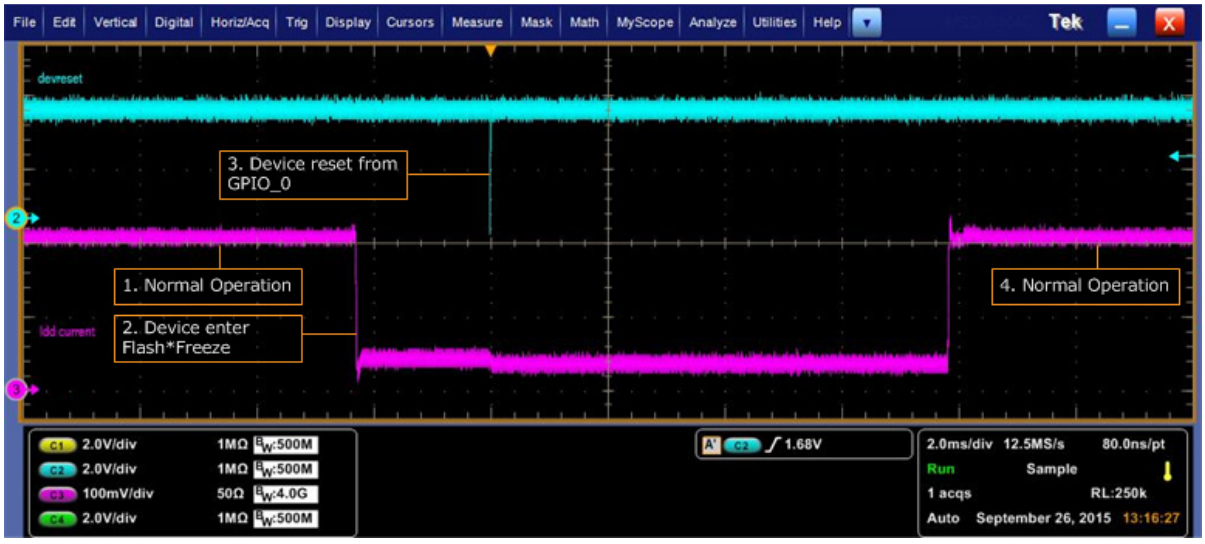

***Figure 10* • IDD Current During SmartFusion2 Device Reset – When Device in Flash*Freeze**

Board-Level Changes Required

To run the sample design on the SmartFusion2 090 evaluation kit, the following board changes are required:

1. Remove the R15 resistor to disconnect the voltage sensing circuit from DEVRESET_N.
2. Connect RVI header J4-15 pin (DEVRESET_N pin) to the I^2C header H1-3 pin (MSS GPIO_0 pin). The MSS GPIO_0 pin is connected to DEVRESET_N, as shown in Figure 11.

   The above procedure can be followed if the users require to implement it on their boards.

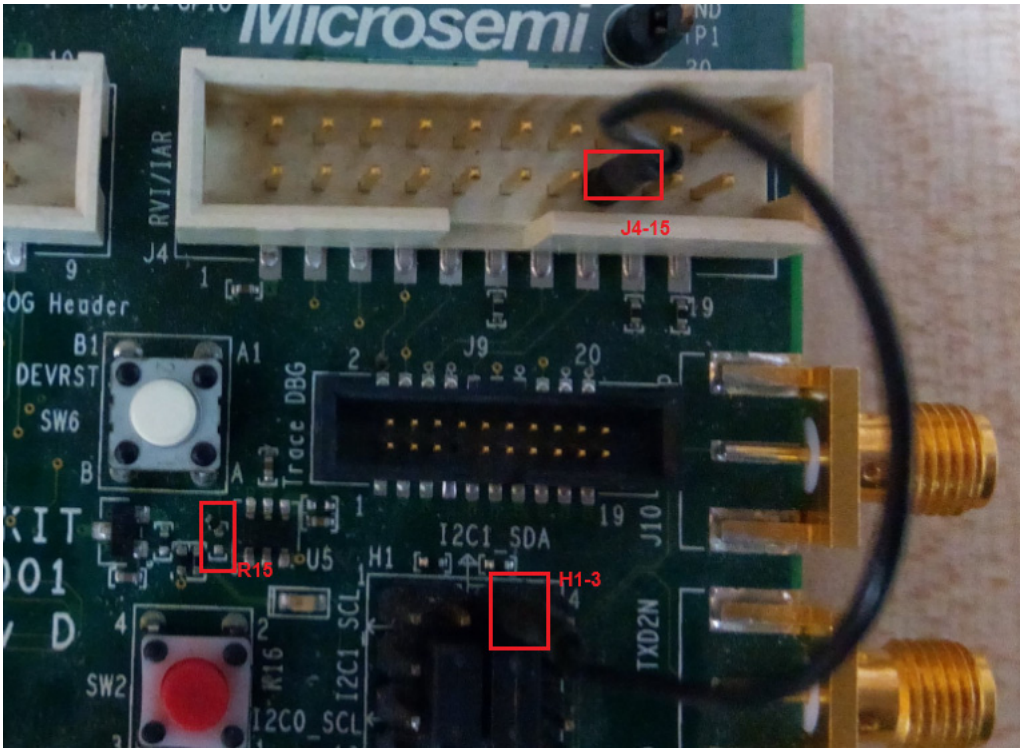

***Figure 11* • Board Level Changes**

Conclusion

This application note describes methods to limit surge current during SmartFusion2/IGLOO2 device reset. Implementation and validation results are provided for issuing a device reset after setting the fabric in Flash*Freeze mode.

Appendix: Design Files

Download the following design files from Microsemi website:

http://soc.microsemi.com/download/rsc/?f=m2s_m2gl_ac452_liberov11p7_df

The design file consists of Libero SoC Verilog project, SoftConsole software project, and programming files (*.stp) for the SmartFusion2 security evaluation kit board. Refer to the `Readme.txt` file included in the design file for the directory structure and description.

Appendix: Observed Surge Currents in Evaluation and Development Kits

Figure 12 shows IDD surge current, VDD, and VPP variations on SmartFusion2 security evaluation kit during device reset operation.

***Figure 12* • IDD Surge Current Observed on M2S090 Security Evaluation Kit**

Figure 13 shows IDD surge current, VDD, and VPP variations on SmartFusion2 advanced development kit during device reset operation.

***Figure 13* • IDD Surge Current Observed on M2S150 Advanced Development Kit**

List of Changes

The following table shows important changes made in this document for each revision.

Revision	Changes	Pages
Revision 1 (March 2016)	Initial release.	NA

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