Layout Guidelines for RTG4-Based Board Design

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Introduction

This document provides guidelines for the hardware board layout, that incorporates RTG4 devices. Good Board layout practices are required to achieve the expected performance from the printed circuit boards (PCB) and RTG4 devices. They help achieve high quality and reliable results such as low noise levels, signal integrity, impedance, and power requirements. The guidelines mentioned in this document act as a supplement to the standard board-level layout practices.

Note: A good understanding of the RTG4 chip, experienced in digital and analog board layout, knowledge of transmission line theory and signal integrity are essential to be able to follow the guidelines in this document. See the *AC439: Board Design Guidelines for RTG4 FPGA Application Note* to design RTG4-based boards.

Disclaimer: The target impedance calculated with respect to the development board. The target impedance depends on the logic implemented on RTG4, so Microsemi recommends calculating the target impedance of the board. The simulations show the impedance that meets the target impedance of the development board.

Power Supply

In power supply design, it is important to know the target impedance of power planes, which varies depending on the design. This helps in planning the required number of decoupling capacitors based on the target impedance. The number of decoupling capacitors varies based on the design.

Complex FPGA designs have increasing amounts of current transients switching across the power bus. Simultaneously switching outputs (SSO) contribute to a major share of instantaneous current issues. Decoupling is necessary to prevent the instantaneous currents. Decoupling is only effective when inductance is minimized. Low inductance decoupling provides localized high frequency energy to decouple noise from the switching currents of the device power bus. This is most effective when capacitors are in close proximity to the device. Some of these high frequency capacitors are required to be placed directly by the FPGA.

Target impedance is calculated based on *EQ 1*:

$$Z_{Min} = \%\ Ripple \times \frac{V_{supply}}{I_{trans}}$$

EQ 1

Where,

V_{supply}: Supply voltage of the power plane

% Ripple: Percentage of ripples allowed on the power plane; see the *DS0131: RTG4 FPGA Datasheet* for details.

I_{trans}: Transient current drawn on the power plane. Generally, transient current is half of the maximum current, which is taken from the power calculator sheet.

Z_{min}: Target impedance of the plane

Subsequent sections display simulation results based on target impedance calculated using *EQ 1*. Microsemi strongly recommends calculating the target impedance and performing simulations for the impedance profile of the power plane. These simulations help in optimizing the decoupling capacitors to reduce the production cost and have optimal placement. The plane shapes given in this document are with reference to the *UG0617: RTG4 FPGA Development Kit User Guide*. The plane shapes vary depending on the design. For simulation topology, see "Appendix E: Power Integrity Simulation Topology" section on page 39.

RTG4 power supplies are majorly classified as:

- Core power supply
- I/O power supply
- Serializer/Deserializer (SerDes) power supply
- Double data rate (DDR) power supply
- Phase-locked Loop (PLL) power supply

Core Supply (VDD)

The core power supply must have low-noise and low-ripple voltages, as prescribed in the datasheet. Proper care should be taken while designing the power supply (VDD) for core. Optimal placement of decoupling capacitors and the plane geometry greatly influences the power supply distribution for RTG4 devices.

Component Placement

Component placement for capacitors for VDD Plane are as follows:

- The bulk capacitors should be placed near the RTG4 device.
- The bypass capacitors should be placed near, or if possible, on the periphery of the device. A sample placement of capacitors is shown in Figure 1.

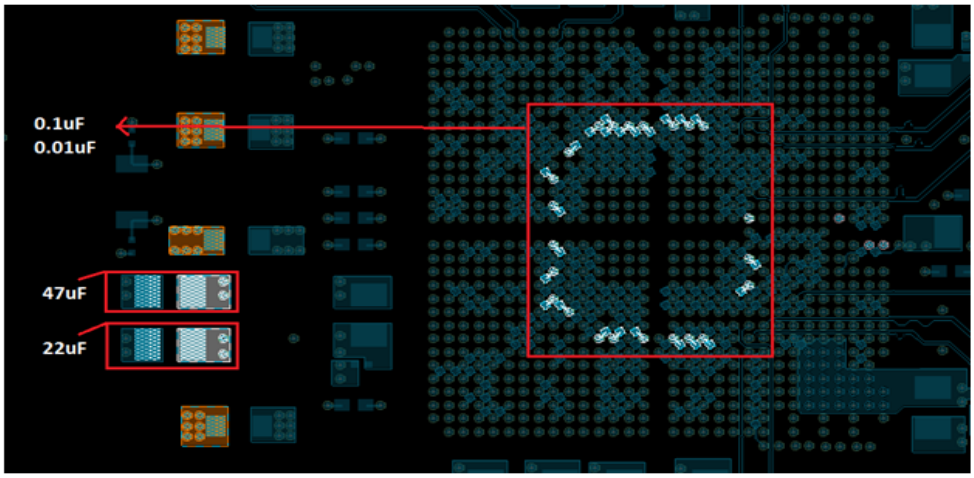


***Figure 1* • Placement of Capacitors for VDD Plane**

- All decoupling capacitors should be as small as possible as they are required to be mounted on back side of the board. There can be sharing of via for ground pins if the capacitors are 0603 in size and if it is difficult to accommodate the capacitors on back side of the board. Microsemi recommends keeping the capacitor pad close to corresponding via. The footprint of capacitors should be optimized based on size of capacitor to accommodate all the capacitors. Users need to consult assembly house for the change in footprint.

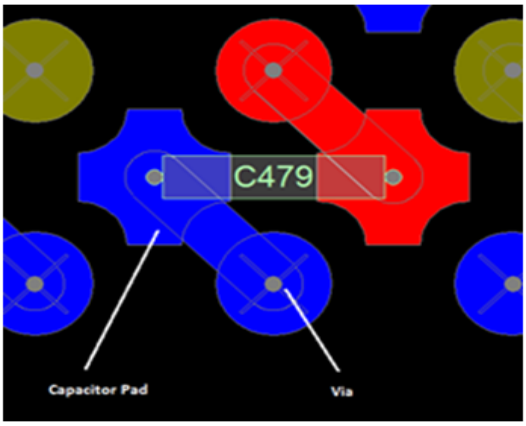


***Figure 2* • Capacitor Placement under BGA Vias**

Plane Layout

Microsemi recommends using the VDD plane, as shown in Figure 3.

Note: There are many ways the plane can be routed. The goal is to have a dedicated, low-impedance plane.

***Figure 3* • VDD Plane**

Simulations

The effect of the decoupling capacitors can be visualized through power integrity simulations. The target impedance of the VDD is calculated as 40 mΩ, based on the following values (see *EQ 1)*:

- V_{SUPPLY} = 1.2 V
- I_{trans} = 1.5 A
- Ripple = 5%

Figure 4 shows the Sample impedance profile of the VDD plane. It shows that the capacitors used are adequate to improve the impedance profile over the bandwidth. Good coupling between the planes can be achieved by placing the power plane and ground plane in adjacent layers. Once all the capacitors (0.1 uF and 0.01 uF) are placed, the impedance of the VDD plane impedance profile improves over the frequency range. The simulation results shown in this document, are done in Sigrity® PowerSI tool. For more information about using this tool and how to do the simulation, see the Sigrity PowerSI tutorial.

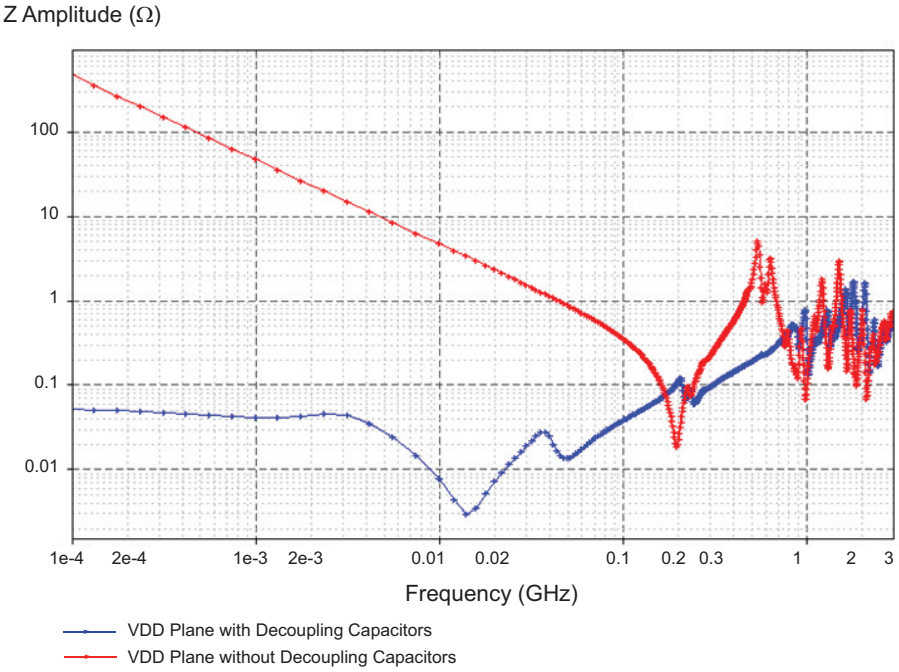


***Figure 4* • Impedance Profile of VDD Plane with Respect to Frequency**

SerDes

PCB designers often overlook the need to isolate noise generated by the digital components with the SerDes high-speed designs. It is necessary to provide a low-noise supply to the sensitive analog portions of the SerDes devices. Noise due to variations in the power supply voltage can be coupled into the analog portion of the chip, causing unwanted fluctuations in the sensitive stages of the device. The performance of the SerDes highly depends on the layout techniques. This section discusses the layout guidelines for power supply for the SerDes. SerDes PLL layout guidelines for the SerDes differential traces are discussed in a separate section.

Component Placement

SerDes I/O Power (SERDES_x_VDDAIO)

- The decoupling capacitors (0.1 µF and 0.01 µF) are placed on the pad adjacent to the BGA via of the corresponding pin, as shown in Figure 1 on page 3. At least one of the capacitors (0.1 µF or 0.01 µF) should be placed for each SerDes bank. The capacitor pad to via trace should be as small as possible.
- The bypass capacitor (10 µF) should be placed at the edge of the IC.

SerDes PLL

Two power supply nodes required for the SerDes—SERDES_x_VDDAPLL and SERDES_x_PLL_VDDA. Both the supplies require separate filter circuits. Figure 5 shows the filter circuit for SERDES_x_VDDAPLL. (A typical filter circuit for SERDES_x_PLL_VDDA is shown in Figure 16 on page 14.)

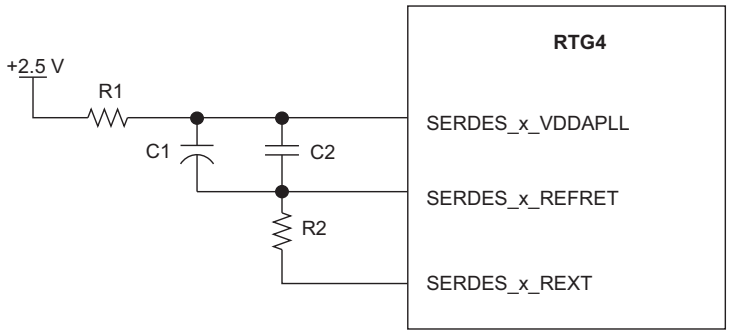


***Figure 5* • Filter Circuit for SerDes PLL Power Supply**

- The R1 and the series resistor should be placed near the device as close to the R2 capacitor as possible. A sample placement is shown in Figure 8 on page 8.
- The R2 capacitor must be placed near the BGA via. The capacitor pad to via-trace should be as small as possible.
- A precision resistor (C2) should be placed between the SERDES_x_REXT and SERDES_x_REFRET pins, near the BGA via of SERDES_x_REXT pin. Any other aggressive signal traces should be kept away from this connection to avoid unwanted noise from coupling into the critical circuit.
- For exact value of filter components, see the *AC439: Board Design Guidelines for RTG4 FPGA Application Note*.

Plane Layout

SerDes Core Power (SERDES_x_VDD)

Even though the Bank0 (SERDES0) and Bank1 (SERDES1) cores share the same power supply, separate planes must be made while connecting to corresponding banks. This reduces the noise coupling between the SERDES0 (SERDES block 0) and SERDES1 (SERDES block 1) blocks.

Figure 6 shows the layout for SERDES_X_VDD plane.

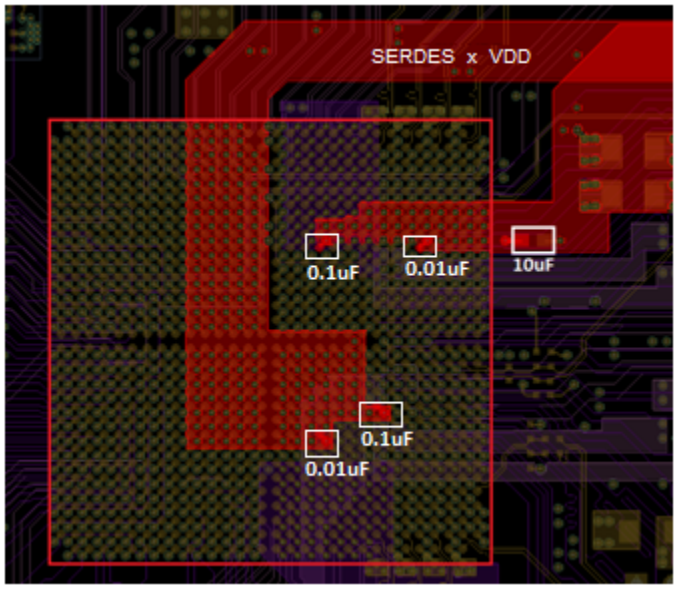


***Figure 6* • Layout for SERDES_x_VDD Plane**

SerDes I/O Power (SERDES_x_VDDAIO)

Even though SERDES0 and SERDES1 I/Os share the same power supply, separate planes should be made while connecting to the corresponding pins, as shown in Figure 7 on page 8. Each plane is named differently (SERDES_0_L01_VDDAIO, SERDES_0_L23_VDDAIO, SERDES_1_L01_VDDAIO, and SERDES_1_L01_VDDAIO) to reduce noise coupling between the differential lanes.

SerDes PLL

- Plane routing for SERDES_1_L01_VDDAPLL and SERDES_1_L01_REFRET is shown in Figure 8 on page 8.
- SERDES_1_L01_VDDAPLL and SERDES_1_L01_REFRET should not be routed as traces. A small trace width causes poor noise performance due to the high inductive behavior of the trace. Even though the current requirement is low, supply traces should be routed as small planes, as shown in Figure 8 on page 8.
- ***The Connections of 1.21 KΩ resistor and SERDES_1_L01_REXT of RTG4 should not be routed as a thick plane.*** It should be routed as a signal trace in order to meet the minimum capacitance requirement of the SERDES_1_L01_REXT pin. The length of the trace should be as short as possible. Figure 9 on page 9 shows the sample layout.

- The same layout guidelines should be followed for the remaining SerDes PLL power supplies.

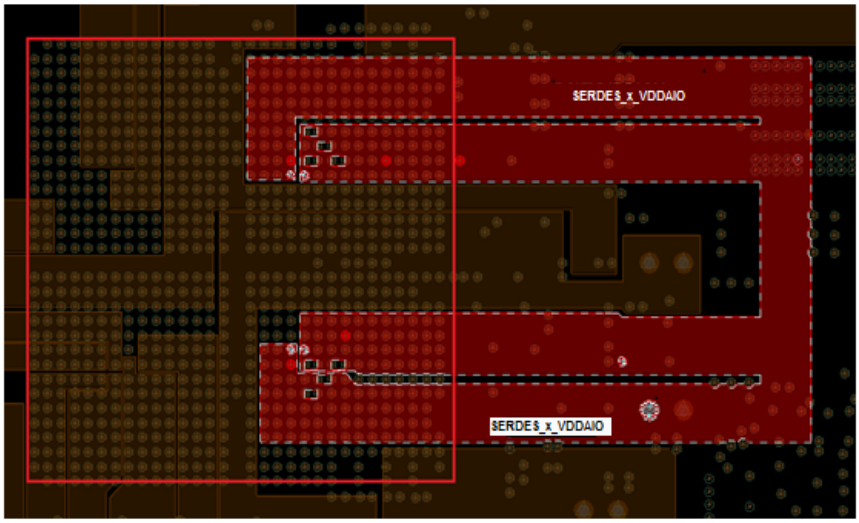


***Figure 7* • Layout of SERDES_x_VDDAIO Plane**

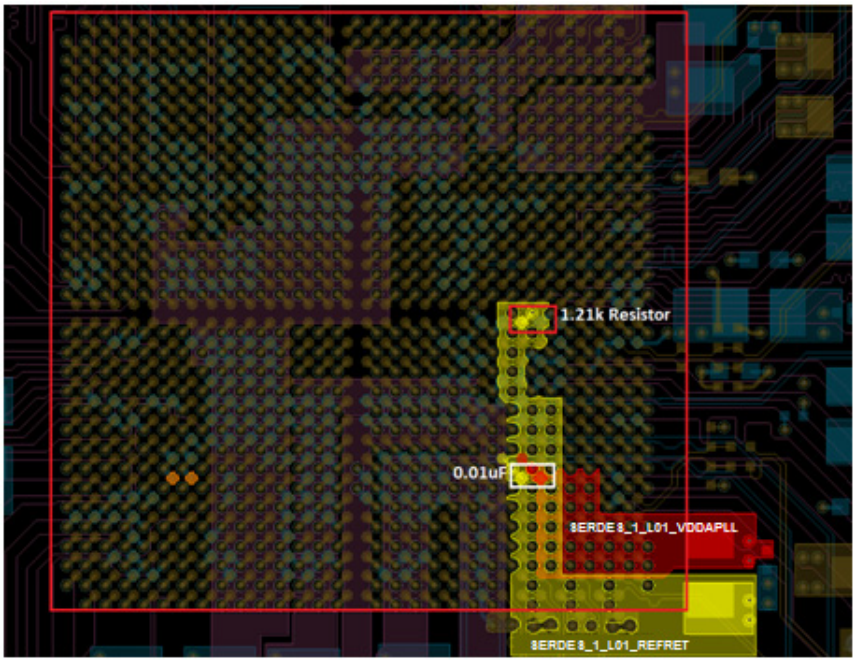


***Figure 8* • Layout of SERDES_1_L01_VDDAPLL and SERDES_1_L01_REFRET**

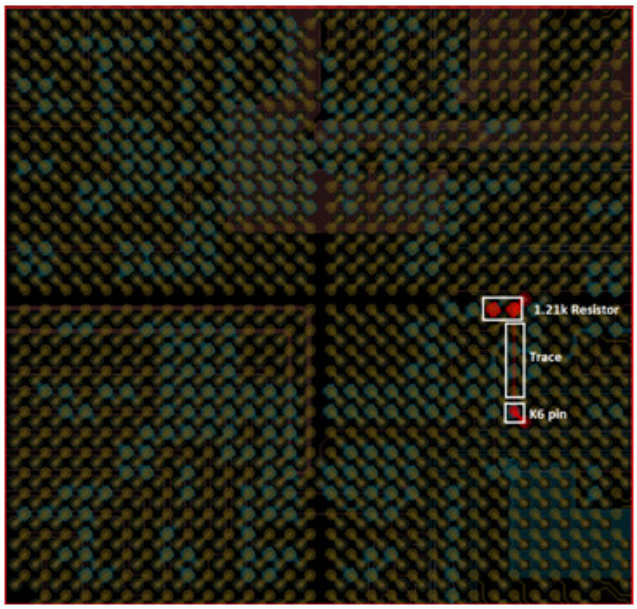


***Figure 9* • Trace Between 1.21 K Resistor and K6 Pin**

Simulations

SerDes I/O Power (SERDES_x_VDDAIO)

The target impedance of the SERDES_x_VDDAIO is calculated as 240 mΩ based on the following values (see EQ 1):

- V_{SUPPLY} = 1.2V
- I_{trans}= 250mA
- Ripple = 5%

Figure 10 shows the impedance of the plane (SERDES_x_VDDAIO) improved by the decoupling capacitors. The impedance of the plane is kept under 0.2 Ω till 100 MHz.

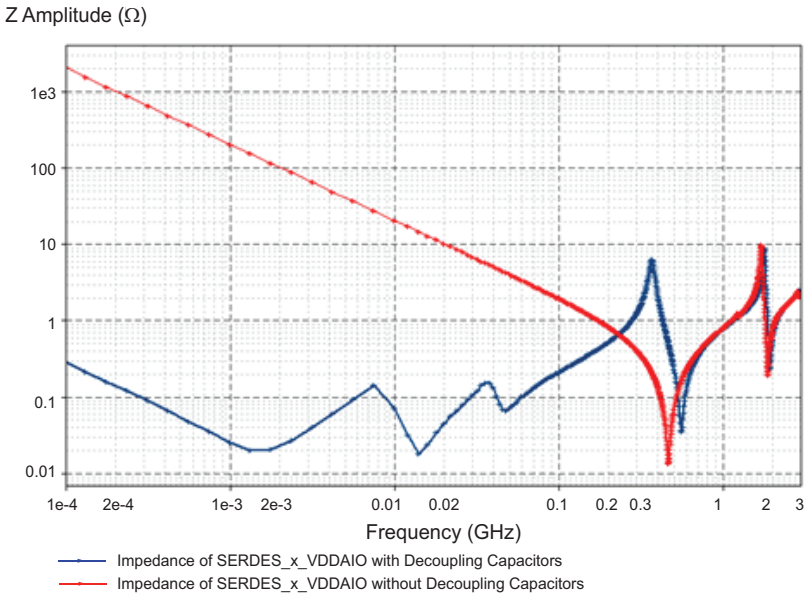


***Figure 10* • Impedance Profile of SERDES_x_VDDAIO Plane Over Frequency Range**

DDR

The layout guidelines of the respective VDDIO should be followed. It requires VREF voltage for an internal reference. Noise on VREF impacts the read performance of RTG4 devices. VREF lines should be away from aggressive nets or switching power supplies. For DDR memory layout guidelines, see the *Micron DDR3 Memory Layout Guidelines*. The VDDIO guidelines should be followed for DDR bank VDDIO. This section explains the guidelines to be used for VREF.

Component Placement

VREF

- The bypass capacitor (10 uF) should be placed near the device, or if possible, at the edge of the device.
- All decoupling capacitors (0.1 uF and 0.01 uF) should be 0402 or of a smaller package size as they are required to be mounted on the reverse side of the board. They should be fit between the adjacent vias of the BGA package pins. These decoupling capacitors are selected to have low impedance over the operating frequency and temperature range.
- The capacitor pad to via trace should be as small as possible. Figure 1 on page 3 shows how capacitors are mounted. Microsemi recommends placing the capacitor pad directly on the corresponding vias.

VDDIO

- The bypass capacitors (47 µF and 22 µF) should be placed near, or if possible, at the edge of the device.
- All decoupling capacitors (0.1 µF and 0.01 µF) should be 0402 or of a smaller package size as they are required to be mounted on the reverse side of the board. They should be fit between the adjacent vias of the BGA package pins. These decoupling capacitors are selected to have low impedance over the operating frequency and temperature range.
- The capacitor pad to via trace should be as small as possible. Figure 1 on page 3 shows how these capacitors are mounted. The capacitors can also be mounted directly on the pad available on the vias.

Plane Layout

VREF

Noise on VREF impacts the read performance of RTG4 devices. The VREF lines should be routed with no aggressive net or switching power supply nearby. Even though the current is low, VREF should not be routed as trace as it is very susceptible to noise. Figure 11 shows the VREF5 used for MDDR.

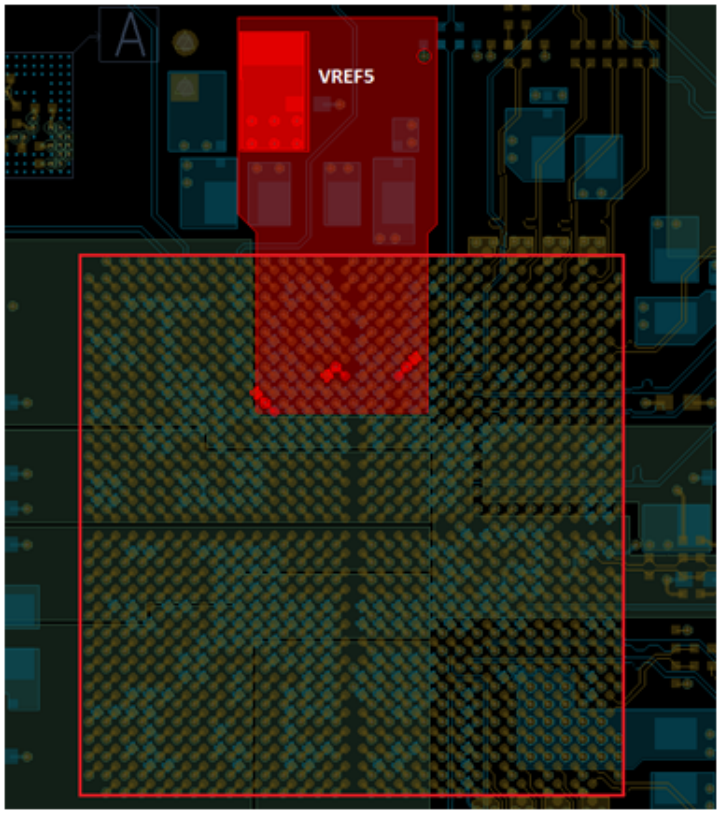


Figure 11 • **Layout of VREF5**

VDDIO

There is no specific requirement for the shape of the plane. The width of the plane should be sufficient enough to carry the required current. Figure 12 and Figure 13 show the sample layout for the VDDIO0 plane and the VDDIO5 plane respectively.

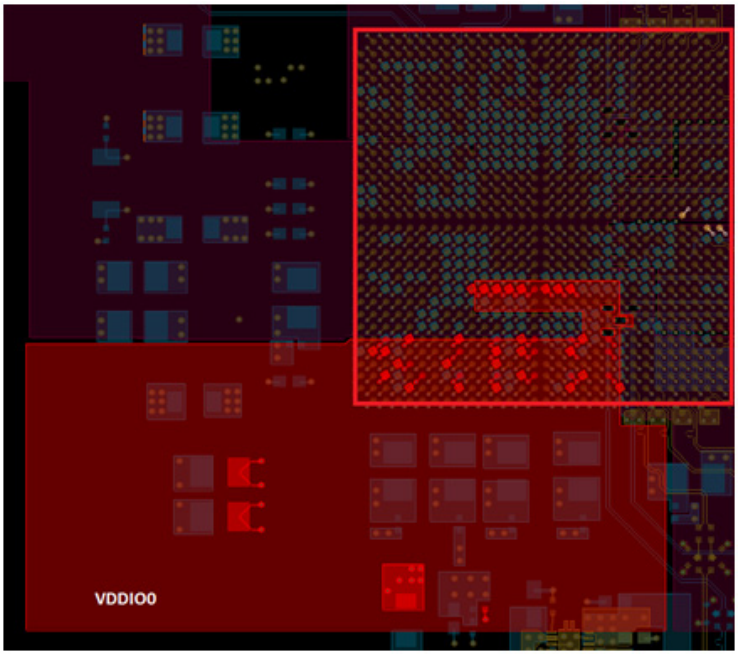


***Figure 12* • Layout of VDDIO0 Plane**

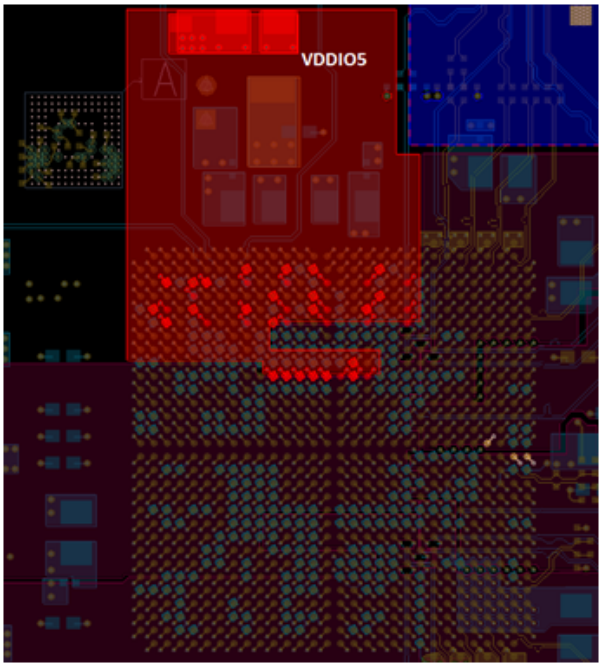


***Figure 13* • Layout of VDDIO5 Plane**

Simulations

The target impedance of the DDR VDDIO is calculated as 240 mΩ, based on the following values (see *EQ 1)*:

- V_{SUPPLY} = 1.5V,
- I_{trans} = 250 mA
- Ripple = 5%

The impedance profile of the DDR VDDIO plane over frequency range is shown in Figure 14 and Figure 15 on page 14. The impedance improves with the decoupling capacitors provided. The target impedance of 0.3 Ω was achieved till 100 MHz.

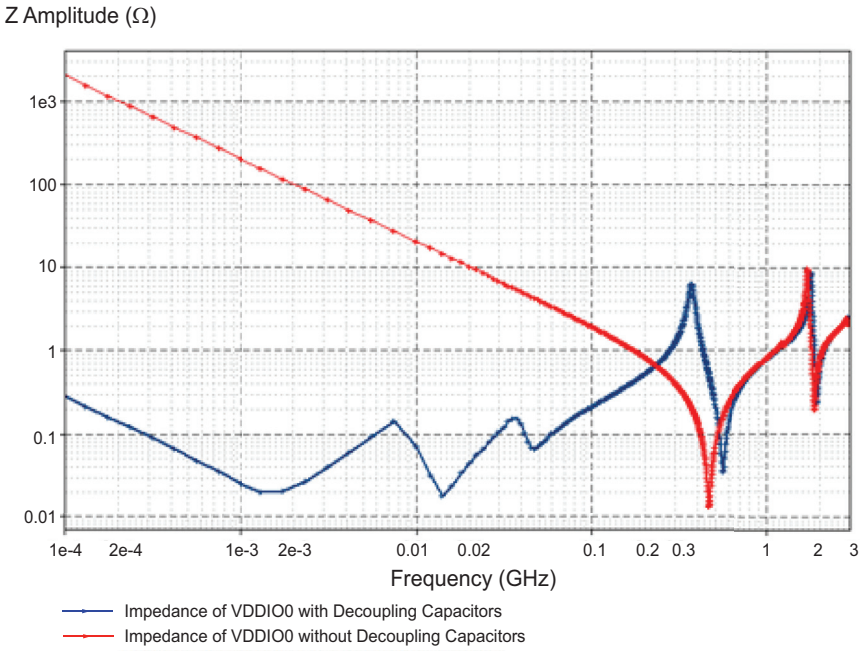


***Figure 14* • Impedance Profile of VDDIO0 Plane over Frequency Range**

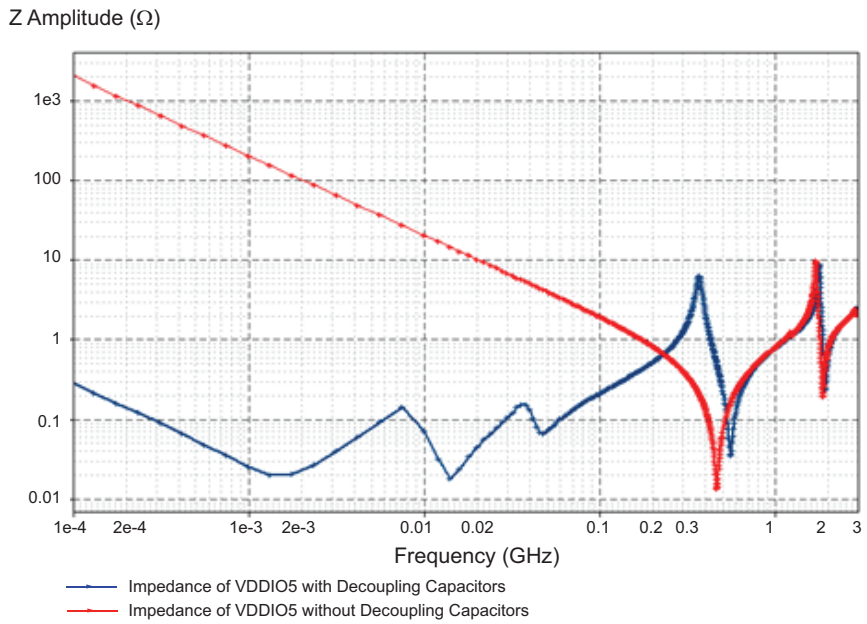


***Figure 15* • Impedance Profile of VDDIO5 Plane over Frequency Range**

PLL

To achieve a reasonable level of long term jitter, it is vital to deliver an analog-grade power supply to the PLL. Typically, an R-C or R-L-C filter is used with the C being composed of multiple devices to achieve a wide spectrum of noise absorption. Though the circuit is simple, there are specific board layout requirements. Board layout around the high-frequency capacitor and the path to the pads is critical. It is vital that quiet ground and power are treated similar to analog signals. The entire VDDPLL and PLLVSSA wiring path should not be coupled with any signal aggressors – especially, any high-swing and high-slew rate signals such as TTL, CMOS, or SSTL signals used in DDR buses, and so on.

Figure 16 shows the recommended circuit for the power supply filter.

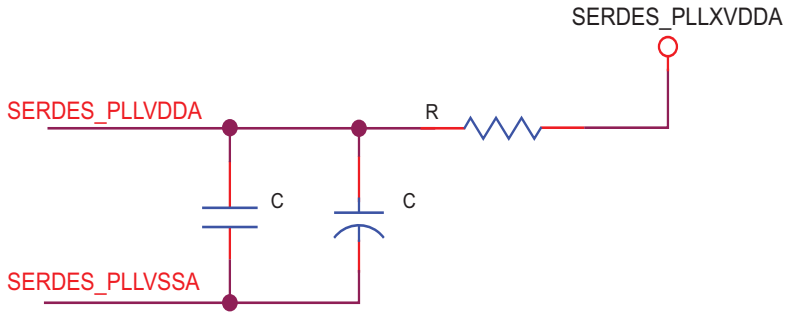


***Figure 16* • Filter Circuit for PLL**

Note: To know the accurate values of resistor and capacitors for filter circuit of PLL, see the *DS0131: RTG4 FPGA Datasheet*.

Component Placement

- The capacitor and series resistor should be placed near the device as close to the capacitor as possible. A sample placement is shown in Figure 17.
- The decoupling capacitor should be placed near the BGA via. The capacitor pad to via trace should be as small as possible.

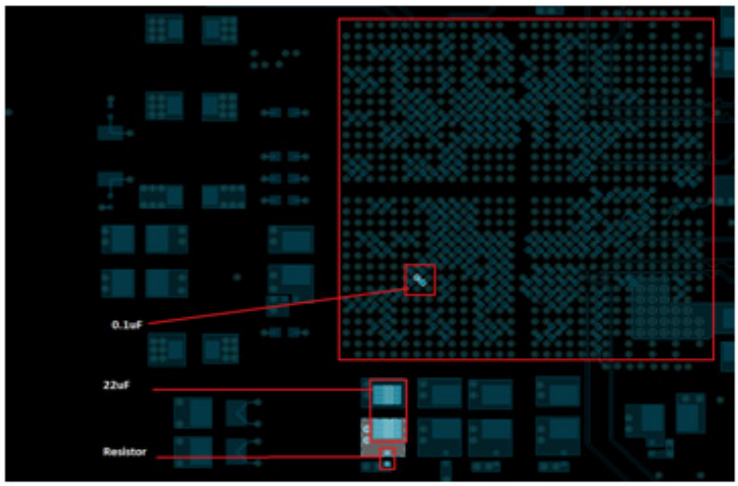


***Figure 17* • Placement of Capacitors for PLL Filter Circuit**

Plane Layout

- Figure 18 shows the plane routing for PLL0VDDA and PLL0VSSA with respect to the schematic shown in Figure 16 on page 14.
- The capacitor (22 uF) and series resistor should be placed near the device as close as possible to the 0.1 uF cap. A sample placement is shown in Figure 18.

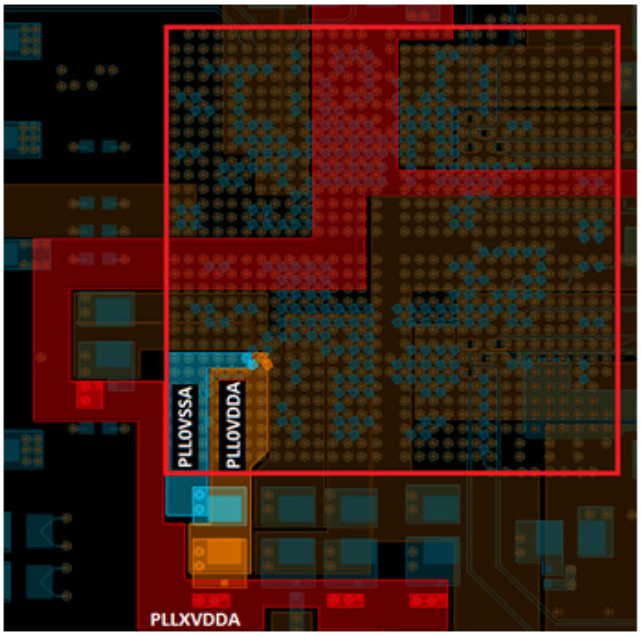


***Figure 18* • Routing for PLL Filter Circuit**

- PLL0VDDA and PLL0VSSA should not be routed with a small trace width as this increases the inductance, resulting in ripples. These supply traces should be routed as plane (as shown in Figure 18 on page 15), even though the current requirements are low.
- The layout guidelines for PLL0VDDA and PLL0VSSA/supply traces should also be followed for DDR PLLs power supplies. Guidelines for PCIe PLL are provided in the "SerDes" section on page 6.

Simulations

The target impedance of the PLL0VDDA plane is calculated as 16.5 Ω based on the following values (see *EQ 1*):

- V_{SUPPLY} = 3.3 V
- 3.3 V, I_{trans} = 10 mA
- Ripple = 5%

The impedance of the plane (Z) should be 16.5 Ω or less. Plane impedance with and without filter circuit is shown in Figure 19.

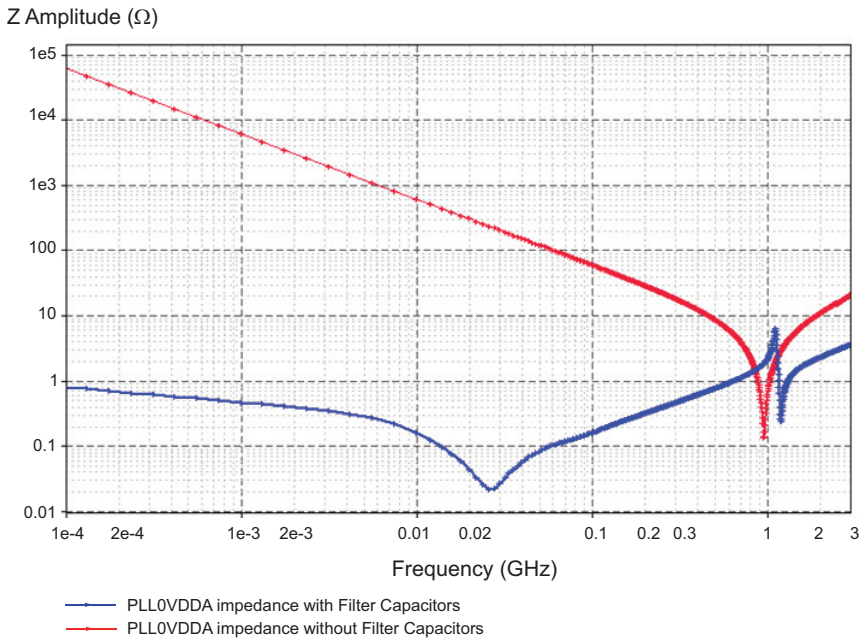


***Figure 19* • PLL0VDDA Plane Impedance**

I/O Power Supply

Component Placement

- The bypass capacitors (47 µF and 22 µF) should be placed near, or if possible, at the edge of the device.
- All decoupling capacitors (0.1 µF and 0.01 µF) should be 0402 or of a smaller package size as they are required to be mounted under BGA package. They should be fit between the adjacent vias of BGA package pins. These decoupling capacitors are carefully selected to have low impedance over operating frequency and temperature range.

The capacitor pad to via trace should be as small as possible. Figure 1 on page 3 shows how these capacitors are mounted. The capacitors can also be mounted directly on the pad available on the vias. The decoupling capacitors should not be shared via connections.

Plane Layout

There is no specific requirement for the shape of the plane. The width of the plane should be sufficient enough to carry the required current.

Simulations

The target impedance of the VDDIO1 plane is calculated as 330 mΩ based on the following values (see *EQ 1*):

- V_{SUPPLY} = 3.3 V,
- I_{trans}= 500 mA
- Ripple = 5%

Figure 20 and Figure 21 on page 18 show the impedance of the planes (VDDIO1 and VDDIO2). The impedance of the plane has been improved by decoupling capacitors and is kept under 0.2 Ω till 100 MHz.

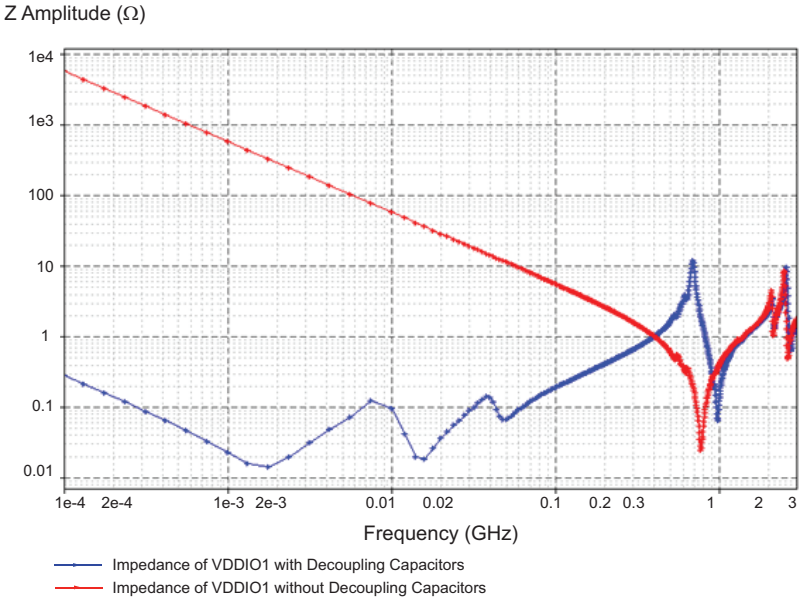


Figure 20 • **Impedance Profile of VDDIO1 Plane over Frequency Range**

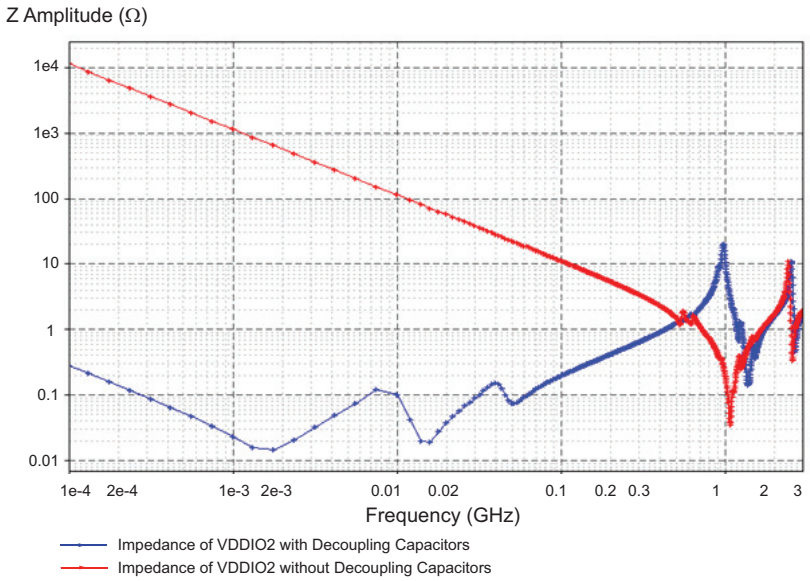


Figure 21 • **Impedance Profile of VDDIO2 Plane over Frequency Range**

Programming Power Supply (VPP)

VPP is used as an input for the internal charge pump that generates the required voltage to program flash.

Component Placement

- The bypass capacitors (47 µF and 22 µF) should be placed near, or if possible, at the edge of the device.
- All decoupling capacitors (0.1 uF and 0.01 uF) should be 0402, or of a smaller package size, as they are required to be mounted on the back side of the board. They should be fit between the adjacent vias of BGA package pins. These decoupling capacitors are carefully selected to have low impedance over the operating frequency and temperature range.
- The capacitor pad to via trace should be as small as possible. Figure 1 on page 3 shows how these capacitors are mounted. The capacitor can also be mounted directly on the pad available on the vias.

Plane Layout

There is no specific requirement for the shape of the plane. The width of the plane should be sufficient enough to carry the required current.

Simulations

The target impedance of the VPP is calculated as 3.3 Ω, based on the following values (see *EQ 1)*:

- V_{SUPPLY} = 3.3 V,
- I_{trans} = 50 mA
- Ripple = 5%

The simulation result (see Figure 22) shows that it meets the required impedance levels.

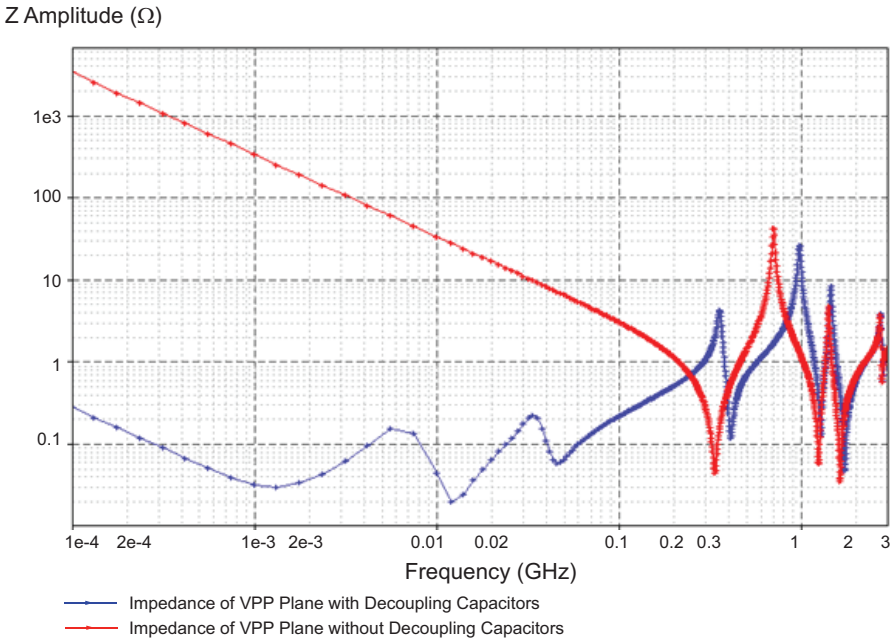


***Figure 22* • Impedance Profile of VPP Plane Over Frequency Range**

High Speed Serial Link (SerDes)

Layout Considerations

Differential Traces

A well-designed differential trace has the following qualities:

- No mismatch in impedance
- No insertion and return loss
- No skew within the differential traces

To achieve these qualities, the following points need to be considered while routing high-speed differential traces

- Differential traces should be routed with tight length-matching (skew) Asymmetry in length causes conversion of differential signals to common mode signals. The differential pair should be routed such that the skew within differential pairs is less than 5 mils.

Figure 23 shows guidelines and techniques that can be used for skew matching..

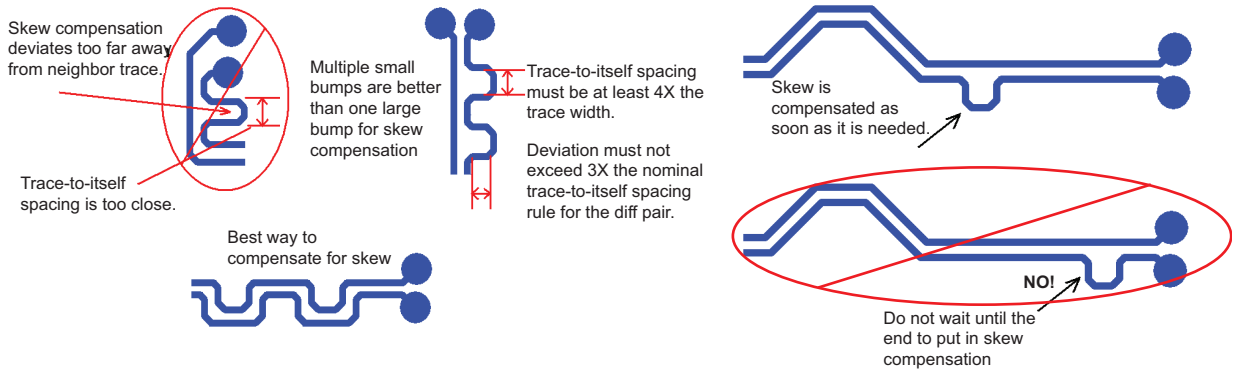


Figure 23 • **Skew Matching Guidelines**

- The length of differential lanes should be matched within the TX and RX group.

Applies only to specific protocols such as XAUI.

- Differential pairs should be routed symmetrically in to, and out of structures, as shown in Figure 24.

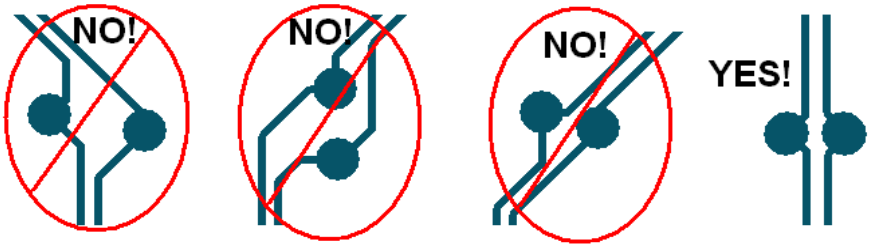


Figure 24 • **Example of Asymmetric and Symmetric Differential Pair Structure**

– Skin effect dominates as the speed increases. To reduce the skin effect, the width of the trace should be increased (loosely coupled differential traces). Increased trace width causes an increase in dielectric losses. To minimize the dielectric loss, use low dissipation factor (Df) PCB materials such as Nelco 4000-13. This is approximately double the cost of FR4 PCB material, but can provide increased eye-opening performance when longer trace interconnections are required. Be sure to maintain 100 Ω differential impedance. This is an important guideline to be followed when data rate is 5 Gbps or higher.

– Far end crosstalk is eliminated by using stripline routing. However, this type of routing causes more dielectric loss and more variation in impedance. Crosstalk impacts only when there is high-density routing. In order to reduce dielectric loss, it is recommended to route as a microstrip, if there is enough space between differential pairs (> 4 times the width of the conductor). Simulations are recommended to see the best possible routing.

– 2116 or 2113 glass-weaving PCB materials should be used to avoid the variations in impedance.
– Zig-zag routing should be used instead of straight line routing to avoid glass weaving effect on impedance variations as shown in the Figure 25.
Instruct the fabrication vendor to use these PCB materials before manufacturing.

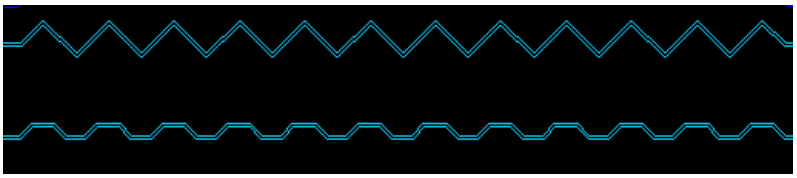


Figure 25 • **Zig-Zag Routing**

– These traces should be kept away from the aggressive nets or clock traces.
– Separation between coupled differential trace pairs should be 1x. Spacing between channels should be > 3x the separation. Trace stubs should be avoided. The stub length should not exceed 40 mils for a 5 Gbps data rate.
– Trace lengths should be kept as small as possible.
– It is recommended to use low roughness, that is, smooth copper. As the speed increases insertion loss due to the copper, roughness increases. The attenuation due to skin effect is increased proportional to the square root of frequency. The roughness courses this loss proportional to frequency. Microsemi recommends instructing the PCB fabrication house to use smooth copper, if the frequency exceeds 2 Gbps.

• Split reference planes should be avoided. Ground planes must be used for reference for all the SerDes lanes.

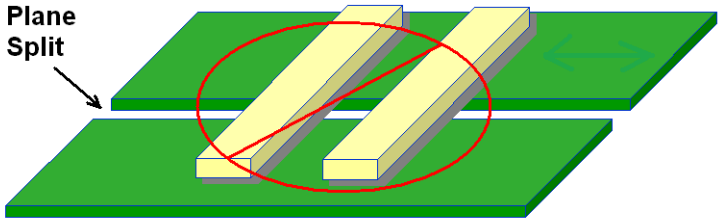


Figure 26 • **Ground Planes for Reference**

Via

- The target impedance of vias are designed by adjusting the pad clearance (anti-pad size). Field solver should be used to optimize the via according to the stack-up.

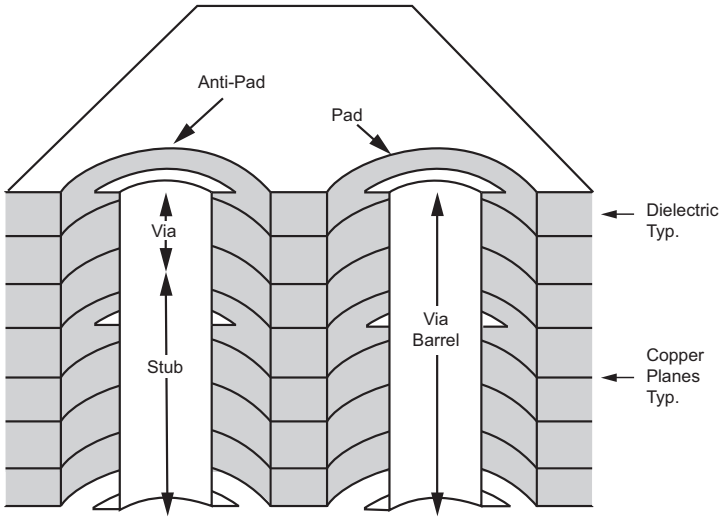


***Figure 27* • Via Illustration [References 2]**

- Number of vias on differential traces should be avoided or minimized. SerDes signals should be routed completely on a single layer with the exception of via transitions from the component layer to the routing layer (3-via maximum).
- The length of via stubs should be minimized by back-drilling the vias, routing signals from the near-top to the near-bottom layer, or using blind or buried. Using blind-vias and back-drilling are good ways to eliminate via stubs and reduce reflections.
- The stub length should be kept below 100 mils, if the data rate is 2.5 Gbps and 40 mils, if the data rate is 5 Gbps.
- If feasible, non-functional pads, that is, pads on the via that have no trace connected,should be removed. Removal of such pads reduces the via capacitance and stub effect of pads.

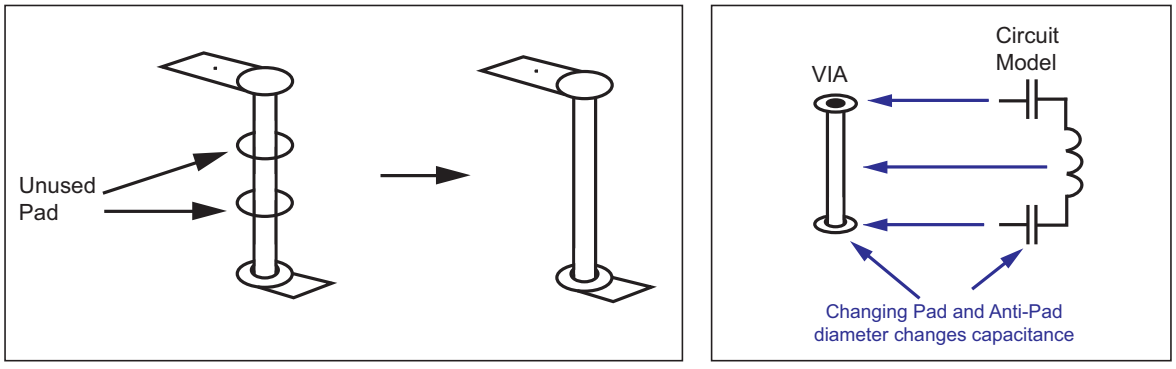


***Figure 28* • Non Functional Pads of Via**

- Using tight via-to-via pitching helps reduce the cross talk effect, as shown in Figure 29.

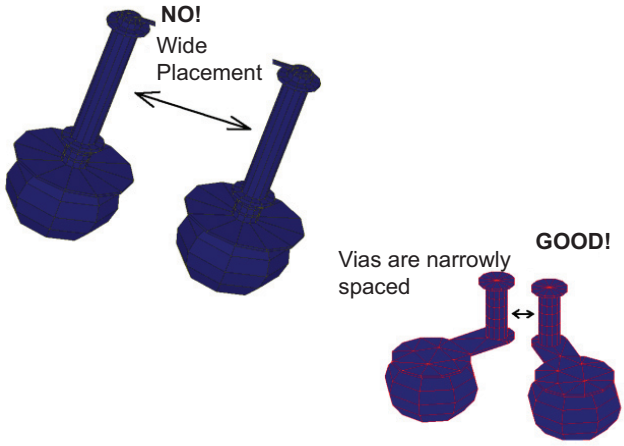


***Figure 29* • Via-to-Via Pitch**

- Symmetrical ground vias (return vias) should be used to reduce discontinuity for the common mode signal component, as shown in Figure 30. The common mode of a part of the signal requires continuous return path RX to TX and GND. Return vias help in maintain continuity.

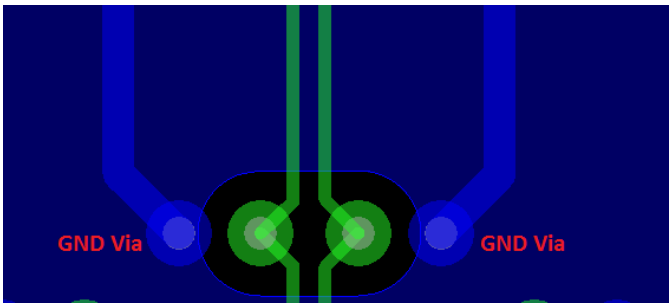


***Figure 30* • GND Via or Return Via**

DC Blocking Capacitors

The plane underneath the pads of DC blocking capacitors should be removed (see Figure 31) in order to match the impedance of the pad to 50 Ω. This is required only for the immediate reference plane, not for all planes.

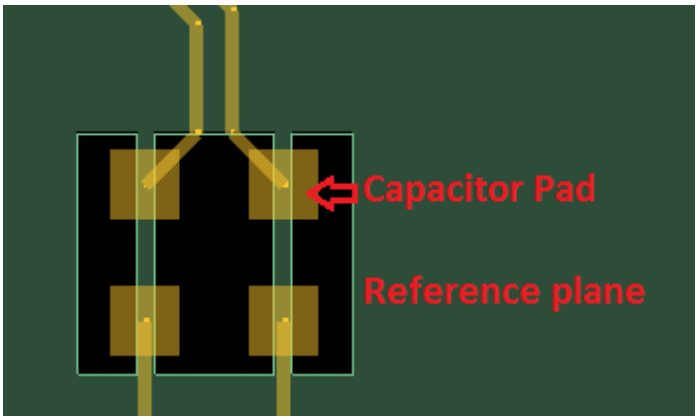


Figure 31 • **Capacitor Pad Reference Plane**

Connectors

The plane keep-out clearance should be optimized from the pin in order to get 50 Ω impedance when through-hole SMAs or connectors are used. This minimizes reflection loss.

Considerations for Simulation

Microsemi recommends simulations to confirm the quality of the received signal. The following files are required to simulate the serial channel:

- IBIS: AMI files for RTG4 and any other devices that are connected to SerDes
- Package files (optional). S-parameter of package improves the accuracy instead of using package parameters present in IBIS file
- Board traces model file that includes via models
- Connector models, if required

Steps to run the serial channel simulations are as follows:

Step1: Gathering the Required Files

IBIS-AMI Models

The IBIS-AMI models of RTG4 and the IBIS-AMI models of IC that is going to interface with RTG4 can be downloaded from the following link on the Microsemi website:
http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models/ibis-models-military-and-aerospace.aspx

Package Models

The package models (S-parameter models) of RTG4 can be downloaded from the following link on the Microsemi website:
http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models/ibis-models-military-and-aerospace.aspx

The accuracy of simulation improves with S-parameter model of package file instead of using package models available in the IBIS file. If S-parameter models are used, the package details in IBIS should be commented.

PCB Trace Models

The PCB file should be converted into a format compatible with the simulator software. For example, the `.HYP` file format of PCB is required to be simulated in Hyperlynx, and SPD file format for simulation in Sigrity. Once the PCB file is loaded in the simulation tool, the stack-up that matches the PCB stack-up should be checked. The dielectric constant (Dk), and Df of the PCB material should be defined. The tool may not extract the correct models, if these factors are not defined properly. SerDes traces must be identified and the ports on both sides of the traces assigned.

The S-parameter models of traces should be extracted. The following tools can be used to extract S-parameter models of PCB traces:

- Agilent's ADS
- Mentor's Hyperlynx
- Sigrity's PowerSI

It is not mandatory to use the above-mentioned tools; several other tools that help extract S-parameter models are available in the market.

Step2: Creating Simulation Topology

Figure 32 shows the typical topology of blocks involved in the serial link analysis. All SerDes simulations in this document, including the blocks represented in Figure 32, are done using Sigritys SystemSI tool. Simulations can be done in any tool that supports the serial link analysis, as the topology is the same in all the tools.

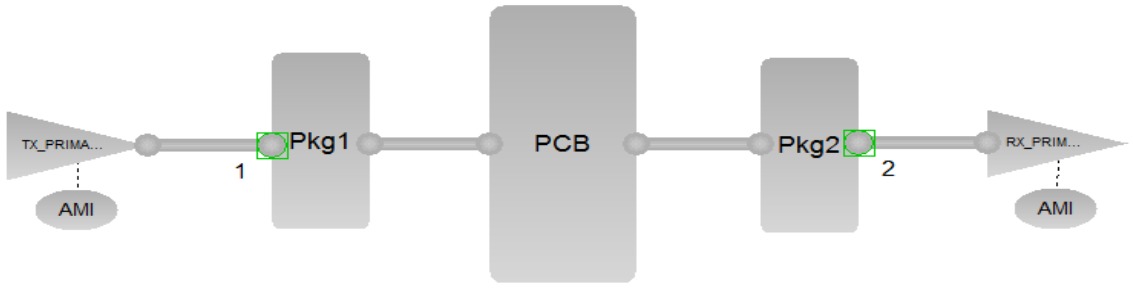


***Figure 32* • Typical Topology for SLA Simulation**

From Figure 32:

- AMI: AMI models of Tx and Rx
- TX_PRIMARY: IBIS model of Tx I/O
- Pkg1 and Pkg2: Package model of Tx and Rx I/O
- PCB: S-parameter model of RTG4 Development Kit SerDes Traces
- RX_PRIMARY: S-parameter model of either the connector or the IBIS model of the receiver IC device

Once all the model files are imported into the topology, the default configuration in the AMI model should be left to calculate the appropriate coefficients and run the simulations.

Step3: Configuring the AMI Model

The following configurations on the AMI model are required before simulating the serial channel.

TX AMI Model

Figure 33 shows the block diagram of the 3-tap feed-forward equalizer structure for the TX. The output of the TX is calculated using the transfer function $t_{n-1} + t_nZ^{-1} + t_{n+1}Z^{-2}$. The TX output depends on the tap coefficient values. The following are the details of coefficients.

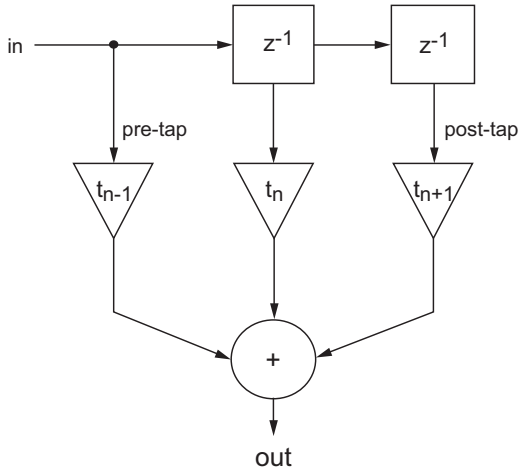


***Figure 33* • Block Diagram of the 3-Tap Feed Forward Equalizer (FFE)**

- **t0:** Pre-cursor tap setting; set to 0 for automatic generation. The range is from -0.4 to 0, default value is 0.
- **t1:** Main tap; set to 0 for automatic generation. The range is from 0 to 1, default value is 0.
- **t2:** Post-cursor tap; set to 0 for automatic generation. The range is from -0.5 to 0, default value is 0.
- **TapsFromFile:** Explicit FFE coefficients can be set through this file. If a file is used, it overrides the manual tap settings and automatic generation.
- **TapsToFile:** Output FFE tap coefficients to this file when automatic generation coefficients is used.

RX AMI Model

SerDes supports programmable single-pole continuous time linear equalization (CTLE) at the receiver. The continuous time linear equalization involves amplifying higher frequency components that have been more severely attenuated by the interconnect, or attenuating lower frequency components to a greater degree than the higher frequency components.

The low frequency attenuation level and flat-band bandwidth are programmable, as shown in Figure 34.

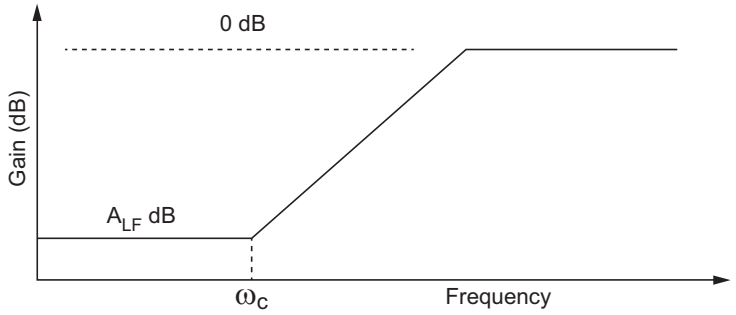


***Figure 34* • Continuous Time Linear Equalization Response**

Both ALF and ω_c (f0) can be set to maximize the signal quality of the receiver for achieving the highest possible bit-error rate (BER).

- Alf: Low frequency dB loss of the filter. The range is from 0 to 50; the default value is 6.
- f0: High pass cutoff frequency. The range is from 1e6 to 5e10; the default value is 1e9.

Step 4: Results

Qualification of simulation results is done based on the eye-height, eye-width, and BER curves. Check the eye-height and eye-width at a target BER of 10e-12. These results found in the report generated by the simulation tool. For example, Sigrity tool gives the following information at Rx:

At BER of 10e-12, running at 5 Gbps bit rate

- The eye-width is 0.68 UI (Unit Interval)
- The eye-height is 213 mV

This simulation is on the RTG4 Development Kit using Sigrity tool and the waveforms are shown in Figure 35. The simulation result shows that it meets the PCIe 2.0 requirements

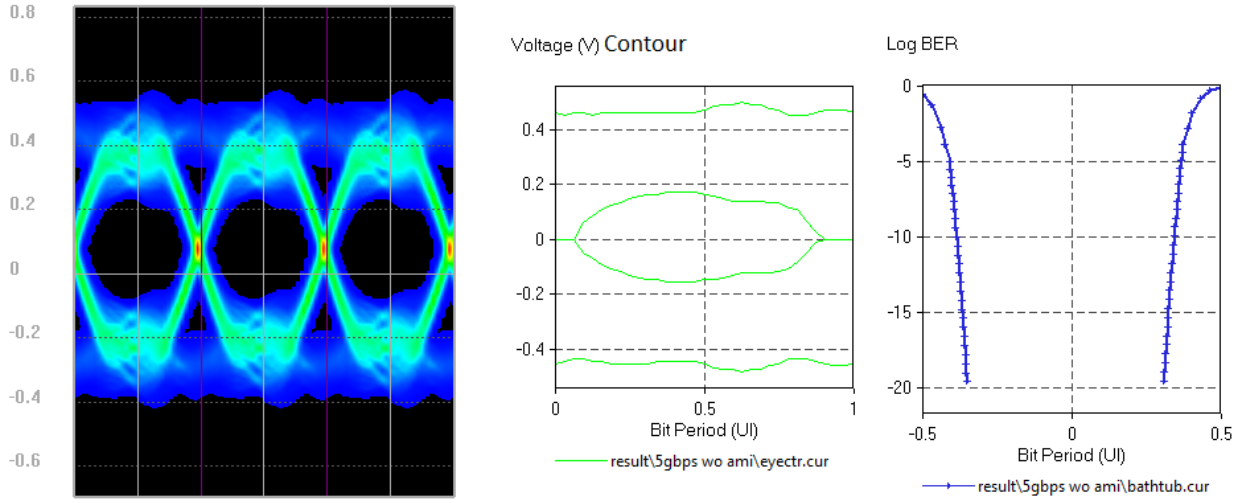


***Figure 35* • Expected Results from Simulations (Eye Diagram, Eye Contour, and Bath Tub Curve)**

Table 1 lists the specifications of the received signal for PCIe.

Table 1 • **Specifications of the Received Signal for PCIe**

Bit rate	Min Height of the eye at Rx	Min Width of the eye at Rx
2.5 Gbps	175 mV	0.6 UI

For more information on PCIe 2.0, see *PCI Express Base specification*.

DDR3 Layout Guidelines

Placement

It is required to ensure an L-shaped placement of DDR3 memories looks like *L*-shape, where memories are at the bottom of the *'L'* and controllers are at the top of the '*L'*. This allows enough space to route DQ signals with less number of layers. This is not mandatory to follow the suggested placement. However, the placement also depends on the board constraints. The trace length of each signal in the placement should not exceed seven inches.

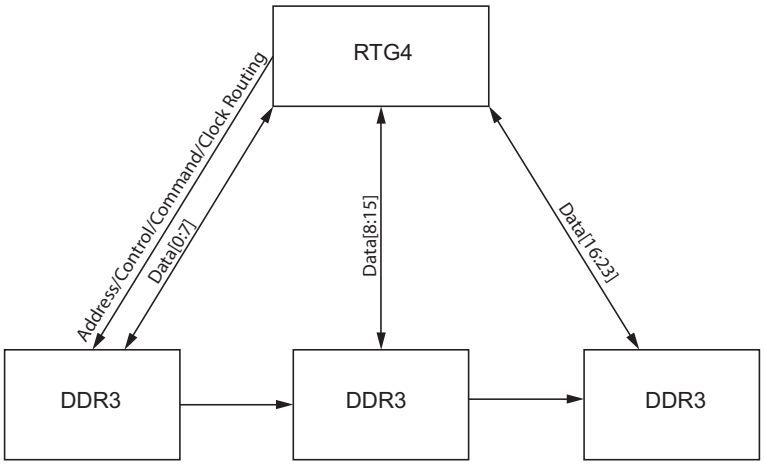


Figure 36 • **DDR3 Memories**

Termination resistors are not required for the DQ and DQS signals as these signals have on-chip ODTs. These termination resistors are placed at the end of the address, command, control, and clock signals as these signals use fly-by topology. The VTT plane/island is thick enough to handle the current required by termination resistors; a minimum of 150 mil trace is required. The sense pin of the VTT regulator should be connected at the center of the VTT island.

Routing

The reliability of DDR interface depends on the quality of the layout. There are many layout guidelines available from memory vendors. The following recommendations can also be used for routing the DDR3 signals. DDR3 signals are grouped as follows:

- Data
- Address/Command
- Control
- Clocks
- Power

Table 2 shows the grouping of DDR3 signals.:

Table 2 • **Grouping of DDR3 Signals**

Group	Signals
Data	DQ[0:7], DQ[8:15], DQ[16:23], DQ[24:31] and DQS[0:3], DM[0:3]
Address/Command	A[0:15], BA[0:2], RAS#, CAS#, and WE#
Control	CS#, CKE], and ODT
Clock	CK and CK#

Data Group Signal Routing

The following guidelines should be followed when routing data group signals:

- Data signals should not be over the split planes.
- The reference plane for data signals should be GND plane and should be contiguous between memory and RTG4.
- Traces should not be routed at the edge of the reference plane and over via anti pads.
- When routing data signals, the longest signals should be routed first, this allows to adjust the length for the short length signals, when routing the data signals.
- Serpentine routing should be used to adjust the data group signals to meet this requirement.
- The DQS signal should be routed along with associated data byte lane on the same critical layer with the same via count. Avoid using more than three vias in the connection between the FPGA controller and memory device.
- The impedance for the data traces depends on stack-up and trace width. There are options to select the impedance based on the stack-up and trace width.
  - 40 Ω impedance, which requires wide traces (~7 to 8 mils). This gives the less cross talk and less spacing between the traces (~2x). Spacing between non DDR signals and DDR signals should be ~4x.
  - 50 Ω impedance, which requires smaller trace width (~4 to 6 mils). This requires more spacing between the traces (~3x). Spacing between non DDR signals and DDR signals should be ~4x.
- All data lanes should be matched within 0.5 inch.
- Within each of the data lanes, each traces should be matched to within ±10 mils of the associated data strobe.
- The DQS and DQS# need to be matched within +/- 5 mils.
- The differential impedance should be between 75 to 95 Ω. If the data rate is more than 1600 MT/s, then the impedance should be in the range of 90 to 95 Ω.
- The differential traces adjacent to noisy signals or clock chips.
- Spacing between differential lines should be 5 to 8 mils.

Address, Control, Command, and Clock Routing

- These signals should be routed using fly-by topology, and terminated by using appropriate termination resistor at the end of the signals. The resistor termination should not have a stub longer than 600 mil.
- The impedance for the trace depends on the stack-up and trace width. There are options to select the impedance based on the stack-up and trace width:
  - 40 Ω impedance, which requires wide traces (~7 to 8 mils). This gives the less cross talk and less spacing between the traces (~2x). Spacing between non DDR signals and DDR signals should be ~4x.
  - 50 Ω impedance, which requires smaller trace width (~4 to 6mils). This requires more spacing between the traces (~3x). Spacing between non DDR signals and DDR signals should be ~4w to avoid crosstalk issues.
  - Address and control signals can be referenced to a power plane if a ground plane is not available. The power plane should be related to the memory interface. However, a ground reference is preferred. Address and control signals should be placed on a different routing layer than DQ, DQS, and DM signals to isolate crosstalk between the signals.

Clock

- Clock signals are routed differentially, and the length matches between traces should be +/- 5 mils The clock trace length should be more than strobe length.
- Clock signals should be referenced to a ground plane.
- The space between clock and other signals should be 25 mils.
- One clock signal is routed per rank of the DIMM, that is, one clock for single-ranked DIMM, two clock signals for dual ranked DIMM. For non-DIMM systems, the differential terminations used by the CK/CK# pair must be located as close as possible to the memory.
- The max skew between the clock and each DQS should be less than 10 inches.
- If more than one clock signal is used, the same clock to DQS skew should be applied to all CS.
- Address/control signals and the associated CK and CK# differential FPGA clock should be routed with trace matching of ± 100 mil.

Note:

1. Short the MDDR_TMATCH_0_IN and MDDR_TMATCH_0_OUT pins under BGA using short trace.
2. Short the MDDR_TMATCH_1_IN and MDDR_TMATCH_1_OUT pins under BGA using short trace.
3. Short the MDDR_TMATCH_ECC_IN and MDDR_TMATCH_ECC_OUT pins under BGA using short trace.
4. Short the FDDR_TMATCH_0_IN and FDDR_TMATCH_0_OUT pins under BGA using short trace.
5. Short the FDDR_TMATCH_1_IN and FDDR_TMATCH_1_OUT pins under BGA using short trace.
6. Short the FDDR_TMATCH_ECC_IN and FDDR_TMATCH_ECC_OUT pins under BGA using short trace.

Figure 37 shows an example layout.

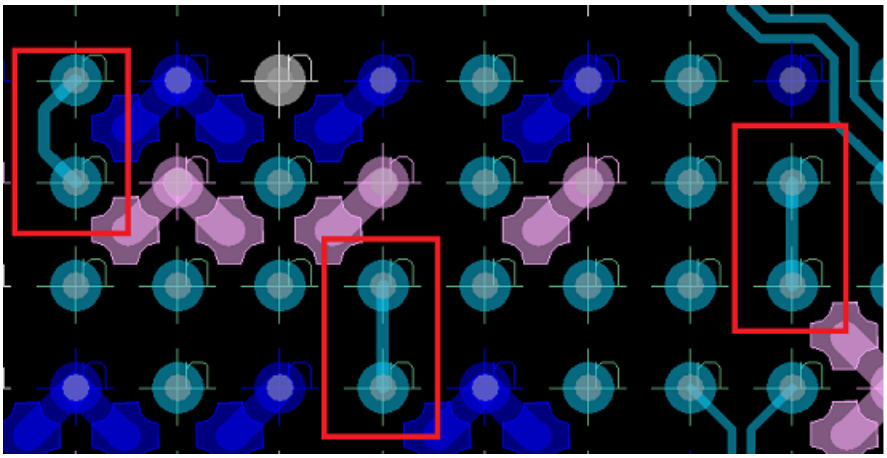


***Figure 37* • TMATCH Signals (Example Layout)**

Simulation

Simulations ensure that the DDR and controller meet timing requirements. They also ensure that the quality of the received waveform in terms of undershoot, overshoot and jitter and so on.

The following files are required for DDR3 simulation:

- RTG4 IBIS file
- DDR3 memory IBIS file
- RTG4 board PCB files and the PCB files of the DIMM, if used
- Connector models if DIMM is used

Following are the steps to run the serial channel simulations:

Step 1: Gathering the Required Files

IBIS Models

To download the IBIS models of RTG4 and the IBIS-AMI models of DDR3 memory which is going to interface with RTG4, refer to the following links on the Microsemi website:
http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models/ibis-models-military-and-aerospace.aspx

PCB Trace Models

The PCB file needs to be converted into a format compatible with the simulator software. For example hyp file format of PCB is required to simulate in Hyperlynx and SPD file format of PCB for simulation in Sigrity. Once the PCB file is loaded in the simulation tool, check the stack-up that matches the PCB stack-up and define the dielectric constant, Dk and Dissipation factor, and Df of PCB material. The tool extracts wrong models, if the above points not defined properly. Some tools run the simulations on PCB file itself like Hyperlynx and some tools need S-parameter files of DDR3 traces to continue the simulations.

To extract S-parameter models of PCB traces assign the ports on both sides of the traces and extract the S-parameter models of traces. The following tools can be used to extract S-parameter models of PCB traces:

- Agilent's ADS
- Mentor's Hyperlynx
- Sigrity's PowerSI

It is not mandatory to use above-mentioned tools; several other tools that help extract S-parameter models are available in the market.

Step 2: Creating Simulation Topology

Figure 38 shows the typical topology of blocks involved in DDR3 simulations. These blocks are taken from the Sigrity tool. The simulation can be done in any tool which supports DDR3 simulation, as the topology is the same in all the tools.

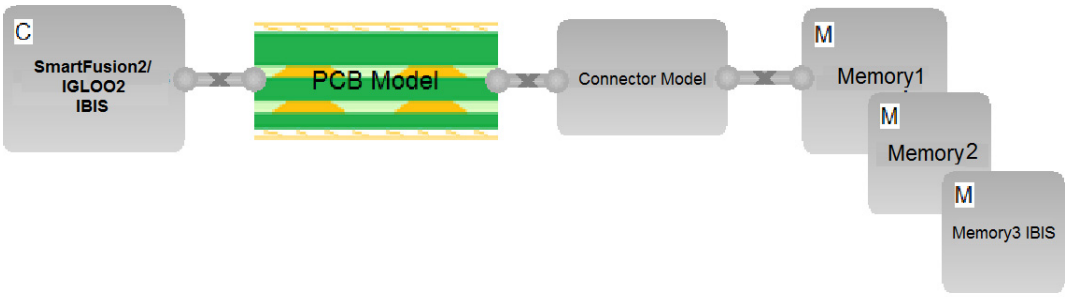


***Figure 38* • DDR3 Simulation Topology**

From Figure 38:

- RTG4 IBIS: IBIS model of RTG4
- PCB: S-parameter model of PCB file, connector models and DIMM PCB models
- Connector model: Spice models of connector
- Memory IBIS: IBIS models of DDR3 memory

Step 3: Simulation Setup

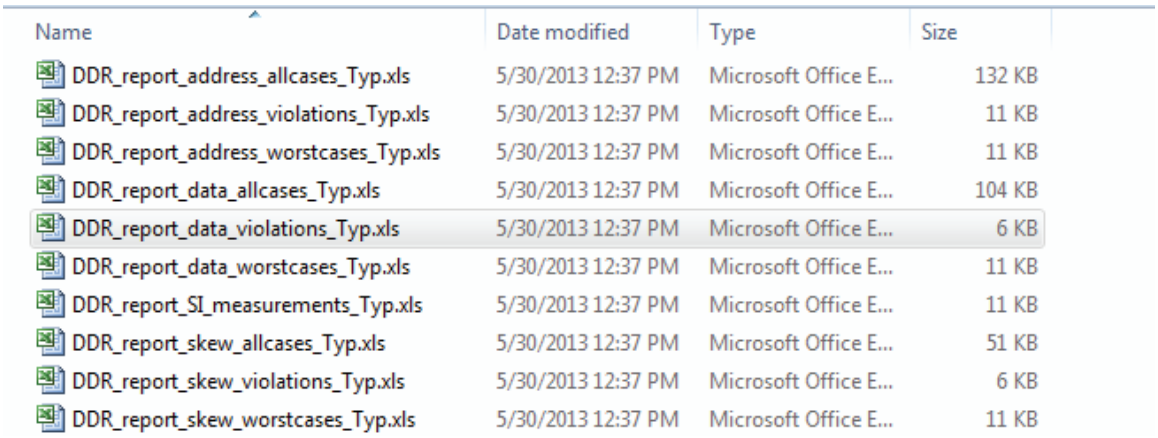
- Assign IBIS models to RTG4 and memory
- Assign the connector model, if used
- Assign the models for on-board termination resistors
- Identify the DDR3 nets and classify according to data, control, and address bus
- Set the appropriate ODT for SF2 and memory.
- Set 40 to 60 Ω ODT for data and 80 to 120 Ω for DQS signals
- Set the maximum frequency at which the system will operate. For RTG4, it is 333 MHz

Step 4: Results

The important things that needs to be observed from the results are:

- Setup and hold time between data signals and the respective DQS over all corners
- Setup and hold time between Control/Command/Address signals and the clock over all corners
- Overshoot and undershoot of all signals with respect to JEDEC specifications over all corners. And also DC threshold multi crossing that occurred due to the excessive ringing

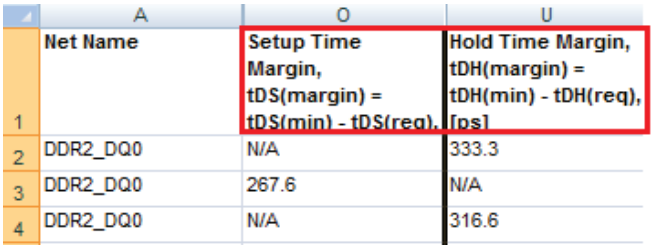
The simulation tool generates the report where all the details are available. For example, Hyperlynx generates the set of excel sheets, that contain all setup and hold margin, overshoot and undershoot information for all corners. It also generates driver and receiver waveforms for all the nets. Figure 39 shows list of files generated by Hyperlinx, with all the simulation information.



Name	Date modified	Type	Size
DDR_report_address_allcases_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	132 KB
DDR_report_address_violations_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	11 KB
DDR_report_address_worstcases_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	11 KB
DDR_report_data_allcases_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	104 KB
DDR_report_data_violations_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	6 KB
DDR_report_data_worstcases_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	11 KB
DDR_report_SI_measurements_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	11 KB
DDR_report_skew_allcases_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	51 KB
DDR_report_skew_violations_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	6 KB
DDR_report_skew_worstcases_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	11 KB

***Figure 39* • List of Hyperlynx Simulation Reports Generated**

Figure 40 shows an example report for an A0 net. It shows that the A0 has enough setup and hold time margins.



	A	O	U
1	Net Name	Setup Time Margin, tDS(margin) = tDS(min) - tDS(req), [ps]	Hold Time Margin, tDH(margin) = tDH(min) - tDH(req), [ps]
2	DDR2_DQ0	N/A	333.3
3	DDR2_DQ0	267.6	N/A
4	DDR2_DQ0	N/A	316.6

***Figure 40* • Setup and Time Margins of A0**

If any of the net is violating the setup and holding time margins, the length of the net should be changed accordingly. If there is a high-peak overshoot or undershoot, it could be because of the high value termination resistor. It is required to adjust the value of ODT and re-iterate the simulation.

Figure 41 shows how to setup and hold time margins for DQ and DQS signals. Same is applicable to the margin between the Command/Control/Address and CLK signals.

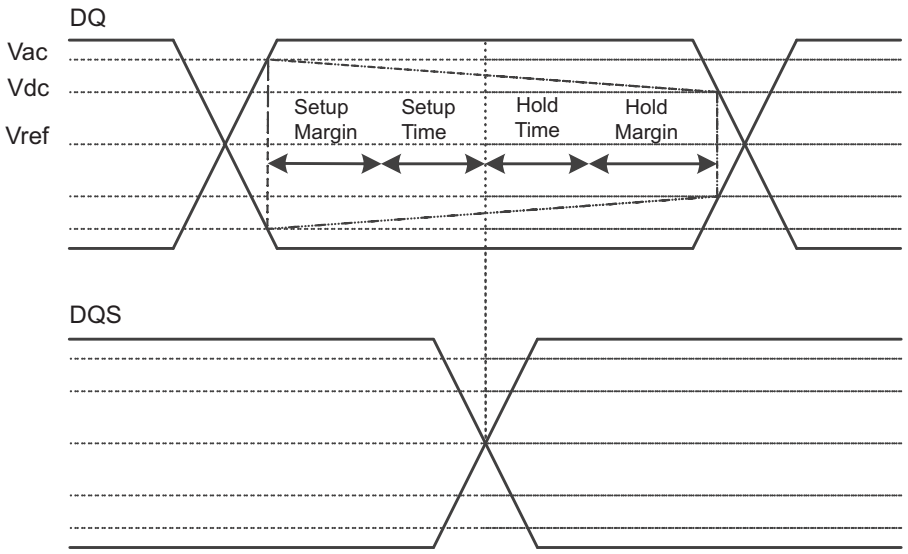


***Figure 41* • Setup and Time Margins for DQ and DQS Signals**

Appendix A: Layout Checklist

S.No.	Description	Page	Yes/No
	Power		
1.	Are 0402 or lesser size capacitors used for all decaps (less than value?)	N/A	
2.	Is the power supply filter implemented on Serdes Core supply (SERDES_x_VDD) as shown in Figure 5 on page 6?	6	
3.	Are power supply filters implemented on SERDES_x_VDDAPL and SERDES_x_PLL_VDDA as shown in the Figure 5 on page 6 and Figure 16 on page 14 respectively?	6 and 14	
4.	Is a precision 1.21K resistor used between SERDES_x_REFRET and SERDES_x_REXT?	7	
5.	Are placement and layout guidelines followed for the 1.21 K resistor?	7	
6.	Is the target impedance met on all power planes?	N/A	
7.	Are VREF planes for the DDRx reference supply isolated from the noisy planes?	11	
8.	Are sufficient number of decoupling capacitors used for the DDRx core and VTT supply?	3	
9.	Is one 0.1 µF capacitors for two VTT termination resistors used for DDRx?	N/A	
10.	Is the VTT plane width sufficient?	28	
	DDR3		
11.	Are the length-match recommendations for DDR3 followed?	28	
	SerDes		
12.	Are the length-match recommendations for SerDes followed?	19	
13.	Are DC blocking capacitors used for the SerDes TX, and, if required, on RX lines?	24	
14.	Is tight-controlled impedance maintained along the SerDes traces?	19	
15.	Are differential vias well designed to match SerDes trace impedance?	19	
16.	Are DC blocking capacitor pads designed to match SerDes trace impedance?	24	
	Dielectric Material		
17.	Is proper PCB material selected for critical layers?	38	

Appendix B: Special Layout Guidelines for Crystal Oscillator

The crystal oscillator should be placed close to the RTG4 device. Two capacitors should be placed symmetrically around the crystal oscillator so that the length from the crystal pad to capacitor are equal, as shown in the Figure 42. Both the traces from the crystal to the device should be equal in length.

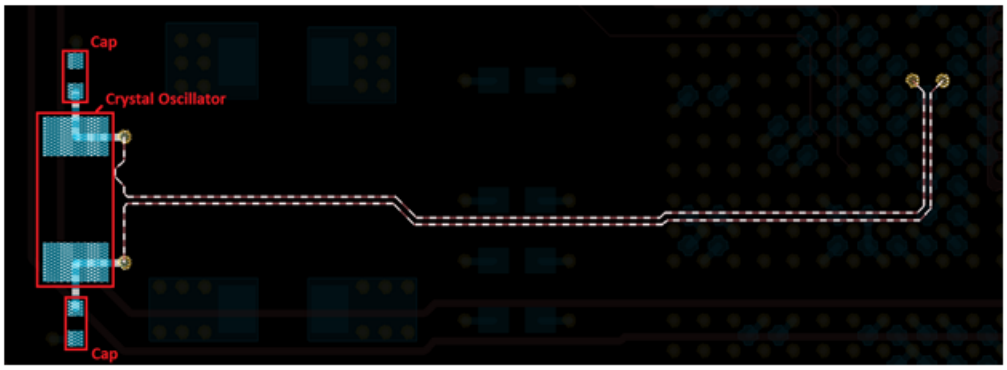


***Figure 42* • Crystal Oscillator Layout**

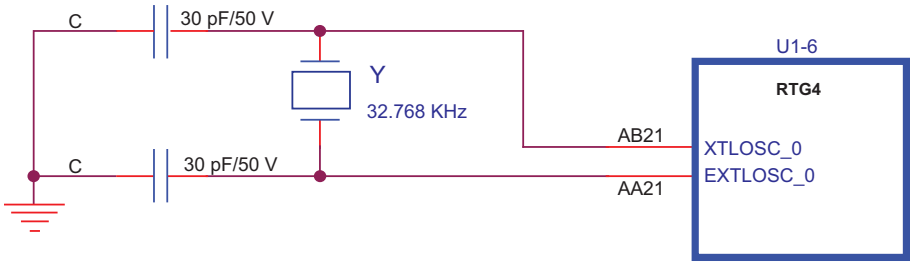


***Figure 43* • Crystal Oscillator Schematics**

Appendix C: Stack-Up

A good stack-up leads to better performance. The number of layers in the stack-up depends on factors such as the board's form factor, the number of signals to be routed, and the power requirements. Based on these factors, the designer chooses how many layers the board requires. The RTG4 Development Kit has a 16-layer stack-up as shown in Figure 10 on page 10.

Note: All the guidelines in this document are with respect to a 16-layer board stack-up.

The upper power layers should be used for high priority supplies. High-switching current supplies should be placed vertically, close to the devices to decrease the distance the currents need to travel through the vias. Ground planes should be placed adjacent to the high-transient current power planes to reduce inductance and to couple the high-frequency noise.

It is good to have power and ground layers side-by-side such inter-plane capacitance provides better decoupling at high frequencies.

The effect of vias on power pins is reduced by placing a power plane near the device.

Signal integrity depends on how well the traces have controlled impedance, so it is always recommended to have controlled impedance.

Microsemi recommends that all critical high-speed signals such as DDR and PCIe signals, need to have a ground reference. All signal layers should be separated from each other by ground or power planes. This minimizes crosstalk and provides balanced and clean transmission lines with properly controlled characteristic impedance between devices and other board components.

For best performance, use dedicated ground plane layers that are continuous across the entire board area. Power planes can provide adequate reference, however, the power planes should be related to the signals they serve to reference.

Note: Refrain from using unrelated power planes as a signal reference.

Slots should not interrupt the planes, or else they can possibly force current to find an alternate return path. This undesired return path may cause a localized bounce on the power or ground plane that can possibly be capacitively coupled to all signals adjacent to the planes.

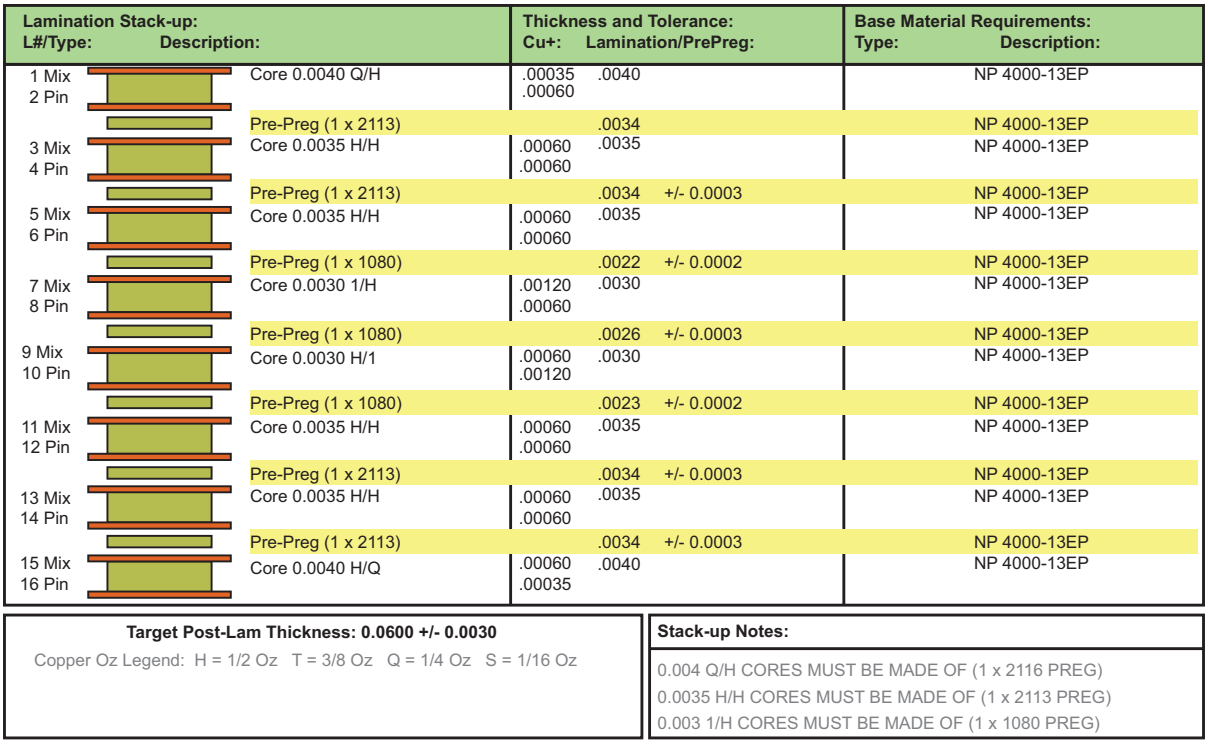


Figure 44 • **Stack-up Used in Development Board**

Appendix D: Dielectric Material

The impedance of traces depends on the geometry of the traces and the dielectric material used. The skew of the signal depends on the dielectric constant, and loss of signal strength depends on the loss tangent of the material. The RTG4 Development Kit board uses Nelco 4000-13 dielectric material. However, the material is selected based on the speed and length of the high speed traces. Simulations are recommended on high-speed serial links to converge on the type of the material used.

If the total trace length is less than 20 inches with a speed at or below 3.125 Gbps, FR-4 may be acceptable. Another design option is to use low-loss dielectric PCB material, such as Rogers 4350, GETEK, or ARLON. It can provide increased eye-opening performance when longer trace interconnections are required. If longer traces or faster speed is required, consider using a high-speed material such as ROGERS 3450.

While designing for gigabit serial links, the weaving structure of the PCB dielectric material should be taken into consideration. A PCB dielectric substrate is constructed from woven fiberglass fabrics strengthened and bound together with epoxy resin. A typical weaving of PCB dielectric material is shown in Figure 45.

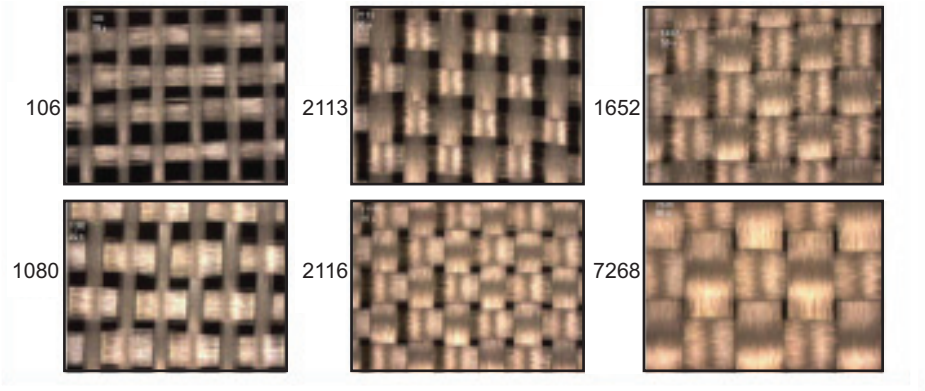
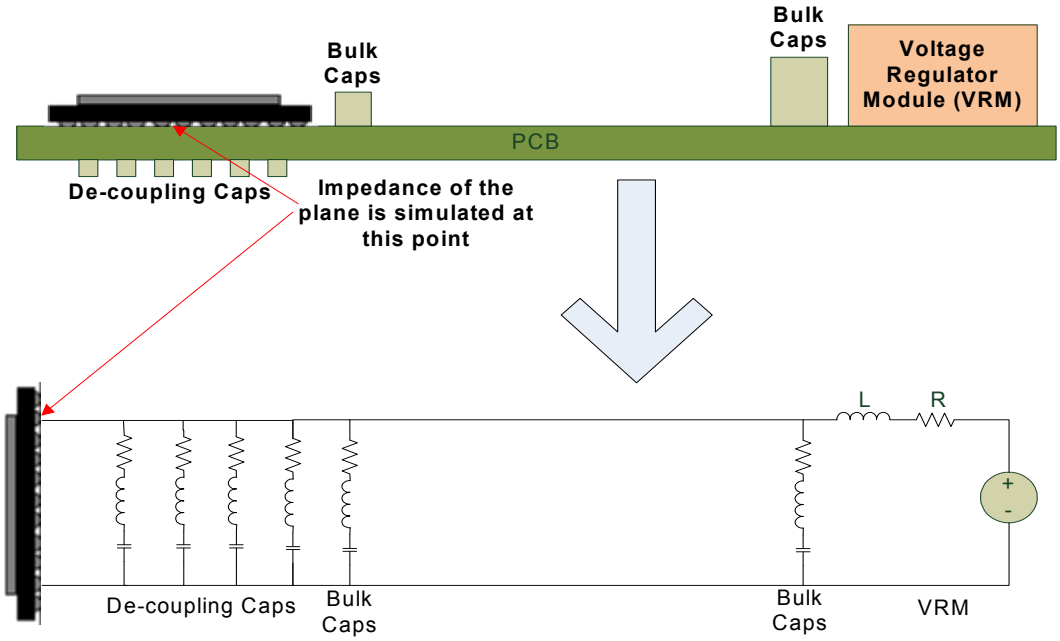


***Figure 45* • Fiberglass Weaving [References3]**

Depending on the density of weaving, PCB materials are numbered as 106, 1080, 2113, 2116, 1652, and 7268. Trace routed on the PCB is non-homogeneity in dielectric constant due to weaving. This causes discontinuities in the trace impedance, resulting in improper eye-opening at the receiving end. For more information about, see the *Solving PCB Fiber Weave Issues*.

Appendix E: Power Integrity Simulation Topology

Figure 46 shows the topology considered for simulating the power plane for Power Integrity analysis.



Note: Package parameters of RTG4 are not considered for simulations.

***Figure 46* • Power Integrity Simulation Topology**

References

- Power Distribution Network (PDN) by Eric Bogatin
- "Method of Modeling Differential Vias", White Paper, Jan 2011by L. Simonovich, E. Bogatin, Y. Cao.
- *signal-integrity.tm.agilent.com/2011/pcb-fiber-weave/*
- Sigrity PowerSI tutorial

List of Changes

The following table lists critical changes that were made in each revision of the document.

Revision	Changes	Page
Revision 1 (March 2016)	Initial release.	NA

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