Libero SoC v11.6 Timing Validation and Design Migration User's Guide

Microsemi

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1 – Libero SoC v11.6 Timing Validation and Design Migration

Introduction

Libero SoC v11.6 has critical timing updates. This document describes how to check the timing of your pre-Libero SoC v11.6 designs, and what actions you can take to meet your timing requirements if you have timing violations after migrating your design to Libero SoC v11.6.

Important Guidelines for Running Place and Route

When migrating your design to Libero SoC v11.6, it may be required that you rerun the design flow—compile and place and route and timing verification—to complete your design and meet your timing requirements. You must follow two important requirements/guidelines:

GUIDELINE 1: Because of changes done to the MSS FIC_2 interface timing model, the MSS FIC_2 (SERDES and DDR configuration bus created by System Builder), must be properly constrained. If it is not, timing violations may be reported which are not true violations. Constrain this interface as described in the SmartFusion2/IGLOO2 FPGA Timing Constraints User's Guide.

GUIDELINE 2: It is highly recommended to have the new Min-delay Repair feature selected (it is on by default) when running Place and Route. Min-delay Repair is new feature offered with Libero SoC v11.6 that automatically attempts to fix design hold violations.

Designs Targeting M2S060(T/TS)/M2GL060(T/TS)-FCS(G)325 Devices

If your design targets any of the M2S060(T/TS)/M2GL060(T/TS)-FCS(G)325 devices, the design will be reset to the pre-compile state because of a critical package pin mapping fix for these devices. You will need to recompile, place and route, and revalidate your timing requirements for this design.

Designs Containing MSS DDR (MDDR) or Fabric DDR (FDDR) with AXI Interface

If your design uses MSS DDR (MDDR) or Fabric DDR (FDDR) with the AXI interface, with a DDR clock to Fabric clock ratio greater than 1, the design will be invalidated because of critical timing changes on the AXI-DDR interface. Follow the steps in Appendix A, "Instructions for Migrating Designs that use MSS DDR (MDDR) or Fabric DDR (FDDR) with the AXI Interface" of this document to complete the migration of the design.

Validating Timing of a Placed and Routed Design

To validate your design timing, perform Static Timing Analysis on your design by following these steps:

1. Make a copy of your original pre-Libero SoC v11.6 design.
   - This copy should be used for timing verification only.
   - Make sure that the project file timestamps are preserved when making the copy of the project to preserve the integrity of the project database.

2. Open your pre-Libero SoC v11.6 design. If it gets invalidated because of one of the reasons presented above, follow the previous instructions to complete the migration of your design. If the design was not invalidated, proceed to step 3.
3. Run the Libero 'CoreResetP/ConfigP Timing Constraints and Verification' Tcl script as described in Appendix D, "CoreResetP/ConfigP Timing Constraints and Verification Script".

   This script will add timing constraints to your design to properly constrain the MSS FIC_2 to CoreConfigP connectivity. It will also add false paths to the CoreResetP component between asynchronous clock domains where special cross-clock domain logic synchronization has been implemented.
4. Run Static Timing Analysis (STA) on the design using the Verify Timing tool in the Libero SoC Design Flow.

If the design does not have any max or min delay violations after running Static Timing Analysis, no further analysis is required and your timing verification is complete.

If there are timing violations present in your design that need to be repaired, follow these steps:

1. Open the original pre-Libero SoC v11.6 design. It is always recommended to create a backup.
2. Refer to "Important Guidelines for Running Place and Route" earlier in this chapter before running Place and Route.
3. Run the design implementation flow to meet your timing requirements. For guidelines about closing timing, refer to Appendix B, "Fixing Max Delay Timing Violations"and Appendix C, "Fixing Min-delay Violations".

Summary

The steps for migrating a design from a pre-Libero SoC v11.6 Libero SoC release to Libero SoC v11.6 have been presented. If you need further clarification and assistance with any of the information in this document, contact Microsemi Technical Support at: soc_tech@microsemi.com.

A – Instructions for Migrating Designs that use MSS DDR (MDDR) or Fabric DDR (FDDR) with the AXI Interface

This appendix provides instructions for migrating designs that use MSS DDR (MDDR) or Fabric DDR (FDDR) with the AXI interface, with a DDR clock to Fabric clock ratio greater than 1.

If the design contains the MDDR and uses directly the MSS component, open the MSS component and regenerate it before rerunning the flow (Synthesis, Compile, Place and Route).

If the design contains the MDDR and uses a System Builder component, open the System Builder component, navigate to the last page and click the **Finish** button to regenerate this component before rerunning the flow (Synthesis, Compile, Place and Route).

If the design contains the FDDR, upgrade the Fabric DDR Memory Controller core to the latest version (v1.1.301) and regenerate it before rerunning the flow (Synthesis, Compile, Place and Route).

If you are no longer able to achieve timing closure after running Place and Route, refer to the section "Timing Optimization Technique for AXI" in UG0446: SmartFusion2 and IGLOO2 FPGA High Speed DDR Interfaces User Guide for timing optimization techniques.

B – Fixing Max Delay Timing Violations

To fix max delay violations, use standard practices to achieve timing closure for the design. Refer to he following recommendations:

- Run Timing Driven Place and Route (TDPR) in High-effort mode.
- Use the Multi-pass feature to run multiple passes of place and route. Choose the number of passes desired, and Place and Route to attempt to meet the timing requirements using that number of random seeds.
- SmartTime timing scenarios can be useful for testing the impact of different sets of constraints. If there are specific paths which are not being satisfied, such as inter-clock domain constraints, or constraints involving I/Os, create a TDPR timing scenario in the Timing Constraints Editor. Selectively add Max Delay constraints to the TDPR scenario which would force the Place and Route tool to optimize a specific connection. Inter-clock domain paths are reported in the SmartTime GUI, but the Placer does not currently optimize their slacks.
  - Open the Timing Constraints Editor.
  - Click **View** >**Scenarios**.
  - Right-click to create a clone of your "Primary" timing scenario.
  - Mark the clone as being used for TDPR. (This will automatically set the original Primary scenario as the default "Analysis" scenario.)
  - In the TDPR scenario, add a Max Delay constraint between the logic source(s) and sink(s) which you wish to optimize. The Max Delay constraint will be detected by the Place and Route tool and the timing for these paths should improve when you rerun Place and Route.
- If timing closure is not achieved using the above Place and Route options, you can go return to Synthesis and attempt various optimization techniques. You should begin by asking yourself the following questions:
  - Were timing constraints specified during Synthesis?
  - Are the timing constraints correct (not over-constrained)?
  - Are the violated paths legitimate errors, or should they have been marked as false paths?

  Specifying realistic timing constraints for the Synthesis tool can lead to better design implementations, and allow the Synthesis tool to more accurately trade off design area to achieve performance.
- Finally, you may need to rework your design to help achieve timing closure.

C – Fixing Min Delay Timing Violations

Min delay violations can be fixed by using the Repair Min-delay Violations feature when using TDPR. Repair Min-delay Violations is a new feature introduced in Libero SoC v11.6 where the Place and Route tool attempts to repair hold violations in your design without creating max-delay violations. This feature is 'On' by default.

First, run Place and Route in Incremental mode to fix these violations. Repair Min-delay Violations will attempt two passes of repair, addressing up to 200 violations with each pass. You may run Incremental Place and Route more than once if all violations have not been fixed with the previous pass. If running multiple passes no longer yields repairs, then the automatic tool is not able to fix all violations in the design. If all violations cannot be fixed automatically, you may need to review the clocking architecture of your design. You can also analyze your design to identify false paths (for example, between clock domains).

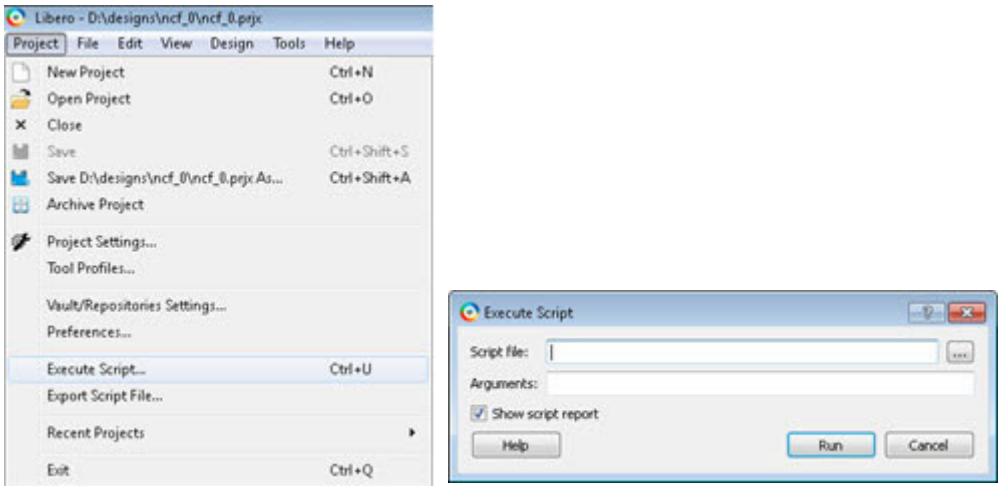
D – CoreResetP/ConfigP Timing Constraints and Verification Script

You can run the verification script by following these instructions:

- Copy the script to your machine. The script can be found at:

http://www.microsemi.com/document-portal/doc_download/135436-coreresetp-configp-timing-constraints-and-verification-tcl-script-libero-soc-v11-6

- Open your project using Libero SoC v11.6.
- Make sure that the Place and Route tool state is complete (checked green).
- Select **Execute Script** in the **Project** menu, browse to the location where you have saved the verification script, and click **Run**.



- The script will abort if:
  - The design has not been placed and routed.
  - The design does not contain a CoreConfigP connected to the MSS FIC_2 interface.
  - The design contains CoreConfigP but does not have a timing constraint on the MSS FIC_2 clock (CLK_CONFIG_APB).
- The script will print one of two messages to the Libero log window when the analysis is complete:
  - *"Your design does not have any 'true' hold violations in the CLK_CONFIG_APB clock domain between the MSS FIC_2 interface and the CoreConfigP component."*
  - *"Your design has hold violations in the CLK_CONFIG_APB clock domain between the MSS FIC_2 interface and the CoreConfigP component connected to it. Please contact Microsemi Tech Support."*.
    Contact Microsemi's Technical Support at soc_tech@microsemi.com if this situation occurs.

This script adds timing constraints to your design to properly constrain the MSS FIC_2 to CoreConfigP connectivity. It also adds false paths to the CoreResetP component between asynchronous clock domains where special cross-clock domain logic synchronization has been implemented. You can then proceed to complete the timing validation of your design using the Verify Timing tool in the Design Flow.

E – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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