

AC439
Application Note
RTG4 FPGAs Board Design and Layout Guidelines



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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 14.0

The following is a summary of the changes made in this revision.

- Removed TapsFromFile and TapsToFile options from [TX AMI Model](#), page 41.
- Updated [Recommended Operating Conditions during Programming](#), page 15.
- Updated the number of VDDPLL pins to 13 in a note in [Power Supplies](#), page 5.
- Updated the length matching guideline for DB0 versus DB1 and DB2 groups [Length Matching Guidelines](#), page 45.
- Updated how I/O are tristated in blank devices, see [I/O State During Programming](#), page 15.
- Removed the DQ Line Interchange section as it is not supported.

1.2 Revision 13.0

Updated the capacitor recommendations for following rails of RTG4 1657 package:

- VDD, VDDI1,2,7,8, VDDI4,5,6, and VDDI0,9. See, [Table 2](#), page 6.

1.3 Revision 12.0

The following is a summary of changes made in this revision.

- Updated the recommended PCB decoupling capacitors for CQ352 package, see [Table 3](#), page 8.
- Updated [Figure 2](#), page 10.

1.4 Revision 11.0

The following is a summary of changes made in this revision.

- Updated information about the [SerDes](#), page 30.
- Updated the information about the decoupling capacitors on unused SERDES Quads, PLL, and I/O Banks. See the last note in [Unused Pin Configurations](#), page 10.
- Added a DEVRST_N recommendation in [Reset Circuit](#), page 12.
- Updated the 10 μ F decoupling capacitor requirement for VDDI1 pin from 3 to 1 in [Table 2](#), page 6.
- Added information about the resistor recommendation when all PLLs are used in the design. See the note after [Figure 1](#), page 5.
- Updated the information about the power-down sequences that cause I/O glitch and in-rush current, see [Power-up and Power-Down Sequence](#), page 9.
- Updated the termination resistors in [Figure 7](#), page 14.

1.5 Revision 10.0

The following is a summary of the changes made in this revision.

- Updated [Figure 2](#), page 10.
- Updated [Figure 7](#), page 14.
- Renamed and updated [RTG4 Decoupling Capacitors](#), page 6 from Power Supply Decoupling.
- Updated [Unused Pin Configurations](#), page 10.
- Added [Board Design Checklist](#), page 49.

1.6 Revision 9.0

The following is a summary of the changes made in this revision.

- A new section, [Power-up and Power-Down Sequence](#), page 9 is added.
- PLL lock status and recovery details are added. To know more, see, [Clocks](#), page 11.

- A new figure to show PLL lock monitoring is added. To know more, see, [Figure 4](#), page 12.
- A new figure to show DDR3 memories is added. To know more, see [Figure 37](#), page 43
- [Figure 3](#), page 11, [Figure 10](#), page 20 and [Figure 12](#), page 21 are edited.
- New section, [Length Matching Guidelines](#), page 45 is added.

1.7 Revision 8.0

The following is a summary of the changes made in this revision.

- Removed the SPI Slave Programming Mode section from this document.
- Removed the Appendix: Special Layout Guidelines for Crystal Oscillator chapter from this document
- Updated the note information for PCIe transmit pins in the AC coupling section (see [AC Coupling](#), page 16).
- Updated the description in the unused pin configurations section (see [Unused Pin Configurations](#), page 10).
- Added the Status of the VREF Pin Assigned Rule for IOA table.
- Updated the System Controller SPI section (see [Device Programming](#), page 13).

1.8 Revision 7.0

Revision 7.0 was published in July 2017. The following is a summary of the changes made in this revision.

- Merged Layout Guidelines for RTG4-Based Board Design as a part of board-design guidelines application note. For more information, see [Layout Guidelines for RTG4-Based Board Design](#), page 28.
- Added a note about failsafe in the Fabric I/O Configurations section. For more information, see [SerDes](#), page 15.
- Added information about layout recommendations and plane shapes are in the disclaimer paragraph. For more information, see [Layout Guidelines for RTG4-Based Board Design](#), page 28.
- Removed references of 0.1 uF and 0.01 uF capacitors from the [Simulations](#), page 30 section as capacitors of different sizes are also available for board design.
- Updated information about differential traces in the [Data Group Signal Routing](#), page 44.

1.9 Revision 6.0

The following is a summary of the changes made in this revision.

- The revised values are updated PCB decoupling capacitors for RTG4150-CG1675 package. For more information, see [Table 2](#), page 6.
- Added PCB decoupling capacitors for RTG4150-CQ352 package. For more information, see [Table 3](#), page 8.
- Revised the instructions for measuring the temperature. For more information, see [Temperature Sensing](#), page 22.
- Cold sparing section is revised based on the change in the software. For more information, see [Cold Sparing](#), page 24.
- Added a note about User I/O's support in cold sparing section. For more information, see [Cold Sparing](#), page 24.
- The input reference voltage section is added.

1.10 Revision 5.0

The following is a summary of the changes made in this revision.

- Information about AC coupling was updated. For more information, see [AC Coupling](#), page 16.
- Information about cold sparing was updated. For more information, see [Cold Sparing](#), page 24.
- Information about power supplies was updated. For more information, see [Power Supplies](#), page 5.
- Changed the document to the new template.

1.11 Revision 4.0

The following is a summary of the changes made in this revision.

- Updated [SerDes](#), page 15.
- Updated [DDR3 Guidelines](#), page 21.
- Updated [Temperature Sensing](#), page 22.

1.12 Revision 3.0

The Cold Sparing section was updated. For more information, see [Cold Sparing](#), page 24.

1.13 Revision 2.0

The following is a summary of the changes made in this revision.

- The PLL Filter section was updated. For more information, see [PLL Filter](#), page 17.
- Capacitance values were updated. For more information, see [Table 2](#), page 6.
- The Unused Pin Configurations section was updated. For more information, see [Figure 3](#), page 11.

1.14 Revision 1.0

The first publication of this document.

2 Board Design Guidelines for RTG4 FPGAs

Good board design practices are required to achieve expected performance from the PCB and RTG4 devices. High quality and reliable results depend on minimizing noise levels, preserving signal integrity, meeting impedance and power requirements, and using appropriate transceiver protocols. These guidelines should be treated as a supplement to the standard board-level design practices.

This chapter assumes that the reader has a good understanding of the RTG4 device, is experienced in digital board design. It discusses power supplies, high-speed interfaces, various control interfaces, and the associated peripheral components of RTG4 FPGAs.

2.1 Designing the Board

RTG4 is a radiation-tolerant flash-based FPGA that supports high-speed interfaces such as Double-data rate (DDR2, DDR3, LPDDR) and SpaceWire using high-speed fabric I/O such as MSIO, MSIOD, and DDRIO. RTG4 FPGAs also support serializer/deserializer (SerDes) using SerDes I/Os, which are dedicated to high-speed serial communication protocols such as PCI Express (PCIe) 2.0, 10 Gbps attachment unit interface (XAUI), extended physical code sublayer (EPCS), multi protocols (PCIe and EPCS), serial-gigabit media independent interface (SGMII), and JESD204B, as well as user defined high-speed serial protocol implementation in the fabric.

Subsequent sections discuss the following:

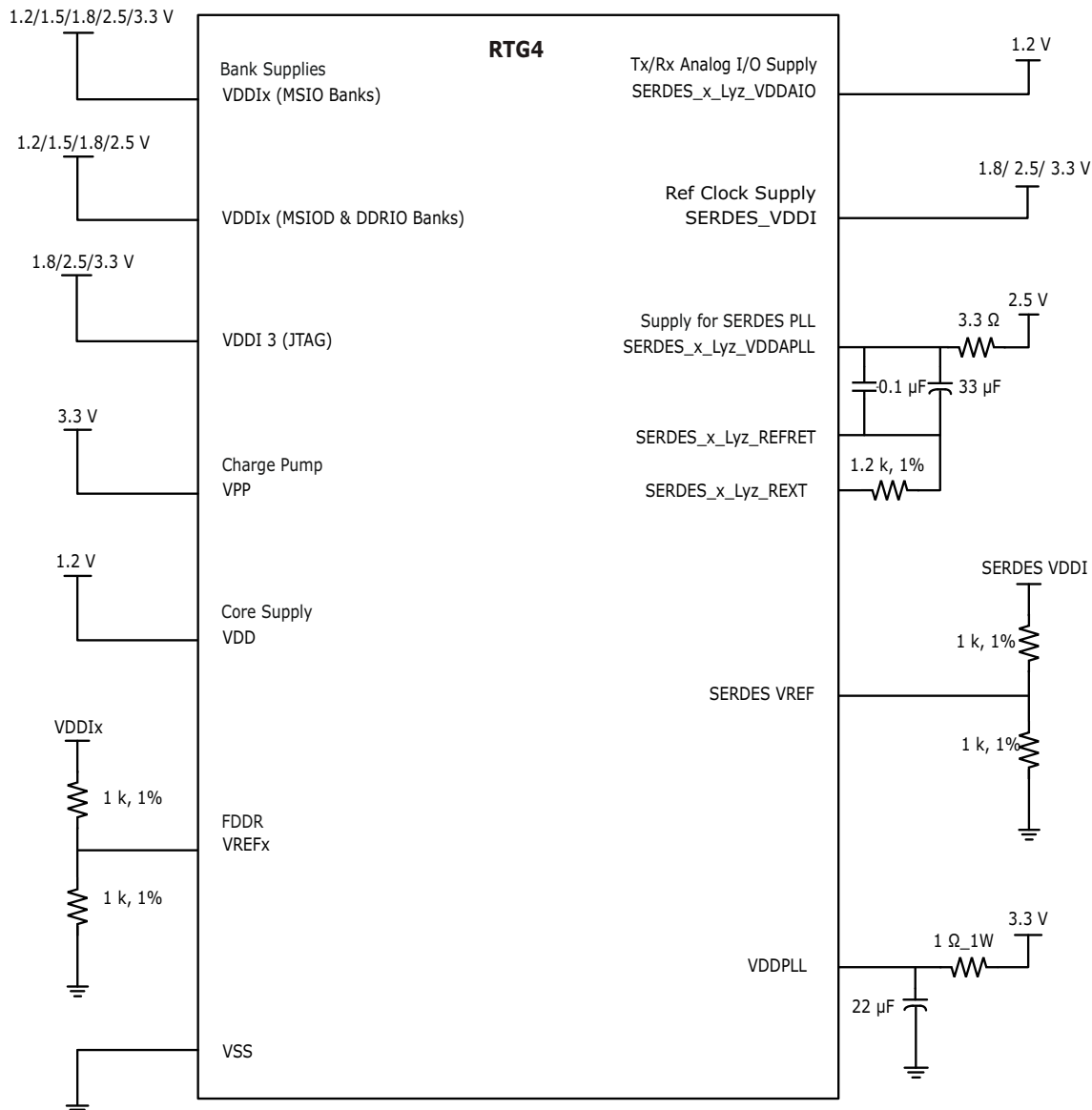
- [Power Supplies](#), page 5
- [Clocks](#), page 11
- [Reset Circuit](#), page 12
- [Device Programming](#), page 13
- [Device Programming](#), page 13
- [SerDes](#), page 15
- [SerDes](#), page 15
- [LPDDR, DDR2, and DDR3](#), page 17
- [SpaceWire Interface](#), page 22
- [Temperature Sensing](#), page 22
- [Additional Pins](#), page 23
- [Configuring Pins in Open Drain](#), page 24
- [Cold Sparring](#), page 24
- [Brownout Detection](#), page 25
- [Guidelines for PLL Jitter](#), page 26

Note: The board design guidelines provided in this document supersede the design of the RTG4 development board.

2.2 Power Supplies

The following figure illustrates typical power supply requirements, including PLL RC values, for RTG4 devices. For information on decoupling capacitors associated with individual power supplies, see [RTG4 Decoupling Capacitors](#), page 6.

Figure 1 • Power Supplies



Note: It is recommended to use 1Ω with a 1W resistor when all PLLs are used in the design. If a lesser number of PLLs are used, the wattage rating of the resistor (not the value) can be reduced. For reducing the wattage, estimate each PLL to consume ~12.5 mW of power.

Note: VDD and SERDES_x_Lyz_VDDAIO can use separate power supplies as long as they power up and down simultaneously.

Note: Each VDDPLL pin consumes 12.5 mW. Use a 1Ω-1W resistor when all 13 VDDPLL pins are used. Otherwise, calculate the resistor value based on the number of VDDPLL pins used.

For the device to operate successfully, power supplies must be free from unregulated spikes and the associated grounds must be free from noise. All voltages must be within the absolute maximum ratings provided in the [DS0131: RTG4 FPGA Datasheet](#).

For detailed description of various power supplies in an RTG4 device, see [DS0130: RTG4 FPGA Pin Descriptions](#).

2.2.1 Power Supply Flow

The following table lists the various power supplies required for RTG4 FPGAs.

Table 1 • Power Supplies in RTG4 Devices

Power Supply Name	Description
VDD ¹	DC core supply voltage
VPP	Power supply for charge pumps
VDDPLL	Power for eight PLLs, PLLs in SerDes PCIe/EPCS blocks, and FDDR PLLs
VDDIx	I/O bank supplies
VREFx	Reference voltage for DDR signals, powered through the corresponding bank supply (VDDIx).
SERDES_x_Lyz_VDDAIO ¹	TX/RX analog I/O voltage for SerDes lanes. Should be shorted to the device's core supply.
SERDES_x_Lyz_VDDAPLL	Analog power for SerDes TXPLL and CDRPLL
SERDES_VDDI	Power for SerDes reference clock receiver supply
SERDES_VREF	Supply for the SerDes reference clocks on the board use a single ended reference standard. Not used with differential clock signals.

- The VDDAIO supplies (SerDes) must be powered at the same voltage as the core VDD supply. These voltage supplies must be ramped up and down at the same time, and this condition is also applicable for the cold sparing feature.

2.2.2 RTG4 Decoupling Capacitors

The RTG4 Evaluation Kit contains commercial grade capacitors for decoupling. The following table lists the required number of PCB decoupling capacitors for RT4G150-CG1657 and LG1657 devices.

Table 2 • Power Supply Decoupling Capacitors for CG1657 and LG1657

Pin Name	External on Board Capacitors									
	Internal Capacitance	0.01 μ F	0.1 μ F	10 μ F	4.7 μ F	22 μ F	33 μ F	47 μ F	100 μ F	330 μ F
		Ceramic Caps					Tantalum Caps			
VDD	2 \times 0.18 μ F/6.3V	10	10					2		3
VDDI0	1 \times 0.18 μ F/6.3V	5						1		
VDDI1	1 \times 0.18 μ F/6.3V	2						1		
VDDI2	1 \times 0.18 μ F/6.3V	2						1		
VDDI3	1 \times 0.18 μ F/6.3V	1	1	1						
VDDI4	1 \times 0.18 μ F/6.3V	2						1		
VDDI5	1 \times 0.18 μ F/6.3V	2						1		
VDDI6	1 \times 0.18 μ F/6.3V	2						1		
VDDI7	1 \times 0.18 μ F/6.3V	2						1		

Table 2 • Power Supply Decoupling Capacitors for CG1657 and LG1657 (continued)

Pin Name	External on Board Capacitors									
	Internal Capacitance	0.01 μ F	0.1 μ F	10 μ F	4.7 μ F	22 μ F	33 μ F	47 μ F	100 μ F	330 μ F
		Ceramic Caps					Tantalum Caps			
VDDI8	1 \times 0.18 μ F/6.3V	2						1		
VDDI9	1 \times 0.18 μ F/6.3V	5						1		
VDDPLL	1 \times 0.18 μ F/6.3V	13	13	1		1				
VPP		5	4	1						
VREF0		1	1							
VREF9		1	1							
SERDES_VDDI		2	2	1						
SERDES_VREF			2							
SERDES_PCIE_0_L01_VDDA IO			6							
SERDES_PCIE_0_L23_VDDA IO			6	1						
SERDES_1_L01_VDDAIO			6	1						
SERDES_1_L23_VDDAIO			6	1						
SERDES_2_L01_VDDAIO			6	1						
SERDES_2_L23_VDDAIO			6	1						
SERDES_3_L01_VDDAIO			6	1						
SERDES_3_L23_VDDAIO			6	1						
SERDES_4_L01_VDDAIO			6	1						
SERDES_4_L23_VDDAIO			6	1						
SERDES_PCIE_5_L01_VDDA IO			6	1						
SERDES_PCIE_5_L23_VDDA IO			6	1						
SERDES_PCIE_0_L01_VDDA PLL			1				1			
SERDES_PCIE_0_L23_VDDA PLL			1				1			
SERDES_1_L01_VDDAPLL			1				1			
SERDES_1_L23_VDDAPLL			1				1			
SERDES_2_L01_VDDAPLL			1				1			
SERDES_2_L23_VDDAPLL			1				1			
SERDES_3_L01_VDDAPLL			1				1			
SERDES_3_L23_VDDAPLL			1				1			
SERDES_4_L01_VDDAPLL			1				1			
SERDES_4_L23_VDDAPLL			1				1			
SERDES_PCIE_5_L01_VDDA PLL			1				1			
SERDES_PCIE_5_L23_VDDA PLL			1				1			

The following table lists the recommended number of PCB decoupling capacitors for an RT4G150-CQ352 device.

Table 3 • Power Supply Decoupling Capacitors per Rail for CQ352

Pin Name	Internal Capacitance	External On Board Capacitors						
		0.01 μ F	0.1 μ F	4.7 μ F	10 μ F	47 μ F	100 μ F	330 μ F
		Ceramic Caps				Tantalum Caps		
VDD ¹	6 x 0.18 μ F 6.3V	10		2		2		3
VDDI3			2		1			
VDDI4	2 x 0.18 μ F 6.3V	2				1		
VDDI5	2 x 0.18 μ F 6.3V	2				1		
VDDI6	2 x 0.18 μ F 6.3V	2				1		
VDDAIO		1			1			
VDDPLL	4 x 0.18 μ F 6.3V				1			
VPP		1	1		1			

1. The CQ352 package has a much higher amount of package capacitors than CG1657 and LG1657 packages.

2.2.3 Power-up and Power-Down Sequence

Specific Power sequences need to be followed for the RTG4 family to address below issues.

- Hold PLLs in reset till the device is powered up completely and a valid reference clock has been provided.
- DEVRSTN should always be pulled up through a 10K resistor to VPP
- Mitigate IO glitches
 - The glitch may occur at power-up or power down. In either cases, the devices are not affected with any reliability issues. The IO glitch may occur at power-up or power-down after the device boots up/down. The device is not affected with any reliability issues nor do they cause any issues in user designs. See Note¹.
- The below recommendations mitigate any inrush currents.

Note: ¹There are some parasitic short term capacitive glitches which may occur regardless of any power sequence when the VDDI supplies power-up before the device boot-up. A maximum of 1V with a 0.4 ms wide glitch may be seen. These glitches cause no reliability issues to the device nor issues in the user designs as it is only seen during the early portion of the VDDI ramping process. For mitigation the user may add 1K pull-down resistor at each output for critical signals like resets and clocks. This will avoid any trigger or event on another device on the clock and reset signals. The resistor can be of any size and tolerance with a minimum voltage of 6V and a minimum power rating of 0.1W.

2.2.3.1 Power-Up Recommendations

- VDD -> VPP/VDDPLL -> Wait time of at least 51ms -> VDDIx (Any IO Bank)
 - No IO Banks are enabled until all of the IO banks of the RTG4 device have been powered up. All glitches would be mitigated with this sequence except the parasitic short term capacitive glitches.
 - VDD and VPP/VDDPLL may be powered up simultaneously
- VDD -> VPP/VDDPLL/VDDI_3.3V -> Wait time of at least 51ms -> VDDIx (except IO banks connected to 3.3V)
 - VPP, VDDPLL configured to 3.3V may be tied to VDDI Banks which are also configured to 3.3V
 - VDD and VPP/VDDPLL/VDDI_3.3V may also be powered up simultaneously
 - Use 1K ohm resistor pull down on critical IOs like clocks and resets on IO banks configured to VDDI_3.3V.
- Serdes_x_Lyz_VDDAIO and VDD should either be tied together to the same regulator and powered up/down together OR they can be sourced from different regulators but powered up/down simultaneously.

2.2.3.2 Power-Down Recommendations

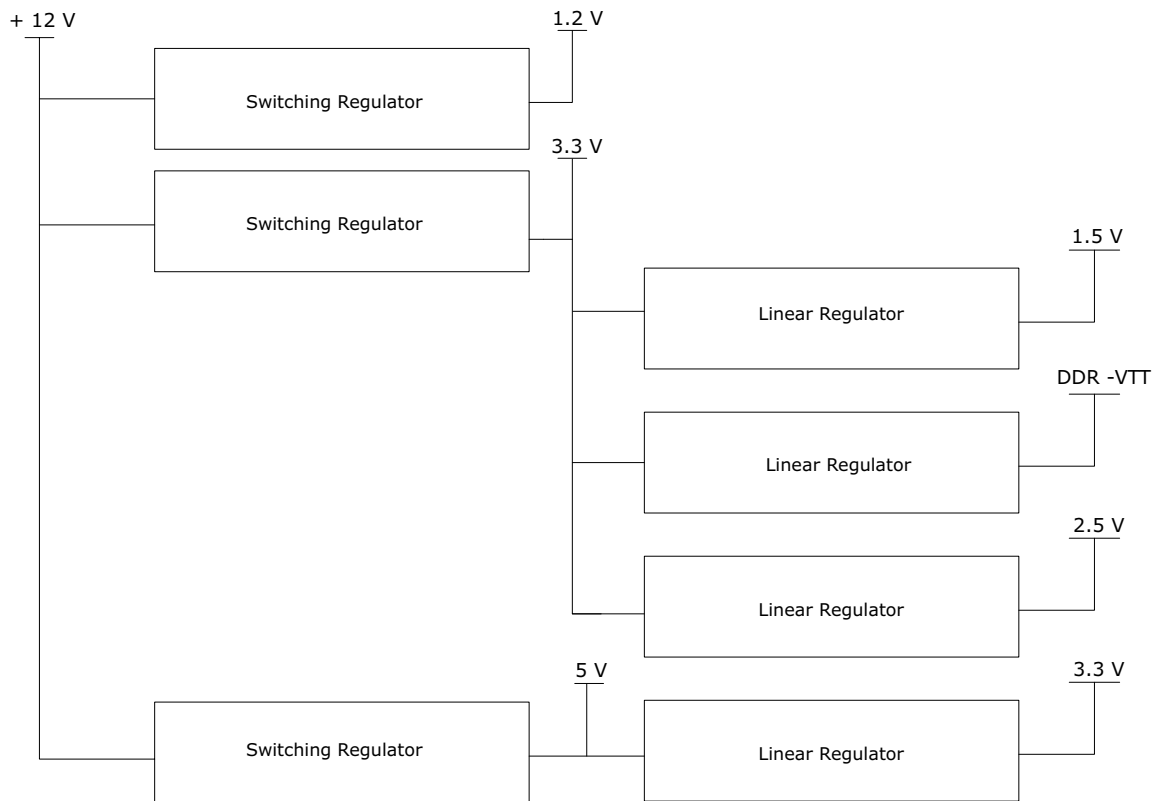
To mitigate IO glitches:

- Power down VPP-3.3V last after all other rails have been powered down
- If the user has other IO voltage rails at 3.3V in the design, such as 3.3V for JTAG/IO bank and the user needs to tie them together then the below sequence may be followed is as follows:
 - VDDIx (non-3.3V) -> VDD -> VPP, VDDPLL, VDDIx (3.3V)

In this case the user needs to add a 1K pull down resistor only on the 3.3V IO bank on all critical nets (like clocks and resets where output glitches may affect other devices driven by the RTG4 device). The resistor can be of any size and tolerance with a minimum voltage rating of 6V and a minimum power rating of 0.1W.

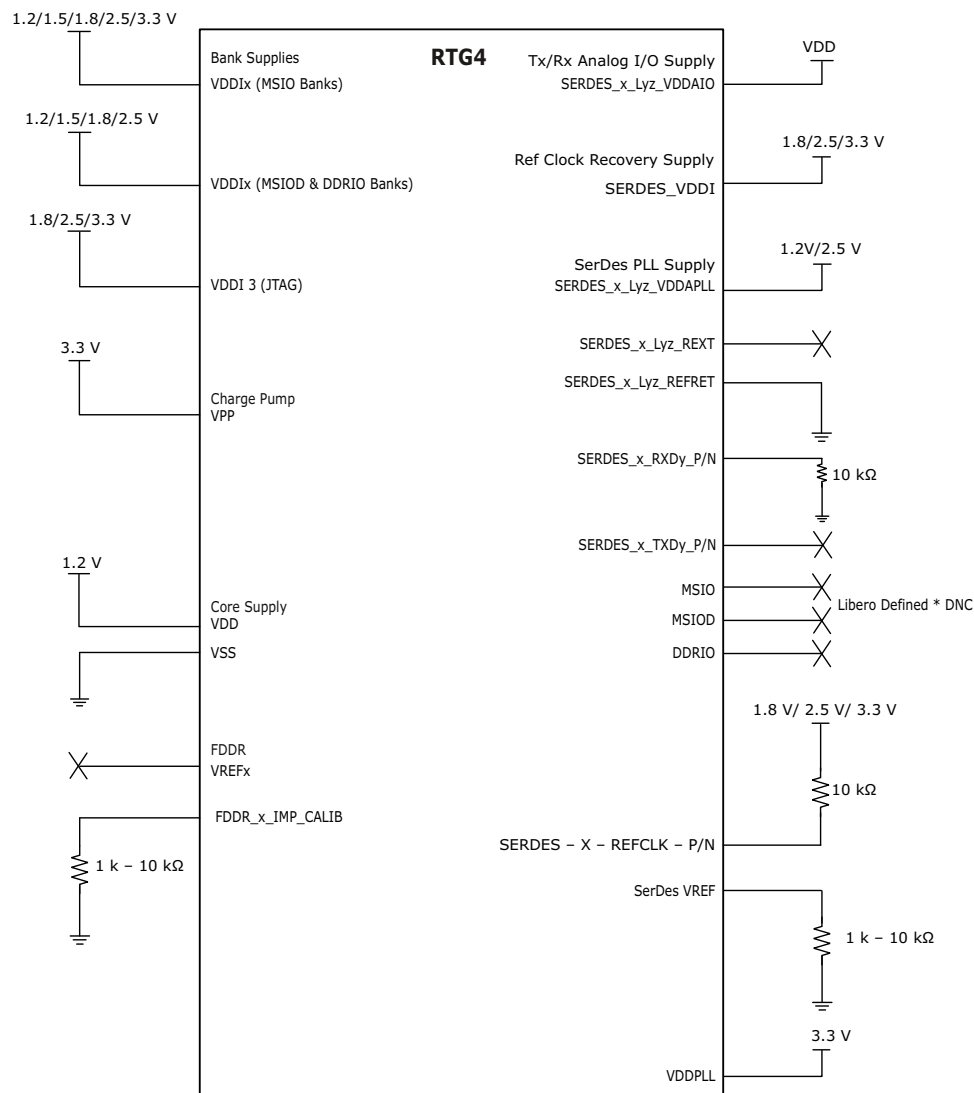
Serdes_x_Lyz_VDDAIO and VDD should either be tied together to the same regulator and powered up/down together OR they can be sourced from different regulators but powered up/down simultaneously. [Figure 2](#), page 10 shows a topology for generating the required power supplies from a single 12 V source.

These power-up and power-down recommendations should always be used, but if they are not followed more information as to the estimated chip behavior is found in the [AC439 Addendum](#) to this application note.

Figure 2 • Example Power Supply Topology

2.2.4 Unused Pin Configurations

Figure 3, page 11 shows the recommendations for unused pins.

Figure 3 • Recommendations for Unused Power Supply Pin Configurations

Note: The SERDES_x_RXD pin must be connected to VSS through a 10 kΩ pull-down resistor. If the board space is a constraint, you can group up to eight RXD pads to an external 10 kΩ pull-down resistor. Due to reliability issues, you must not connect RXD pads to VSS directly.

Note: Unused VREF pins can be DNC or connect to VSS.

Note: SERDES_VREF pins can also be tied together and pulled-down to GND via a 10K resistor instead of each pin tied to GND via a 10K resistor.

Note: Unused SERDES Quads, PLLs, and I/O Banks do not require any decoupling capacitors on VDDIO, VDDAIO, VDDAPLLs, and VDDPLL.

2.3 Clocks

RTG4 devices have one on-chip RC oscillator operating at 50 MHz.

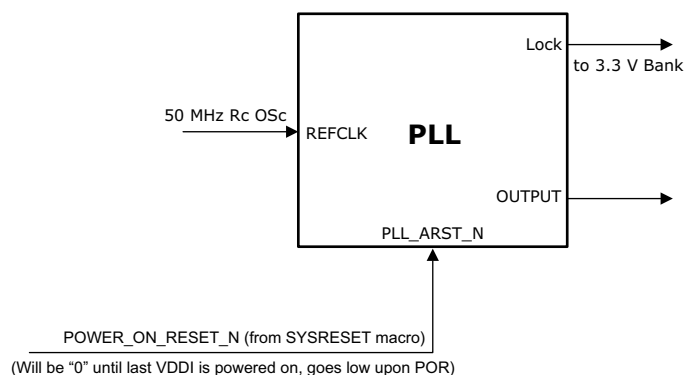
2.3.1 PLL Lock Monitoring

PLL_ARST_N, PLL_POWERDOWN_N are signals which are driven by user logic or from external source. In this example, PLL_ARST_N or PLL_POWERDOWN_N signals are driven to external I/O pins and connected to a push-button switch or to the user logic, based on the application. These signals are

used to recover the PLL lock, when it is lost because of radiation. The PLL LOCK status can be observed by connecting to the LED.

PLL Lock is an output with logic high polarity. During normal operation, the PLL high lock output indicates that the output clocks are valid. Monitoring this PLL output validates the PLL clock outputs. This signal can be used for internal monitoring in the user logic or can be driven to a LED for indication.

Figure 4 • PLL Lock Monitoring



PLL_ARST_N is used to reset the PLL core and asynchronously reset all the internal digital blocks and PLL outputs are driven low. PLL_POWERDOWN_N powers down the PLL for the lowest quiescent current and PLL outputs are driven low.

For more information about clocking in RTG4 devices, see the [UG0586: RTG4 FPGA Clocking Resources User Guide](#).

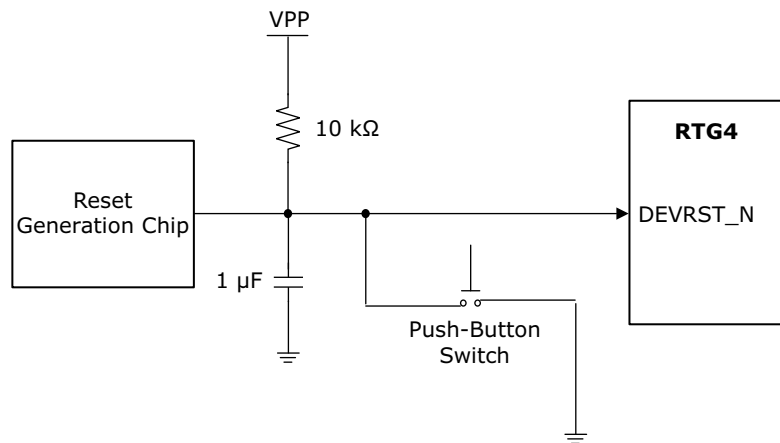
2.4 Reset Circuit

RTG4 devices have a dedicated asynchronous Schmitt-trigger reset input pin (DEVRST_N) with a maximum ramp time as specified in [DS0131: RTG4 FPGA Datasheet](#). This active-low signal should be asserted only when the device is unresponsive due to some unforeseen circumstances. It is not recommended to assert this pin during programming operation. Asserting the DEVRST_N signal tristates all user I/O and resets the system. De-asserting this signal enables the system controller to begin its startup sequence.

If unused, DEVRST_N must be pulled up to VPP through a 10 kΩ resistor. Adding a capacitor to ground on DEVRST_N prevents high-frequency noise and unwanted glitches that could reset the device. The DEVRST_N pad should not be pulled higher than the VPP supply.

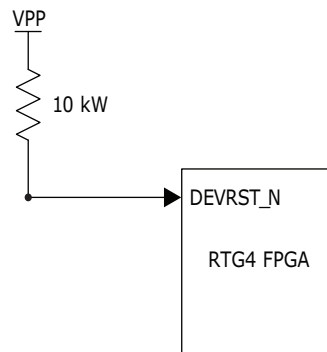
For more information about device reset, see the [DS0131: RTG4 FPGA Datasheet](#).

Figure 5 • Reset Circuit



If the reset device is not used, DEVRST_N must be pulled up to VPP through a 10 kΩ resistor, as shown in the following figure.

Figure 6 • Without Reset Circuit



2.4.1 Global Asynchronous Reset

Global asynchronous reset is a single resource. It can also be driven by an internal fabric signal. For more information, see [UG0741: RTG4 FPGA I/O User Guide](#).

2.5 Device Programming

The RTG4 device can be programmed through the dedicated JTAG interface.

2.5.1 JTAG Programming Mode

The RTG4 device supports programming through a dedicated JTAG port using the Libero SoC software or a standalone FlashPro software (FlashPro4 or FlashPro5), as shown in the following figure. The power supplies and the toggling of the JTAG signals must meet the specifications provided in the [DS0131: RTG4 FPGA Datasheet](#).

Proper signal integrity measures must be used to ensure that the power supplies and JTAG signals are free from noise. While programming in JTAG mode, all I/O (MSIO, MSIOD, and DDRIO) are controlled by boundary scan registers.

The JTAG interface is used for device programming and testing or for debugging instantiated soft processor firmware, as listed in the following table. JTAG I/Os are powered by the VDDI3 supply associated with the bank where the I/O reside.

Table 4 • JTAG Pins

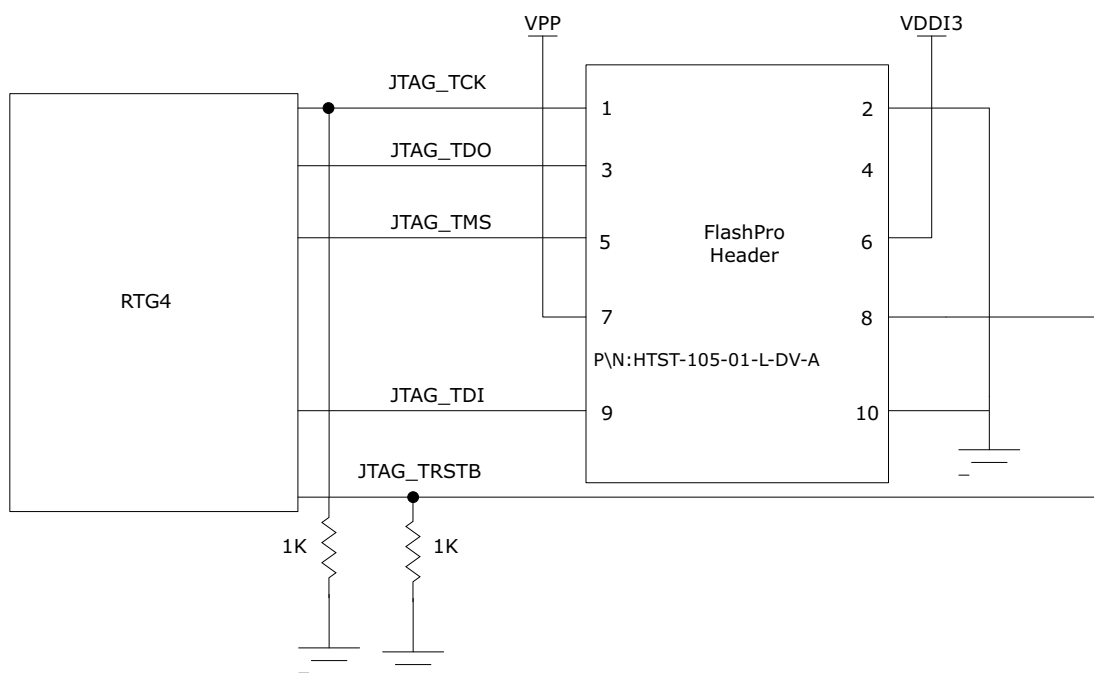
Pin Names	Direction	Weak Pull-up	Description
JTAG_TMS	Input	Yes	JTAG test mode select. In unused condition it is do not connect (DNC).
JTAG_TRSTB	Input	Yes	JTAG test reset.
JTAG_TDI	Input	Yes	JTAG test data in. In unused condition it is DNC.
JTAG_TCK	Input	No	JTAG test clock.
JTAG_TDO	Output	No	JTAG test data out. In unused condition, it is DNC.

Pin 6 and 7 of FlashPro header need to be connected to 3.3 V. All JTAG signals come under LVCMOS33.

JTAG pins should be connected as shown in the following figure.

Note: For unused JTAG pins, see the [Packaging Pin Assignment Table \(PPAT\)](#).

Figure 7 • JTAG Programming



Pin 6 and 7 must be routed with a thick trace because these are the power pins.

For detailed information on hardware connections for each programming mode, see the [UG0602: RTG4 FPGA Programming User Guide](#).

2.5.2 I/O State During Programming

I/Os are tristated and pulled high during programming by default. The I/O states during programming can be chosen as either tristate, low, high, or last known state.

If the RTG4 device is already programmed, the I/O must be held in previous state or tristate during programming. This applies to all I/O except the JTAG pins and the dedicated SPI pins. I/Os are tristated with weak pull up in a blank device, that is, factory shipped unprogrammed device. For more information about the state of I/Os, see the State of RTG4 Components During Programming section of [UG0602: RTG4 FPGA Programming User Guide](#).

2.5.2.1 Recommended Operating Conditions during Programming

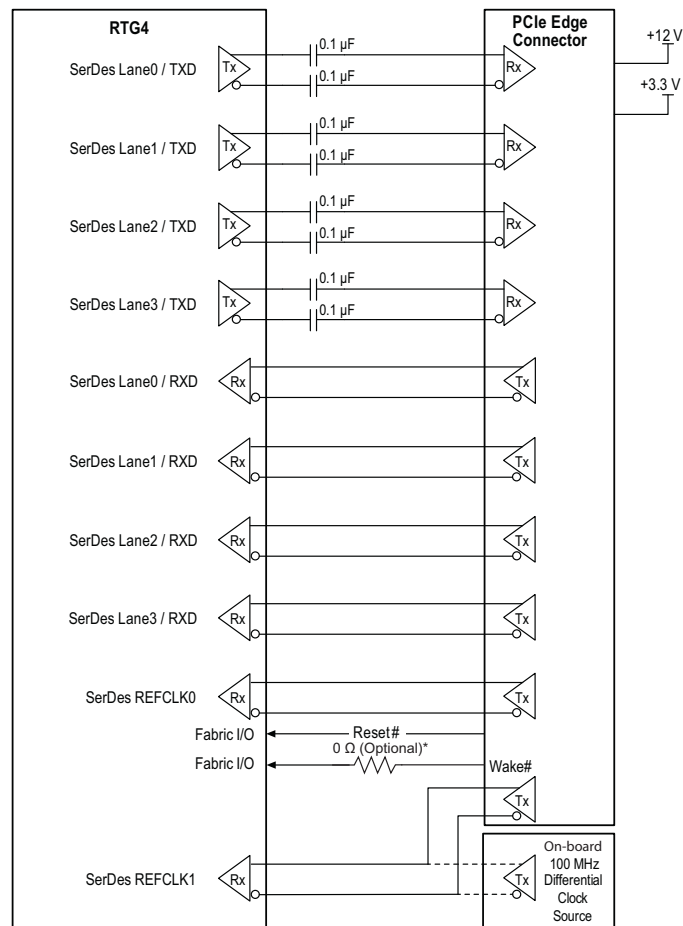
Follow the power-up guidelines mentioned in [Power Supplies](#), page 5.

2.6 SerDes

RT4G150-CG1657 device has six SerDes blocks (SERDES_PCIE_0, SERDES_1, SERDES_2, SERDES_3, SERDES_4, and SERDES_PCIE_5), each residing in a dedicated bank with the same name as the block that it contains. For more information, see [UG0567: RTG4 FPGA High-Speed Serial Interfaces User Guide](#).

2.6.1 PCI Express (PCIe)

PCIe is a point-to-point serial differential low-voltage interconnect supporting up to four channels. Each lane consists of two pairs of differential signals: a transmit pair, TXDy_P/N, and a receive pair, RXDy_P/N. Each signal has a 2.5 GHz embedded clock. The following figure illustrates the connectivity between the RTG4 SerDes interface and the PCIe edge connector.

Figure 8 • SerDes Schematics

2.6.2 AC Coupling

Each transmit channel of a PCIe lane must be AC coupled to allow detection. Capacitors used for AC coupling must be external to the device and large enough to avoid excessive low-frequency drops when the data signal contains a long string of consecutive identical bits.

For non-PCIe applications, the RTG4 device requires the receive inputs to be AC coupled to prevent common-mode mismatches between devices. Suitable values (for example, 0.1 μ F) for AC-coupling capacitors must be used to maximize link signal quality and must conform to the electrical specifications available in the [DS0131: RTG4 FPGA Datasheet](#).

Note: The AC coupling capacitors need to be placed close to the PCIe transmit pins, and the other protocols such as XAUI, SGMII, SRIO, and XGMII are as per the IEEE standards.

2.6.3 SerDes Reference Clock Requirements

For SerDes reference clock pins, external termination may be required depending on the I/O standard and SERDES_VDDI voltage selected. LVDS33 reference clock inputs require an external 200 Ω differential termination resistor. LVDS25 reference clocks may require external termination depending on the input common mode voltage at the RTG4 REFCLK input. Similarly, LVPECL reference clock inputs may require external termination to allow $V_{ID} \geq V_{ICM}$ at the reference clock receiver. For more information, see the specifications in [DS0131: RTG4 FPGA Datasheet](#).

The following are the requirements for the SerDes reference clock:

- Must be within the range of 100 MHz to 160 MHz.

- Must be within the tolerance range of the I/O standard.
- The input clock for PCIe is typically a 100-MHz reference clock provided by the host slot for an endpoint device through the PCIe connector of the motherboard. If two components connected through the PCIe bus use the same 100-MHz clock source, it is called common clock mode. In any other case, the PCIe device is in separated clock mode, where one component does not use a 100-MHz reference clock or uses a 100-MHz reference clock that does not have the same source and phase as the one used by the connected component.
- PCIe reference clocks typically require SERDES_VDDI to be 2.5 V and the RTG4 reference clock receiver is set to LVDS25 I/O standard. For more information, see [UG0567: RTG4 FPGA High Speed Serial Interfaces User Guide](#).

See the *PCI Express Base specification Rev 2.1* for detailed PHY specifications. Also, see the *PCIe Add-in Card Electro-Mechanical (CEM) specifications*.

2.6.4 PLL Filter

To achieve a reasonable level of long-term jitter, it is vital to supply the PLL with analog-grade power. Typically, an RC or RLC filter is used, where C is composed of multiple devices to achieve a wide spectrum of noise absorption. Although the circuit is simple, its effectiveness depends on the specific board layout requirements. See [Figure 1](#), page 5 for an illustration of a typical power supply connection.

- The DC series resistance of this filter should be limited. Microsemi recommends limiting the voltage drop across this device to less than 5% under worst-case conditions.
- Place a main ceramic or tantalum capacitor (see [Figure 1](#), page 5) in the filter design to achieve a good low-frequency cut-off. At least one low ESL and low ESR capacitor need to be placed in parallel to enable the filter to maintain its attenuation through moderately high frequencies.
- For the SerDes block, SERDES_x_Lyz_REFRET serves as the local on-chip ground return path for SERDES_x_Lyz_VDDAPLL. Therefore, the external board ground must not be short with SERDES_x_Lyz_REFRET under any circumstances.

See [Figure 1](#), page 5 for SerDes analog power connections. A high-precision 1.2 K_1% resistor is required for the external reference resistor connected between SERDES_x_Lyz_REXT and SERDES_x_Lyz_REFRET.

2.7 LPDDR, DDR2, and DDR3

DDRIO is a multi-standard I/O buffer optimized for LPDDR, DDR2, and DDR3 performance. All DDRIO can be configured as differential I/O or two single-ended I/O. DDRIO can be connected to the respective DDR subsystem PHY or used as user I/O.

The following table lists the differences between LPDDR, DDR2, and DDR3 interfaces.

Table 5 • LPDDR/DDR2/DDR3 Parameters

Parameter	LPDDR	DDR2	DDR3
VDDQ	1.8 V	1.8 V	1.5 V
VTT, VREF		0.9 V	0.75 V
Clock, address, and command (CAC) layout	Asymmetrical tree branch	Symmetrical tree branch	Daisy chained (fly-by)
Data strobe	Single-ended	Differential	Differential
ODT	None	Static	Dynamic
Match Addr/CMD/Ctrl to clock tightly	Yes	Yes	Yes
Match DQ/DM/DQS tightly	Yes	Yes	Yes
Match DQS to clock loosely	Yes	Yes	Not required
Interface	LVC MOS_18	SSTL_18	SSTL_15
Impedance calibration	Optional	150_1%	240_1%

Note: Using an impedance calibration resistor is a must for DDR2 and DDR3 memory interfaces, though optional for LPDDR memory. If an impedance calibration resistor is not set for DDR2 and DDR3 interfaces, the RTG4 device will not initialize.

A major difference between DDR2 and DDR3 SDRAM is the use of data leveling. To improve signal integrity and support higher frequency operations, a fly-by termination scheme is used with the clock, command, and address bus signals. Fly-by termination reduces simultaneous switching noise by deliberately causing flight-time skew between the data strobes at every DDR3 chip. This requires controllers to compensate for this skew by adjusting the timing per byte lane.

For more information about DDR memories, refer to the following documents:

- *JESD209B-JEDEC Standard—Low Power Double Data Rate (LPDDR) SDRAM Standard*
- *JESD79-2F-JEDEC Standard—DDR2 SDRAM Specification*
- *JESD79-3F-JEDEC Standard—DDR3 SDRAM Standard*

2.7.1 FDDR Impedance Calibration

The FDDR has a DDRIO calibration block. DDRIO can use fixed impedance calibration for different drive strengths, and these values can be programmed using the Libero SoC software for the selected I/O standard. If DDR interface is not used, impedance calibration pin can be left floating or pulled to VSS through a 1 k Ω resistor.

Before initiating DDRIO impedance calibration, either of the following must be done:

- Power sequencing, where the DDRIO bank VDDI_x supply must be up and stable before VDD core supply.
- DDRIO recalibration through the APB interface after VDDI_x (DDRIO banks) and VDD are up and stable.

For more information about impedance calibration, see the [UG0741: RTG4 FPGA I/O User Guide](#). For information about restrictions applicable to FDDR use models, see the [RTG4 CG1657 Package Pin Assignment Table](#).

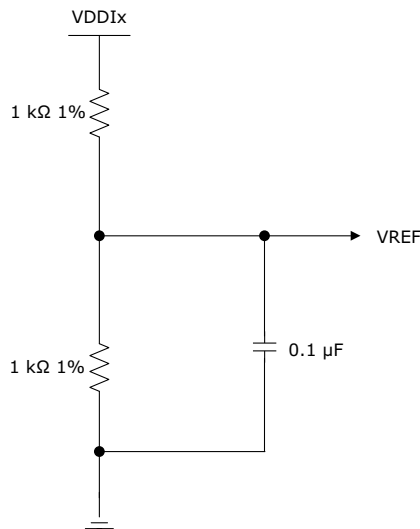
2.7.2 VREF Power

Voltage reference (VREF) is a low-power reference voltage equal to half of VDDQ. It must also be equal to $V_{TT} \pm 40$ mV.

The following are the guidelines for connecting VREF power:

- For light loads (less than four DDR components), connect VDDQ to VSSQ through a simple resistor divider composed of two equivalent 1% 1 k Ω resistors, as shown in the following figure.
- Generate a local VREF at every device, rather than generating a single VREF with one divider and routing it from the controller to the memory devices.
- Decouple at each device or connector to minimize noise.
- If more than four DDR devices are used in a design, use a separate voltage regulator to generate the reference voltage for DDR memory.

Note: Use discrete resistors, not a resistor pack, to generate VREF.

Figure 9 • VREF Generation

2.7.3 VTT Power

VTT is memory bus termination voltage. To maintain noise margins, VTT must be equal to VDDQ/2, with an accuracy of $\pm 3\%$. VTT terminates command and address signals to VDDQ/2 using a parallel resistor (RT) tied to a low-impedance source.

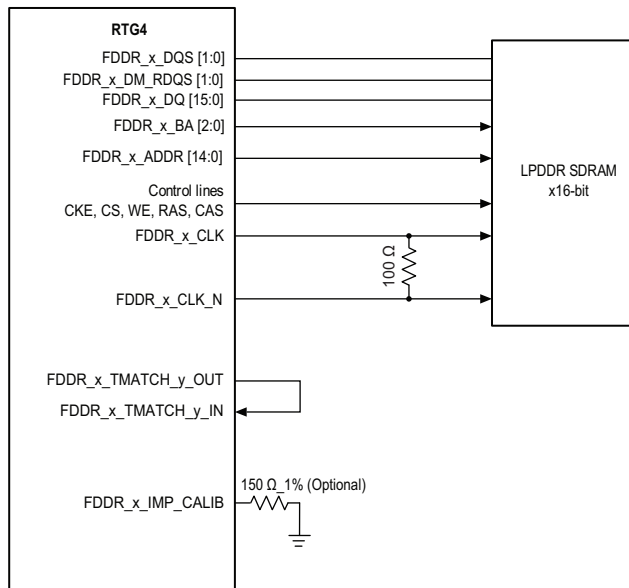
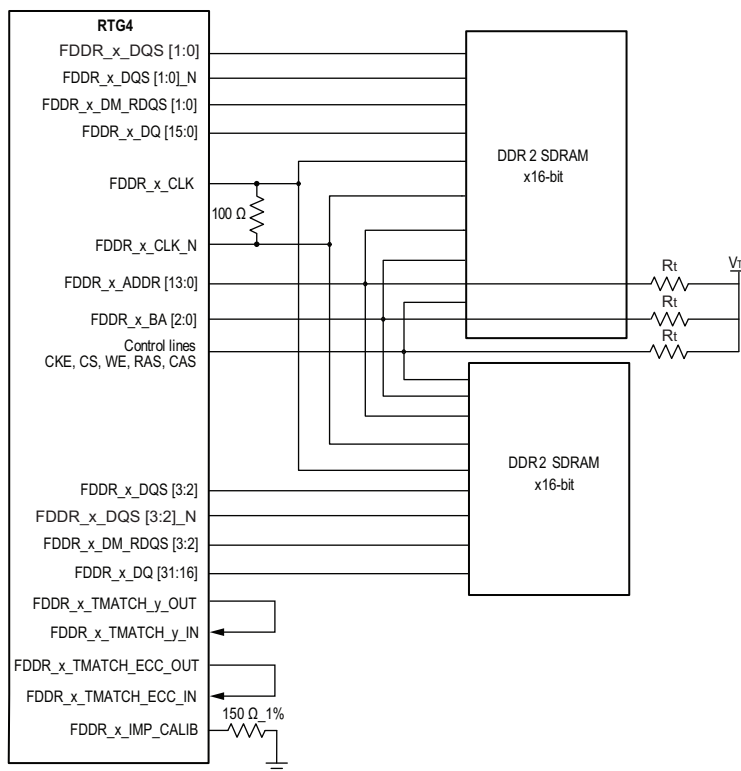
VTT does not terminate any DDR clock pairs. Rather, the xDDR_CLK and xDDR_CLK_N termination consists of a parallel 100-120 Ω resistor between the two lines.

- VTT islands require at least two additional decoupling capacitors (4-7 μ F).
- Each data line is connected to VTT with relatively low impedance. This supply must be extremely stable. Any noise on this supply directly affects the data lines.
- Sufficient bulk and bypass capacitance must be provided to keep this supply at VDDQ/2. VREF power must not be derived from VTT, but must be derived from VDDQ with a 1% or better resistor divider.

2.7.4 LPDDR and DDR2 Design

This document assumes that the designer is familiar with the specifications and basic electrical operation of the LPDDR/DDR2 interface. Data bus, data strobe, and data mask (byte enable) signals are point-to-point, whereas all other address, control, and clock signals are not.

The following figures show the connectivity of the RTG4 LPDDR interface and a 32-bit DDR2 interface respectively.

Figure 10 • LPDDR Interface**Figure 11 • DDR2 Interface**

With short traces, the address, control, and command signals may not require both parallel (RT) and series (RS) termination. In a worst-case scenario, a small series resistor (RS) of about $10\ \Omega$ or less is required. The series termination is not used for impedance matching, but for dampening the signals.

Note: To ensure correct signal delay compensation, short the TMATCH_OUT to TMATCH_IN pins under the FPGA pins.

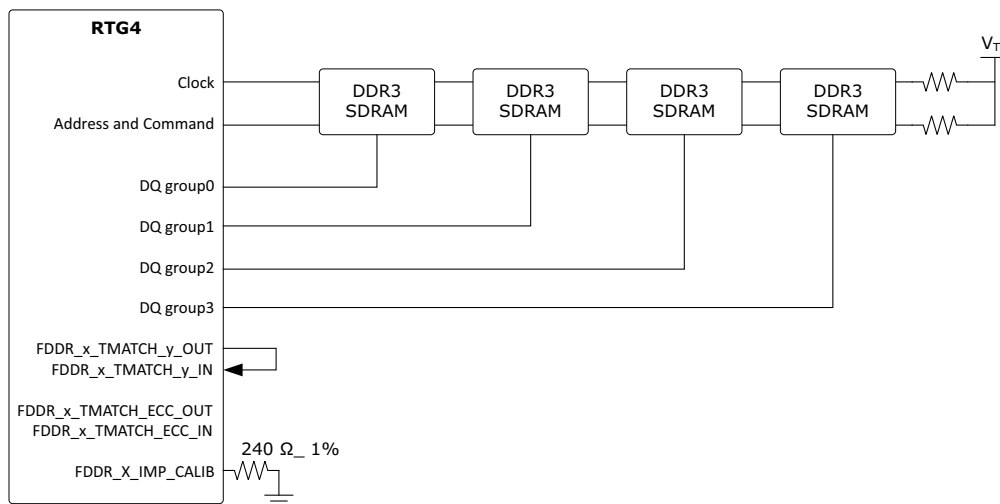
2.7.5 DDR3 Guidelines

The following are the guidelines for connecting to DDR3 memory:

- DDR3 data nets have dynamic ODT built in the controller and SDRAM. For configurations with 40, 60, and 140 Ω . terminations, VTT pull-up is not required.
- Characteristic impedance (Z_0) is typically 50 Ω , and Z_{diff} (differential) is 100 Ω .

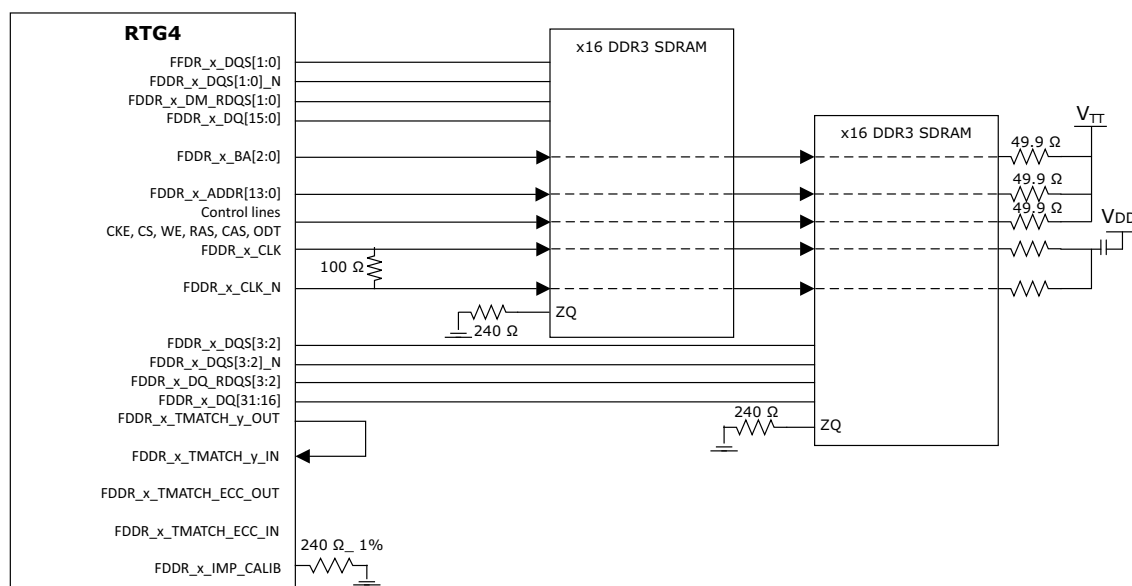
DDR3 interfacing with RTG4 devices for 8-bit interface is shown in the following figure.

Figure 12 • 8-Bit DDR3 Interface



For more information, see [DDR3 Layout Guidelines](#), page 42.

Figure 13 • 16-Bit DDR3 Interface



Note: When ECC bits are used in design, the ECC_TMATCH_OUT and IN signals should be shorted. In other conditions, there is no need to short them.

Note: To ensure correct signal delay compensation, short the TMATCH_OUT to TMATCH_IN pins under the FPGA pins.

2.8 SpaceWire Interface

The RTG4 device has 16 built-in RX clock recovery blocks with the jitter required for SpaceWire applications. SpaceWire links operate from 2 to 400 Mbps over a full-duplex, point-to-point serial link. SpaceWire uses a data-strobe (DS)-encoding scheme that encodes the transmission clock and data from the transmitter into data (D) and strobe (S). The clock can then be recovered at the receiver end by simply XORing the data (D) and strobe (S) lines together. SpaceWire uses low-voltage differential signaling (LVDS) for the D and S signals. LVDS employs balanced signals to provide very high-speed interconnection using a low-voltage swing (350 mV typical). The two dedicated D and S input pads can be configured as either single-ended or differential.

The optional ODT capability within the FPGA I/O provides good signal integrity without any external resistors on the PCB. If ODT is not used, external termination resistors (100 Ω) may be required to compensate for the unwanted impedance mismatches.

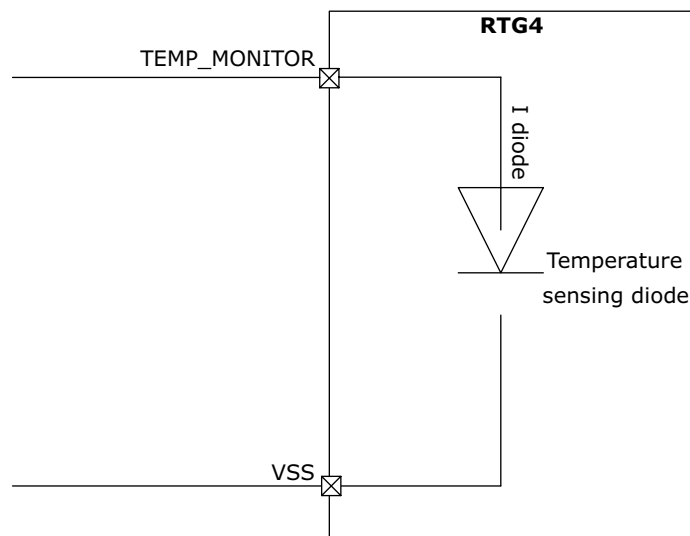
Note: Four of the 16 SpaceWire clock and data recovery circuits use DDRIO pins that are not capable of using the LVDS I/O standard.

2.9 Temperature Sensing

A temperature sensing diode is located internally in the RTG4 device, as shown in the following figure. It acts as an internal thermometer providing the voltage drop (VBE), based on which the temperature (T_J) can be calculated.

The temperature sensing diode has a dedicated input pin, TEMP_MONITOR, connected to the anode of the diode. The cathode of the diode is connected to VSS of the die.

Figure 14 • RTG4 Temperature Sensing



Measure the temperature using the following steps:

1. With no power supplied to the RTG4 device, apply a known current ($I_{\text{diode}} = 100 \mu\text{A}$) at a known temperature to the TEMP_MONITOR pin.
2. Measure the temperature at two temperatures. For example, 0 °C and 125 °C.
3. With power supplied to the RTG4 device, the diode measures the die temperature. This is the actual application of the diode. To know more information about TEMP_MONITOR and VSS pins, see the schematic in [RTG4 Development Kit Board References](#).
4. Measure the VBE between the TEMP_MONITOR pin and the VSS pins. Take two initial VBE measurements at two known temperatures to calculate the slope, m .
5. Determine the junction temperature (T_J) during operation using the equation:

$$T_J = m \times V_{BE} + T_0$$

where,

$$m = (T_{J2} - T_{J1}) / (V_{BE2} - V_{BE1})$$

$$T_0 = T_{J1} - m \times V_{BE1}$$

The following table lists the example temperature calculations.

Table 6 • Example Temperature (T_J) Calculation

Known Current (I Diode)	Known Temperature	V _{BE}	m	T ₀	T _J
200 μA	125	0.63936	-735.25	595.09	125.00056
200 μA	0	0.80937	-735.25	595.09	0.0007075

Note: When the Temp_Monitor pin is not used, it can either be connected to VSS or left floating.

2.10 Additional Pins

RTG4 devices have the following additional (special) pins.

Table 7 • Special Pins

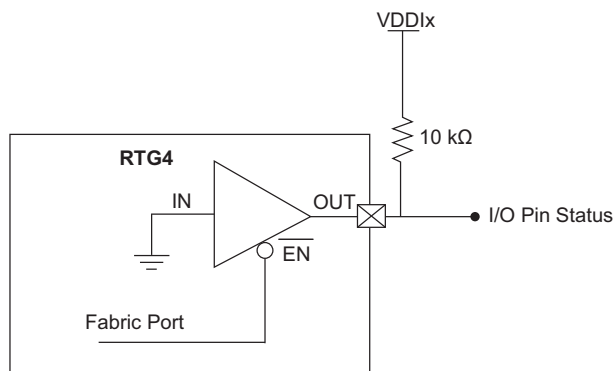
Pin Name	Description
NC	No connect pin. Indicates the pin is not connected to circuitry within the device. NC pins can be driven to any voltage or can be left floating with no effect on the operation of the device.
DNC	Do not connect pin. DNC must not be connected to any signals on the PCB. DNC pins must be left unconnected.
PROBE_CAPTURE ¹	Specifies an internal signal for probing (oscilloscope-like feature). The two live probe I/O cells function as either of the following: - Live probe - User I/O (MSIO) If not used for probing or as user I/O, must be connected to VSS through a 10 kΩ resistor.
PROBE_READ_DATA	

1. PROBE_CAPTURE feature is not available in SmartDebug software.

2.11 Configuring Pins in Open Drain

To configure fabric pins in open-drain mode, the input pin of the tristate buffer must be tied low, and the enable port of the buffer must be driven from the user logic through the fabric port, as shown in the following figure.

Figure 15 • Configure Pins in Open Drain



The following table provides the truth table of configuring pins in open-drain mode.

Table 8 • Truth Table

Buffer Enable Port	Buffer In Port	Buffer Out Port
0 (low)	0 (low)	0 (low)
1 (high)	0 (low)	VDDIx

2.12 Cold Sparing

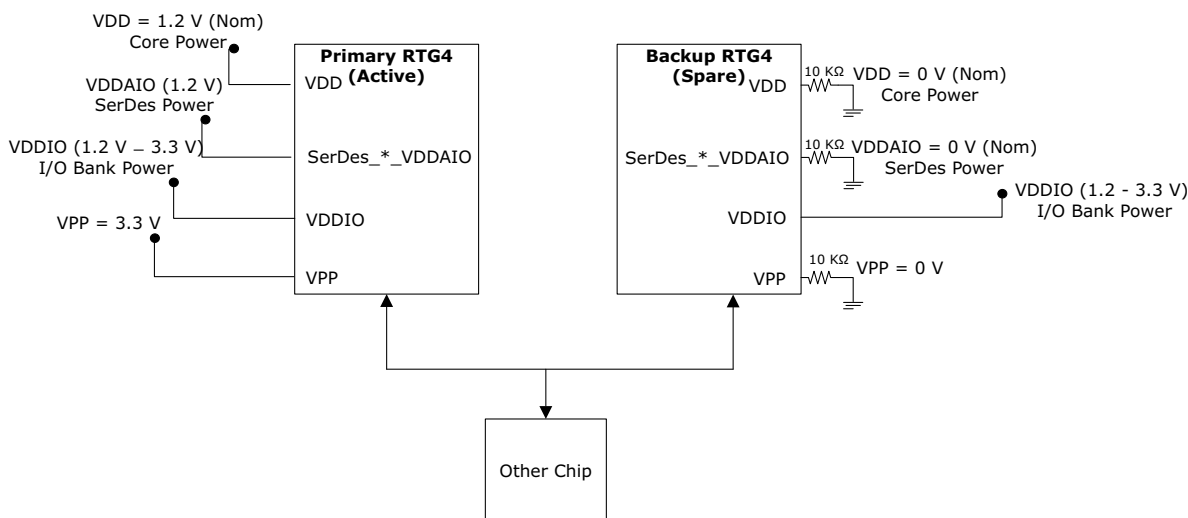
In cold-sparing applications, voltage can be applied to device I/Os before and during power-up. RTG4 fabric I/Os do not inherently support being driven before the I/O bank is powered-up. If the system requires a primary and redundant RTG4 device connected in parallel, as shown in [Figure 16](#), page 25, the following strategies can be applied.

- The system board integrates two parallel RTG4 devices on the board with shared or common I/O connections.
- The primary RTG4 device has its core such as VDD and SerDes VDDAIO powered and fully functional until a point is reached when swap of devices is determined to be necessary.
- The backup (spare) RTG4 device has its I/O banks powered and fabric core unpowered to prevent I/O leakage through the internal ESD diodes. The backup (spare) RTG4 VPP, fabric core, and SerDes supplies are unpowered to establish low power and a protected state.
- At any point, the primary and backup devices may be swapped by powering down VPP core, VDD, and SerDes VDDAIO of the primary RTG4 device, and by powering up VPP core, VDD, and SerDes VDDAIO of the backup RTG4 device and going through the device configuration sequence.
- The parts in primary and backup devices are identical.
- Only one of the two devices may be active at one time.
- Core VDD high activates the device and low de-activates the device.
- The inactive device must have VPP, VDD, and SerDes VDDAIO tied to the ground through 10 kΩ resistors and must not be floating.
- All active bank VDDIO supplies must be powered on the inactive device.
- Cold sparing is supported for a single device.
- SERDES RX pins support cold sparing only when AC coupled SEDRES TX pins are used.
- Electrical levels of SERDES RX pins should not exceed the voltage levels recommended in the datasheet for powered and unpowered devices, only AC coupling must be used for an unpowered device.

The advantages of this primary and redundant RTG4 device configuration are as follows:

- Driving a SERDES RX lane on an unpowered RTG4 from a SERDES TX lane on a powered RTG4 is allowed.
- The device can be powered up in any sequence. Specific power supply sequencing is not required.
- The backup (spare) device is in inactive mode.
- All banks with active I/Os must be powered.
- The I/O buffers of the backup spare device are disabled but powered.
- As per the strategy described in preceding steps and shown in the following figure, excess device leakage does not occur in the backup (spare) device.

Figure 16 • Primary and Redundant (Spare) Device Configuration



The backup RTG4 device functions as a replacement for the primary device. The following table lists the pin names and the board tie-off conditions for the spare device.

Table 9 • Spare Device Board Tie-Off

Supply	Spare Device Board Tie-Off	Description
VDD	10 K Ω to VSS	Low voltage core power
VDDPLL	Supplied or 10 K Ω to VSS	PLL power
VDDI3	Supplied	Power for JTAG I/Os
VPP	10 K Ω to VSS	Power for the programming blocks. Power for the programming analog blocks.
SERDES_*_VDDAIO	10 K Ω to VSS	SERDES analog supplies
SERDES_*_VDDAPLL	Supplied or 10 K Ω to VSS	SERDES PLL supplies
SERDES_VDDI	Supplied	Power for SerDes RefClk receiver
VDDIO ¹	Supplied or 10 K Ω to VSS	I/O power
VREF*	10 K Ω to VSS	FDDR voltage reference pins
SERDES_VREF	10 K Ω to VSS	All SerDes RefClk receivers voltage reference pin

1. Only the banks with inputs being driven must be powered-up.

2.13 Brownout Detection

RTG4 functionality is guaranteed only if VDD is above the recommended voltage level specified in the data sheet. Brownout occurs when VDD drops below the minimum recommended operating voltage. As

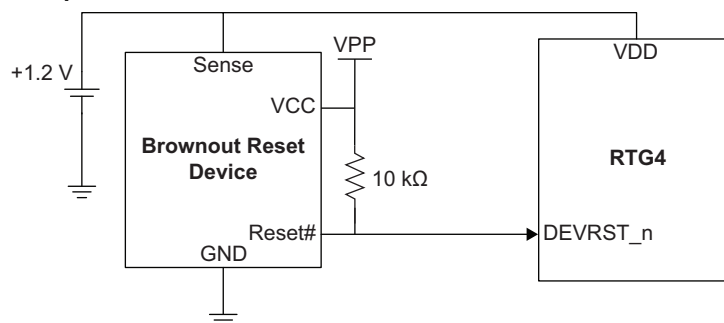
a result, it is not possible to ensure proper or predictable device operation. The design may continue to malfunction even after the supply is brought back to the recommended values, as parts of the device may have lost functionality during brownout. The VDD supply must be protected by a brownout detection (BOD) circuit.

To recover from VDD brownout, the device must either be power-cycled or an external BOD circuit must be used to reset the device for correct operation. The recommended guideline for the threshold voltage of BOD is a minimum of 1.14 V. The BOD circuit must be designed such that if the VDD falls below 1.14 V, the device is held in power-down mode through the DEVRST_N pin.

Note: BOD must be implemented through a standalone circuit or included as part of the power management circuitry.

The RTG4 device does not have a built-in BOD circuitry, but an external BOD circuitry can be implemented, as shown in the following figure.

Figure 17 • BOD Circuit Implementation



The BOD device must have an open-drain output to connect to VPP through a 10 kΩ resistor externally. During power-on, the brownout reset keeps the device powered down until the supply voltage reaches the threshold voltage. Thereafter, the brownout reset device monitors VDD and keeps RESET# output active as long as VDD remains below the threshold voltage. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset.

The delay time is in milliseconds and it starts after the VDD has risen above the threshold voltage. When the supply voltage drops below the threshold voltage, the output becomes active (low) again.

2.14 Guidelines for PLL Jitter

Follow these guidelines to keep the PLL jitter measurements within the target limits:

- Use strong output drivers with low jitter characteristics. Differential output drivers, SSTL/HSTL single ended terminated standard drivers, or LVCMOS33/25/18 drivers with maximum drive minimize impact of jitter in measurements.
- Do not place the reference input PAD/package trace near the output PAD/package trace.
- Use a baseline jitter measurement with PLL in bypass, and subtract this base line from all PLL jitter measurements.

2.15 Simultaneous Switching Noise GND Bounce and VDDI Bounce

When multiple output drivers switch simultaneously, they induce a voltage drop in the chip/package power distribution. The simultaneous switching momentarily raises the ground voltage within the device, relative to the system ground. This apparent shift in the ground potential to a non-zero value is known as simultaneous switching noise (SSN) or, more commonly, ground bounce.

The ground bounce voltage is related to the inductance present between the device ground and the system ground, and the amount of current sunk by each output. It is given in the following equation:

$$V = L \times (di)/(dt)$$

An I/O switching from high to low or low to high is actually discharging or charging the capacitor that loads the I/O. The resulting value of di/dt is cumulative and increases with the number of simultaneously switching outputs (SSOs). Therefore, the higher di/dt , the higher the ground bounce amplitude. For more information, see, [AC263: Simultaneous Switching Noise and Signal Integrity App Note](#).

3 Layout Guidelines for RTG4-Based Board Design

This chapter provides guidelines for the hardware board layout that incorporates RTG4 devices. Good Board layout practices are required to achieve the expected performance from the printed circuit boards (PCB) and RTG4 devices. They help achieve high quality and reliable results such as low noise levels, signal integrity, impedance, and power requirements. The guidelines mentioned in this document act as a supplement to the standard board-level layout practices.

Note: A good understanding of the RTG4 chip, experienced in digital and analog board layout, knowledge of transmission line theory, and signal integrity are essential to be able to follow the guidelines in this chapter. For more information about designing RTG4-based boards, see the [Board Design Guidelines for RTG4 FPGAs](#), page 4.

Disclaimer: The target impedance calculated with respect to the development board. The target impedance depends on the logic implemented on RTG4, so Microsemi recommends calculating the target impedance of the board. The simulations show the impedance that meets the target impedance of the development board. The RTG4 FPGA layout recommendations are based on the development board. The plane shapes given in this document are with reference to the [UG0617: RTG4 FPGA Development Kit User Guide](#).

3.1 Power Supply

In power supply design, it is important to know the target impedance of power planes, which varies depending on the design. This helps in planning the required number of decoupling capacitors based on the target impedance. The number of decoupling capacitors varies based on the design.

Complex FPGA designs have increasing amounts of current transients switching across the power bus. Simultaneously switching outputs (SSO) contribute to a major share of instantaneous current issues. Decoupling is necessary to prevent the instantaneous currents. Decoupling is only effective when inductance is minimized. Low inductance decoupling provides localized high frequency energy to decouple noise from the switching currents of the device power bus. This is most effective when capacitors are in close proximity to the device. Some of these high frequency capacitors are required to be placed directly by the FPGA.

Target impedance is calculated based on [EQ 1](#):

$$Z_{\text{Min}} = \% \text{ Ripple} \times \frac{V_{\text{supply}}}{I_{\text{trans}}}$$

EQ 1

Where,

V_{supply}: Supply voltage of the power plane

% Ripple: Percentage of ripples allowed on the power plane; see the [DS0131: RTG4 FPGA Datasheet](#) for details.

I_{trans}: Transient current drawn on the power plane. Generally, transient current is half of the maximum current, which is taken from the power calculator sheet.

Z_{min}: Target impedance of the plane

Subsequent sections display simulation results based on target impedance calculated using [EQ 1](#). Microsemi strongly recommends calculating the target impedance and performing simulations for the impedance profile of the power plane. These simulations help in optimizing the decoupling capacitors to reduce the production cost and have optimal placement. The plane shapes vary depending on the design. For simulation topology, see [Appendix: Power Integrity Simulation Topology](#), page 55.

RTG4 FPGA power supplies are majorly classified as:

- Core power supply
- I/O power supply
- Serializer/Deserializer (SerDes) power supply
- Double data rate (DDR) power supply
- Phase-locked Loop (PLL) power supply

3.2 Core Supply

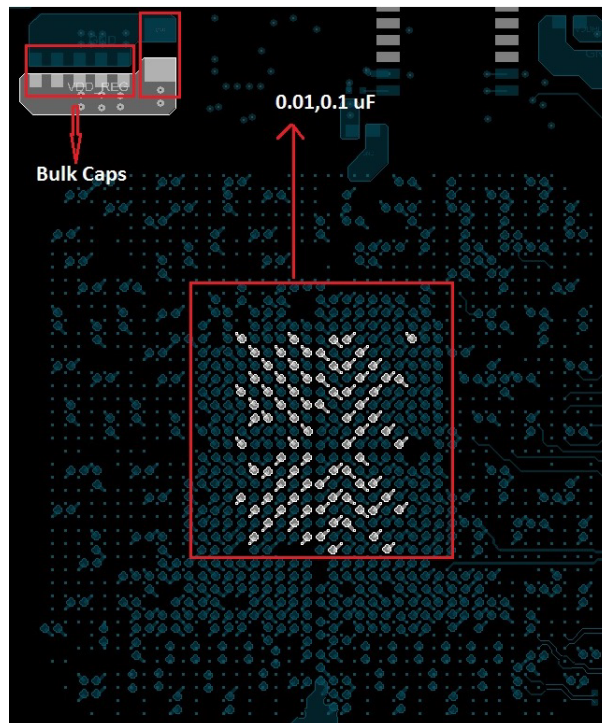
The core power supply must have low-noise and low-ripple voltages, as prescribed in the datasheet. Proper care should be taken while designing the power supply (VDD) for core. Optimal placement of decoupling capacitors and the plane geometry greatly influences the power supply distribution for RTG4 devices.

3.2.1 Component Placement

Component placement for capacitors for VDD plane are as follows:

- The bulk capacitors should be placed near the RTG4 device.
 - The bypass capacitors should be placed near, or if possible, on the periphery of the device.
- A sample placement of capacitors is shown in the following figure.

Figure 18 • Placement of Capacitors for VDD Plane



- All decoupling capacitors should be as small as possible as they are required to be mounted on back side of the board. There can be sharing of via for ground pins and power pins if it is difficult to accommodate the capacitors on back side of the board. Microsemi recommends keeping the capacitor pad close to corresponding via. The footprint of capacitors should be optimized based on size of capacitor to accommodate all the capacitors. Users need to consult assembly house for the change in footprint.

3.2.2 Plane Layout

Microsemi recommends using the VDD plane, as shown in the following figure.

Note: There are many ways the plane can be routed. The goal is to have a dedicated, low-impedance plane.

Figure 19 • VDD Plane



3.2.3 Simulations

The effect of the decoupling capacitors can be visualized through power integrity simulations. The target impedance of the VDD is calculated as 40 mΩ, based on the following values (see [EQ 1](#)):

- $V_{SUPPLY} = 1.2\text{ V}$
- $I_{trans} = 1.5\text{ A}$
- Ripple = 5%

It shows that the capacitors are used to improve the impedance profile over the bandwidth. Good coupling between the planes can be achieved by placing the power plane and ground plane in adjacent layers. After placing all capacitors, the impedance of the VDD plane impedance profile improves over the frequency range. The simulation results shown in this document are done in Sigrity PowerSI tool. For more information about using this tool and how to do the simulation, see the Sigrity PowerSI tutorial.

3.3 SerDes

PCB designers often overlook the need to isolate noise generated by the digital components with the SerDes high-speed designs. It is necessary to provide a low-noise supply to the sensitive analog portions of the SerDes devices. Noise due to variations in the power-supply voltage can be coupled into the analog portion of the chip, causing unwanted fluctuations in the sensitive stages of the device. The performance of the SerDes highly depends on the layout techniques. This section discusses the layout guidelines for power supply for the SerDes. Layout guidelines for the SerDes differential traces are discussed in a separate section.

3.3.1 Component Placement

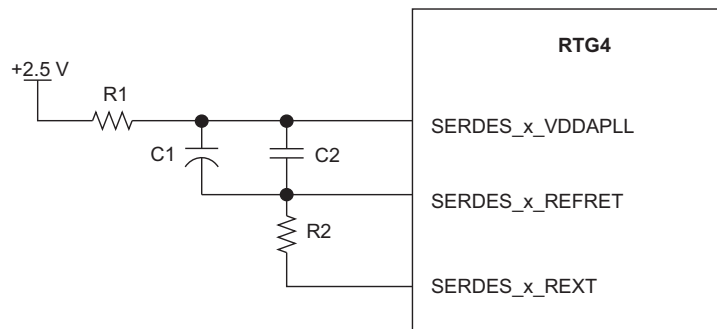
The following sections describe the SerDes components placement.

3.3.1.1 SerDes I/O Power (SERDES_x_VDDAIO)

- The decoupling capacitors (0.1 μ F and 0.01 μ F) are placed on the pad adjacent to the BGA via of the corresponding pin, as shown in [Figure 18](#), page 29. At least one of the capacitors (0.1 μ F or 0.01 μ F) should be placed for each SerDes bank. The capacitor pad to via trace should be as small as possible.
- The bypass capacitor (10 μ F) should be placed at the edge of the IC.

3.3.1.2 SerDes PLL

Figure 20 • Filter Circuit for SerDes PLL Power Supply



- The R1 and the series resistor should be placed near the device as close to the R2 capacitor as possible. A sample placement is shown in [Figure 21](#), page 32.
- The R2 capacitor must be placed near the BGA via. The capacitor pad to via-trace should be as small as possible.
- A precision resistor (C2) should be placed between the SERDES_x_REXT and SERDES_x_REFRET pins, near the BGA via of SERDES_x_REXT pin. Any other aggressive signal traces should be kept away from this connection to avoid unwanted noise from coupling into the critical circuit.
- For exact value of filter components, see the [Figure 1](#), page 5.

3.3.1.3 SerDes I/O Power (SERDES_x_VDDAIO)

Each SERDES quad has two power supplies for SERDES VDDAIO, as follows:

- SERDES_PCIE_x_L23_VDDAIO
- SERDES_PCIE_x_L01_VDDAIO

For best performance, each of these power planes can be routed as a small plane and then tied together to a single power supply. This method minimizes the noise coupling between the differential lanes. SerDes PLL

- Plane routing for SERDES_4_L23_VDDAPLL and SERDES_4_L23_REFRET is shown in [Figure 21](#), page 32.
- SERDES_4_L23_VDDAPLL and SERDES_4_L23_REFRET should not be routed as traces. A small trace width causes poor noise performance due to the high inductive behavior of the trace. Even though the current requirement is low, supply traces should be routed as small planes, as shown in [Figure 21](#), page 32.
- The Connections of 1.2 K Ω resistor and SERDES_4_L23_REXT of RTG4 should not be routed as a thick plane.** It should be routed as a signal trace in order to meet the minimum capacitance requirement of the SERDES_4_L23_REXT pin. The length of the trace should be as short as possible. The following figure shows the sample layout.
- The same layout guidelines should be followed for the remaining SerDes PLL power supplies.

Figure 21 • Layout of SERDES_4_L23_VDDAPLL and SERDES_4_L23_REFRET

3.3.2 Simulations

3.3.2.1 SerDes I/O Power (SERDES_x_VDDAIO)

The target impedance of the SERDES_x_VDDAIO is calculated as 240 mΩ based on the following values (see EQ 1):

- $V_{SUPPLY} = 1.2\text{ V}$
- $I_{trans} = 250\text{ mA}$
- Ripple = 5%

The impedance of the plane is improved by the decoupling capacitors. The impedance of the plane is kept under 0.2Ω till 100 MHz.

The simulation results shown in this document are done in Sigrity PowerSI tool. For more information about using this tool and how to do the simulation, see the *Sigrity PowerSI Tutorial*.

3.4 VREF

The layout guidelines of the respective VDDIO should be followed. It requires VREF voltage for an internal reference. Noise on VREF impacts the read performance of RTG4 devices. VREF lines should be away from aggressive nets or switching power supplies. For DDR memory layout guidelines, see the [Micron DDR3 Memory Layout Guidelines](#). The VDDIO guidelines should be followed for DDR bank VDDIO. This section explains the guidelines to be used for VREF.

3.4.1 Component Placement

3.4.1.1 VREF

- The bypass capacitor (10 uF) should be placed near the device, or if possible, at the edge of the device.
- All decoupling capacitors (0.1 uF and 0.01 uF) should be 0402 or of a smaller package size as they are required to be mounted on the reverse side of the board. They should be fit between the adjacent vias of the BGA package pins. These decoupling capacitors are selected to have low impedance over the operating frequency and temperature range.

- The capacitor pad to via trace should be as small as possible. [Figure 18](#), page 29 shows how capacitors are mounted. Microsemi recommends placing the capacitor pad directly on the corresponding vias.

3.5 VDDIx

- The bypass capacitors (47 μ F and 22 μ F) should be placed near, or if possible, at the edge of the device.
- All decoupling capacitors (0.1 μ F and 0.01 μ F) should be 0402 or of a smaller package size as they are required to be mounted on the reverse side of the board. They should be fit between the adjacent vias of the BGA package pins. These decoupling capacitors are selected to have low impedance over the operating frequency and temperature range.
- The capacitor pad to via trace should be as small as possible. [Figure 18](#), page 29 shows how these capacitors are mounted. The capacitors can also be mounted directly on the pad available on the vias.

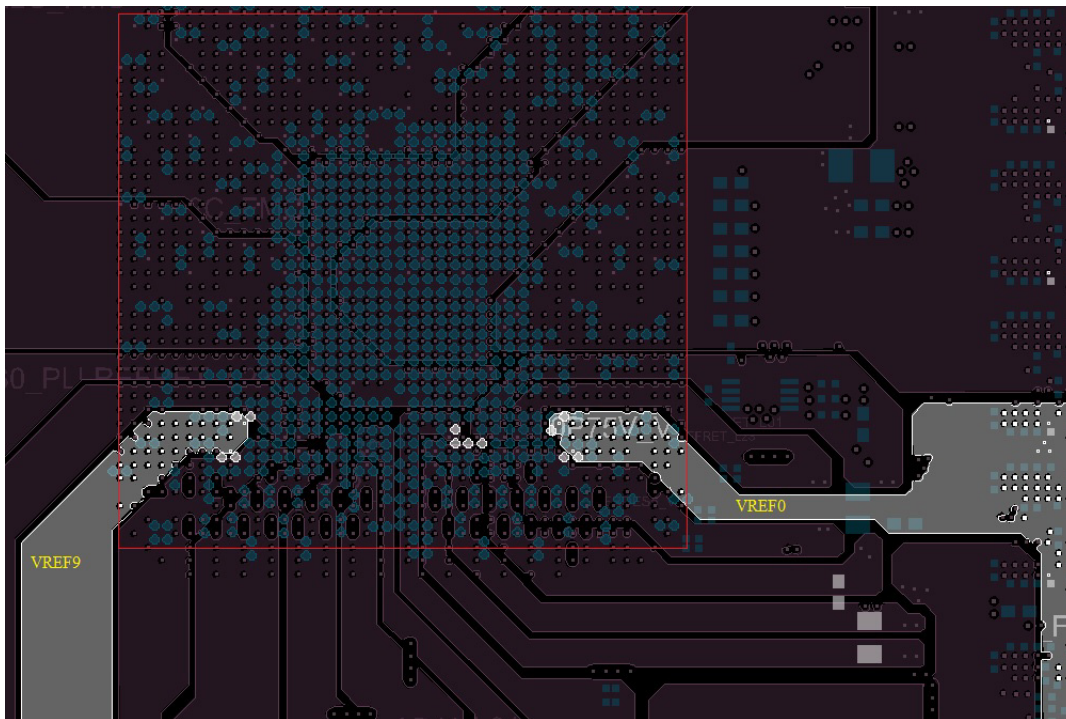
3.5.1 Plane Layout

3.5.1.1 VREF

Noise on VREF impacts the read performance of RTG4 devices. The VREF lines should be routed with no aggressive net or switching power supply nearby. Even though the current is low, VREF should not be routed as trace as it is very susceptible to noise.

The following figure shows the VREF 0 and 9 used for MDDR.

Figure 22 • Layout of VREF 0 and 9

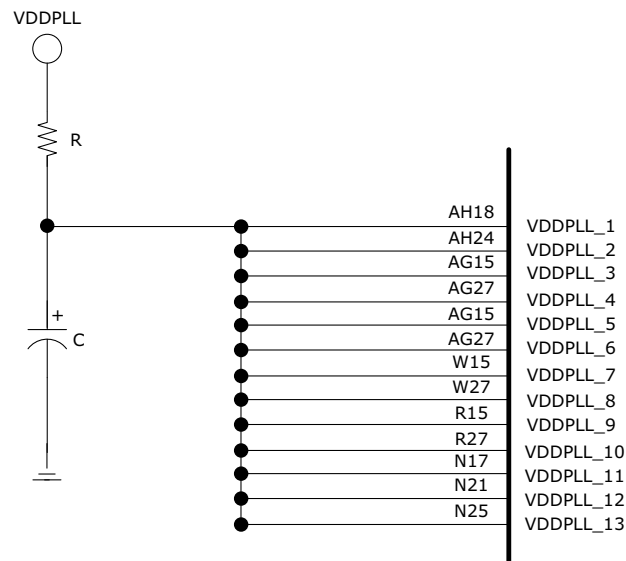


3.6 PLL

To achieve a reasonable level of long term jitter, it is vital to deliver an analog-grade power supply to the PLL. Typically, an R-C or R-L-C filter is used with the C being composed of multiple devices to achieve a wide spectrum of noise absorption. Though the circuit is simple, there are specific board layout requirements. Board layout around the high-frequency capacitor and the path to the pads is critical. It is vital that quiet ground and power are treated similar to analog signals. The entire VDDPLL and PLLVSSA wiring path should not be coupled with any signal aggressors.

The following figure shows the recommended circuit for the power supply filter.

Figure 23 • Filter Circuit for VDDPLL



Note: For R, C values, see [Figure 1](#), page 5.

The target impedance of the VDDPLL plane is calculated as 16.5 Ω based on the following values (see [EQ 1](#)):

- $V_{SUPPLY} = 3.3\text{ V}$
- $I_{trans} = 10\text{ mA}$
- Ripple = 5%

The impedance of the plane (Z) should be 16.5 Ω or less.

3.7 I/O Power Supply

- Component Placement
- The bypass capacitors (47 μF and 22 μF) should be placed near, or if possible, at the edge of the device.
- All decoupling capacitors (0.1 μF and 0.01 μF) should be 0402 or of a smaller package size as they are required to be mounted under BGA package. They should be fit between the adjacent vias of BGA package pins. These decoupling capacitors are carefully selected to have low impedance over operating frequency and temperature range.

The capacitor pad to via trace should be as small as possible. [Figure 18](#), page 29 shows how these capacitors are mounted. The capacitors can also be mounted directly on the pad available on the vias. The decoupling capacitors should not be shared via connections.

3.7.1 Plane Layout

There is no specific requirement for the shape of the plane. The width of the plane should be sufficient enough to carry the required current.

3.7.2 Simulations

The target impedance of the VDDIO plane is calculated as 330 m Ω based on the following values (see [EQ 1](#)):

- $V_{\text{SUPPLY}} = 3.3 \text{ V}$
- $I_{\text{trans}} = 500 \text{ mA}$
- Ripple = 5%

The impedance of the plane is improved by decoupling capacitors and is kept under 0.2 Ω till 100 MHz.

3.8 Programming Power Supply (VPP)

VPP is used as an input for the internal charge pump that generates the required voltage to program flash.

3.8.1 Component Placement

- The bypass capacitors (47 μF and 22 μF) should be placed near, or if possible, at the edge of the device.
- All decoupling capacitors (0.1 μF and 0.01 μF) should be 0402, or of a smaller package size, as they are required to be mounted on the back side of the board. They should be fit between the adjacent vias of BGA package pins. These decoupling capacitors are carefully selected to have low impedance over the operating frequency and temperature range.
- The capacitor pad to via trace should be as small as possible. [Figure 18](#), page 29 shows how these capacitors are mounted. The capacitor can also be mounted directly on the pad available on the vias.

3.8.2 Plane Layout

There is no specific requirement for the shape of the plane. The width of the plane should be sufficient enough to carry the required current.

3.8.3 Simulations

The target impedance of the VPP is calculated as 3.3 Ω , based on the following values (see [EQ 1](#)):

- $V_{\text{SUPPLY}} = 3.3 \text{ V}$
- $I_{\text{trans}} = 50 \text{ mA}$
- Ripple = 5%

The impedance of the plane improves by decoupling capacitors.

3.9 High-Speed Serial Link Layout Considerations

The following sections describe the layout details of a SerDes high speed serial link.

3.9.0.1 Differential Traces

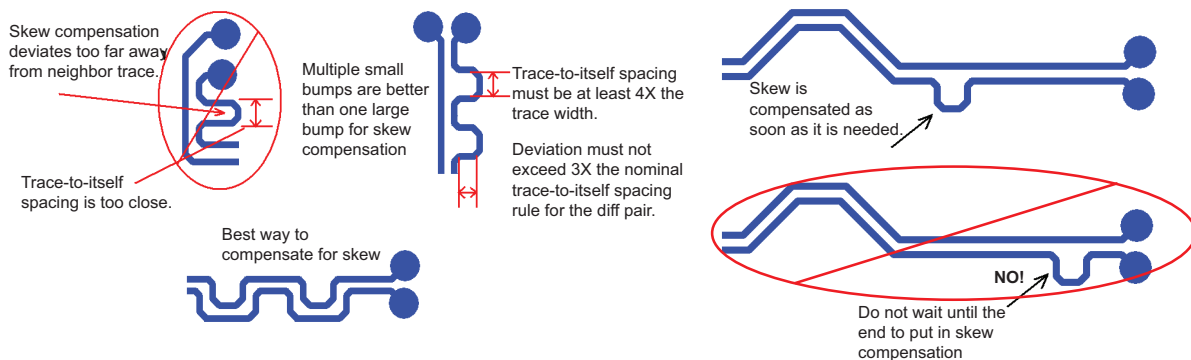
A well-designed differential trace has the following qualities:

- No mismatch in impedance
- Insertion and return loss
- Skew within the differential traces
 - The following points need to be considered while routing high-speed differential traces
- Differential traces should be routed with tight length-matching (skew) within differential traces. Asymmetry in length causes conversion of differential signals to common mode signals.
- The differential pair should be routed such that the skew within differential pairs is less than 5 mils.

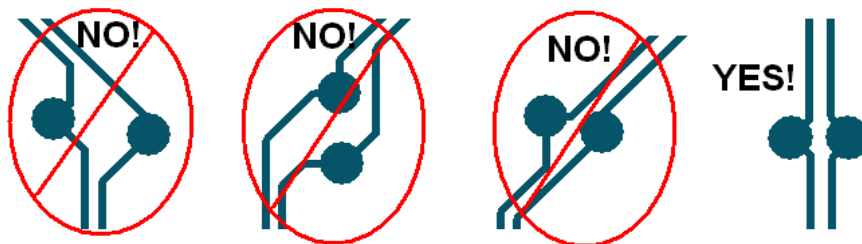
Skew Matching:

- The length of differential lanes should be matched within the TX and RX group.
- Applies only to specific protocols such as XAUI.

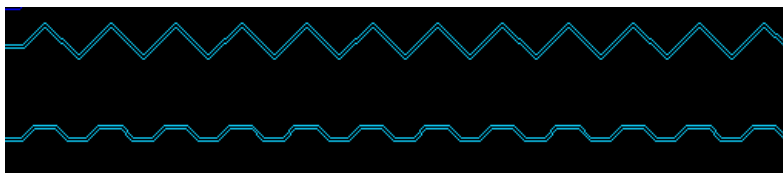
The following figure shows guidelines and techniques that can be used for skew matching.

Figure 24 • Skew Matching Guidelines

- Differential pairs should be routed symmetrically in to, and out of structures, as shown in the following figure.

Figure 25 • Example of Asymmetric and Symmetric Differential Pair Structure

- Skin effect dominates as the speed increases. To reduce the skin effect, the width of the trace should be increased (loosely coupled differential traces). Increased trace width causes an increase in dielectric losses. To minimize the dielectric loss, use low dissipation factor (Df) PCB materials such as Nelco 4000-13EP SI. This is approximately double the cost of FR4 PCB material, but can provide increased eye-opening performance when longer trace interconnections are required. Be sure to maintain 100 Ω differential impedance. This is an important guideline to be followed when data rate is 5 Gbps or higher.
- Far end crosstalk is eliminated by using stripline routing. However, this type of routing causes more dielectric loss and more variation in impedance. Crosstalk impacts only when there is high-density routing. In order to reduce dielectric loss, it is recommended to route as a microstrip, if there is enough space between differential pairs (> 4 times the width of the conductor). Simulations are recommended to see the best possible routing.
- 2116 or 2113 glass-weaving PCB materials should be used to avoid the variations in impedance.
- Zig-zag routing should be used instead of straight line routing to avoid glass weaving effect on impedance variations as shown in the following figure.
Instruct the fabrication vendor to use these PCB materials before manufacturing.

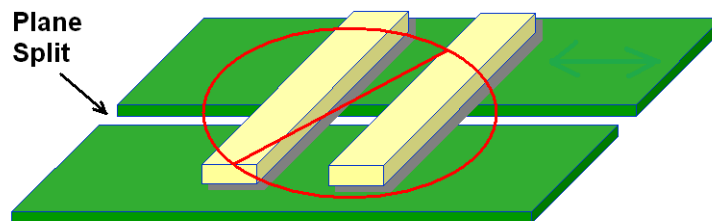
Figure 26 • Zig-Zag Routing

- These traces should be kept away from the aggressive nets or clock traces.
- Separation between coupled differential trace pairs should be 1x. Spacing between channels should be $> 3x$ the separation. Trace stubs should be avoided. The stub length should not exceed 40 mils for a 5 Gbps data rate.
- Trace lengths should be kept as small as possible.
- It is recommended to use low roughness, that is, smooth copper. As the speed increases insertion loss due to the copper, roughness increases. The attenuation due to skin effect is

increased proportional to the square root of frequency. The roughness courses this loss proportional to frequency. Microsemi recommends instructing the PCB fabrication house to use smooth copper, if the frequency exceeds 2 Gbps.

- Split reference planes should be avoided. Ground planes must be used for reference for all the SerDes lanes.

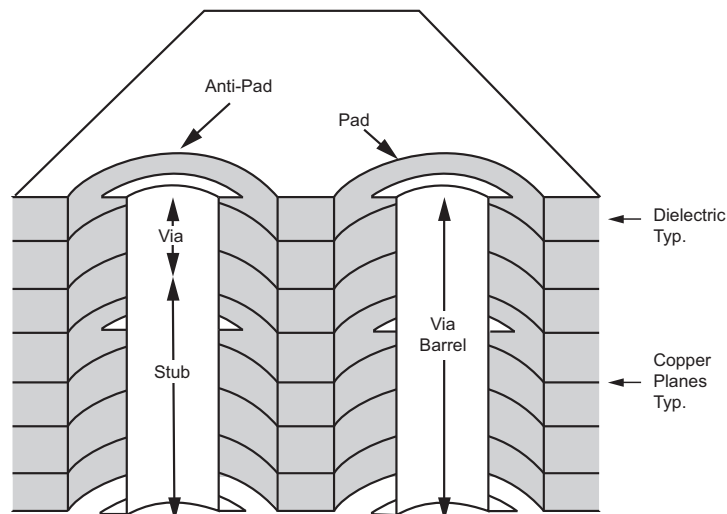
Figure 27 • Ground Planes for Reference



3.9.1 Via

- The target impedance of vias are designed by adjusting the pad clearance (anti-pad size). Field solver should be used to optimize the via according to the stack-up.

Figure 28 • Via Illustration¹

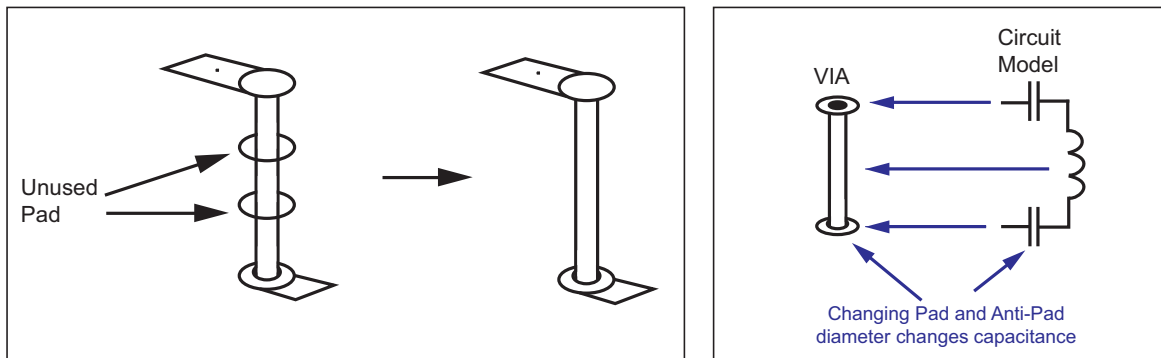


- Number of vias on differential traces should be avoided or minimized. SerDes signals should be routed completely on a single layer with the exception of via transitions from the component layer to the routing layer (3-via maximum).
- The length of via stubs should be minimized by back-drilling the vias, routing signals from the near-top to the near-bottom layer, or using blind or buried. Using blind-vias and back-drilling are good ways to eliminate via stubs and reduce reflections.
- The stub length should be kept below 100 mils, if the data rate is 2.5 Gbps and 40 mils, if the data rate is 5 Gbps.

¹For more information about vias, see [Appendix: Power Integrity Simulation Topology](#), page 55.

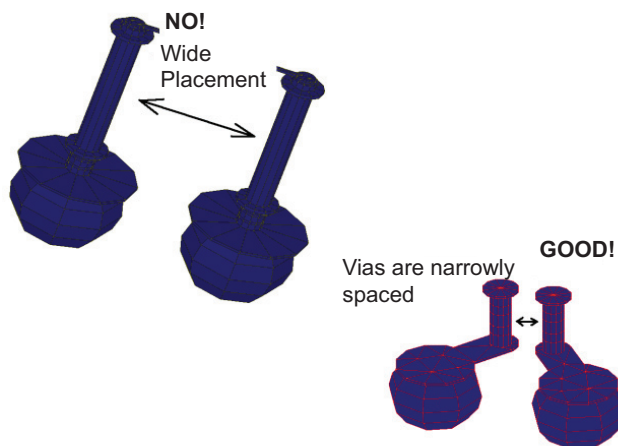
- If feasible, non-functional pads, that is, pads on the via that have no trace connected, should be removed. Removal of such pads reduces the via capacitance and stub effect of pads.

Figure 29 • Non Functional Pads of Via



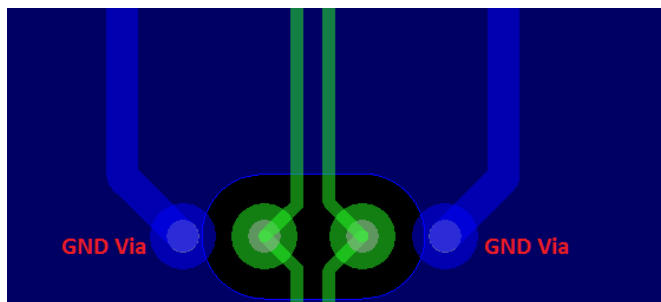
- Using tight via-to-via pitching helps reduce the cross talk effect, as shown in the following figure.

Figure 30 • Via-to-Via Pitch



- Symmetrical ground vias (return vias) should be used to reduce discontinuity for the common mode signal component, as shown in the following figure. The common mode of a part of the signal requires continuous return path RX to TX and GND. Return vias help in maintain continuity.

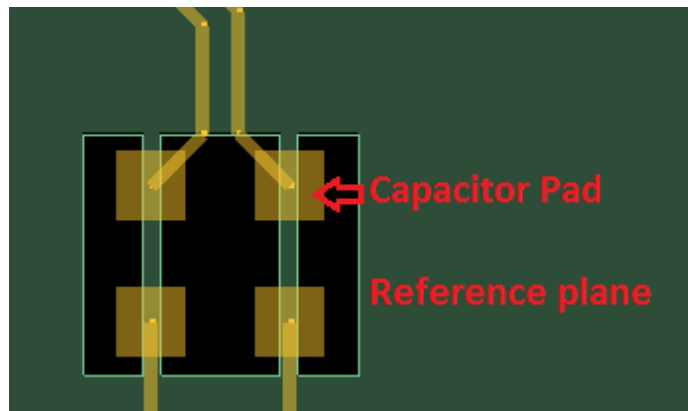
Figure 31 • GND Via or Return Via



3.9.2 DC Blocking Capacitors

The plane underneath the pads of DC blocking capacitors should be removed, as highlighted in the following figure, to match the impedance of the pad to 50 Ω .

Figure 32 • Capacitor Pad Reference Plane



3.9.3 Connectors

The plane keep-out clearance should be optimized from the pin in order to get 50 Ω impedance when through-hole SMAs or connectors are used. This minimizes reflection loss.

3.10 Considerations for Simulation

Microsemi recommends simulations to confirm the quality of the received signal. The following files are required to simulate the serial channel:

- IBIS: AMI files for RTG4 and any other devices that are connected to SerDes
- Package files (optional). S-parameter of package improves the accuracy instead of using package parameters present in IBIS file
- Board traces model file that includes via models
- Connector models, if required

Steps to run the serial channel simulations are as follows:

3.10.1 Step1: Gathering the Required Files

The following sections describe how the required files are obtained in various models.

3.10.1.1 IBIS-AMI Models

The IBIS-AMI models of RTG4 and the IBIS-AMI models of IC that is going to interface with RTG4 can be downloaded from the following link on the Microsemi website:

<http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models/ibis-models-military-and-aerospace.aspx>

Note: The model has a limitation such that the main tap, TX_AMP is always set to the maximum amplitude value and cannot be adjusted in the IBIS AMI model.

3.10.1.2 Package Models

The package models (S-parameter models) of RTG4 can be downloaded from the following link on the Microsemi website:

<http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models/ibis-models-military-and-aerospace.aspx>

The accuracy of simulation improves with S-parameter model of package file instead of using package models available in the IBIS file. If S-parameter models are used, the package details in IBIS should be commented.

3.10.1.3 PCB Trace Models

The PCB file should be converted into a format compatible with the simulator software. For example, the .HYP file format of PCB is required to be simulated in Hyperlynx, and SPD file format for simulation in Sigrity. Once the PCB file is loaded in the simulation tool, the stack-up that matches the PCB stack-up should be checked. The dielectric constant (Dk), and Df of the PCB material should be defined. The tool may not extract the correct models, if these factors are not defined properly. SerDes traces must be identified and the ports on both sides of the traces assigned. The S-parameter models of traces should be extracted. The following tools can be used to extract S-parameter models of PCB traces:

- Agilent's ADS
- Mentor's Hyperlynx
- Sigrity's PowerSI

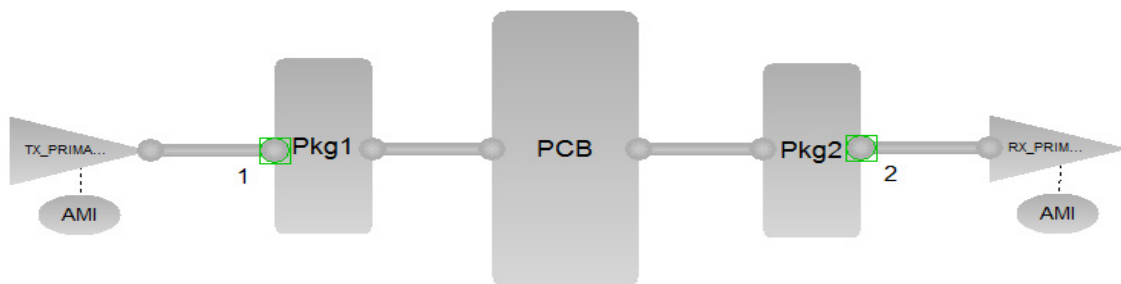
It is not mandatory to use the above-mentioned tools; several other tools that help extract S-parameter models are available in the market.

3.10.2 Step2: Creating Simulation Topology

All SerDes simulations in this document, including the blocks represented in the following figure, are done using Sigrity's SystemSI tool. Simulations can be done in any tool that supports the serial link analysis, as the topology is the same in all the tools.

The following figure shows the typical topology of blocks involved in the serial link analysis.

Figure 33 • Typical Topology for SLA Simulation



From [Figure 33](#), page 40:

- AMI: AMI models of Tx and Rx
- TX_PRIMARY: IBIS model of Tx I/O
- Pkg1 and Pkg2: Package model of Tx and Rx I/O
- PCB: S-parameter model of RTG4 Development Kit SerDes Traces
- RX_PRIMARY: S-parameter model of either the connector or the IBIS model of the receiver IC device

Once all the model files are imported into the topology, the default configuration in the AMI model should be left to calculate the appropriate coefficients and run the simulations.

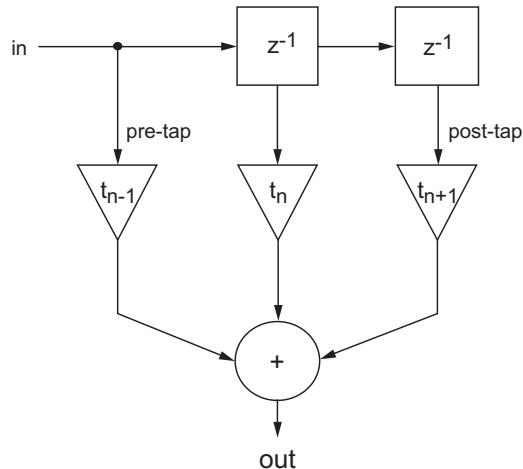
3.10.3 Step3: Configuring the AMI Model

The following configurations on the AMI model are required before simulating the serial channel.

3.10.3.1 TX AMI Model

The following figure shows the block diagram of the 3-tap feed-forward equalizer structure for the TX. The output of the TX is calculated using the transfer function $t_{n-1} + t_n Z^{-1} + t_{n+1} Z^{-2}$. The TX output depends on the tap coefficient values. The following are the details of coefficients.

Figure 34 • Block Diagram of the 3-Tap Feed Forward Equalizer (FFE)



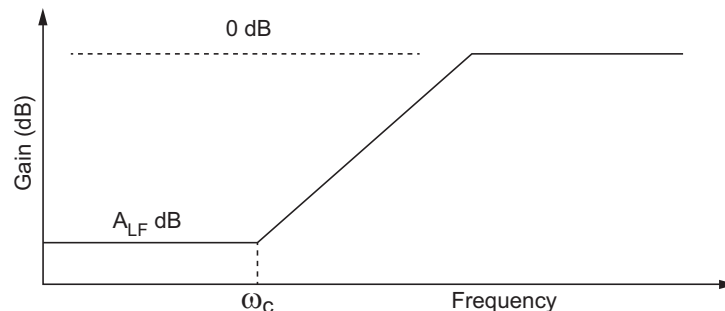
- **t0:** Pre-cursor tap setting
- **t1:** Main tap
- **t2:** Post-cursor tap

3.10.3.2 RX AMI Model

SerDes supports programmable single-pole continuous time linear equalization (CTLE) at the receiver. The continuous time linear equalization involves amplifying higher frequency components that have been more severely attenuated by the interconnect, or attenuating lower frequency components to a greater degree than the higher frequency components.

The low frequency attenuation level and flat-band bandwidth are programmable, as shown in the following figure.

Figure 35 • Continuous Time Linear Equalization Response



Both ALF and ω_c (f_0) can be set to maximize the signal quality of the receiver for achieving the highest possible bit-error rate (BER).

- **Alf:** Low frequency dB loss of the filter. The range is from 0 to 50; the default value is 6.
- **f0:** High pass cutoff frequency. The range is from 1e6 to 5e10; the default value is 1e9.

Step 4: Results

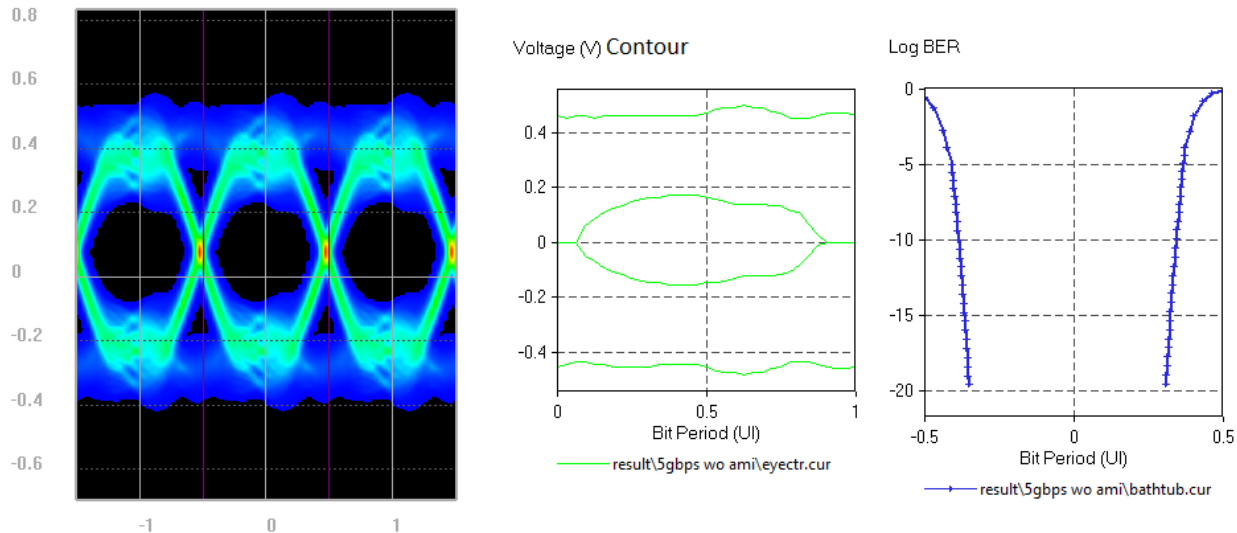
Qualification of simulation results is done based on the eye-height, eye-width, and BER curves. Check the eye-height and eye-width at a target BER of 10e-12. These results found in the report generated by the simulation tool. For example, Sigrity tool gives the following information at Rx:

At BER of 10e-12, running at 5 Gbps bit rate

- The eye-width is 0.68 UI (Unit Interval)
- The eye-height is 213 mV

This simulation is on the RTG4 Development Kit using Sigrity tool and the waveforms are shown in the following figure. The simulation result shows that it meets the PCIe 2.0 requirements

Figure 36 • Expected Results from Simulations (Eye Diagram, Eye Contour, and Bath Tub Curve)



The following table lists the specifications of the received signal for PCIe.

Table 10 • Specifications of the Received Signal for PCIe

Bit Rate	Min Height of the Eye at Rx	Min Width of the Eye at Rx
2.5 Gbps	175 mV	0.6 UI

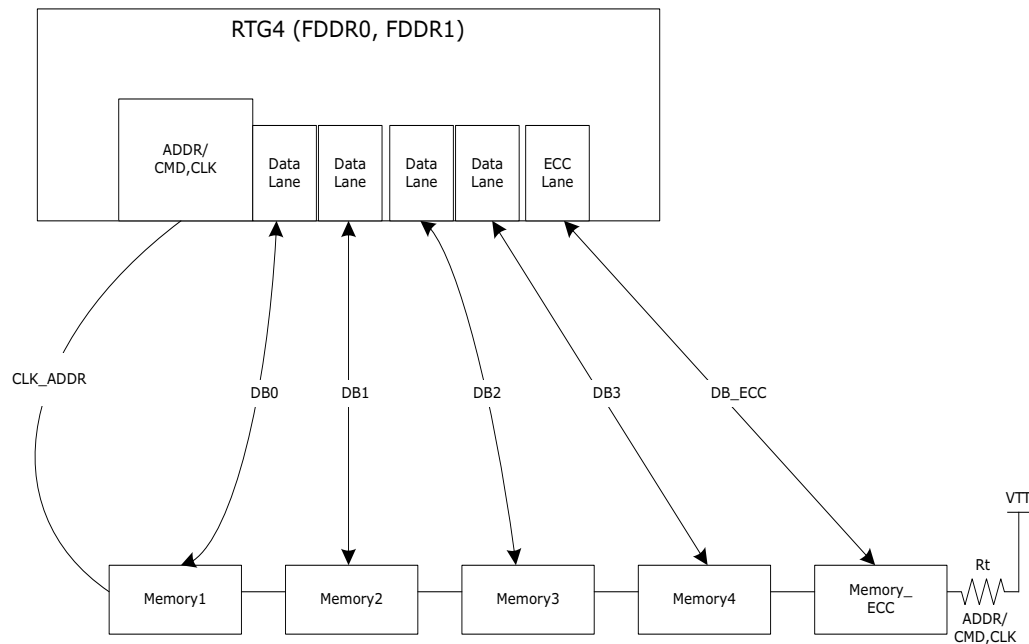
For more information about PCIe 2.0, see [PCI Express Base specification](#).

3.11 DDR3 Layout Guidelines

The following sections describe the DDR3 layout guidelines.

3.11.1 Placement

It is recommended to ensure an L-shaped placement of DDR3 memories looks like *L*-shape, where memories are at the bottom of the '*L*' and controllers are at the top of the '*L*'. This allows enough space to route DQ signals with less number of layers. This is not mandatory to follow the suggested placement. However, the placement also depends on the board constraints.

Figure 37 • DDR3 Memories

Termination resistors are not required for the DQ and DQS signals as these signals have on-chip ODTs. These termination resistors are placed at the end of the address, command, control, and clock signals as these signals use fly-by topology. The VTT plane/island is thick enough to handle the current required by termination resistors; a minimum of 150 mil trace is required. The sense pin of the VTT regulator should be connected at the center of the VTT island.

3.11.2 Routing

The reliability of DDR interface depends on the quality of the layout. There are many layout guidelines available from memory vendors. The following recommendations can also be used for routing the DDR3 signals. DDR3 signals are grouped as follows:

- Data
- Address/Command
- Control
- Clocks
- Power

The following table lists the grouping of DDR3 signals.

Table 11 • Grouping of DDR3 Signals

Group	Signals
Data	DQ[0:7], DQ[8:15]; DQ[16:23], DQ[24:31]; and DQS[0:3], DM[0:3], ECC:DQS_ECC_P\N,DQ_ECC_[0:7].
Address/Command	A[0:15], BA[0:2], RAS#, CAS#, and WE#
Control	CS#, CKE, and ODT
Clock	CK and CK#

3.11.2.1 Data Group Signal Routing

The following guidelines should be followed when routing data group signals:

- Data signals should not be over the split planes.
- The reference plane for data signals should be GND plane and should be contiguous between memory and RTG4.
- Traces should not be routed at the edge of the reference plane and over via anti pads.
- When routing data signals, the longest signals should be routed first, this allows to adjust the length for the short length signals, when routing the data signals.
- Serpentine routing should be used to adjust the data group signals to meet this requirement.
- The DQS signal should be routed along with associated data byte lane on the same critical layer with the same via count. Avoid using more than three vias in the connection between the FPGA controller and memory device.
- The impedance for the data traces depends on stack-up and trace width. There are options to select the impedance based on the stack-up and trace width.
 - 40 Ω impedance, which requires wide traces (~7 to 8 mils). This gives the less cross talk and less spacing between the traces (~2x). Spacing between non DDR signals and DDR signals should be ~4x.
 - 50 Ω impedance, which requires smaller trace width (~4 to 6 mils). This requires more spacing between the traces (~3x). Spacing between non DDR signals and DDR signals should be ~4x.
- Within each of the data lanes, each traces should be matched to within ± 10 mils of the associated data strobe.
- The DQS and DQS# need to be matched within ± 5 mils.
- The differential impedance should be between 75 to 95 Ω . If the data rate is more than 1600 MT/s, then the impedance should be in the range of 90 to 95 Ω .
- The differential traces should not be routed adjacent to noisy signals or clock chips.
- Spacing between differential lines should be 5 to 8 mils.

3.11.2.2 Address, Control, Command, and Clock Routing

- These signals should be routed using fly-by topology, and terminated by using appropriate termination resistor at the end of the signals. The resistor termination should not have a stub longer than 600 mil.
- The impedance for the trace depends on the stack-up and trace width. There are options to select the impedance based on the stack-up and trace width:
 - 40 Ω impedance, which requires wide traces (~7 to 8 mils). This gives the less cross talk and less spacing between the traces (~2x). Spacing between non DDR signals and DDR signals should be ~4x.
 - 50 Ω impedance, which requires smaller trace width (~4 to 6 mils). This requires more spacing between the traces (~3x). Spacing between non DDR signals and DDR signals should be ~4w to avoid crosstalk issues.
 - Address and control signals can be referenced to a power plane if a ground plane is not available. The power plane should be related to the memory interface. However, a ground reference is preferred. Address and control signals should be placed on a different routing layer than DQ, DQS, and DM signals to isolate crosstalk between the signals.

3.11.2.3 Clock

- Clock signals are routed differentially, and the length matches between traces should be ± 5 mils.
- The differential traces should not be routed adjacent to noisy signals or clock chip.
- Clock signals should be referenced to a ground plane.
- The space between clock and other signals should at least be 25 mils.
- Address/control signals and the associated CK and CK# differential FPGA clock should be routed with trace matching of ± 100 mil.

Note: To know more about signal groups routing, see [Figure 37](#), page 43.

3.11.2.4 Length Matching Guidelines

- Within the group CLK_ADDR, all signals should be matched with +/- 250 mils
- The length for CLK_ADDR group routing (RTG4 to Memory1) and data byte group DB0 should be matched to +/- 250 mils.
- The length for DB0 versus DB1 and DB2 groups should be within +/- 150 mils. (for example, if DB0 length is 600 mils, length for DB1 and DB2 should be between 450 - 750 mils.)
- The length of DB3 should be 600 - 700 mils more than DB2. (that is, if DB2 length is 1 inches, DB3 length should be 1.6 inches)
- The length of DB_ECC should be 600 - 700 mils more than DB3.
- Within the data byte groups DB0, DB1, DB2, DB3, the signals (DQS, DQ, DM/DBI) should be matched within +/- 100 mils.

Note:

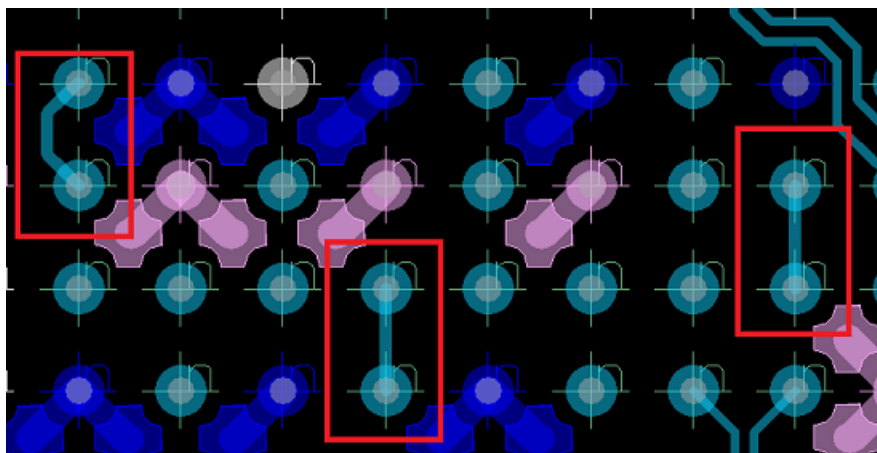
1. Short the FDDR_E_TMATCH_0_IN and FDDR_E_TMATCH_0_OUT pins under BGA using short trace.
2. Short the FDDR_E_TMATCH_1_IN and FDDR_E_TMATCH_1_OUT pins under BGA using short trace.
3. Short the FDDR_E_TMATCH_ECC_IN and FDDR_E_TMATCH_ECC_OUT pins under BGA using short trace.
4. Short the FDDR_W_TMATCH_0_IN and FDDR_W_TMATCH_0_OUT pins under BGA using short trace.
5. Short the FDDR_W_TMATCH_1_IN and FDDR_W_TMATCH_1_OUT pins under BGA using short trace.
6. Short the FDDR_W_TMATCH_ECC_IN and FDDR_W_TMATCH_ECC_OUT pins under BGA using short trace.

Note: For more information about length matching guidelines for DDR3 and DDR2 from Micron, see *TN-47-20: Hardware Tips for Point-to-Point System Design* and *TN-46-19: Hardware Tips for Point-to-Point System Design*.

Note: The length matching guidelines listed in [Length Matching Guidelines](#), page 45, are suitable for both RTG4 STD and -1 speed grade devices. These length matching guidelines supersede the DDR3 board layout used on the RTG4-DEV-KIT. See the analysis of the RTG4 Development Kit DDR3 layout at, [AC439: Board and Layout Design Guidelines for RTG4 FPGA Application Note Addendum](#).

The following figure shows an example layout.

Figure 38 • TMATCH Signals (Example Layout)



3.12 Simulation

Simulations ensure that the DDR and controller meet timing requirements. They also ensure that the quality of the received waveform in terms of undershoot, overshoot and jitter and so on.

The following files are required for DDR3 simulation:

- RTG4 IBIS file

- DDR3 memory IBIS file
- RTG4 board PCB files and the PCB files of the DIMM, if used
- Connector models if DIMM is used

Following are the steps to run the serial channel simulations:

3.12.1 Step 1: Gathering the Required Files

The following sections describe how the required files are obtained in various models.

3.12.1.1 IBIS Models

To download the IBIS models of RTG4 and the IBIS-AMI models of DDR3 memory which is going to interface with RTG4, refer to the following links on the Microsemi website:

<http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models/ibis-models-military-and-aerospace.aspx>

3.12.1.2 PCB Trace Models

The PCB file needs to be converted into a format compatible with the simulator software. For example hyp file format of PCB is required to simulate in Hyperlynx and SPD file format of PCB for simulation in Sigritty. Once the PCB file is loaded in the simulation tool, check the stack-up that matches the PCB stack-up and define the dielectric constant, Dk and Dissipation factor, and Df of PCB material. The tool extracts wrong models, if the above points not defined properly. Some tools run the simulations on PCB file itself like Hyperlynx and some tools need S-parameter files of DDR3 traces to continue the simulations.

To extract S-parameter models of PCB traces assign the ports on both sides of the traces and extract the S-parameter models of traces. The following tools can be used to extract S-parameter models of PCB traces:

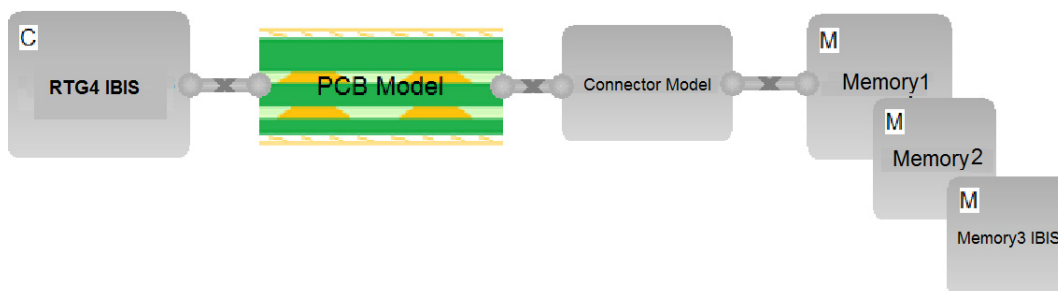
- Agilent's ADS
- Mentor's Hyperlynx
- Sigritty's PowerSI

It is not mandatory to use above-mentioned tools; several other tools that help extract S-parameter models are available in the market.

3.12.2 Step 2: Creating Simulation Topology

The following figure shows the typical topology of blocks involved in DDR3 simulations. These blocks are taken from the Sigritty tool. The simulation can be done in any tool which supports DDR3 simulation, as the topology is the same in all the tools.

Figure 39 • DDR3 Simulation Topology



From Figure 39, page 46:

- RTG4 IBIS: IBIS model of RTG4
- PCB: S-parameter model of PCB file, connector models and DIMM PCB models
- Connector model: Spice models of connector
- Memory IBIS: IBIS models of DDR3 memory

3.12.3 Step 3: Simulation Setup

- Assign IBIS models to RTG4 and memory
- Assign the connector model, if used
- Assign the models for on-board termination resistors
- Identify the DDR3 nets and classify according to data, control, and address bus
- Set the appropriate ODT for SF2 and memory.
- Set 40 to 60 Ω ODT for data and 80 to 120 Ω for DQS signals
- Set the maximum frequency at which the system will operate. For RTG4, it is 333 MHz

Step 4: Results











The important things that needs to be observed from the results are:

- Setup and hold time between data signals and the respective DQS over all corners
- Setup and hold time between Control/Command/Address signals and the clock over all corners
- Overshoot and undershoot of all signals with respect to JEDEC specifications over all corners. And also DC threshold multi crossing that occurred due to the excessive ringing

The simulation tool generates the report where all the details are available. For example, Hyperlynx generates the set of excel sheets, that contain all setup and hold margin, overshoot and undershoot information for all corners. It also generates driver and receiver waveforms for all the nets.

The following figure shows list of files generated by Hyperlynx, with all the simulation information.

Figure 40 • List of Hyperlynx Simulation Reports Generated

Name	Date modified	Type	Size
 DDR_report_address_allcases_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	132 KB
 DDR_report_address_violations_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	11 KB
 DDR_report_address_worstcases_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	11 KB
 DDR_report_data_allcases_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	104 KB
 DDR_report_data_violations_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	6 KB
 DDR_report_data_worstcases_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	11 KB
 DDR_report_SI_measurements_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	11 KB
 DDR_report_skew_allcases_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	51 KB
 DDR_report_skew_violations_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	6 KB
 DDR_report_skew_worstcases_Typ.xls	5/30/2013 12:37 PM	Microsoft Office E...	11 KB

The following figure shows an example report for an A0 net. It shows that the A0 has enough setup and hold time margins.

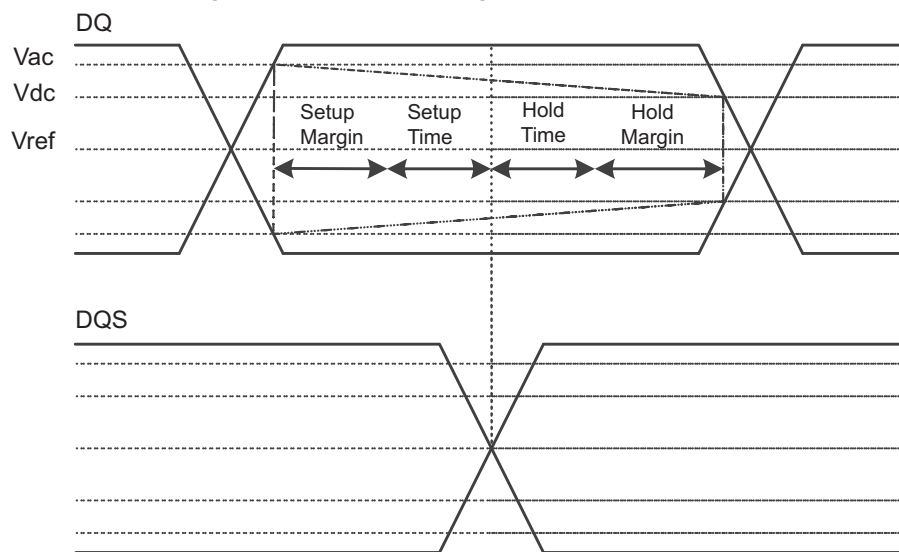
Figure 41 • Setup and Time Margins of A0

	A	O	U
	Net Name	Setup Time Margin, $tDS(\text{margin}) = tDS(\text{min}) - tDS(\text{req})$	Hold Time Margin, $tDH(\text{margin}) = tDH(\text{min}) - tDH(\text{req})$, [ps]
1			
2	DDR2_DQ0	N/A	333.3
3	DDR2_DQ0	267.6	N/A
4	DDR2_DQ0	N/A	316.6

If any of the net is violating the setup and holding time margins, the length of the net should be changed accordingly. If there is a high-peak overshoot or undershoot, it could be because of the high value termination resistor. It is required to adjust the value of ODT and re-iterate the simulation.

The following figure shows how to setup and hold time margins for DQ and DQS signals. Same is applicable to the margin between the Command/Control/Address and CLK signals.

Figure 42 • Setup and Time Margins for DQ and DQS Signals



4 Board Design Checklist

This chapter provides a set of hardware board design checks for designing hardware using Microsemi RTG4 FPGAs. The checklists provided in this chapter are a high-level summary checklist to assist the design engineers in the design process.

This chapter contains the following sections:

1. [Board Design Checklist](#), page 49
2. [Layout Checklist](#), page 51

4.1 Board Design Checklist

The following table lists the checks that design engineers must take care of while designing the system.

Table 12 • Design Checklist

S.No.	Checklist	Yes/No
Prerequisites		
1.	Read datasheet and pin description user guides: – DS0131: RTG4 FPGA Datasheet . – DS0130: RTG4 FPGA Pin Descriptions Datasheet	
2.	Check for available designs and development tools.	
3.	Refer to the board-level schematics of the RTG4 Development Kit . Note: This application note supersedes the RTG4-DEV-KIT board schematic/layout, and thus the guidelines in this document, should be followed when there is a difference between the RTG4 Development Kit and the document.	
Device Selection		
4.	Check for the available device variants for RTG4 FPGA – Select a device based on the I/O pin count, transceivers, package, phase- locked loops (PLLs), and speed grade	
5.	Check device errata. See ER0193: RTG4 FPGA Errata .	
Design Checklist		
6.	Power Analysis Download the RTG4 Power estimator following link and check the power budget: https://www.microsemi.com/document-portal/doc_download/134921-rtg4-power-estimator	
Power Supply		
7.	Power Supplies See Figure 1 , page 5 for used power rails connections and Figure 3 , page 11 for unused connections.	
8.	Decoupling Capacitors Follow Table 2 , page 6 and Table 3 , page 8 based on the die or package combination. Perform PI Analysis for any deviation from the recommended capacitors.	
9.	Brownout Detection (BOD) Circuit Ensure that brownout detection is implemented standalone or included as part of power management circuitry. See Brownout Detection , page 25.	

Table 12 • Design Checklist (continued)

S.No.	Checklist	Yes/No
Clocks		
10.	RTG4 devices have one on-chip RC oscillator, operating at 50 MHz. See, UG0586: RTG4 FPGA Clocking Resources User Guide for more information.	
11.	Global buffer (GB) can be driven through dedicated global I/Os, CCC, or fabric (regular I/Os) routing. The global network is composed of GBs to distribute low-skew clock signals or high-fanout nets. Dedicated global I/Os drive the GBs directly and are the primary source for connecting external clock inputs (to minimize the delay) to the internal global clock network. For more information, see UG0586: RTG4 FPGA Clocking Resources User Guide .	
Reset		
12.	DEVRST_N – Input The DEVRST_N pin must have a 10 K Ω pull-up resistor. The pin must not be left floating. If a push-button switch is used to generate reset, check for switch de-bounce. For more information about DEVRST_N, see Power-up and Power-Down Sequence , page 9.	
Device Programming		
13.	See Device Programming , page 13.	
SerDes Pins		
14.	See SerDes , page 15 and UG0567: RTG4 FPGA High Speed Serial Interfaces User Guide .	
DDR Interface		
15.	DDR Interface For more information about DDR routing and topology, see LPDDR , DDR2 , and DDR3 , page 17.	
16.	I/O Pin Assignment Use a spreadsheet to capture the list of design I/Os. Microsemi provides detailed pinout information that can be downloaded from the website and customized to store the pinout information for specific designs. For pin out details for various packages with different densities, see DS0130: RTG4 FPGA Pin Descriptions Datasheet .	
17.	Check if there are any incompatible I/O standards combined in the same bank.	
18.	Check if there are two interfaces with different voltage standards in the same bank.	
19.	See the bank location diagrams in DS0130: RTG4 FPGA Pin Descriptions Datasheet document to assess the preliminary placement of major components on PCB.	

4.2 Layout Checklist

The following table lists the checks that the designer needs to take care while designing a system on the board:

Table 13 • Layout Checklist

S.No.	Description	Yes/No
Power		
1.	Are 0402 or lesser size capacitors used for all decaps (less than value?)	
2.	Is the power supply filter implemented on SerDes Core supply (SERDES_x_VDD) as shown in Figure 20 , page 31?	
3.	Are power supply filters implemented on SERDES_x_VDDAPLL and SERDES_x_PLL_VDDA as shown in the Figure 20 , page 31 and Figure 23 , page 34 respectively?	
4.	Is a precision 1.21 K resistor used between SERDES_x_REFRET and SERDES_x_REXT?	
5.	Are placement and layout guidelines followed for the 1.21 K resistor?	
6.	Are VREF planes for the DDRx reference supply isolated from the noisy planes?	
7.	Are sufficient number of decoupling capacitors used for the DDRx core and VTT supply?	
8.	Is one 0.1 μ F capacitors for two VTT termination resistors used for DDRx?	
9.	Is the VTT plane width sufficient?	
DDR3		
11.	Are the length-match recommendations for DDR3 followed?	
SerDes		
12.	Are the length-match recommendations for SerDes followed?	
13.	Are DC blocking capacitors used for the SerDes TX, and, if required, on RX lines?	
14.	Is tight-controlled impedance maintained along the SerDes traces?	
15.	Are differential vias well designed to match SerDes trace impedance?	
16.	Are DC blocking capacitor pads designed to match SerDes trace impedance?	
Dielectric Material		
17.	Is proper PCB material selected for critical layers?	

5 Appendix: Stack-Up

A good stack-up leads to better performance. The number of layers in the stack-up depends on factors such as the board's form factor, the number of signals to be routed, and the power requirements. Based on these factors, the designer chooses how many layers the board requires. The RTG4 Development Kit has a 16-layer stack-up, as shown in [Figure 43](#), page 53.

Note: All the guidelines in this document are with respect to a 16-layer board stack-up.

The upper power layers should be used for high priority supplies. High-switching current supplies should be placed vertically, close to the devices to decrease the distance the currents need to travel through the vias. Ground planes should be placed adjacent to the high-transient current power planes to reduce inductance and to couple the high-frequency noise.

It is good to have power and ground layers side-by-side such inter-plane capacitance provides better decoupling at high frequencies.

The effect of vias on power pins is reduced by placing a power plane near the device.

Signal integrity depends on how well the traces have controlled impedance, so it is always recommended to have controlled impedance.

















Microsemi recommends that all critical high-speed signals such as DDR and PCIe signals, need to have a ground reference. All signal layers should be separated from each other by ground or power planes. This minimizes crosstalk and provides balanced and clean transmission lines with properly controlled characteristic impedance between devices and other board components.

For best performance, use dedicated ground plane layers that are continuous across the entire board area. Power planes can provide adequate reference, however, the power planes should be related to the signals they serve to reference.

Note: Refrain from using unrelated power planes as a signal reference.

Slots should not interrupt the planes, or else they can possibly force current to find an alternate return path. This undesired return path may cause a localized bounce on the power or ground plane that can possibly be capacitively coupled to all signals adjacent to the planes.

Figure 43 • Stack-up Used in Development Board

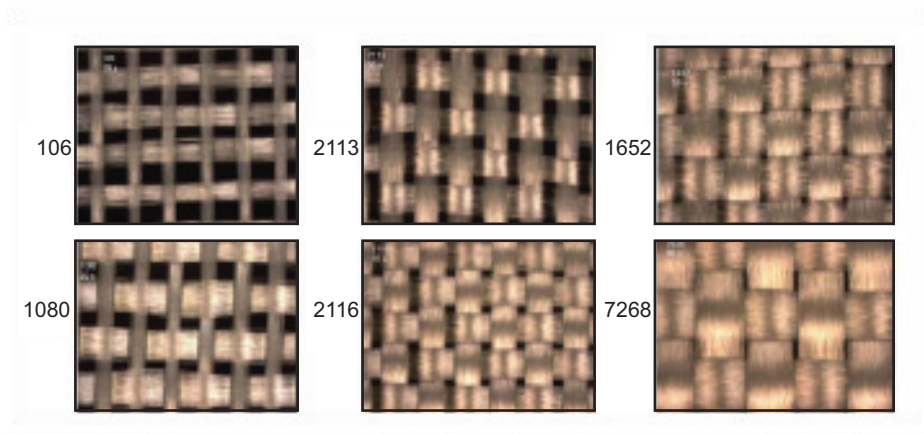
Lamination Stack-up:			Thickness and Tolerance:		Base Material Requirements:	
L#/Type:	Description:		Cu+:	Lamination/PrePreg:	Type:	Description:
1 Mix	 Core 0.0040 Q/H		.00035	.0040		NP 4000-13EP
2 Pin			.00060			
3 Mix	 Pre-Preg (1 x 2113)			.0034		NP 4000-13EP
4 Pin	 Core 0.0035 H/H		.00060	.0035		NP 4000-13EP
5 Mix	 Pre-Preg (1 x 2113)			.0034 +/- 0.0003		NP 4000-13EP
6 Pin	 Core 0.0035 H/H		.00060	.0035		NP 4000-13EP
7 Mix	 Pre-Preg (1 x 1080)			.0022 +/- 0.0002		NP 4000-13EP
8 Pin	 Core 0.0030 1/H		.00120	.0030		NP 4000-13EP
9 Mix	 Pre-Preg (1 x 1080)			.0026 +/- 0.0003		NP 4000-13EP
10 Pin	 Core 0.0030 H/1		.00060	.0030		NP 4000-13EP
11 Mix	 Pre-Preg (1 x 1080)			.0023 +/- 0.0002		NP 4000-13EP
12 Pin	 Core 0.0035 H/H		.00060	.0035		NP 4000-13EP
13 Mix	 Pre-Preg (1 x 2113)			.0034 +/- 0.0003		NP 4000-13EP
14 Pin	 Core 0.0035 H/H		.00060	.0035		NP 4000-13EP
15 Mix	 Pre-Preg (1 x 2113)			.0034 +/- 0.0003		NP 4000-13EP
16 Pin	 Core 0.0040 H/Q		.00060	.0040		NP 4000-13EP
			.00035			
Target Post-Lam Thickness: 0.0600 +/- 0.0030			Stack-up Notes:			
Copper Oz Legend: H = 1/2 Oz T = 3/8 Oz Q = 1/4 Oz S = 1/16 Oz			0.004 Q/H CORES MUST BE MADE OF (1 x 2116 PREG)			
			0.0035 H/H CORES MUST BE MADE OF (1 x 2113 PREG)			
			0.003 1/H CORES MUST BE MADE OF (1 x 1080 PREG)			

6 Appendix: Dielectric Material

The impedance of traces depends on the geometry of the traces and the dielectric material used. The skew of the signal depends on the dielectric constant, and loss of signal strength depends on the loss tangent of the material. The RTG4 Development Kit board uses Nelco 4000-13 EP SI dielectric material. However, the material is selected based on the speed and length of the high speed traces. Simulations are recommended on high-speed serial links to converge on the type of the material used.

While designing for gigabit serial links, the weaving structure of the PCB dielectric material should be taken into consideration. A PCB dielectric substrate is constructed from woven fiberglass fabrics strengthened and bound together with epoxy resin. A typical weaving of PCB dielectric material is shown in the following figure.

Figure 44 • Fiberglass Weaving¹



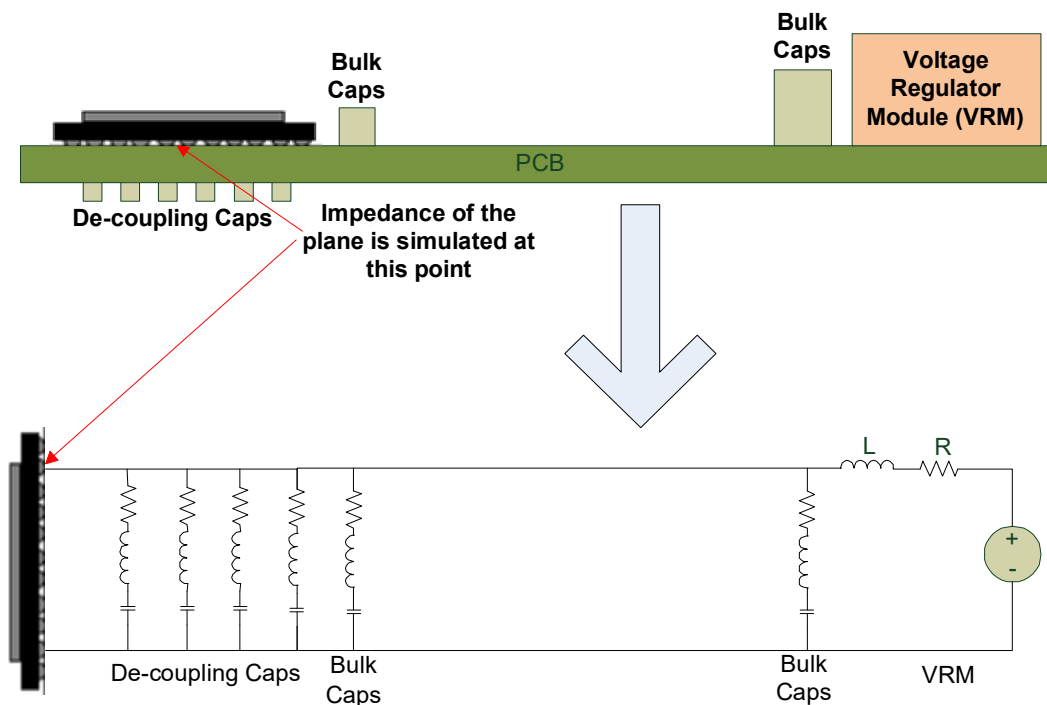
Depending on the density of weaving, PCB materials are numbered as 106, 1080, 2113, 2116, 1652, and 7268. Trace routed on the PCB is non-homogeneity in dielectric constant due to weaving. This causes discontinuities in the trace impedance, resulting in improper eye-opening at the receiving end. For more information about, see the [Solving PCB Fiber Weave Issues](#).

¹For more information about Fiberglass Weaving, see [Appendix: Power Integrity Simulation Topology](#), page 55.

7 Appendix: Power Integrity Simulation Topology

The following figure shows the topology considered for simulating the power plane for Power Integrity analysis.

Figure 45 • Power Integrity Simulation Topology



7.1 References

The following guides are referred in this application note.

- Power Distribution Network (PDN) by Eric Bogatin
- Method of Modeling Differential Vias, White Paper, Jan 2011 by L. Simonovich, E. Bogatin, Y. Cao.
- signal-integrity.tm.agilent.com/2011/pcb-fiber-weave/
- Sigrity PowerSI tutorial
- [UG0573: RTG4 FPGA High Speed DDR Interfaces User Guide](#)
- [UG0567: RTG4 FPGA High Speed Serial Interfaces User Guide](#) are referred.