Total Ionizing Dose Test Report

No. 14T-RTSX72SU-CQ256-D6LRQ1

March 26, 2014

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I. Summary Table

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (SiO2)
2. Power Supply Current (ICCA/ICCI)	Passed 40 krad (SiO2)
3. Input Threshold (VIL/VIH)	Passed 100 krad (SiO2)
4. Output Drive (VOL/VOH)	Passed 100 krad (SiO2)
5. Propagation Delay	Passed 100 krad (SiO2) for 10% degradation criterion
6. Transition Characteristics	Passed 100 krad (SiO2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the base of an extensive database (see TID data of antifuse-based FPGAs at http://www.klabs.org and http://www.microsemi.com/soc) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input or output is grounded through a resistor; during annealing each input or output is grounded through a 1K Ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTSX72SU
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 µm CMOS
DUT Design	TDSX72CQFP256_2Strings_r1
Die Lot Number	D6LRQ1
Quantity Tested	6
Serial Number	100 krad(SiO2): 15368, 15366 60 krad(SiO2): 15361, 15319 40 krad(SiO2): 15225, 15195
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	10 krad(SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 5.0 V/2.5 V

B. Test Method

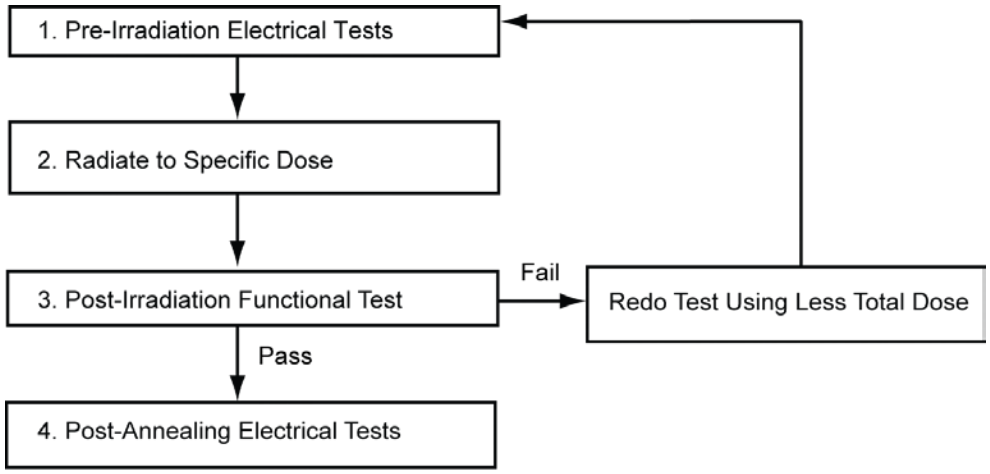


Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart describing the steps for functional and parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging or rebound test mentioned in TM1019.8 is unnecessary, because there is no adverse time-dependent effect (TDE) in Microsemi products manufactured by deep sub-micron CMOS technologies. Elevated temperature annealing basically reduces the effects originating from radiation-induced leakage currents. As indicated by test data in the following sections, the predominant radiation effects in RTSX72SU are due to radiation-induced leakage currents.

Room temperature annealing is performed in this test; the duration is approximately 7 days.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX72CQ256_2Strings_r1) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 1400 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 1536 bits. ICC is measured on the power supply of the logic-array (ICCA) and I/O (ICCI) respectively. The input logic thresholds (VTIL/VIH) and output-drive voltages (VOL/VOH) are measured on combinational nets listed in Row 3 and 4 in Table 2. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at CLOCK input to the time of switching state at output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots showing the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. ICC (ICCA/ICCI)	DUT power supply
3. Input Threshold (VIL/VIH)	Input buffers (DA/QA0, DAH/QA0H, ENCNTRH/YO0H, IDII0/IDIO0, IDII1/IDIO1, IDII2/IDIO2, IDII3/IDIO3, IDII4/IDIO4, IDII5/IDIO5, IDII6/IDIO6, IDII7/IDIO7)
4. Output Drive (VOL/VOH)	Output buffer (DA/QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

III. Test Results

A. Functionality

Every DUT passes the pre-irradiation, post-irradiation, and post-annealing functional tests.

B. Power Supply Current (ICCA and ICCI)

Table 3 summarizes the pre-irradiation, post-irradiation right after irradiation and before anneal, and post-annealing ICCA and ICCI data.

Table 3 Pre-irradiation, Post Irradiation and Post-Annealing ICC

DUT	Total Dose	ICCA (mA)			ICCI (mA)		
		Pre-irrad	Post-irrad	Post-ann	Pre-irrad	Post-irrad	Post-ann
15368	100 krad	1.24	274	201	0.73	210	89
15366	100 krad	1.25	246	185	0.73	188	87
15361	60 krad	1.32	22	21	0.73	26	18
15319	60 krad	1.23	24	25	0.73	27	41
15225	40 krad	1.28	3	2	0.74	1	1
15195	40 krad	1.25	3	2	0.73	1	2

In compliance with TM1019.8, the post-irradiation-parametric limit (PIPL) for the post-annealing ICCA/ICCI in this test is defined as the highest ICCA/ICCI in the RTSXSU spec sheet of 25 mA.

Figure 2 through Figure 7 plot the influx standby ICCA and ICCI versus total dose for each DUT.

There are unexpected ICCI increases during irradiation as shown. In Figures 3 through 7 the ICCI would drop back at some points of time. The suspect is an intermittent continuity problem of the socket on the test board. The post-anneal ICCI measurements are more stable.

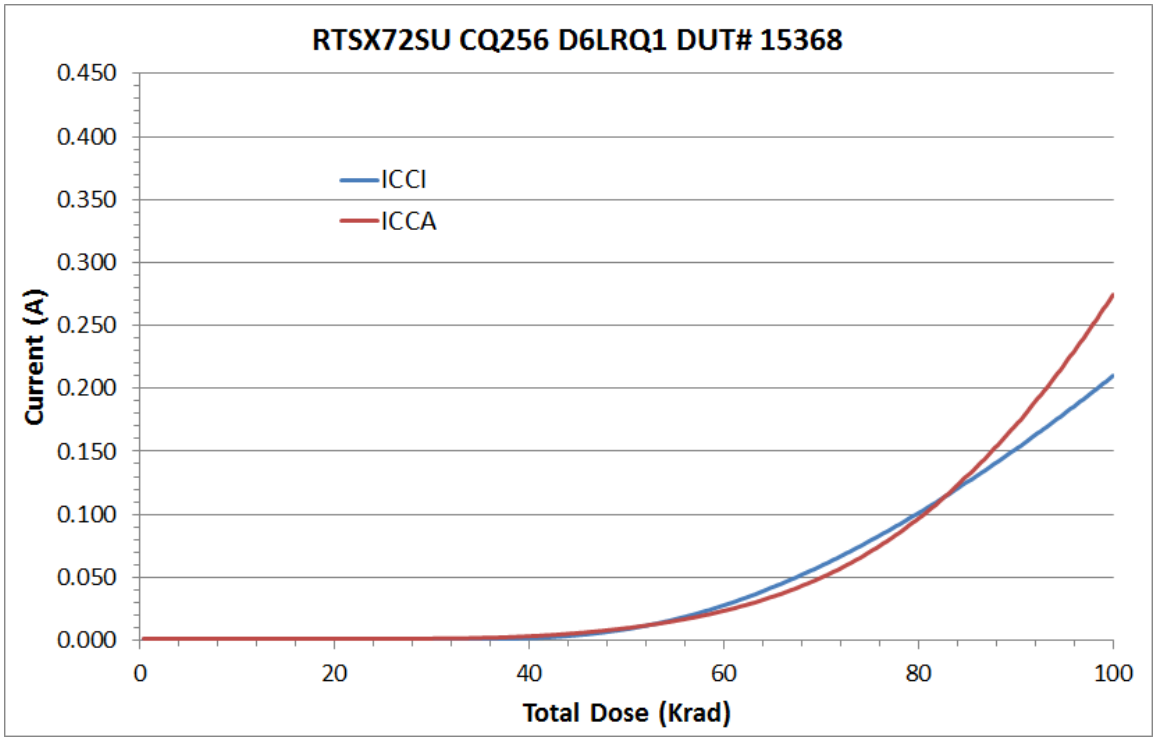


Figure 2 DUT 15368 Influx ICCA and ICCI

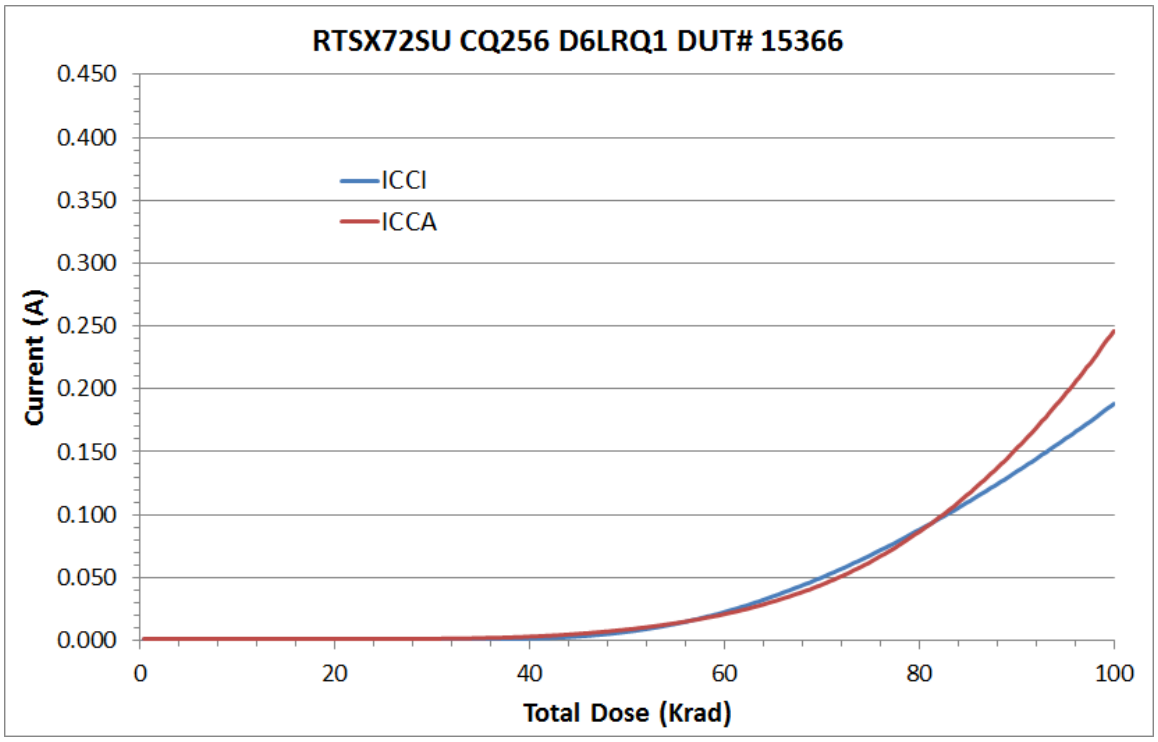


Figure 3 DUT 15366 Influx ICCA and ICCI

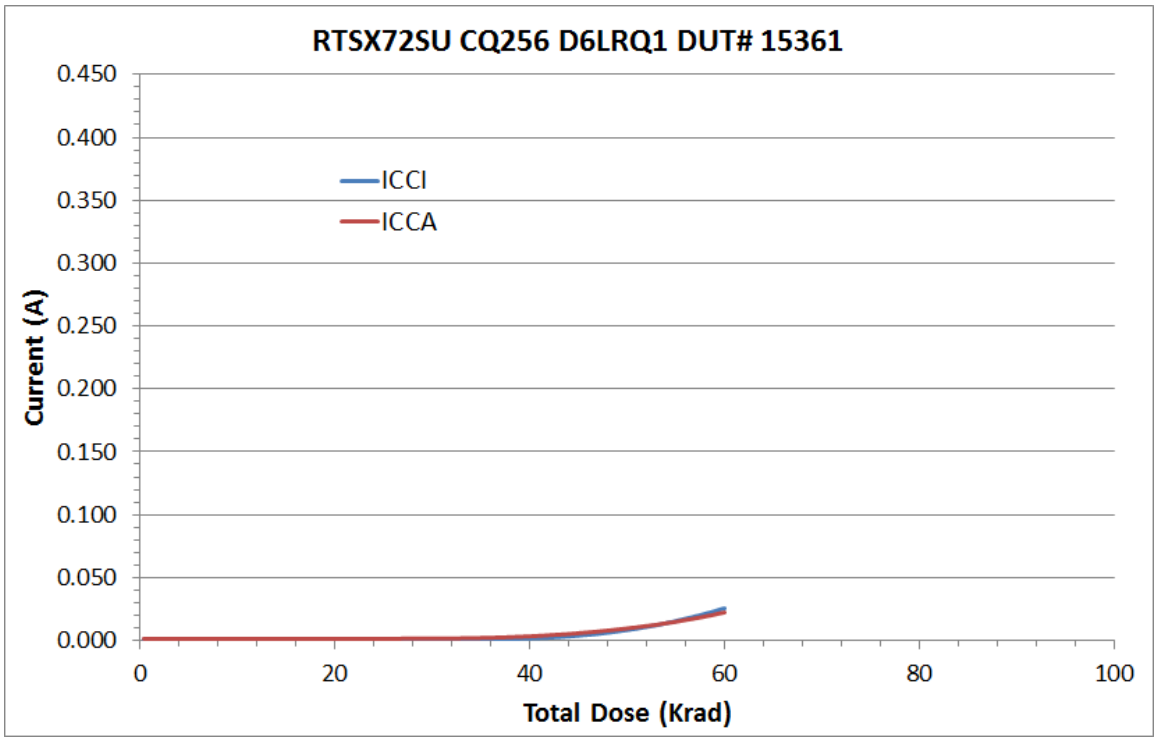


Figure 4 DUT 15361 Influx ICCA and ICCI

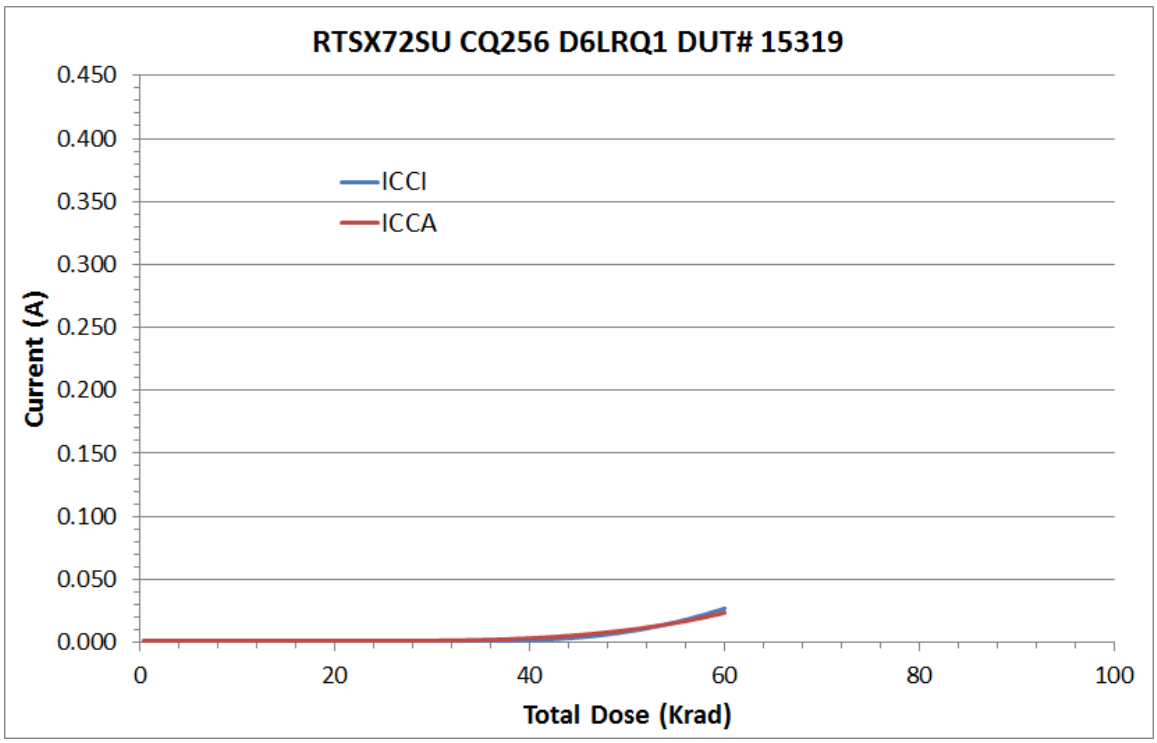


Figure 5 DUT 15319 Influx ICCA and ICCI

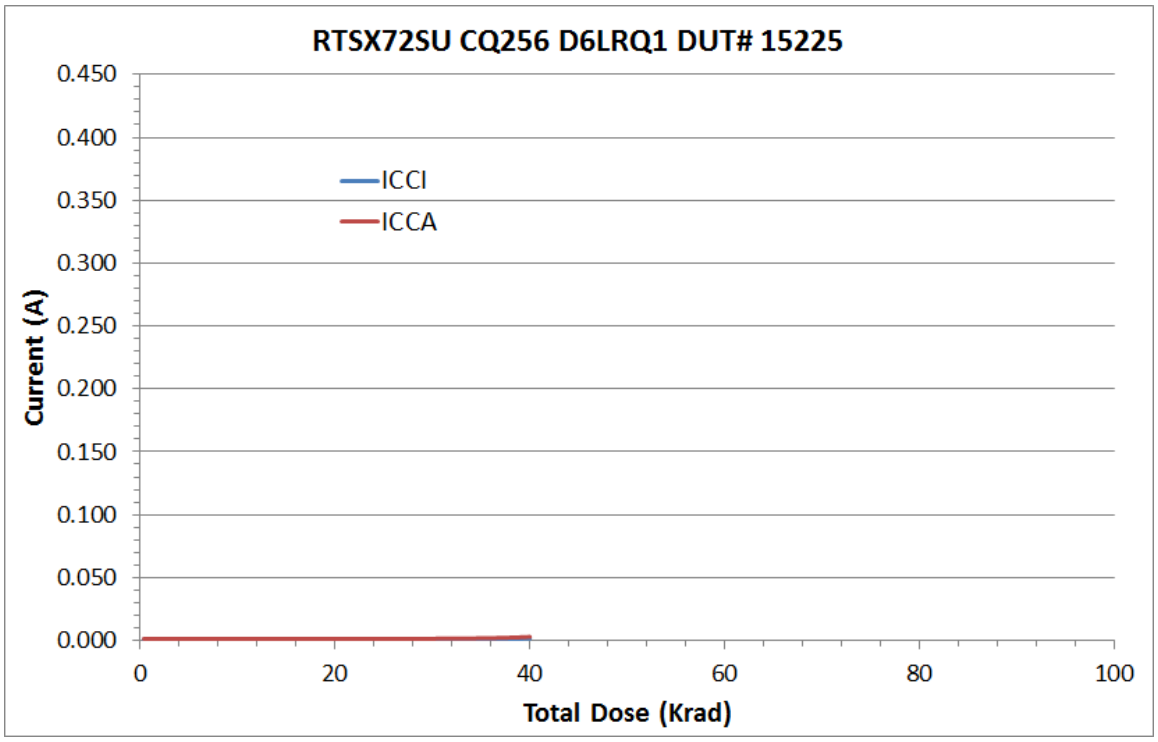


Figure 6 DUT 15225 Influx ICCA and ICCI

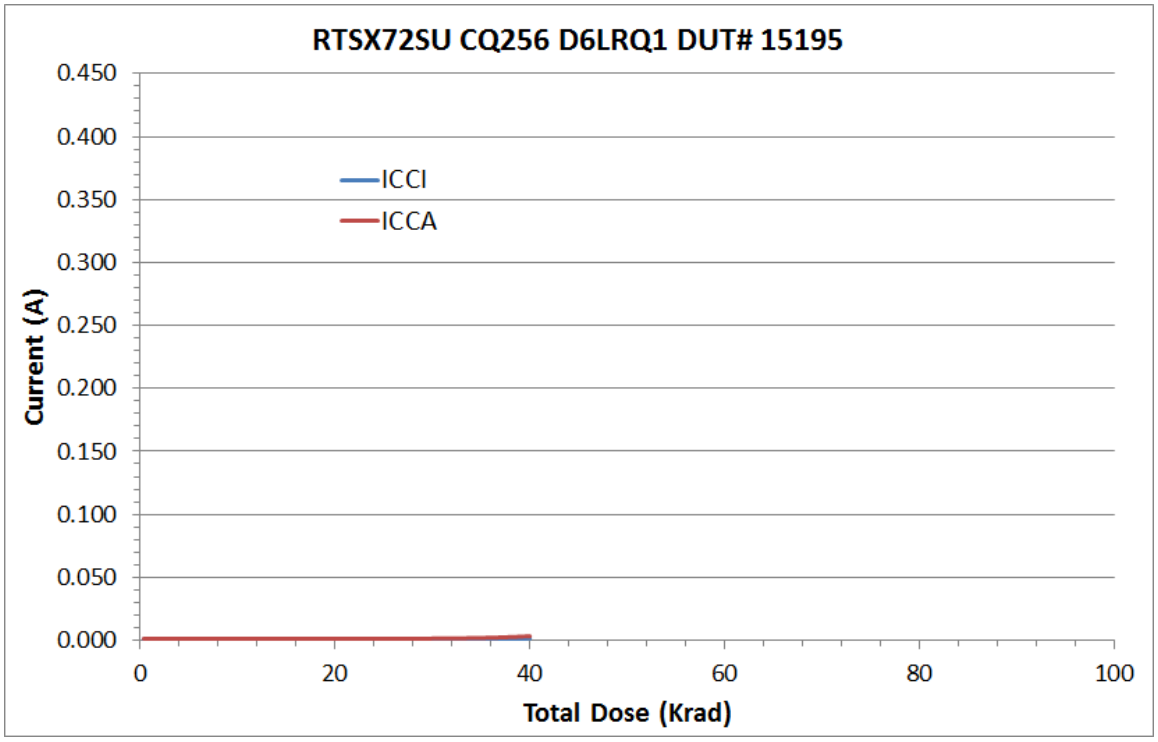


Figure 7 DUT 15195 Influx ICCA and ICCI

C. Input Logic Threshold (VIL/VIH)

Table 4a through Table 4c list the pre-irradiation and post-annealing input logic thresholds.

Some parameters of certain samples show more post-annealing shift, which could be caused by measurement sensitivity from the setup, as no obvious dose dependence is seen.

Table 4a Pre-Irradiation and Post-Annealing Input Thresholds

DUT	15368 (100 krad)				15366 (100 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1160	1135	1495	1425	1125	1180	1545	1425
DAH/QA0H	1440	1425	1460	1390	1405	1415	1495	1375
ENCNTRH/YO0H	1460	1450	1445	1380	1455	1435	1435	1370
IDII0/IDIO0	1400	1360	1480	1405	1380	1360	1470	1420
IDII1/IDIO1	1385	1460	1445	1370	1420	1455	1455	1365
IDII2/IDIO2	1340	1420	1400	1450	1275	1210	1405	1375
IDII3/IDIO3	1475	1425	1405	1360	1380	1420	1425	1355
IDII4/IDIO4	1435	1400	1385	1385	1420	1370	1380	1365
IDII5/IDIO5	1225	1115	1460	1405	1425	1120	1425	1400
IDII6/IDIO6	1425	1340	1445	1365	1410	1380	1405	1370
IDII7/IDIO7	1450	1435	1400	1360	1475	1420	1470	1355

Table 4b Pre-Irradiation and Post-Annealing Input Thresholds

DUT	15361 (60 krad)				15319 (60 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1125	1145	1545	1430	1115	1145	1565	1430
DAH/QA0H	1410	1410	1470	1375	1405	1420	1465	1375
ENCNTRH/YO0H	1000	1435	1780	1375	1440	1425	1435	1370
IDII0/IDIO0	1380	1375	1485	1410	1385	1375	1475	1430
IDII1/IDIO1	1500	1470	1465	1380	1460	1465	1410	1370
IDII2/IDIO2	1340	1425	1450	1380	1225	1225	1380	1430
IDII3/IDIO3	1475	1425	1425	1360	1440	1420	1390	1355
IDII4/IDIO4	1425	1315	1375	1340	1420	1405	1385	1335
IDII5/IDIO5	1415	1115	1435	1405	1410	1115	1400	1405
IDII6/IDIO6	1420	1370	1395	1375	1405	1380	1415	1350
IDII7/IDIO7	1455	1435	1495	1360	1440	1430	1385	1360

Table 4c Pre-Irradiation and Post-Annealing Input Thresholds

DUT	15225 (40 krad)				15195 (40 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1130	1140	1545	1495	1145	1165	1535	1495
DAH/QA0H	1405	1425	1460	1450	1440	1475	1470	1435
ENCNTRH/YO0H	1440	1450	1440	1390	1450	1455	1445	1390
IDII0/IDIO0	1440	1385	1420	1425	1395	1380	1480	1460
IDII1/IDIO1	1480	1470	1455	1420	1395	1480	1430	1400
IDII2/IDIO2	1235	1305	1385	1375	1245	1435	1400	1380
IDII3/IDIO3	1465	1445	1410	1390	1470	1445	1410	1385
IDII4/IDIO4	1425	1410	1420	1360	1435	1415	1375	1395
IDII5/IDIO5	1320	1265	1490	1400	1315	1240	1425	1415
IDII6/IDIO6	1385	1380	1390	1370	1415	1405	1395	1405
IDII7/IDIO7	1420	1435	1400	1385	1450	1455	1485	1385

E. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-annealing VOL/VOH are listed in Tables 5 and 6. The post-annealing data are within the specification limits.

Table 5 Pre-Irradiation and Post-Annealing VOL (mV) at Various Sinking Current

Sourcing Current	15368 (100 krad)		15366 (100 krad)		15361 (60 krad)		15319 (60 krad)		15225 (40 krad)		15195 (40 krad)	
	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
1 mA	10	11	10	11	10	10	10	11	10	11	10	11
12 mA	117	123	117	124	116	121	120	125	117	123	119	124
20 mA	195	204	196	205	193	202	200	208	196	205	198	207
50 mA	490	512	493	515	485	506	502	522	494	516	498	519
100 mA	1004	1046	1008	1051	993	1035	1027	1067	1009	1054	1018	1060

Table 6 Pre-Irradiation and Post-Annealing VOH (mV) at Various Sourcing Current

Sourcing Current	15368 (100 krad)		15366 (100 krad)		15361 (60 krad)		15319 (60 krad)		15225 (40 krad)		15195 (40 krad)	
	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
1 mA	4978	4976	4978	4976	4978	4978	4978	4978	4978	4979	4978	4979
8 mA	4842	4835	4845	4837	4843	4839	4844	4839	4846	4842	4843	4840
20 mA	4604	4587	4611	4594	4606	4595	4607	4596	4612	4602	4606	4597
50 mA	3953	3912	3974	3932	3957	3929	3966	3936	3979	3952	3962	3938
100 mA	2399	2243	2489	2345	2414	2330	2460	2371	2528	2460	2457	2394

F. Propagation Delay

Table 7 lists the pre-irradiation and post-annealing propagation delays, and also lists the radiation-induced degradations in percentage. The radiation delta in every case is well within the 10% degradation criterion; take the worst case for the design-margin consideration.

Table 7 Radiation-Induced Propagation-Delay Degradations

DUT	Total Dose	Pre-Irradiation (µs)	Post-Anneal (µs)	Degradation (%)
15368	100 krad	1.37	1.42	3.28%
15366	100 krad	1.43	1.46	2.46%
15361	60 krad	1.36	1.37	0.74%
15319	60 krad	1.38	1.40	1.09%
15225	40 krad	1.38	1.38	0.00%
15195	40 krad	1.34	1.34	0.37%

G. Transition Characteristics

Figure 9a to Figure 20b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is insignificant.

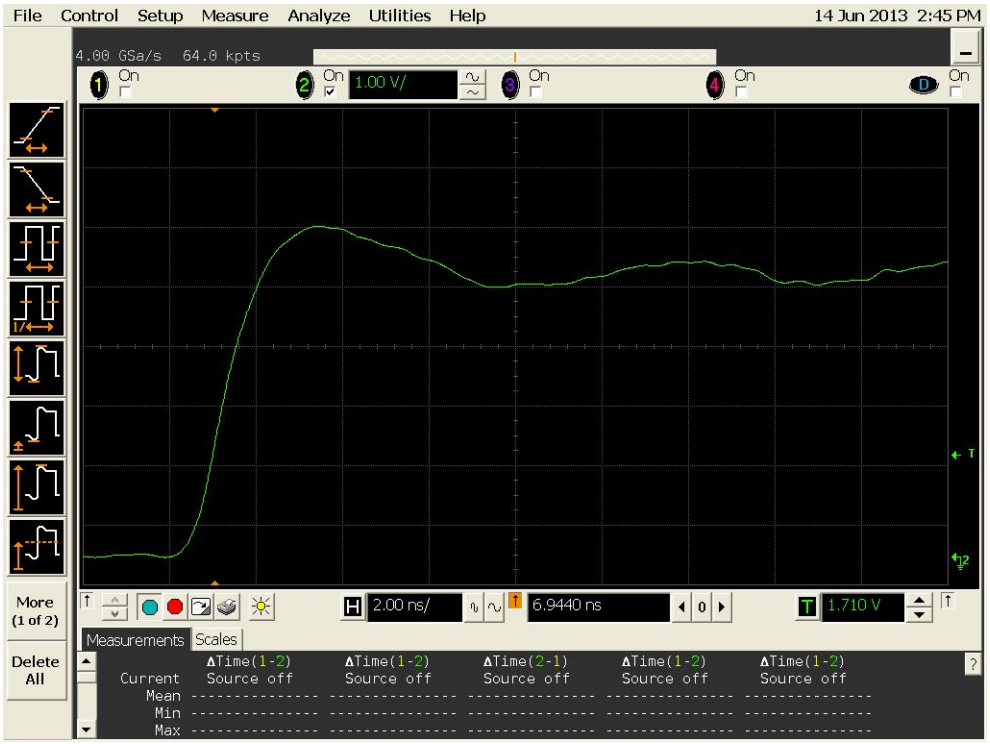


Figure 9a DUT 15368 Pre-Irradiation Rising Edge

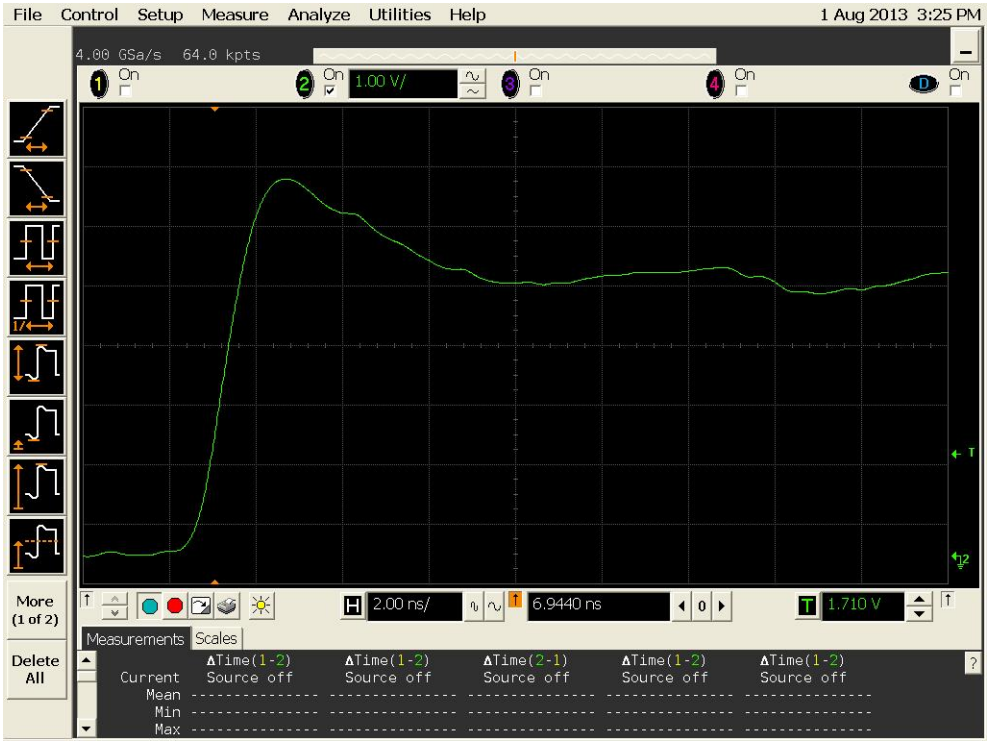


Figure 9b DUT 15368 Post-Annealing Rising Edge

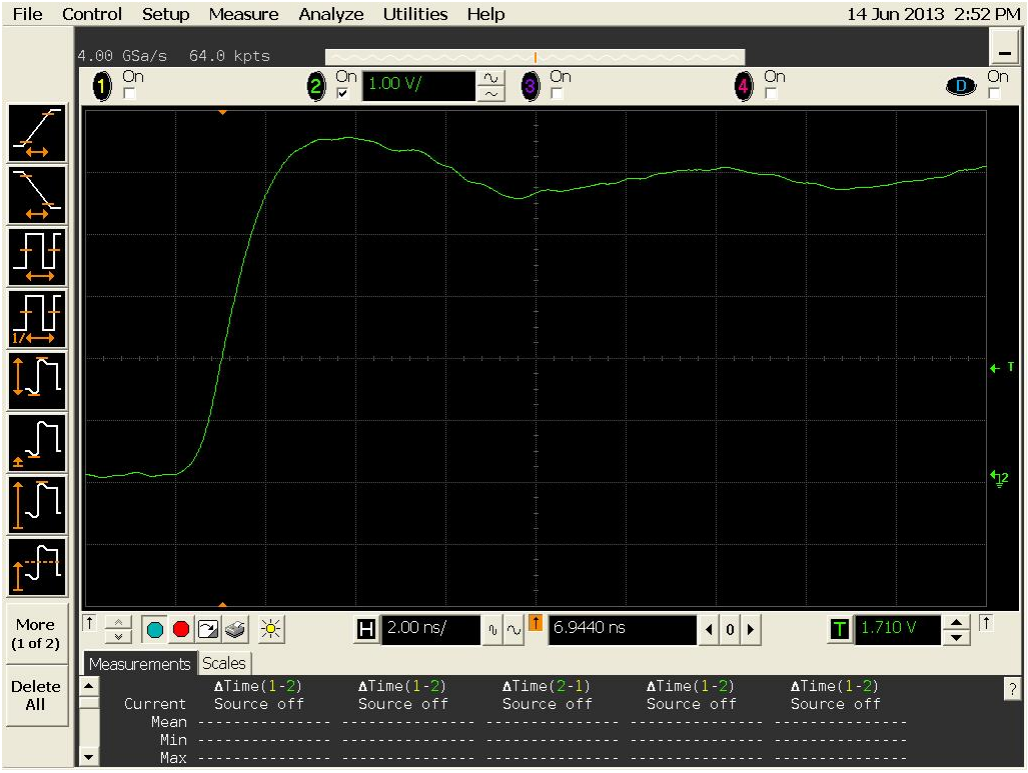


Figure 10a DUT 15366 Pre-Irradiation Rising Edge

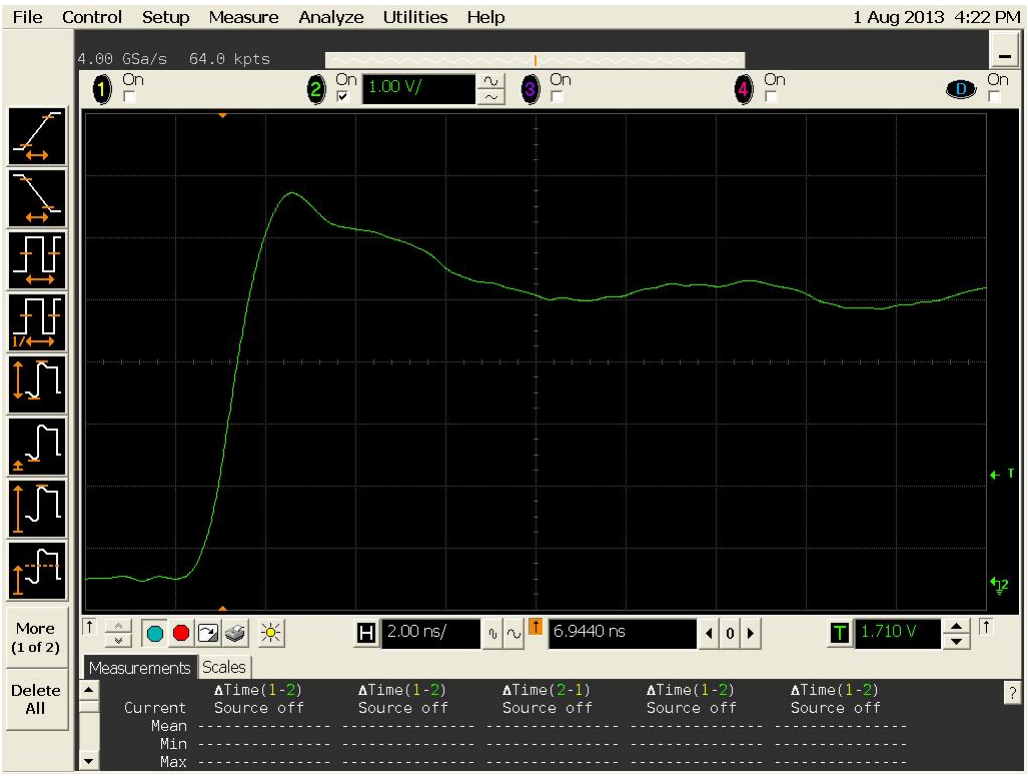


Figure 10b DUT 15366 Post-Annealing Rising Edge

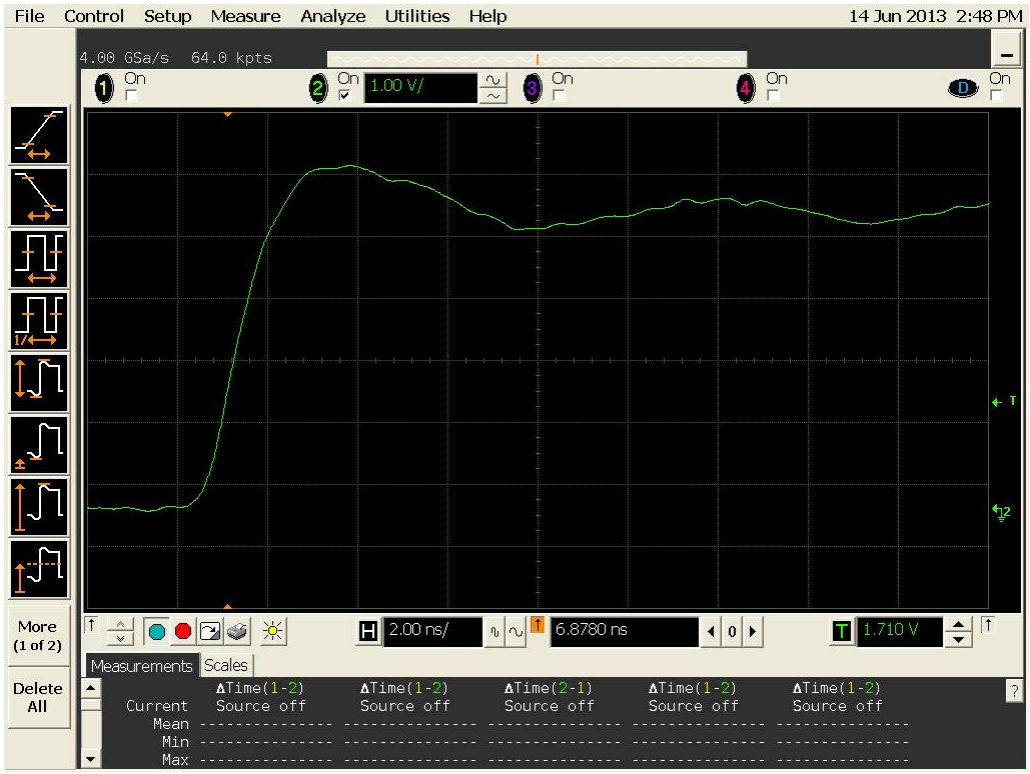


Figure 11a DUT 15361 Pre-Radiation Rising Edge

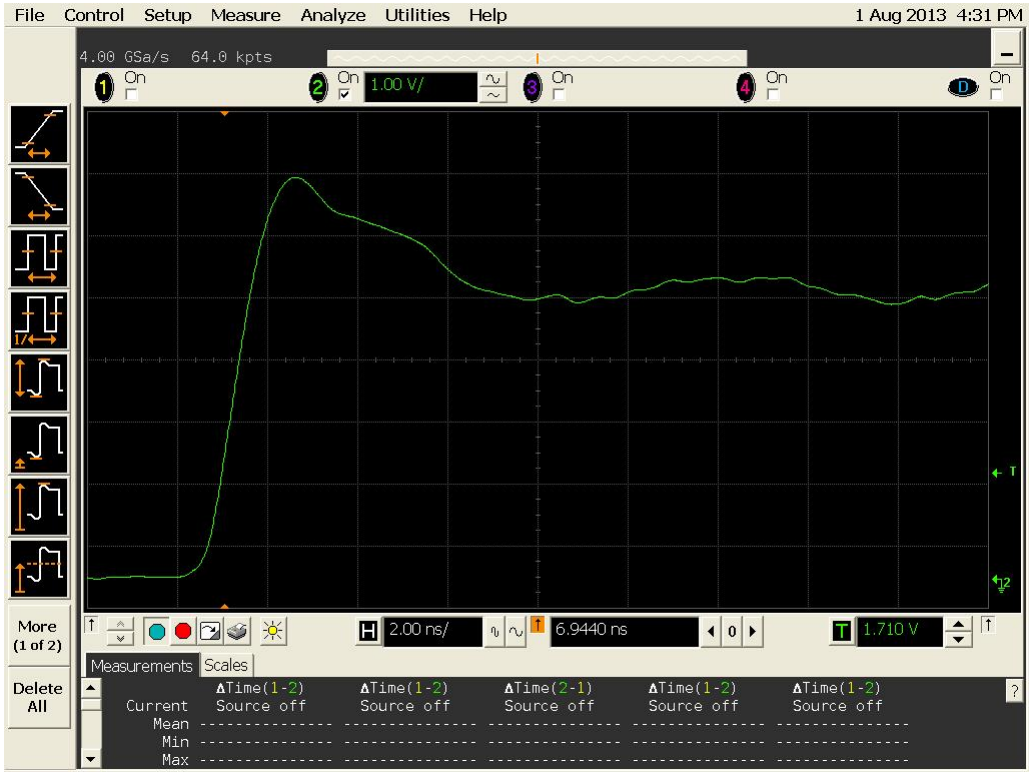


Figure 11b DUT 15361 Post-Annealing Rising Edge

Figure 12a DUT 15319 Pre-Irradiation Rising Edge

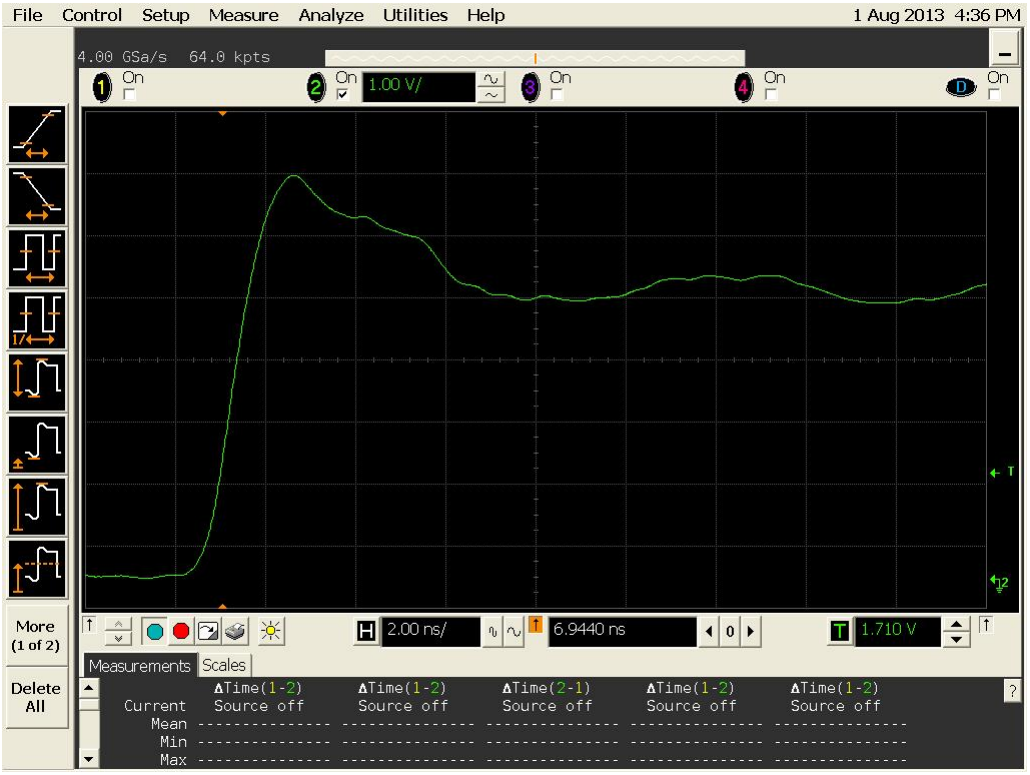


Figure 12b DUT 15319 Post-Annealing Rising Edge

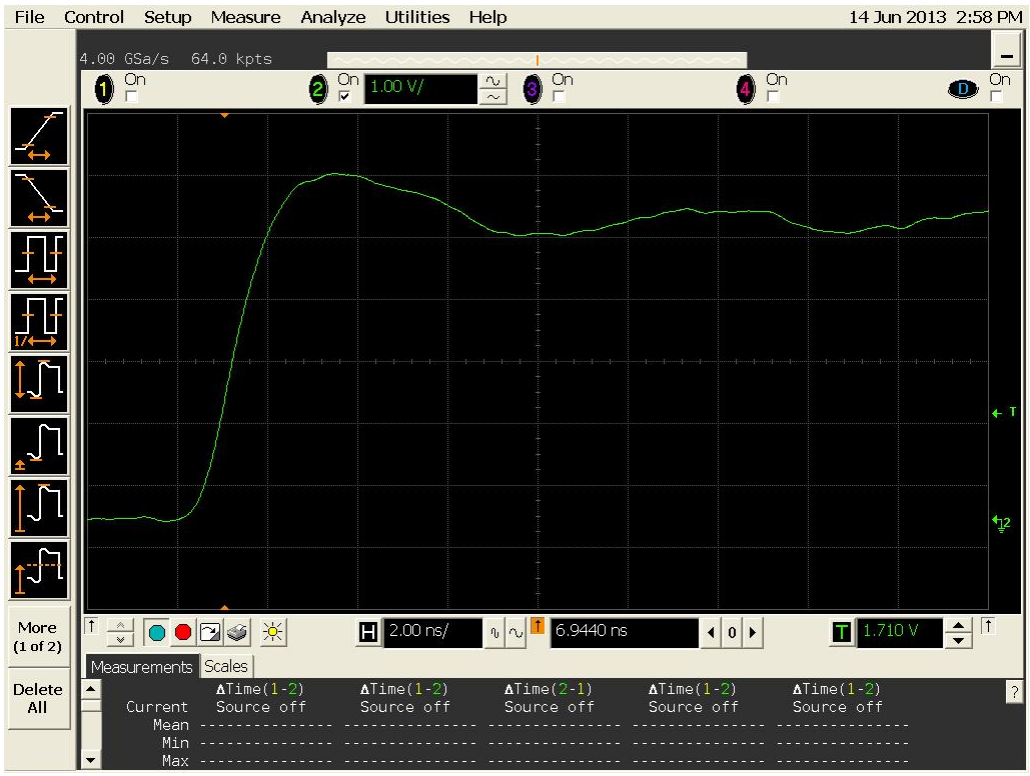


Figure 13a DUT 15225 Pre-Irradiation Rising Edge

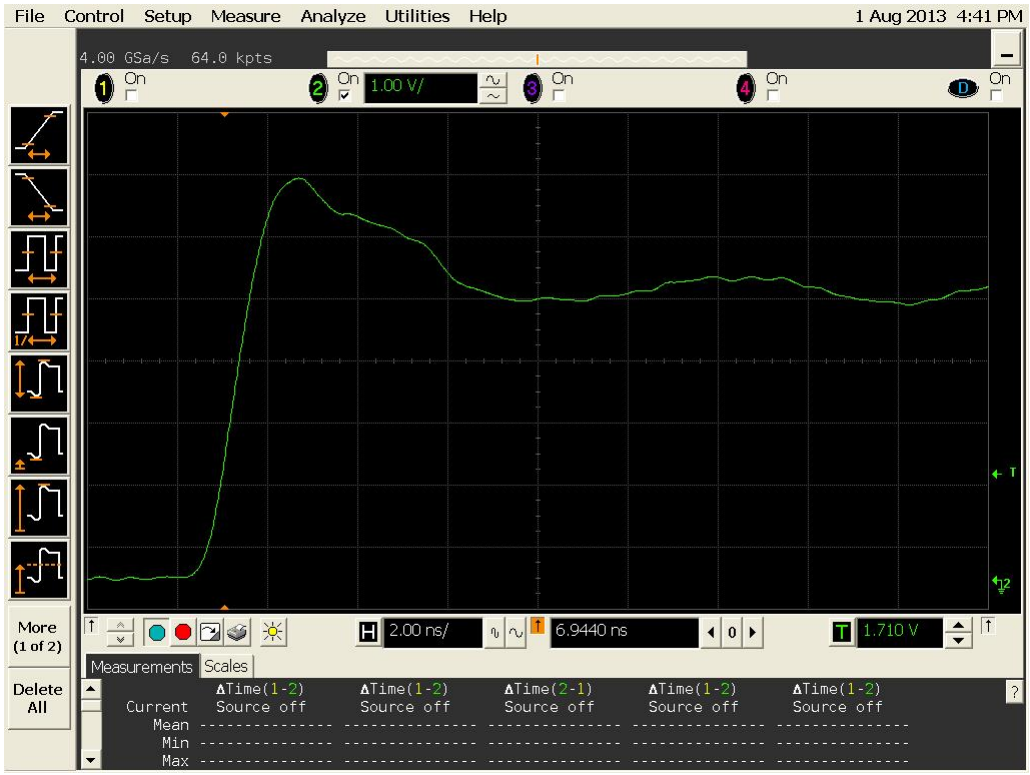


Figure 13b DUT 15225 Post-Annealing Rising Edge

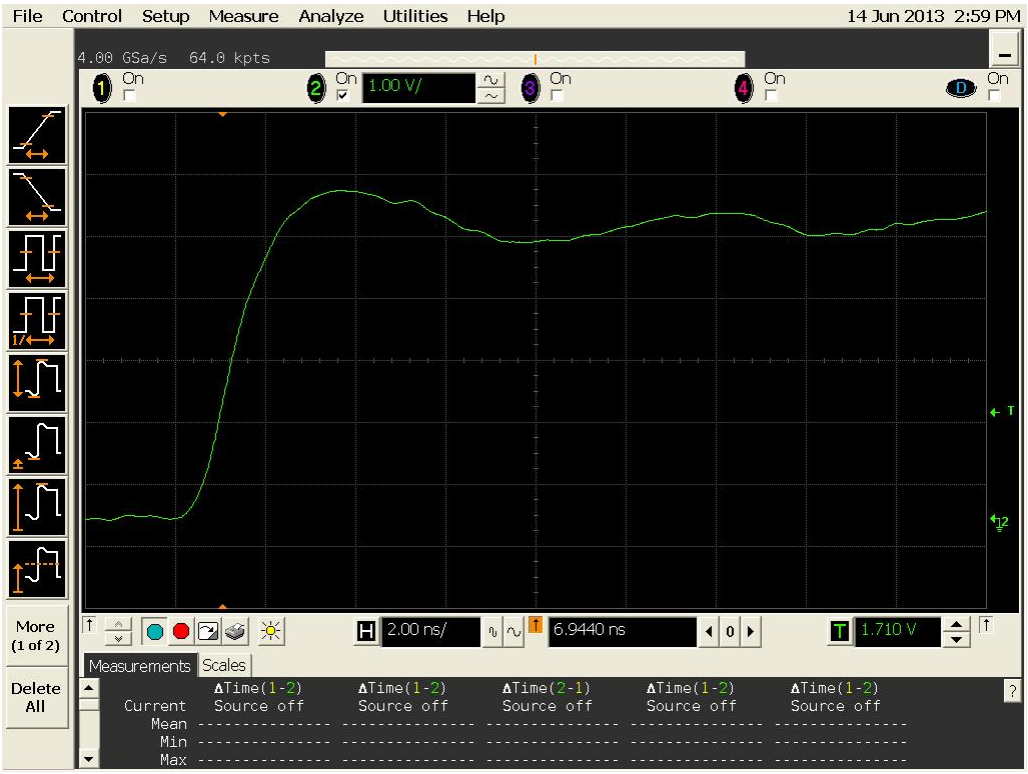


Figure 14a DUT 15195 Pre-Irradiation Rising Edge

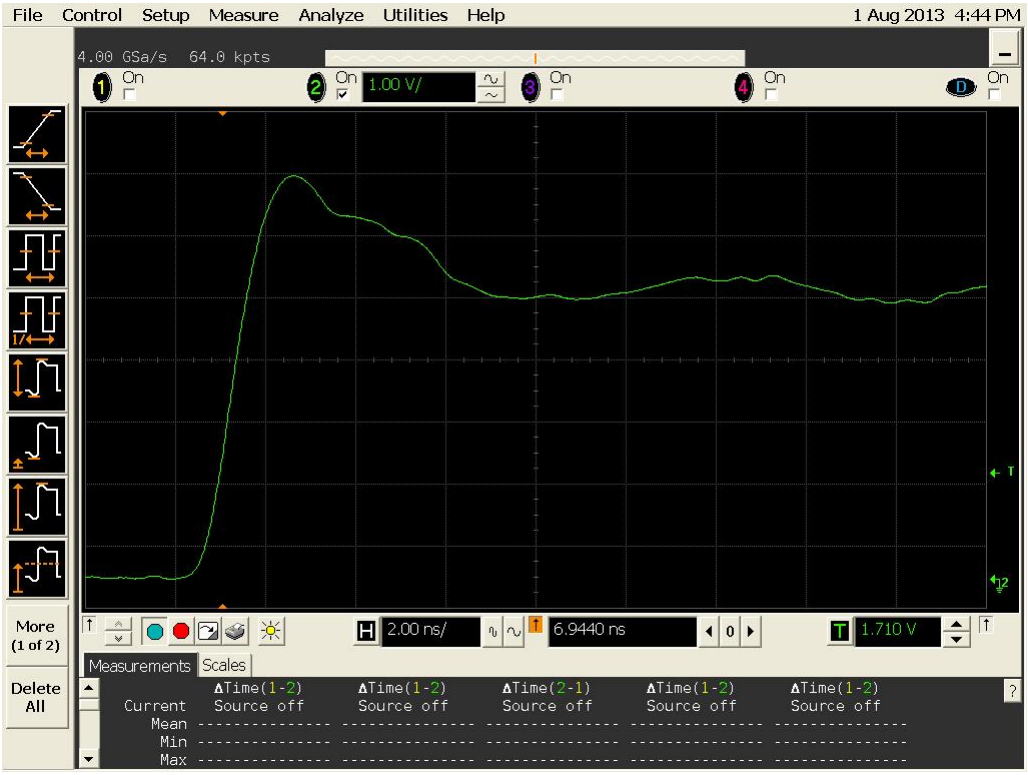


Figure 14b DUT 15195 Post-Annealing Rising Edge

Figure 15a DUT 15368 Pre-Radiation Falling Edge

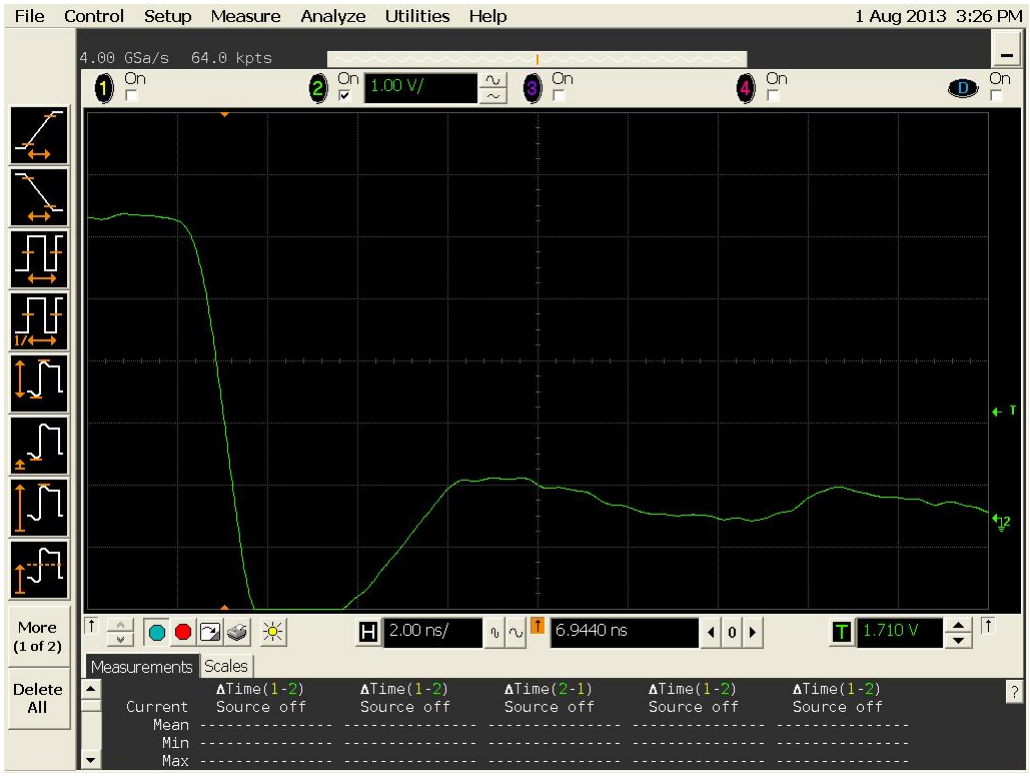


Figure 15b DUT 15368 Post-Annealing Falling Edge

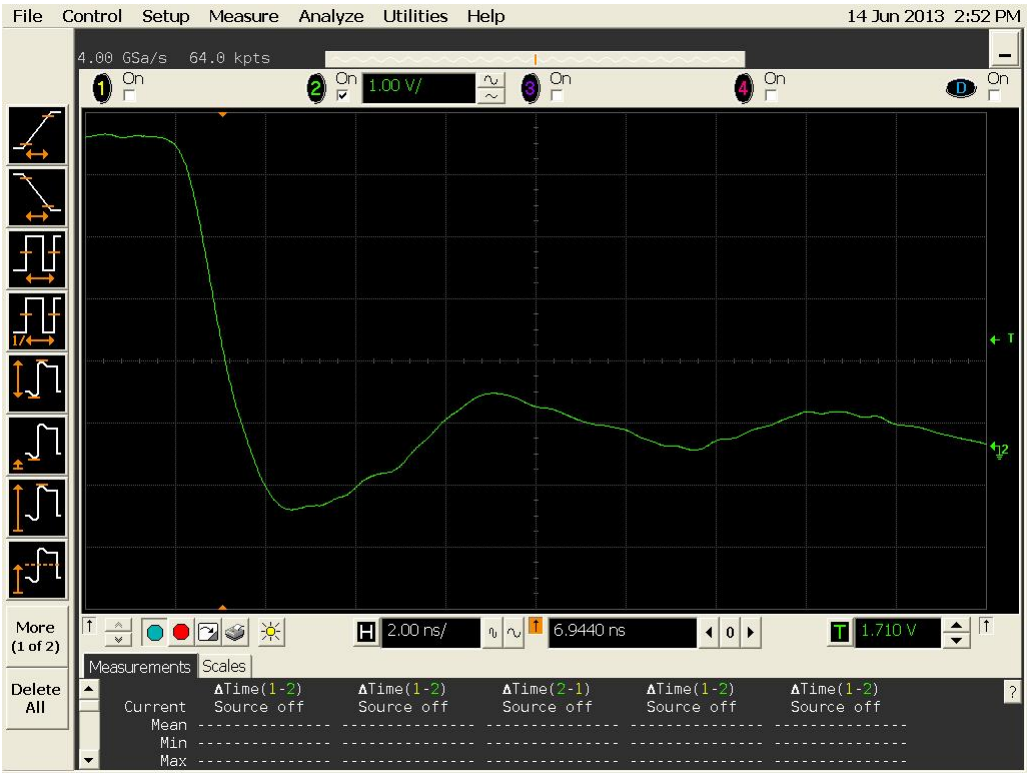


Figure 16a DUT 15366 Pre-Irradiation Falling Edge

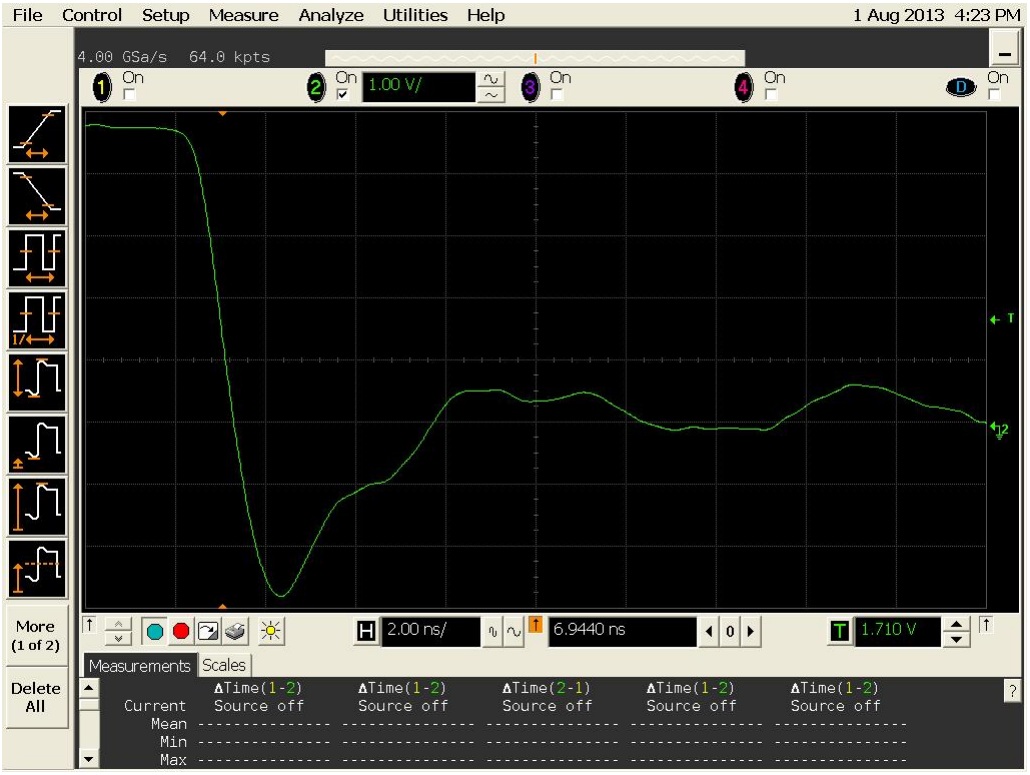


Figure 16b DUT 15366 Post-Annealing Falling Edge

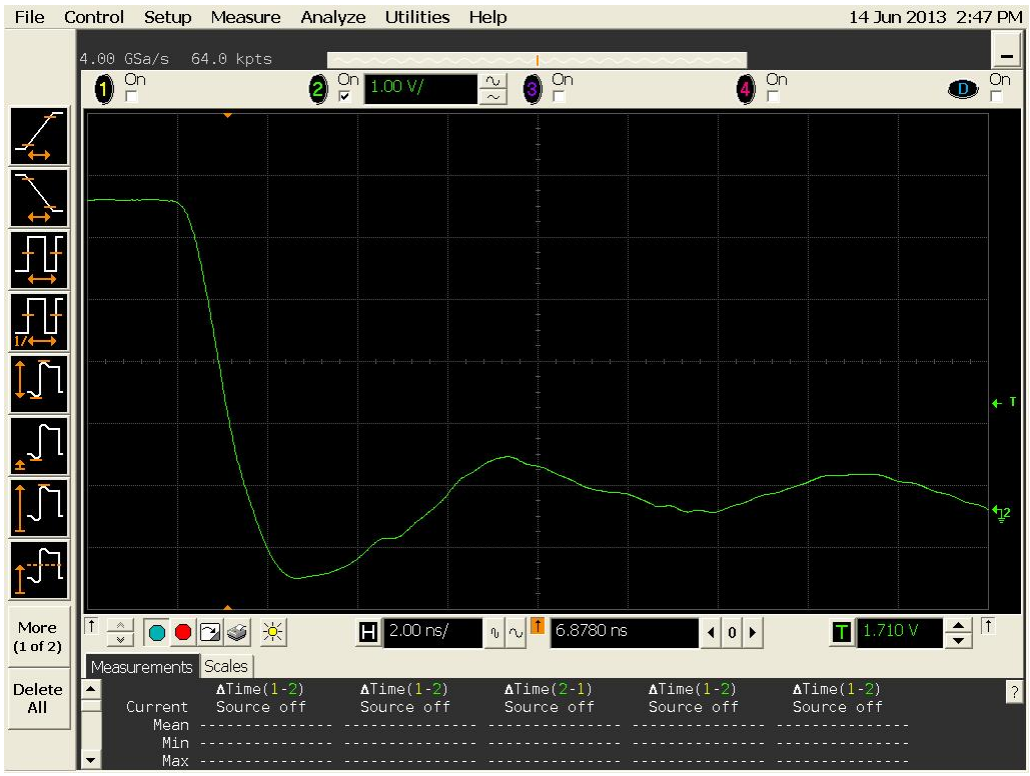


Figure 17a DUT 15361 Pre-Irradiation Falling Edge

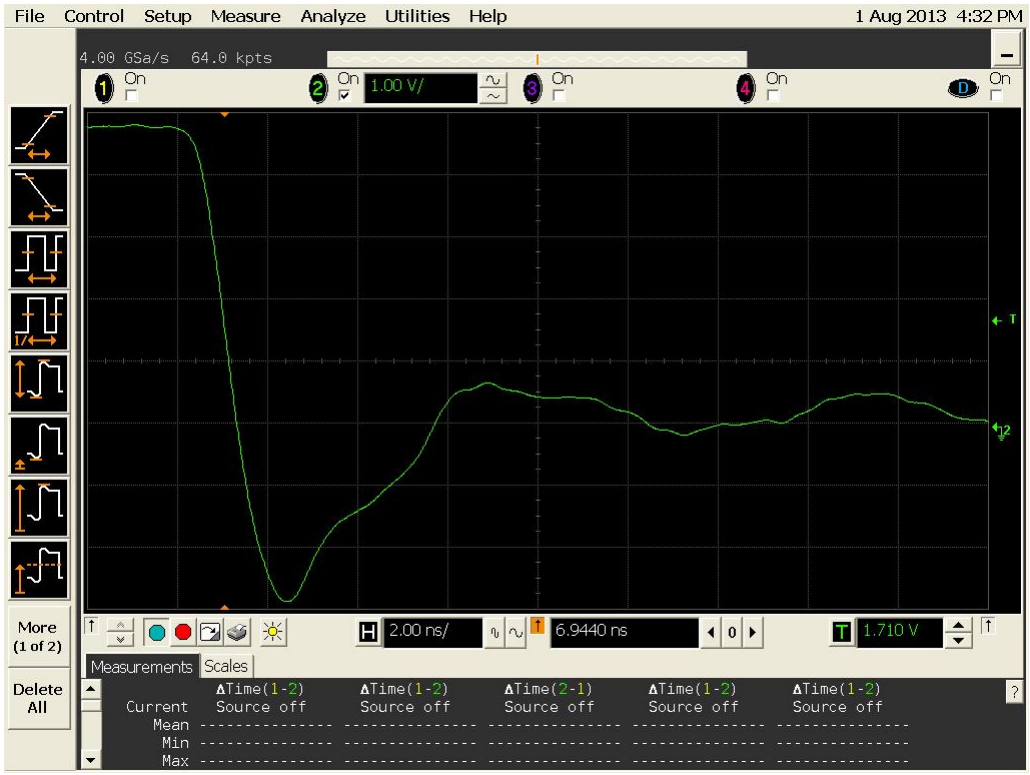


Figure 17b DUT 15361 Post-Annealing Falling Edge

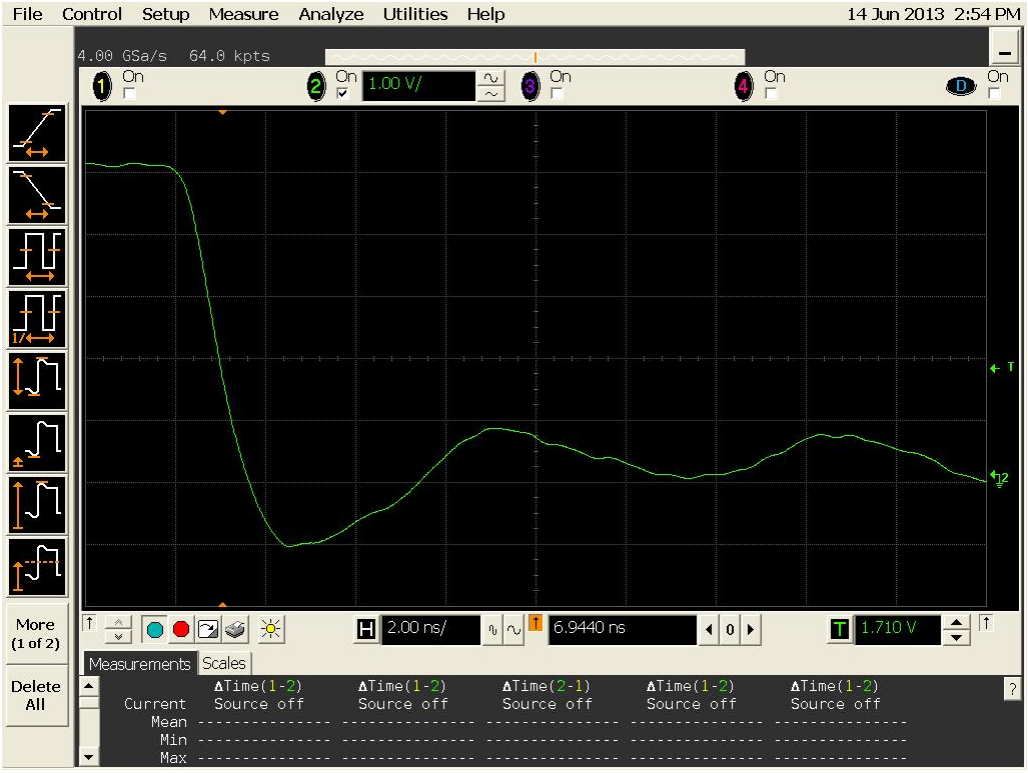


Figure 18a DUT 15319 Pre-Irradiation Falling Edge

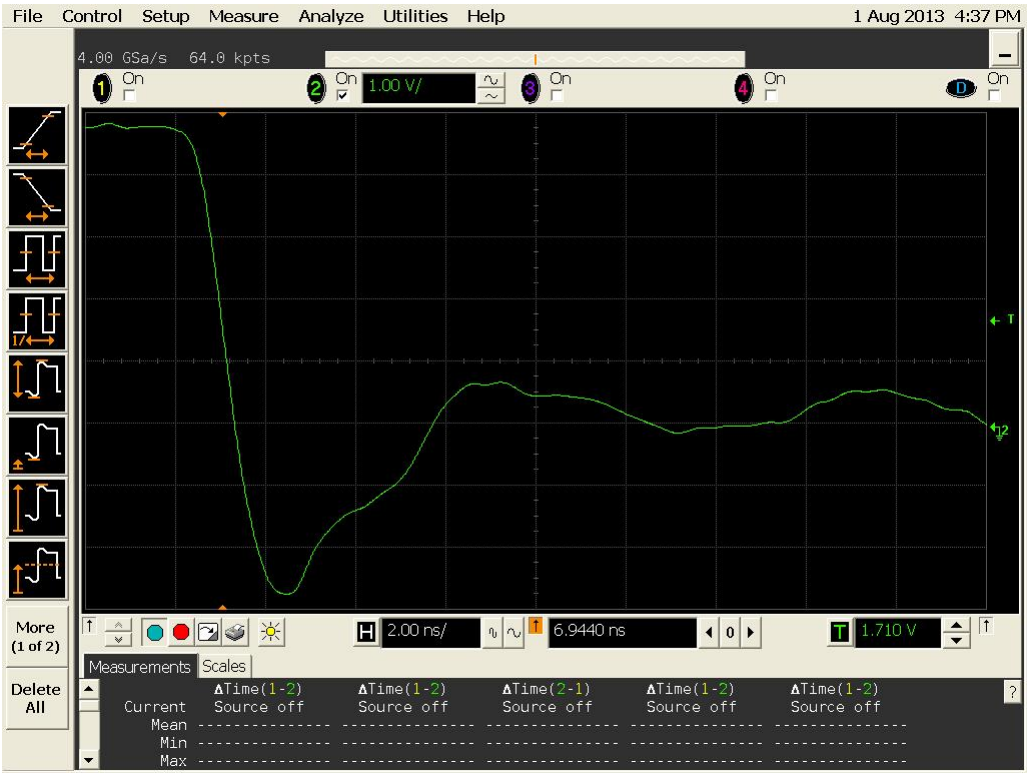


Figure 18b DUT 15319 Post-Annealing Falling Edge

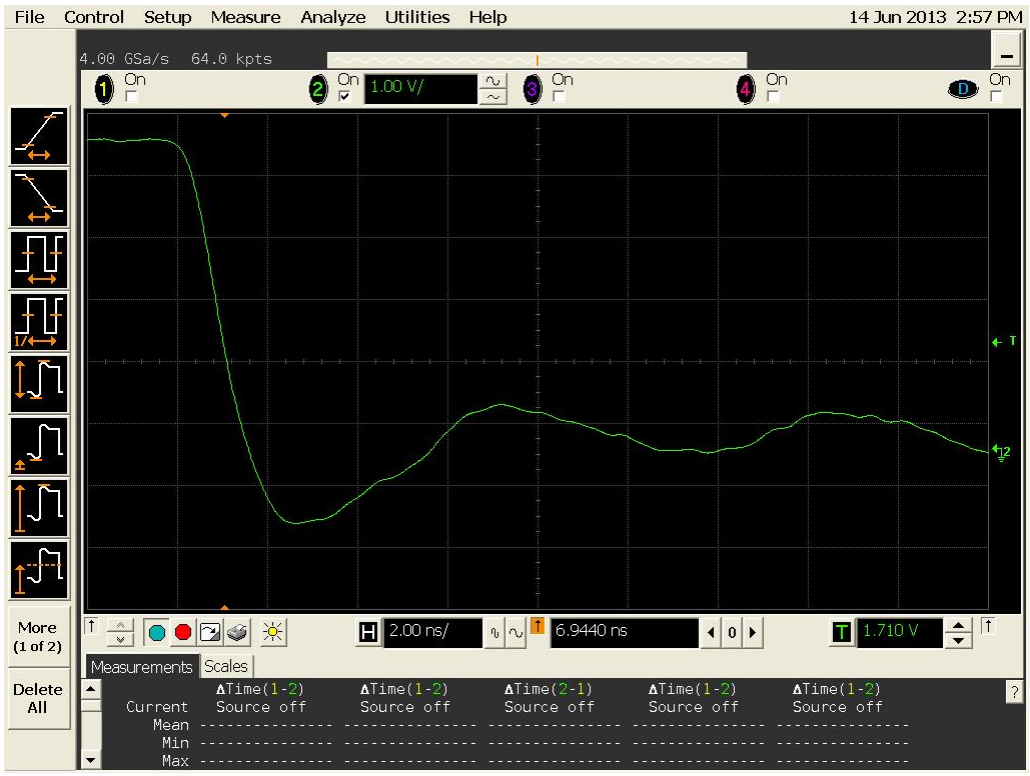


Figure 19a DUT 15225 Pre-Irradiation Falling Edge

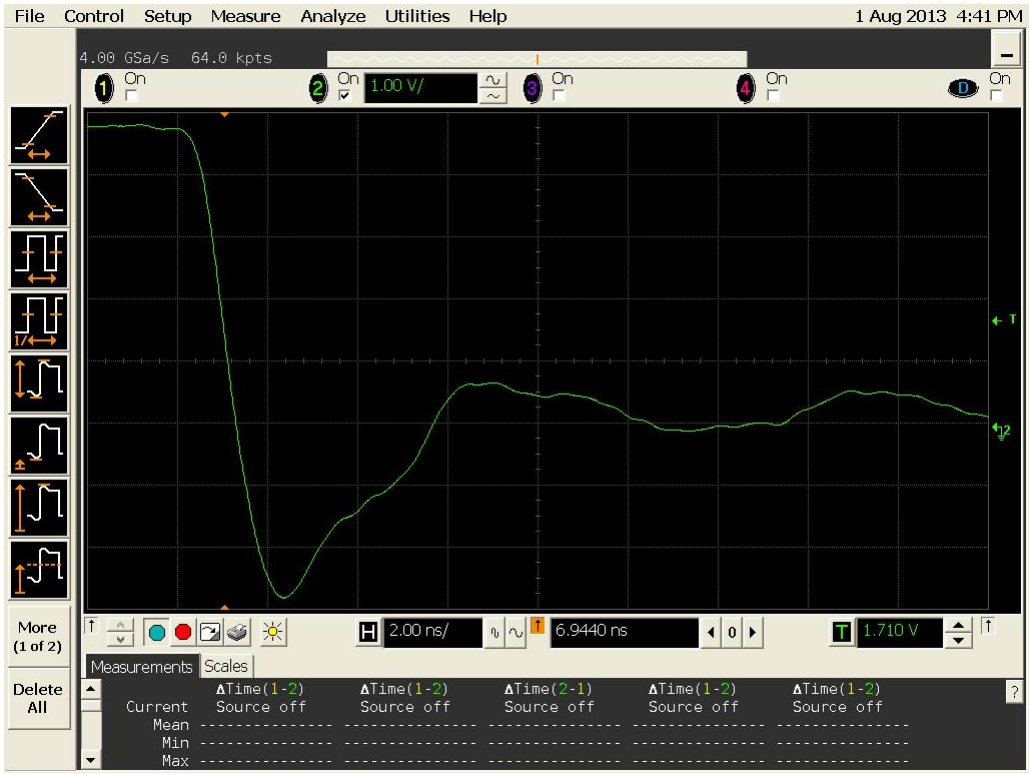


Figure 19b DUT 15225 Post-Annealing Falling Edge

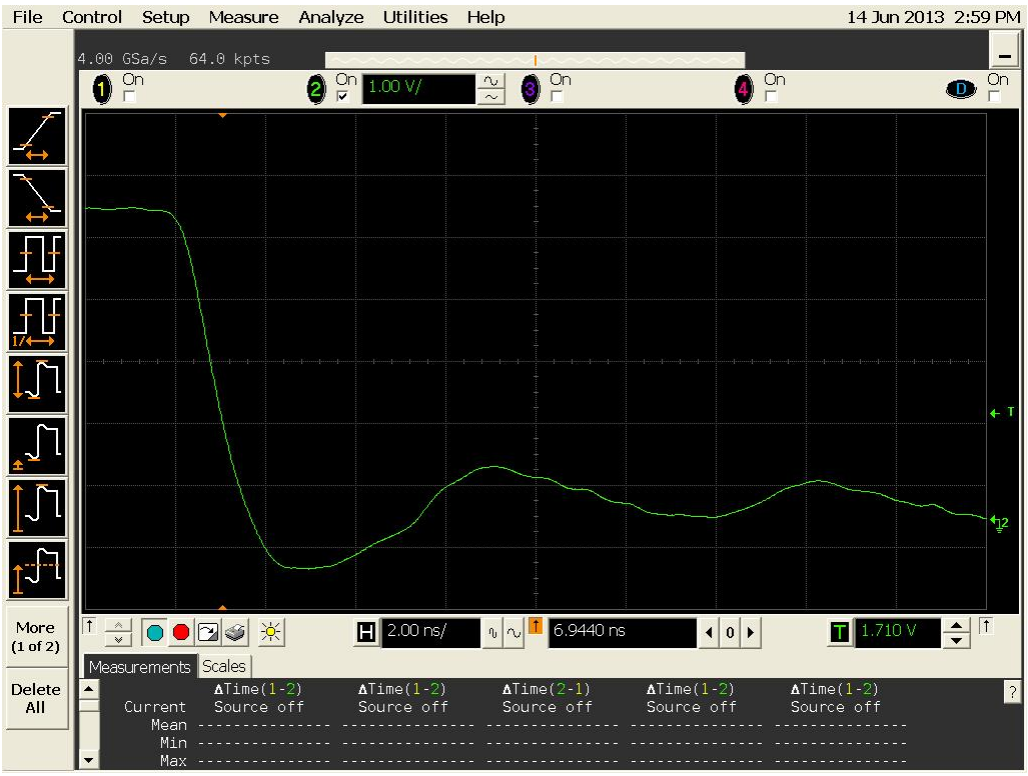


Figure 20a DUT 15195 Pre-Irradiation Falling Edge

Figure 20b DUT 15195 Post-Annealing Falling Edge

Appendix A: DUT Bias

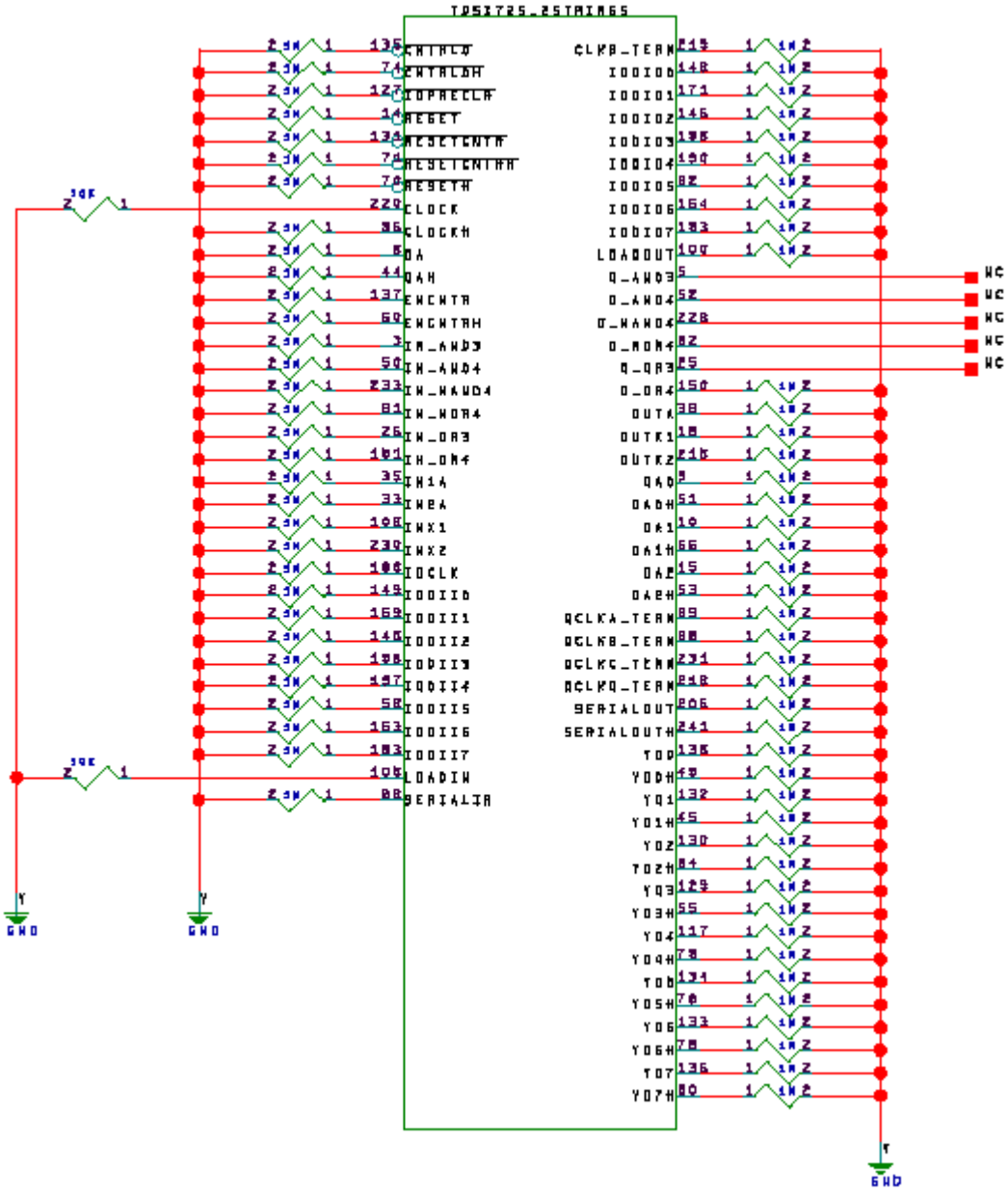


Figure A1 I/O Bias During Irradiation

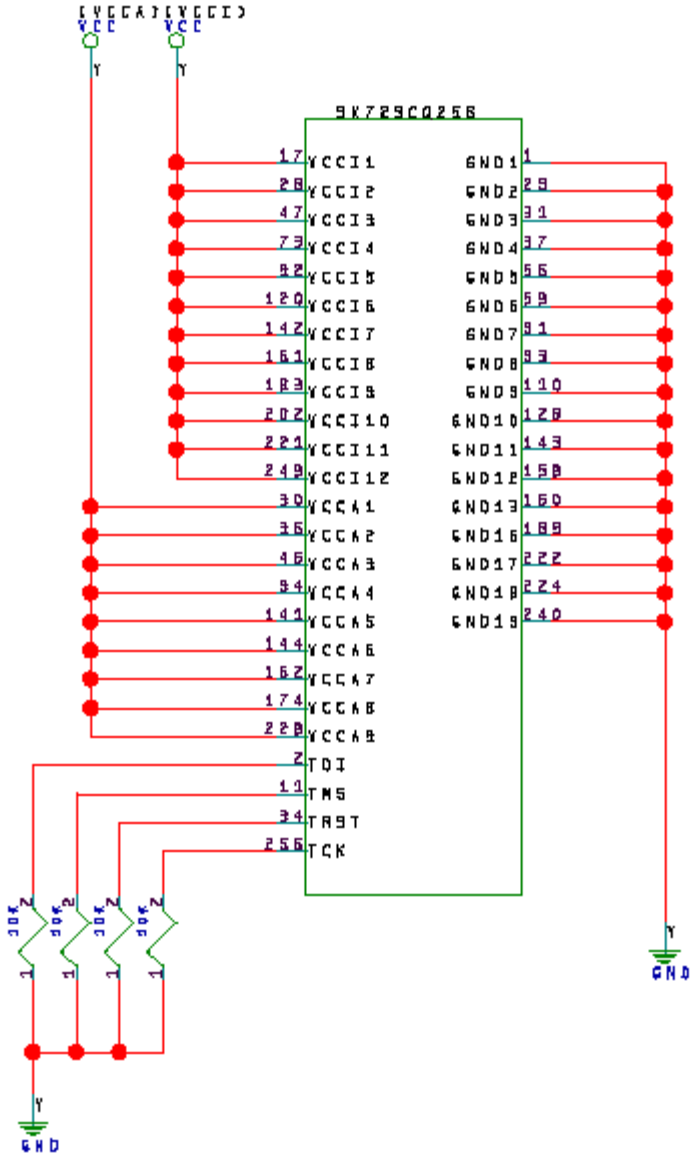
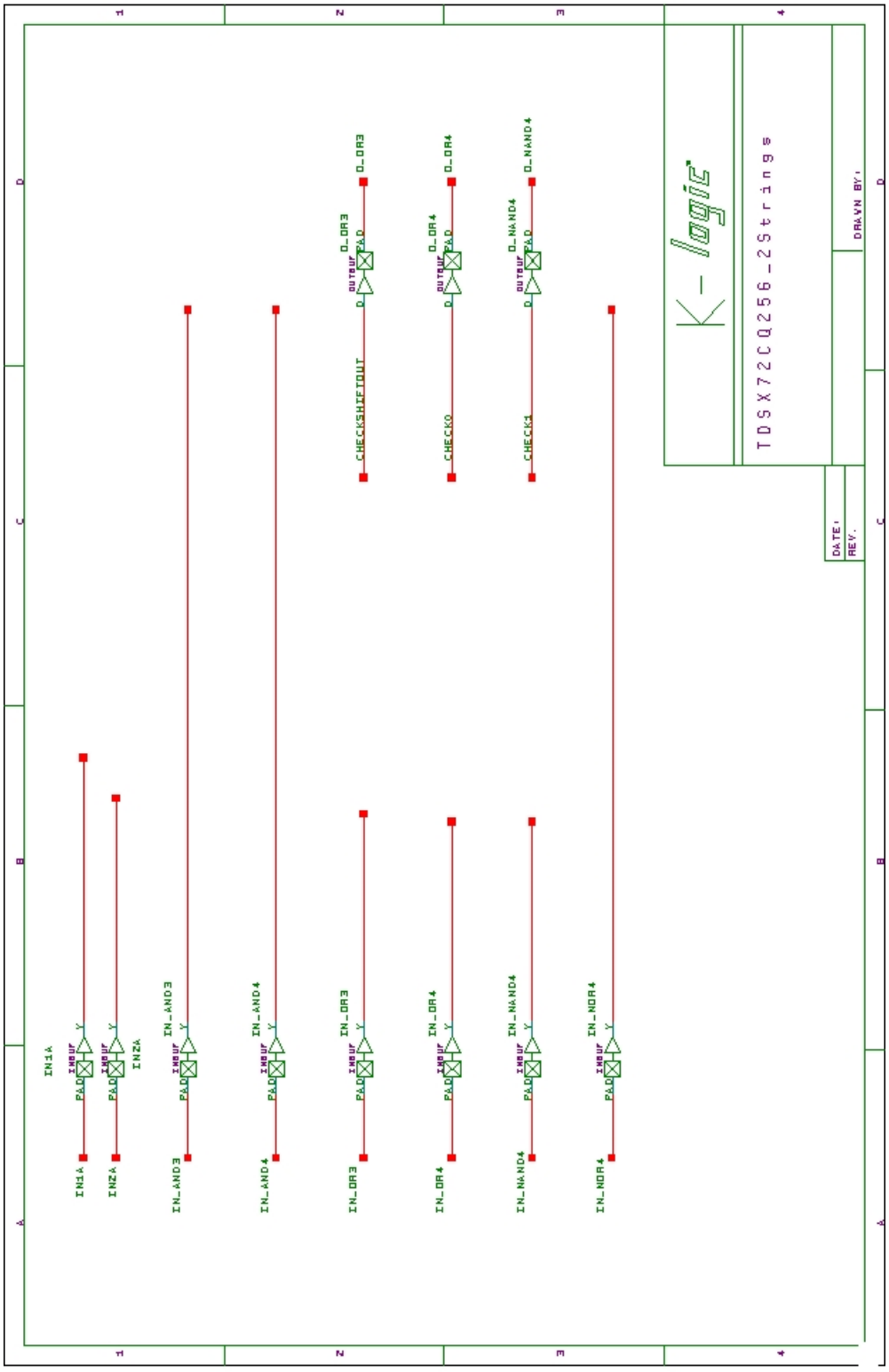
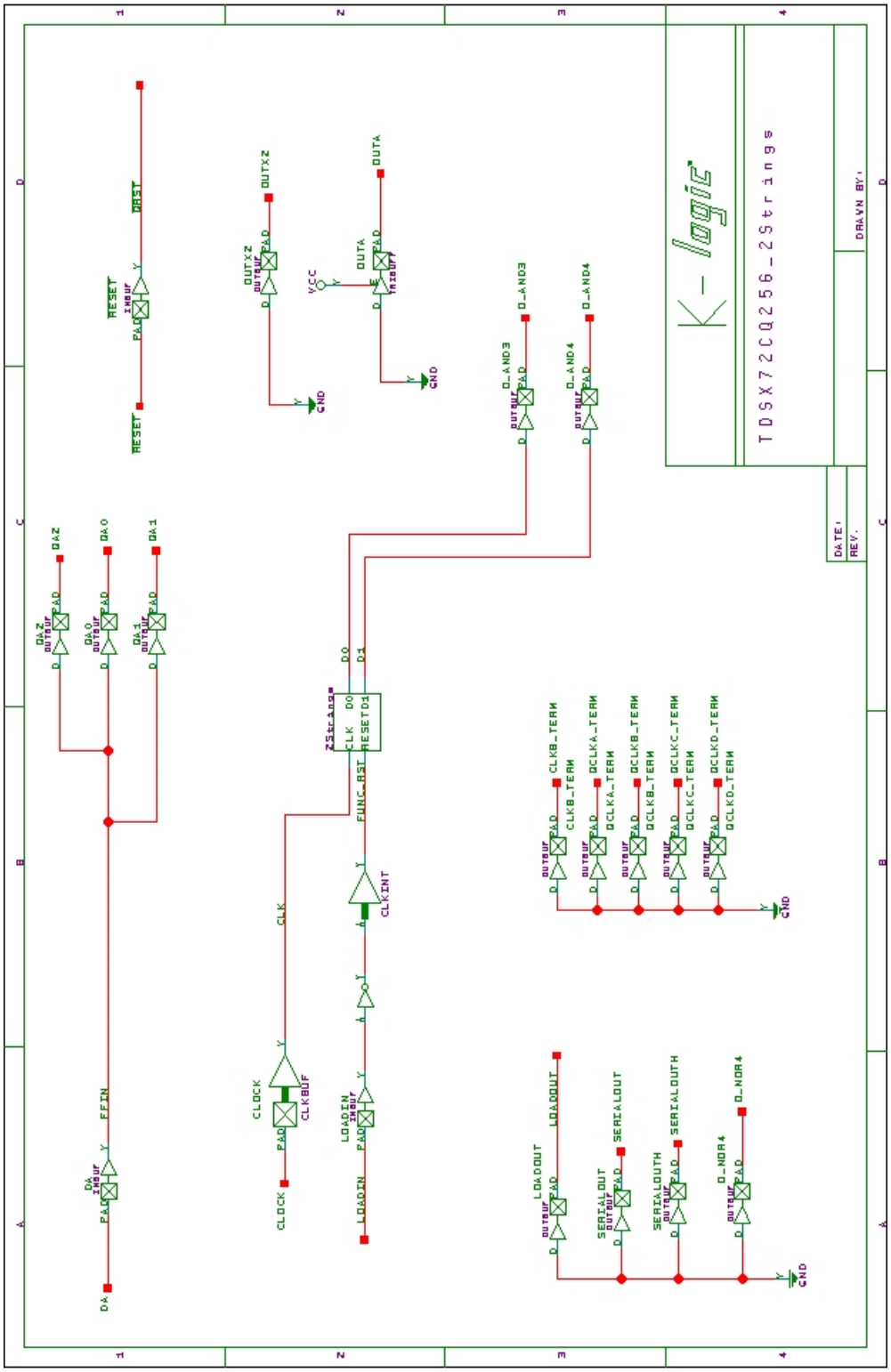
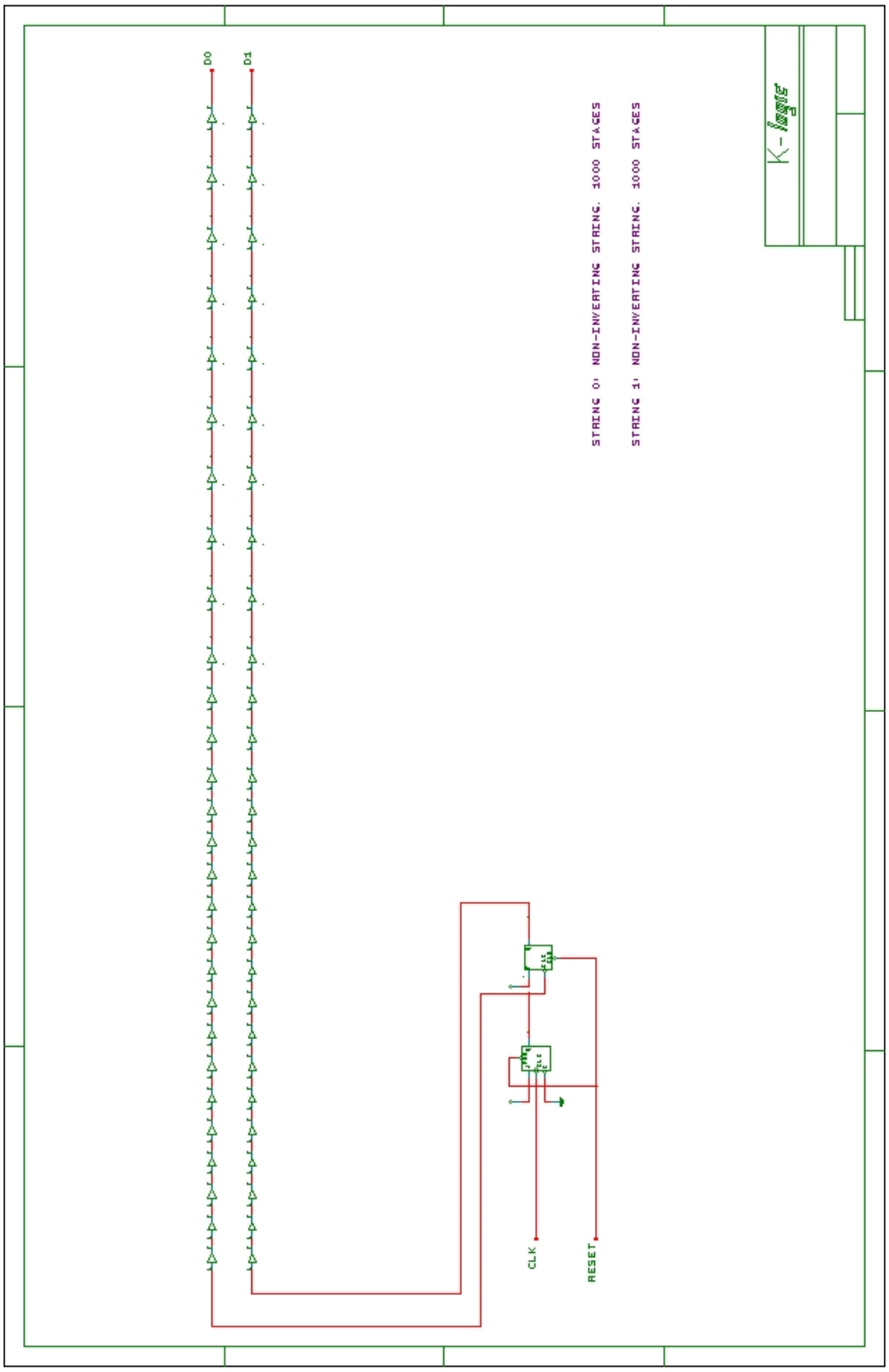


Figure A2 Power Supply, Ground, and Special Pins Bias During Irradiation

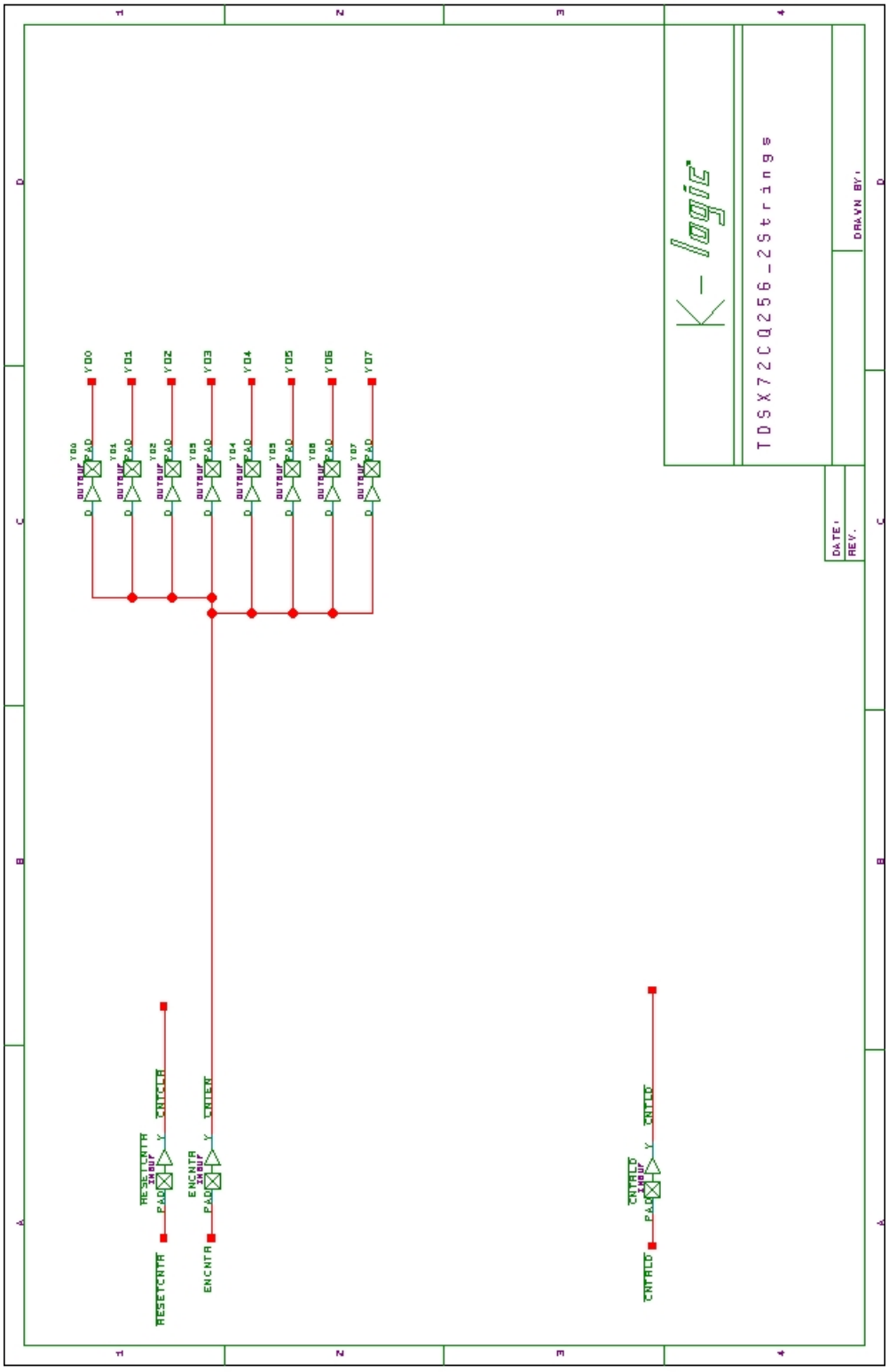
Appendix B: DUT Design Schematics

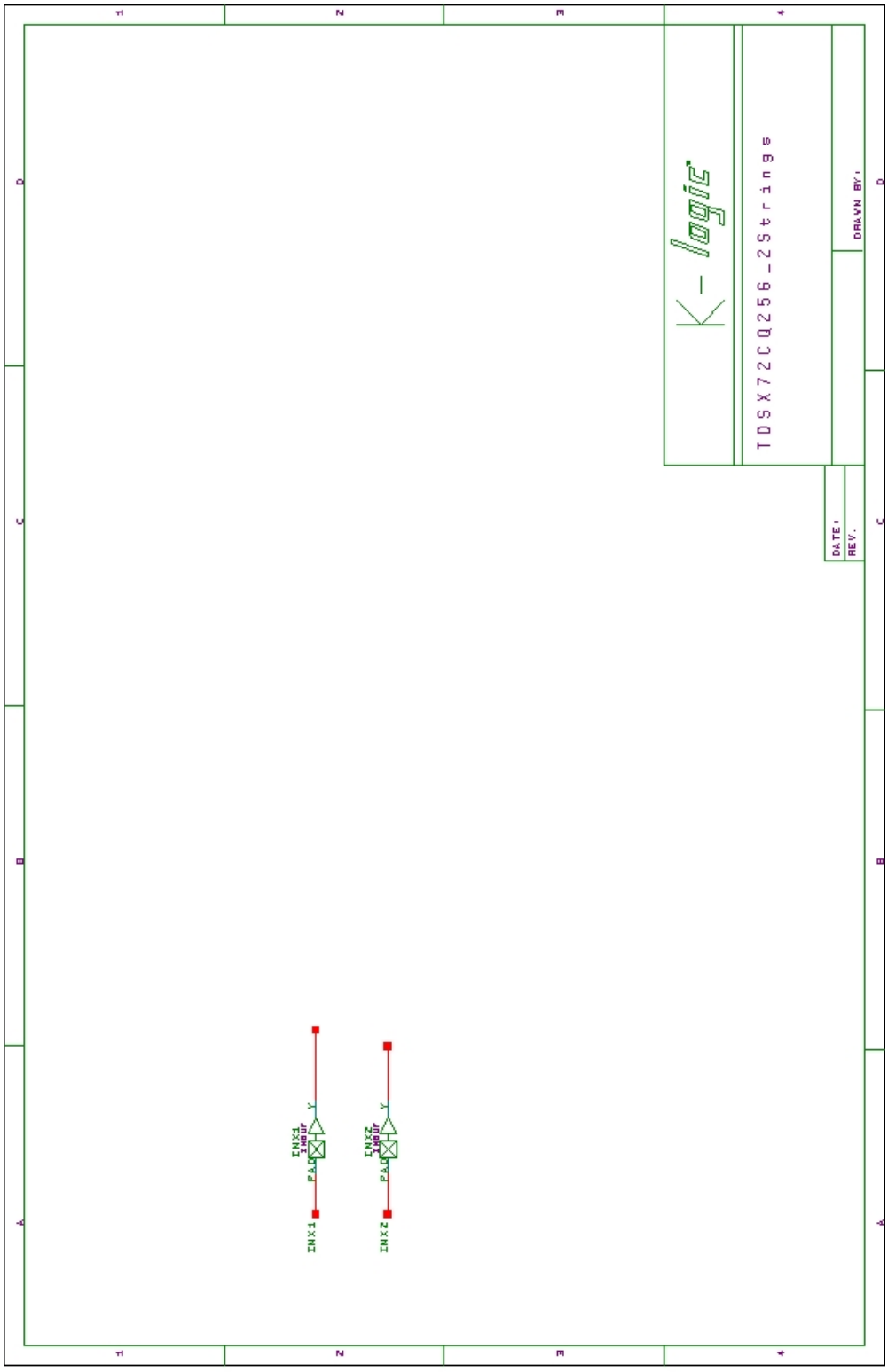


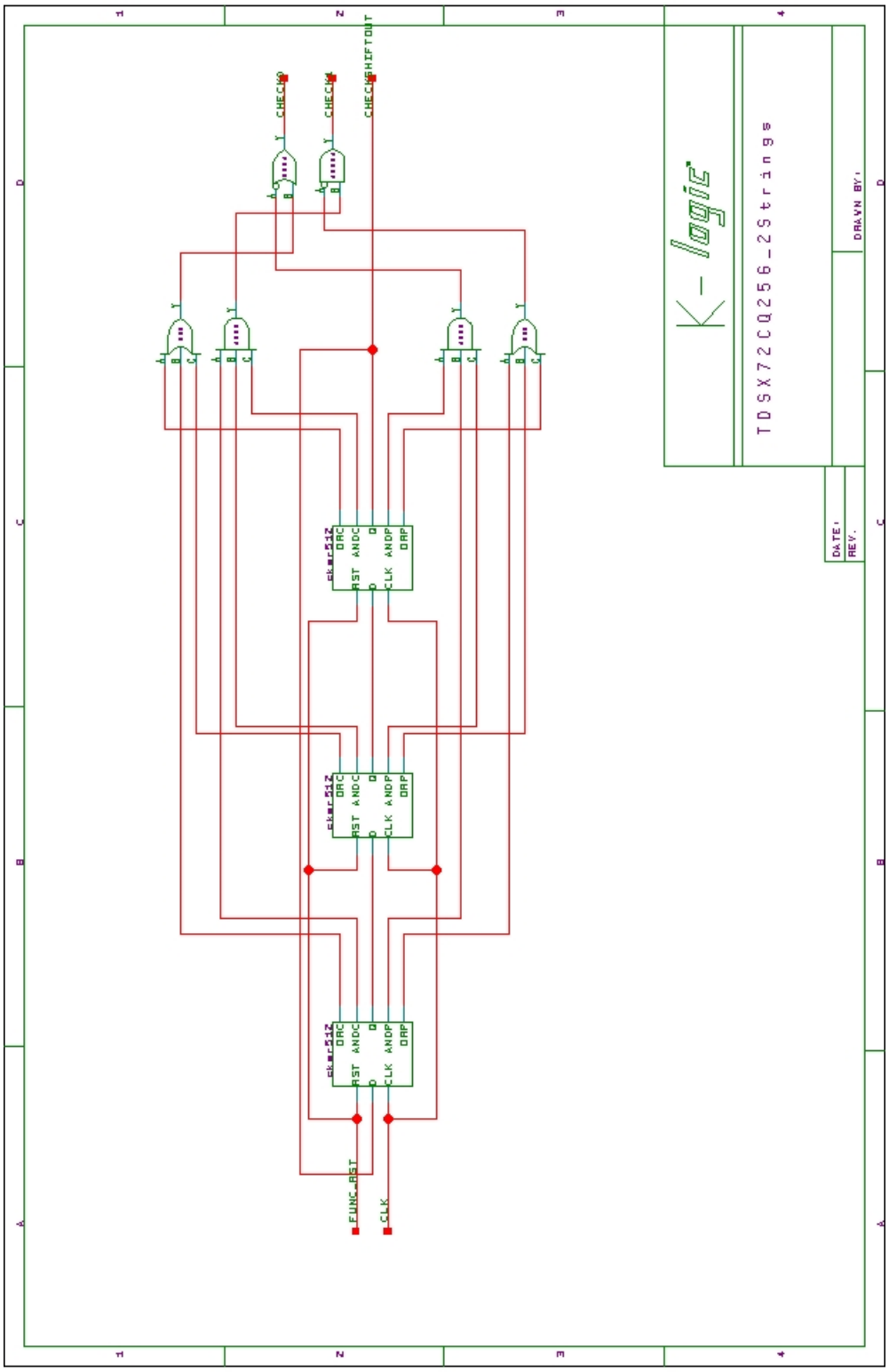

TDSX72CQ256_2Strings
K-logic
DRAWN BY:
DATE:
REV.
RESET
OUTXZ
OUTA
VCC
GND
D_AND3
D_AND4
DA2
DA0
DA1
DA
FFIN
ZStrings
CLK
D0
D1
RESET1
FUNC_RST
CLKINT
CLOCK
CLKBUF
LOADIN
CLKB_TERM
DCLKA_TERM
DCLKB_TERM
DCLKC_TERM
DCLKD_TERM
LOADOUT
SERIALOUT
SERIALOUTH
D_NOR4
PAD
OUTBUF
INBUF

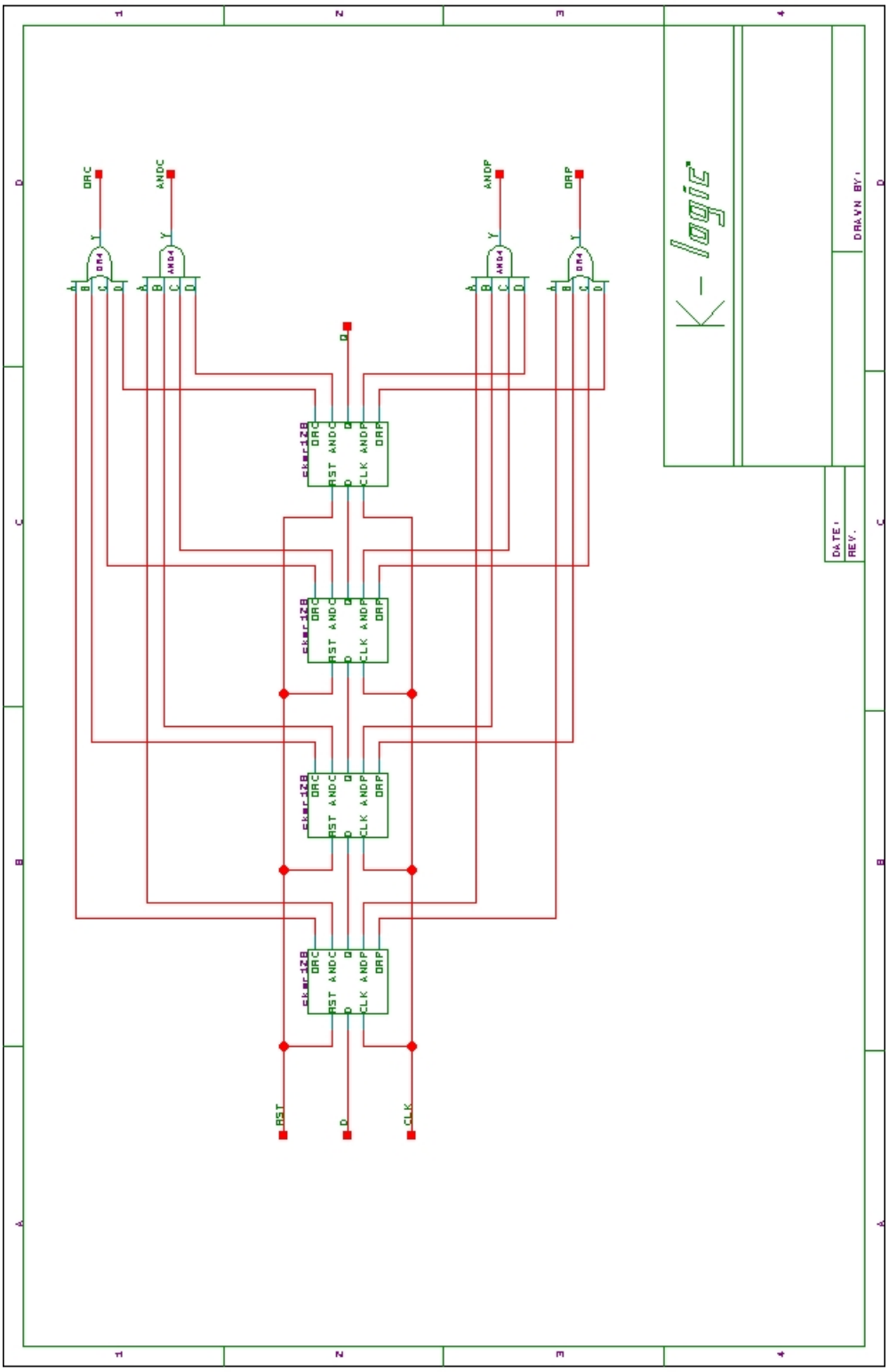

D0
D1
STRING 0: NON-INVERTING STRING, 1000 STAGES
STRING 1: NON-INVERTING STRING, 1000 STAGES
K-Ingg
CLK
RESET

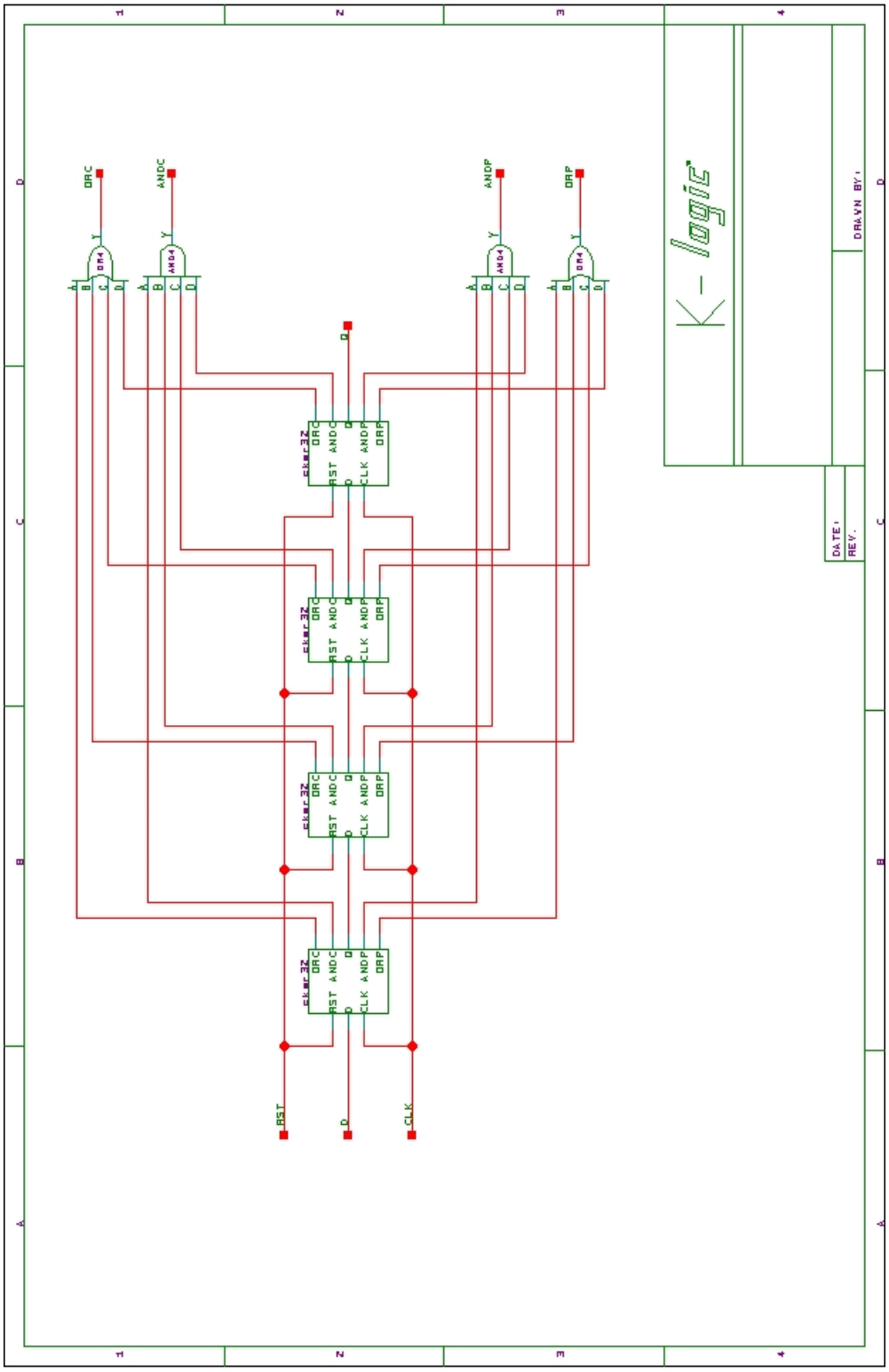

K- logic
T0ACT35XCQ\BUF50NINV
DRAWN BY: RBK
DATE:
REV.
PRESERVE

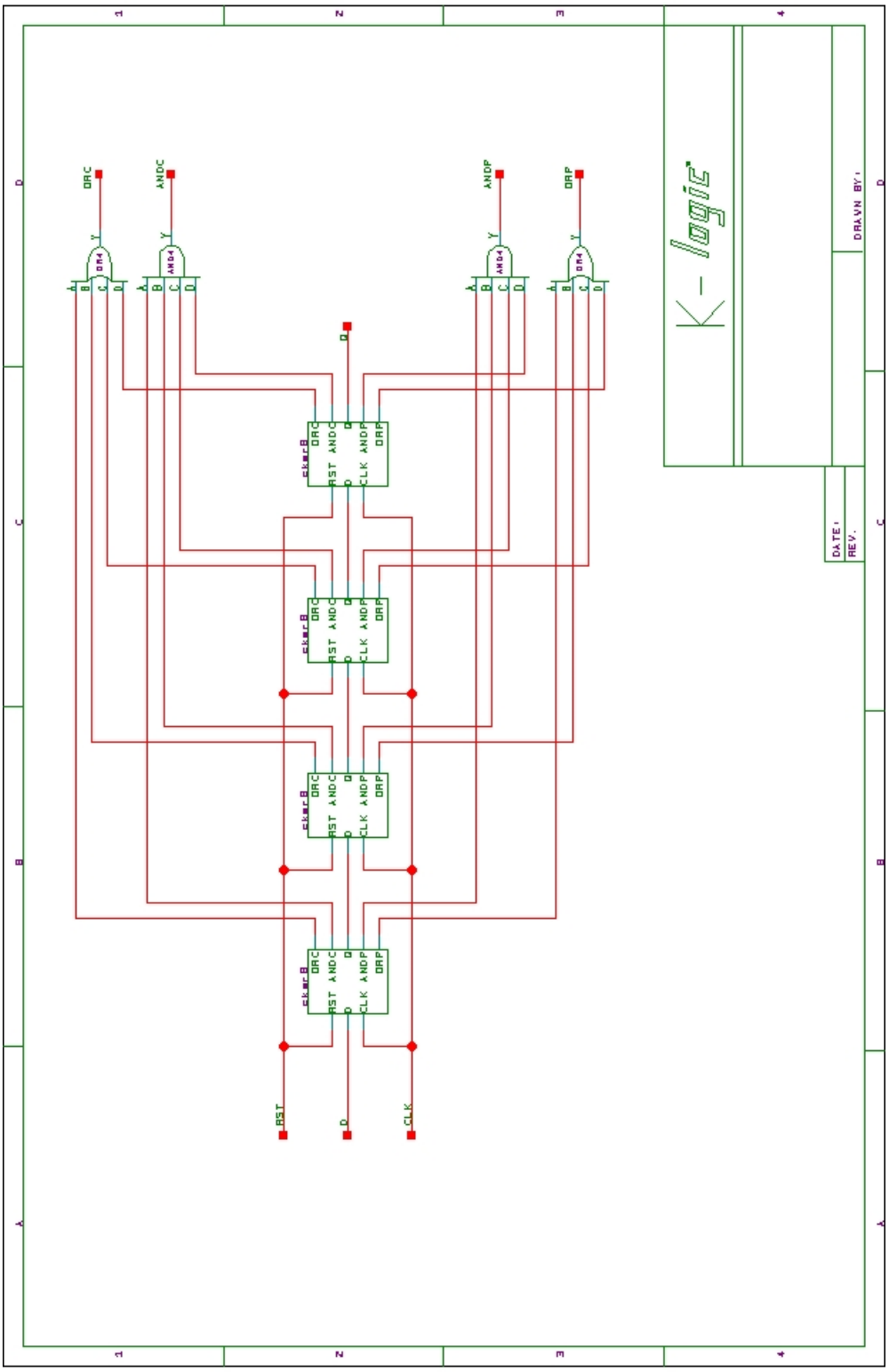

K-logic
TDSX72CQ256-25strings
DRAWN BY:
DATE:
REV.
Y00
Y01
Y02
Y03
Y04
Y05
Y06
Y07
OUTBUF
PAD
RESETCNTR
ENCNTR
CNTRCLR
CNTEN
CNTRCLD

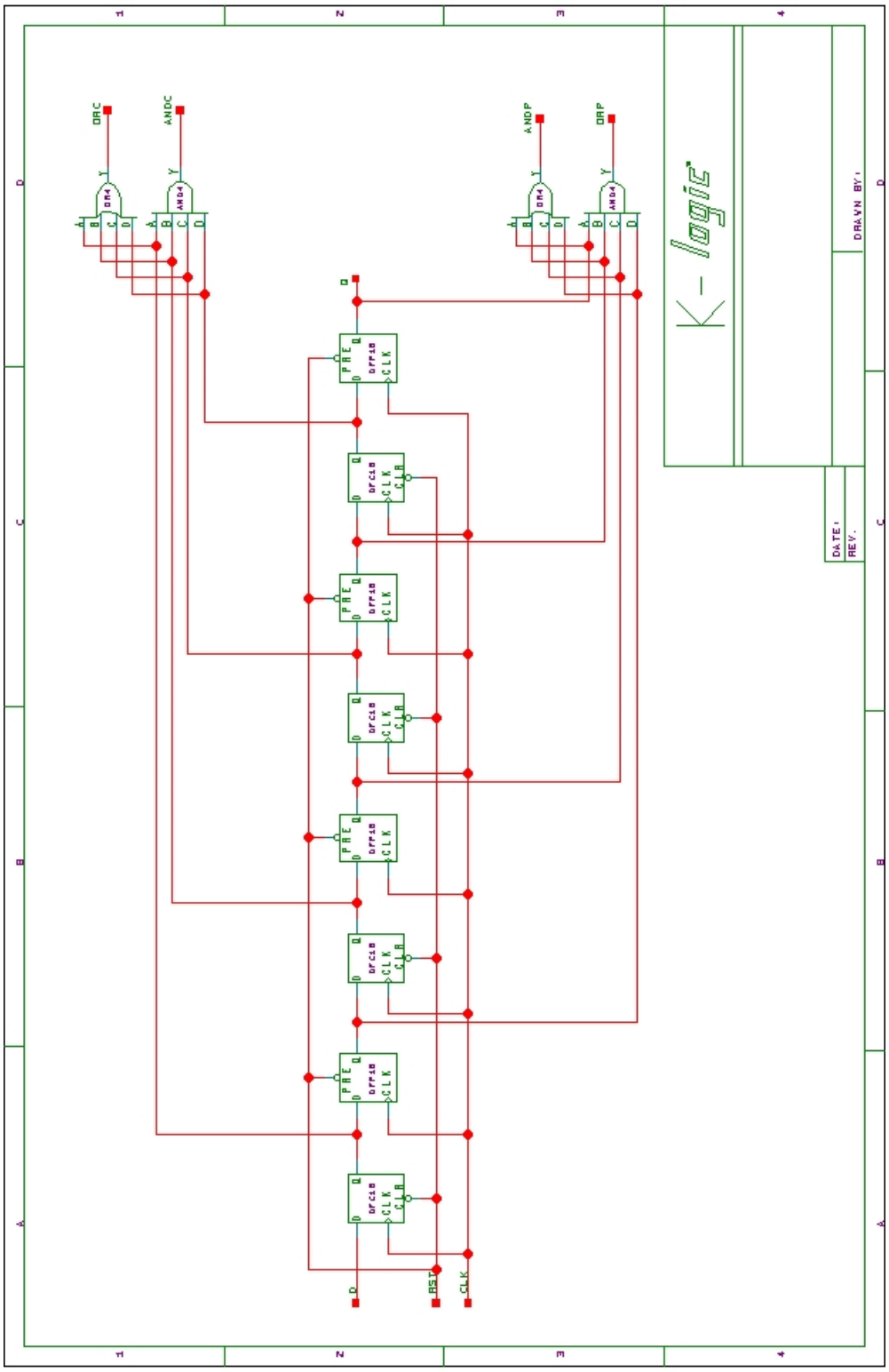

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
INX1
INX2

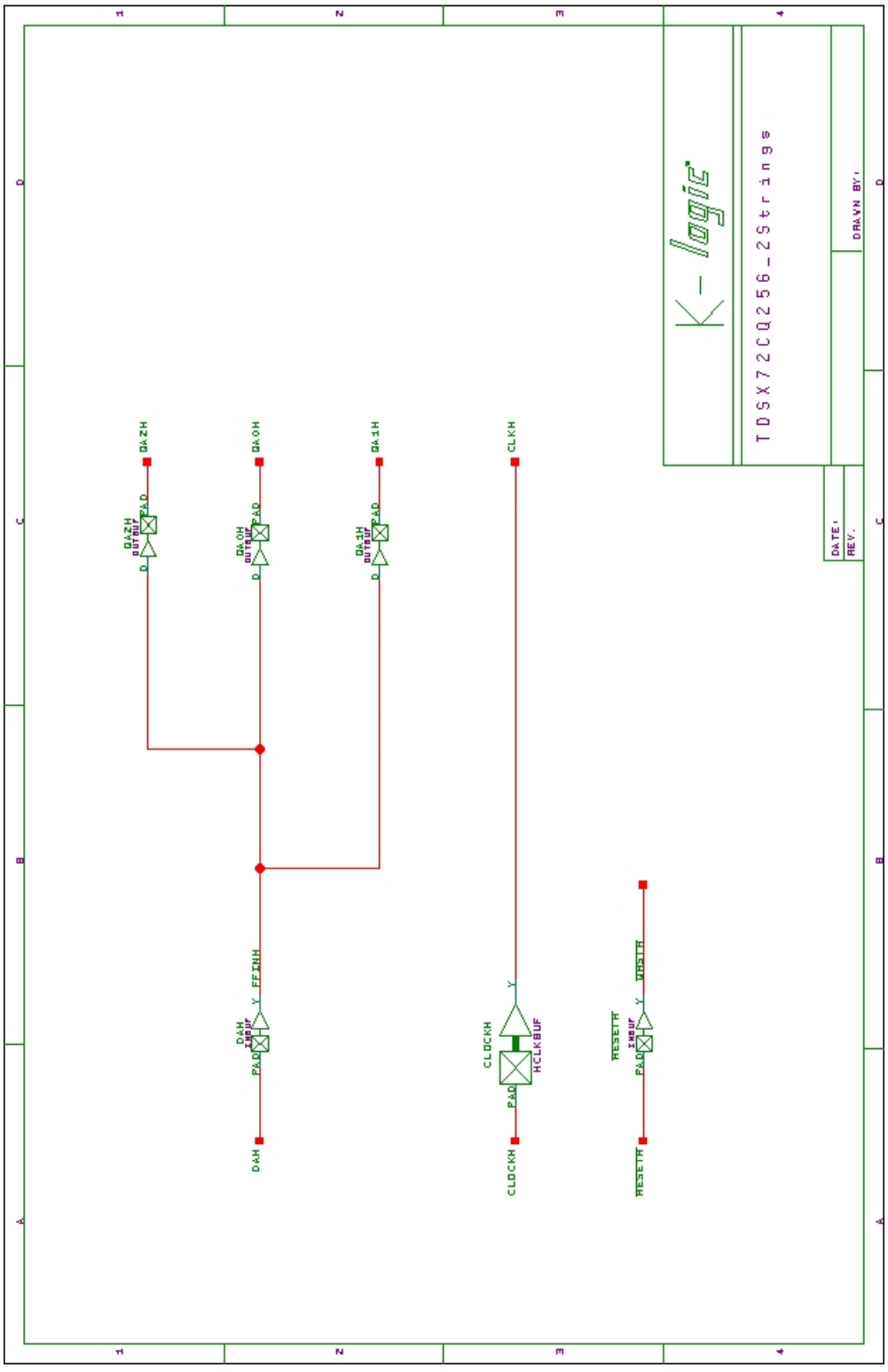

CHECK0
CHECK1
CHECKSHIFTOUT
TDSX72CQ256_2Strings
K-logic
DRAWN BY:
DATE:
REV.
FUNC_RST
CLK

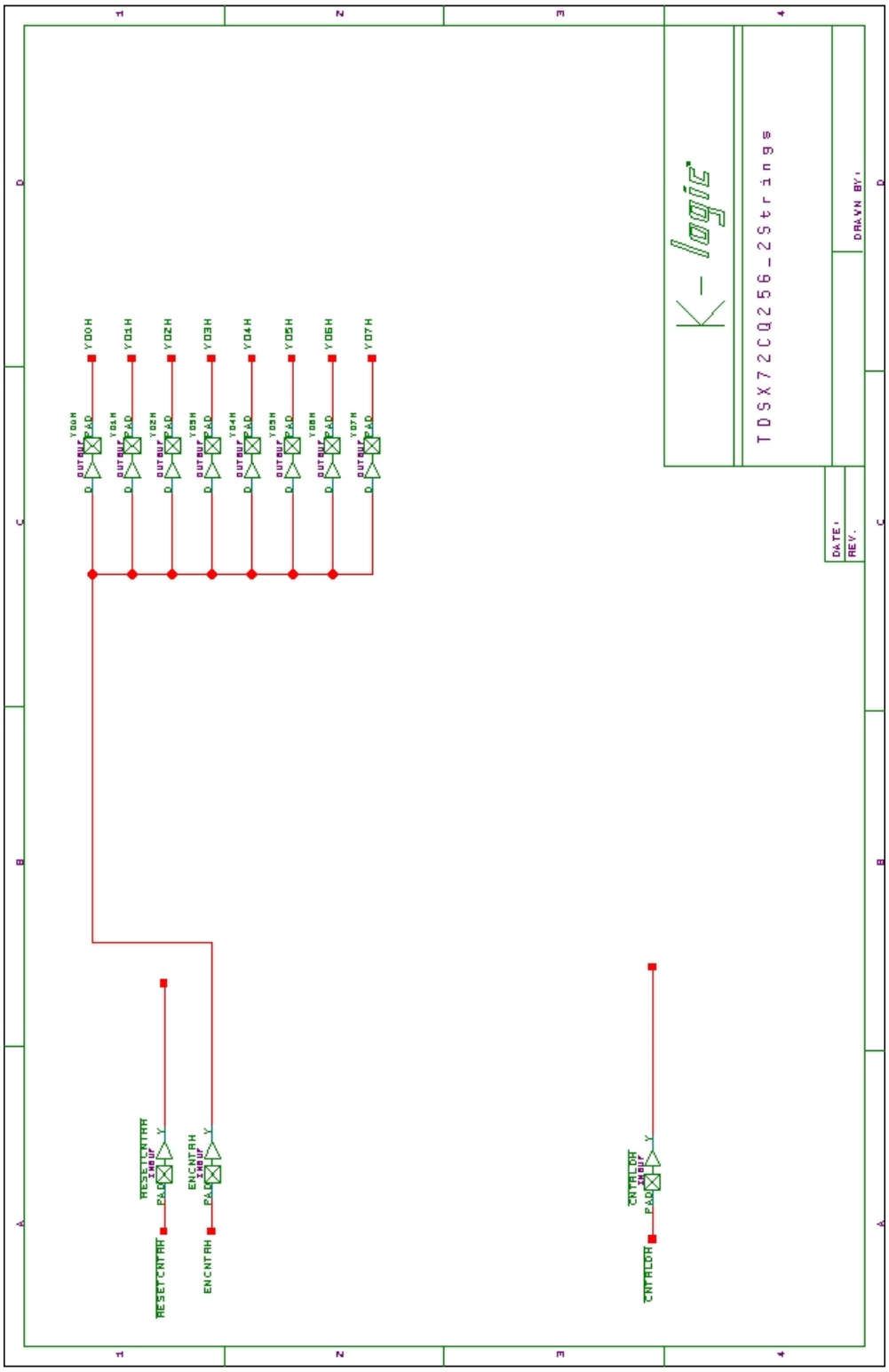

DRC
ANDC
ANDP
DRP
AND4
DFKRC1Z8
RST
CLK
D
Q
K-logic
DRAWN BY:
DATE:
REV.

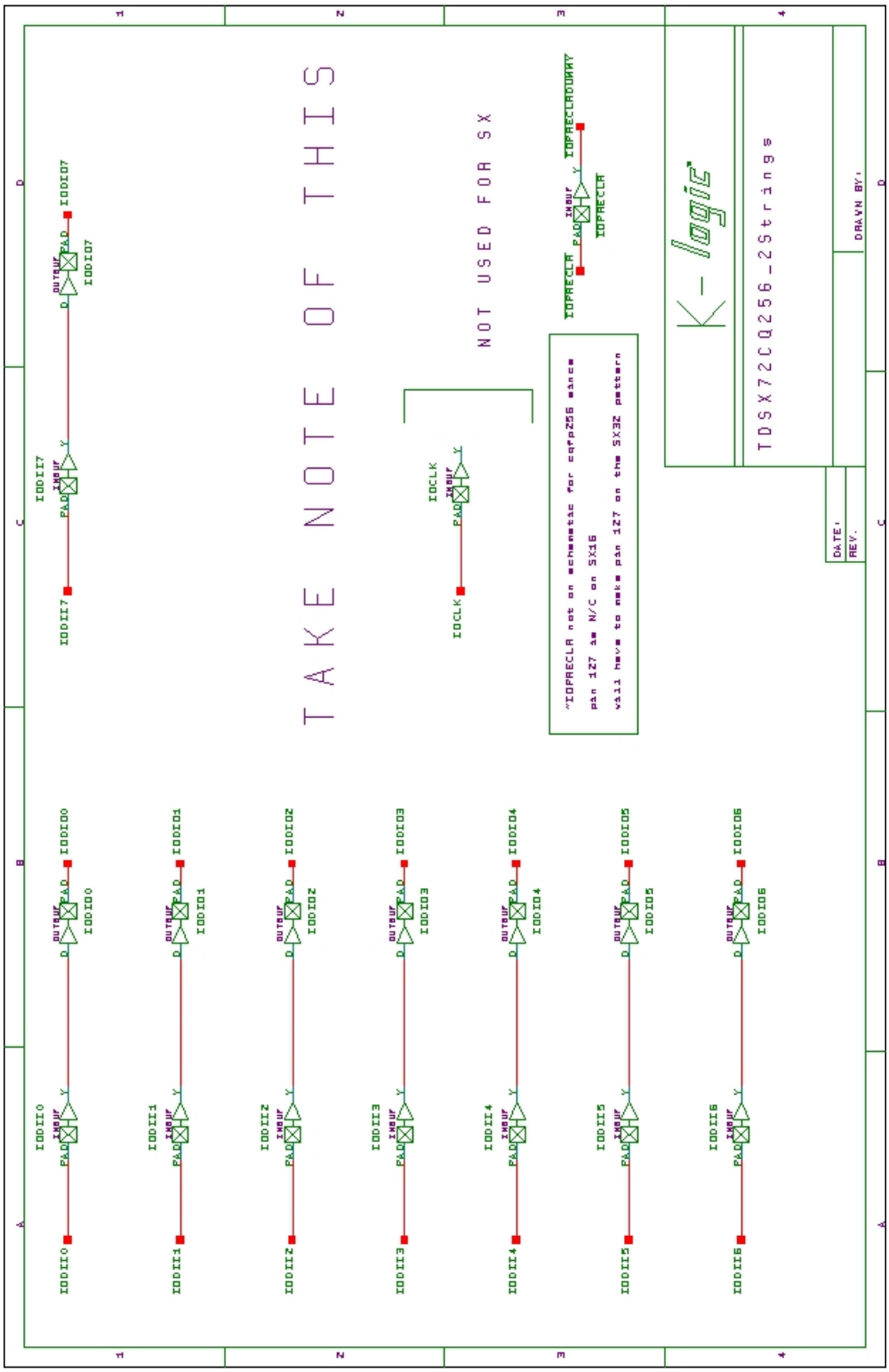

DRC
ANDC
ANDP
DRP
AND4
DRH
Fkmr32
DRC
ANDC
D
RST
CLK
ANDP
DRP
RST
D
CLK
K-logic
DRAWN BY:
DATE:
REV.

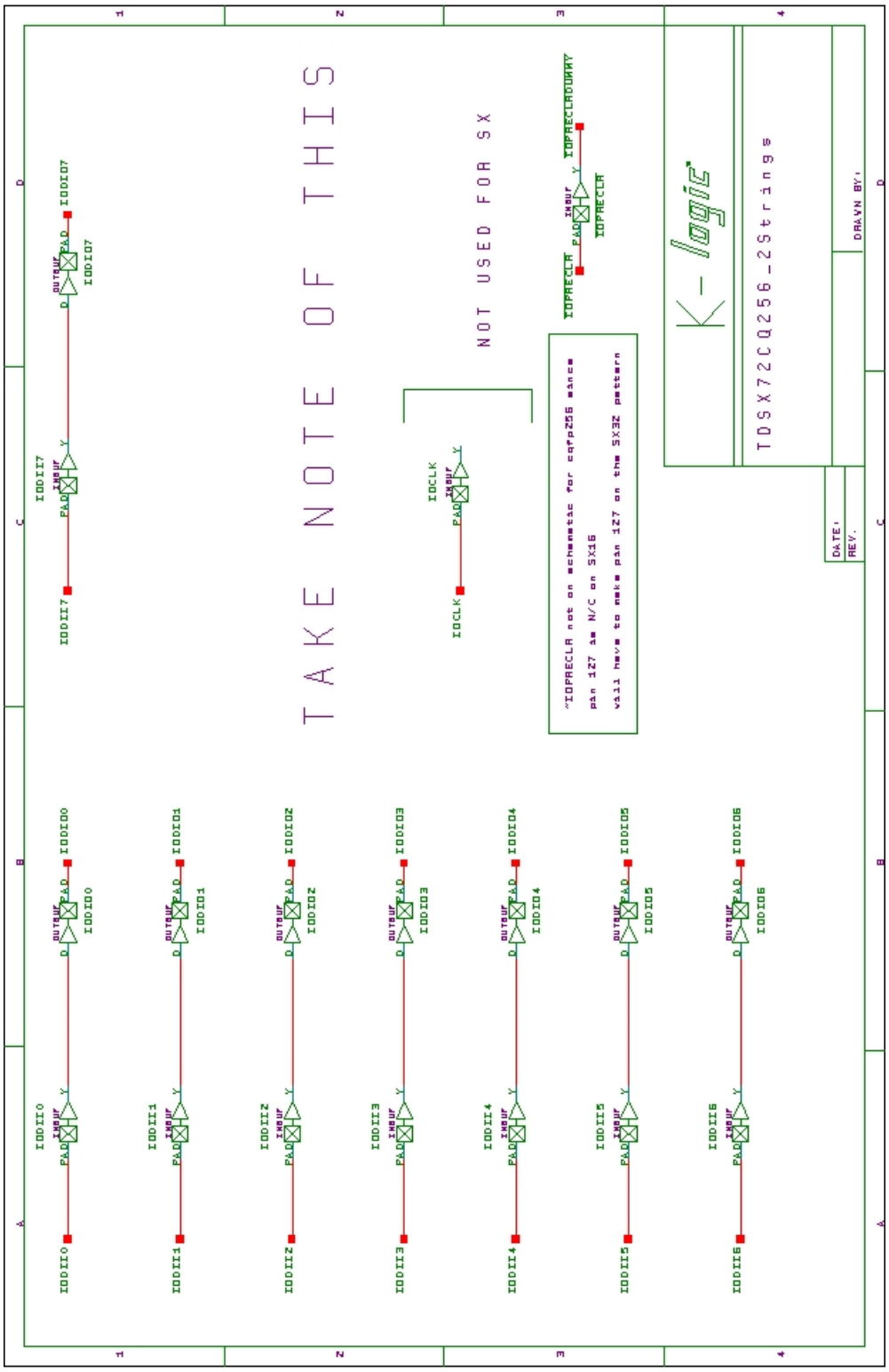

DRC
ANDC
ANDP
DRP
BST
D
CLK
DRAWN BY:
DATE:
REV.

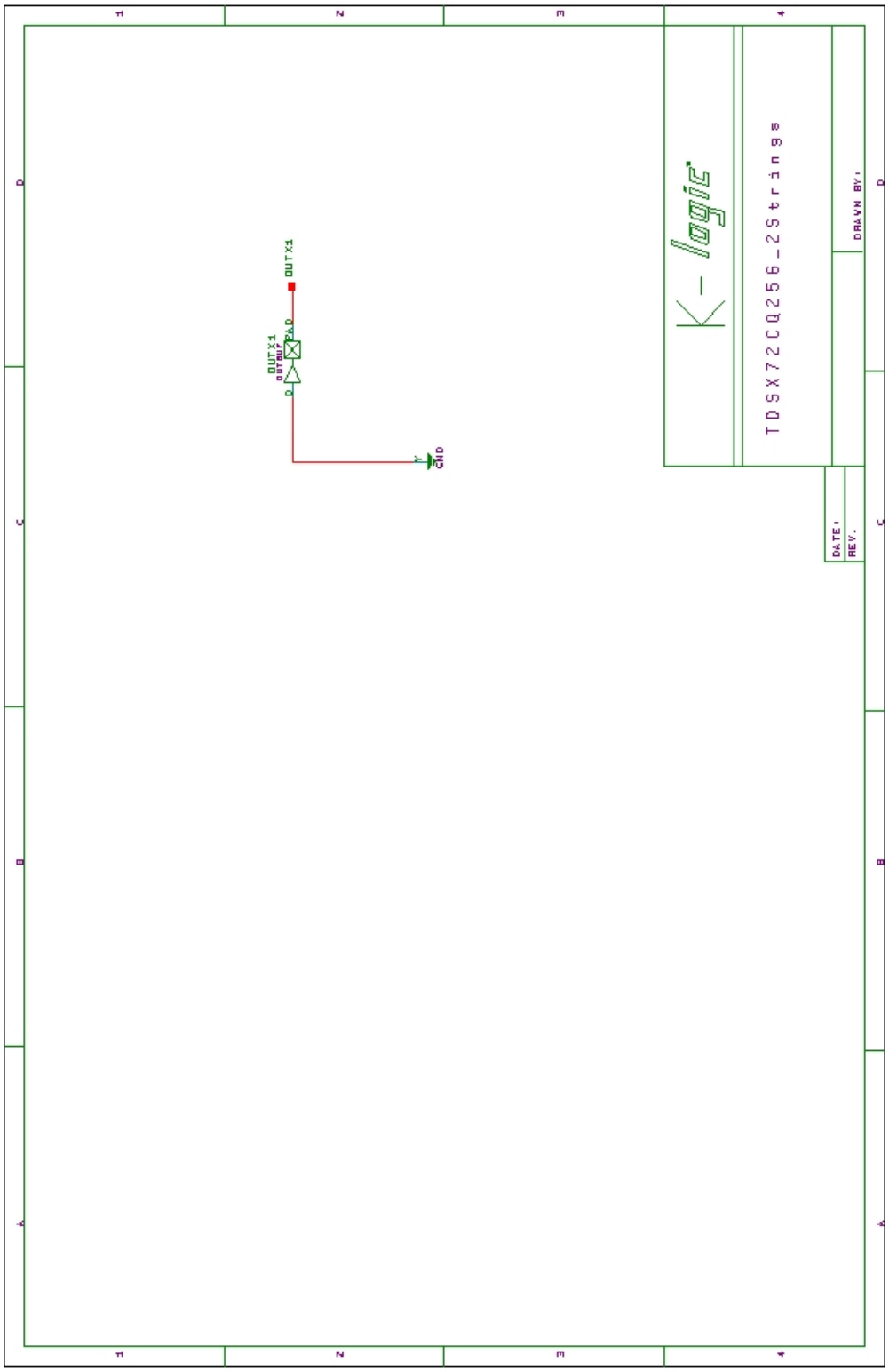

ORC
ANDC
ANDF
ORF
Q
D
RST
CLK
DRAWN BY:
DATE:
REV.


K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
DA2H
DA0H
DA1H
CLKH
DAH
CLOCKH
RESETH
HCLKBUF
PAD
OUTBUF
INBUF
FFINH
WRSTH


K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00H
Y01H
Y02H
Y03H
Y04H
Y05H
Y06H
Y07H
RESETCNTRH
ENCNTRH
CNTRLOH


TAKE NOTE OF THIS
NOT USED FOR SX
K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
IOCLK
IOPRECLR
IOPRECLRDUMMY
"IOPRECLR not on schematic for csp256 since
pin 127 is N/C on SX16
will have to make pin 127 on the SX32 pattern


TAKE NOTE OF THIS
NOT USED FOR SX
K-logic
TDSX72CQ256-2Strings
DRAWN BY:
DATE:
REV.
IOCLK
IOPRECLR
IOPRECLRQUINKY
IODII0
IODII1
IODII2
IODII3
IODII4
IODII5
IODII6
IODII7
IODIO0
IODIO1
IODIO2
IODIO3
IODIO4
IODIO5
IODIO6
IODIO7
INBUF
OUTBUF
PAD


OUTX1
OUTX1
PAD
OUTPUT
D
Y
GND
logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.

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