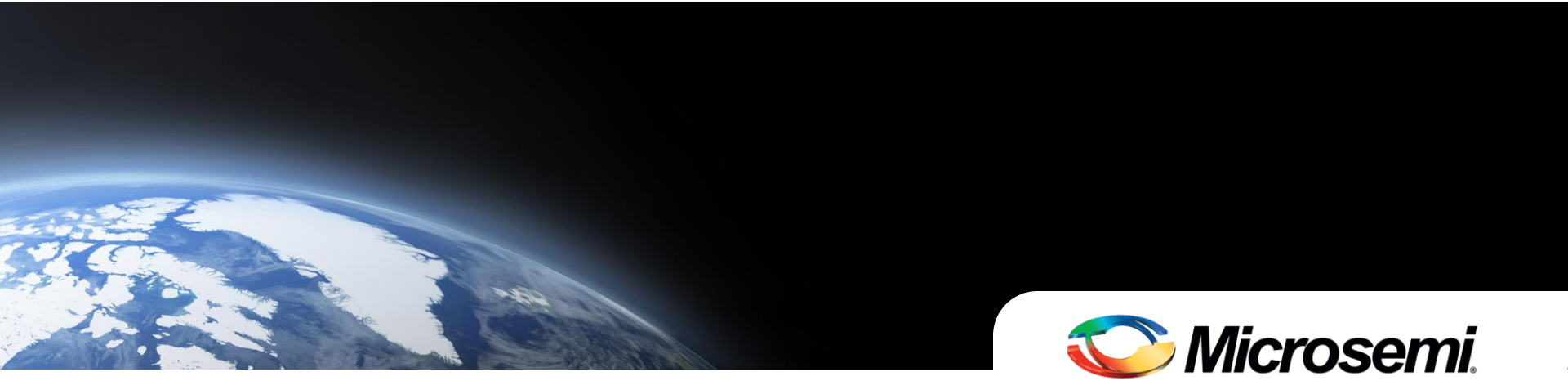
Power Matters.™



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RTG4 Radiation Test Results and Test Plans

Microsemi Space Forum 2015

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Outline

- Total ionizing dose (TID) effects
  1. TID induced effect at the device level
     a. Floating gate devices
     b. CMOS devices
  2. TID induced effect at the product level
     a. Propagation delay
     b. Power supply current
- Single event effects (SEE)
  1. Single event latchup
  2. Single event upset
     - Flash configuration cell
     - Radiation hardened FF (STMRFF)
     - Fabric SRAMs : LSRAM and µSRAM
  3. MBU and MCU
- Radiation Test plan

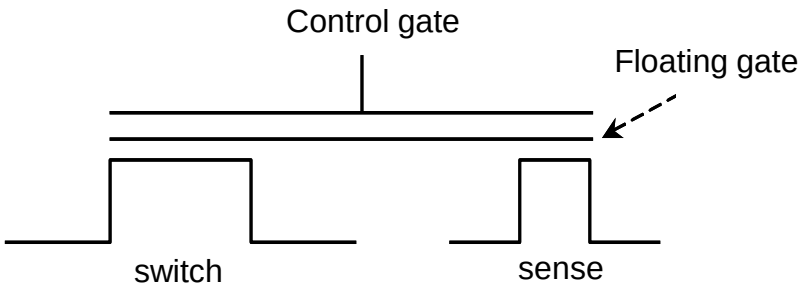
Total ionizing dose (TID) effects

TID Testing

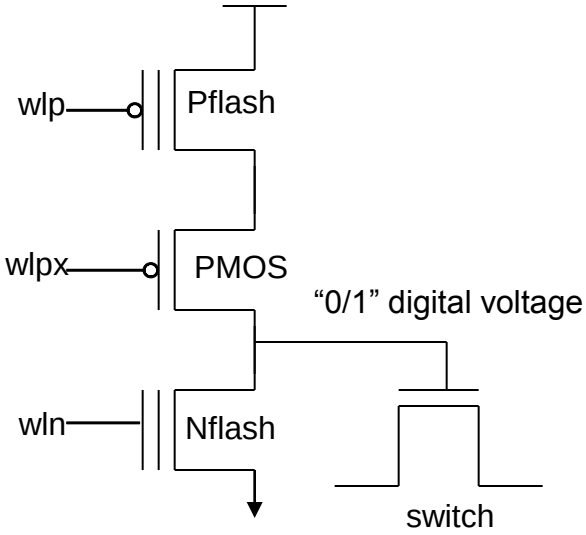
- **Facilities**
  - Air Force Research Laboratory (AFRL), NASA Goddard Space Flight Center, Vanderbilt university (VU)
- **Testing condition**
  - Gamma ray and x-ray
  - Dose rate : 5 krad/min and 18 krad/min
  - Dose steps : 25, 50, **100**, 150, 200 krad
- **Test parameters**
  1. Propagation Delay
  2. Power Supply Current

RTG4 Flash Configuration Cell

SmartFusion2 : Sense-Switch bit cell



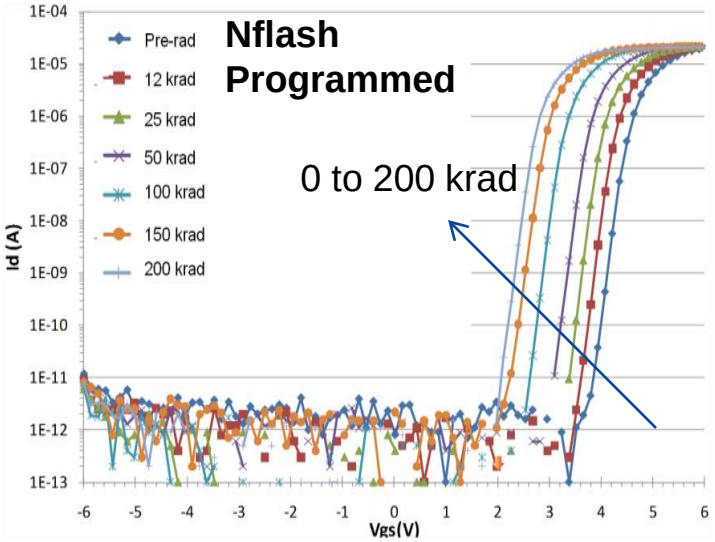
RTG4 : 4T Push-Pull bit cell



- The data signal doesn't pass directly through the flash transistor
- RTG4 Push-Pull cell is significantly more radiation tolerant :
  - Radiation induced V_t change in the Nflash and Pflash cells does not result in a change in the switch state (no propagation delay degradation)
- In SmartFusion2 : Propagation delay reaches 10% degradation after 25 krad
  - TID induced charge accumulation in the FG causes the V_t of the switch transistor to change

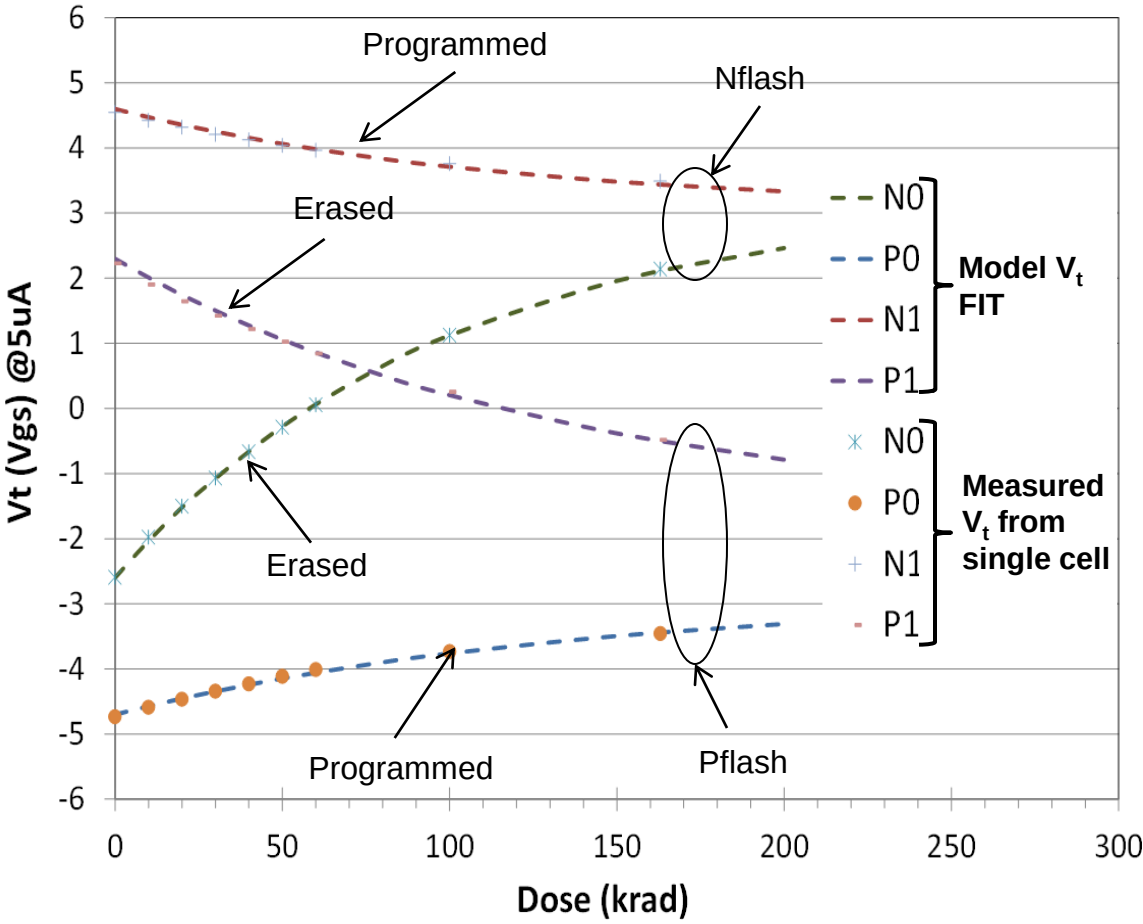
TID induced effects in the floating gate device

- Radiation induced V_t shift model: $V_T(\gamma) = V_T(\infty) + [V_T(0) - V_T(\infty)] . Exp(-A \gamma)$



- No S/D leakage current

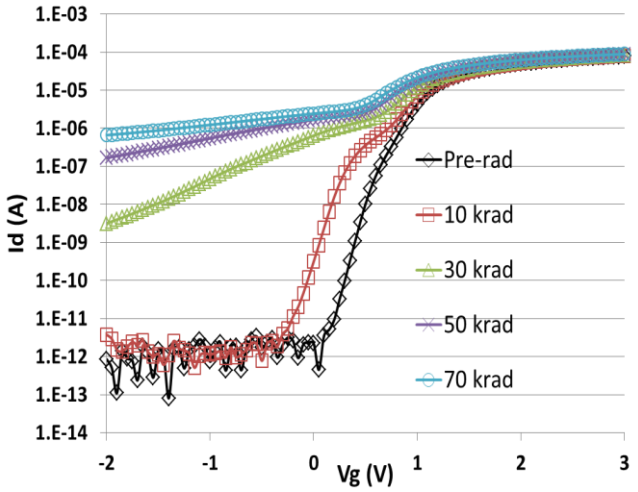
γ : total ionizing dose
$V_T(0)$: pre-rad V_T
$V_T(\infty)$: saturation V_T
A : Fitted decay coefficient



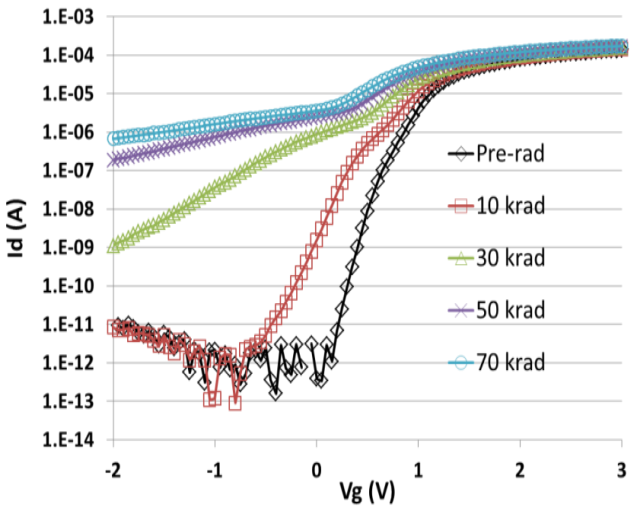
TID effect in the CMOS devices

- NMOS devices in programming and signal path
- Hardened high and medium voltage NMOS devices
- No S/D leakage current

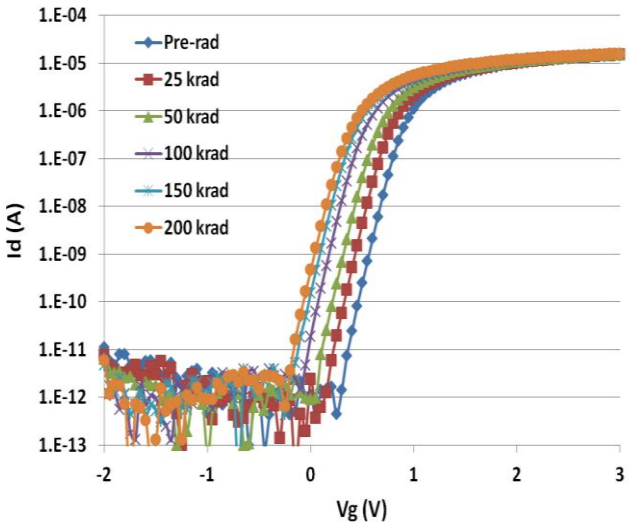
SmartFusion2 High voltage NMOS



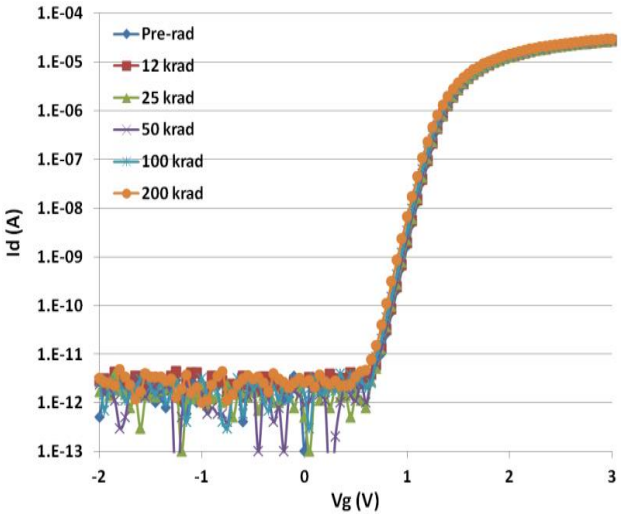
SmartFusion2 Medium voltage NMOS



RTG4 High voltage NMOS



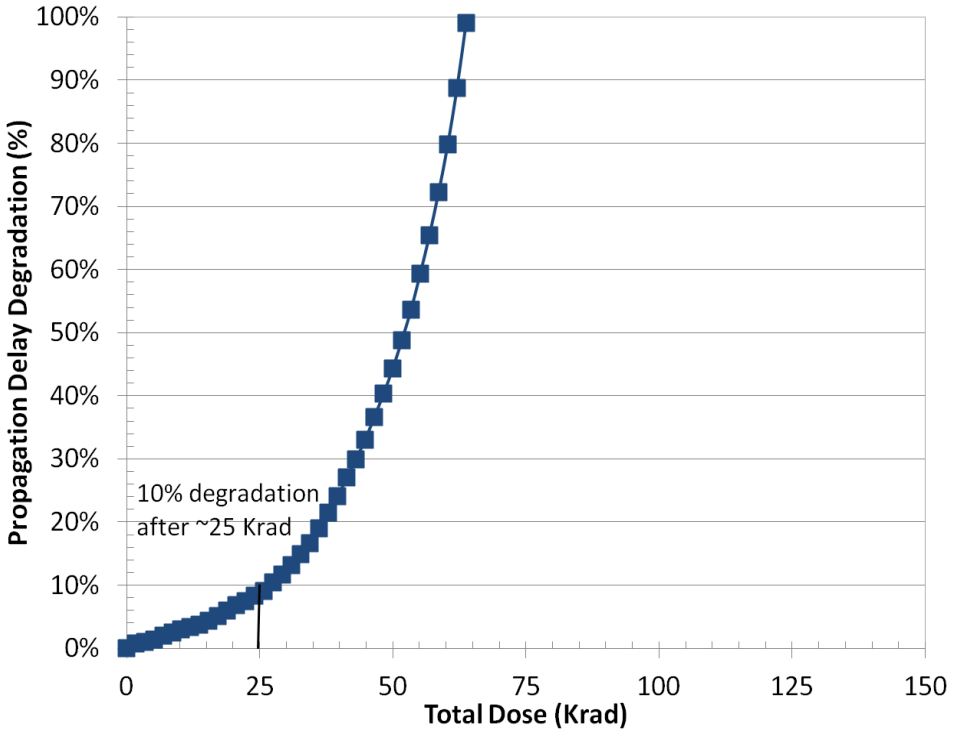
RTG4 Medium voltage NMOS



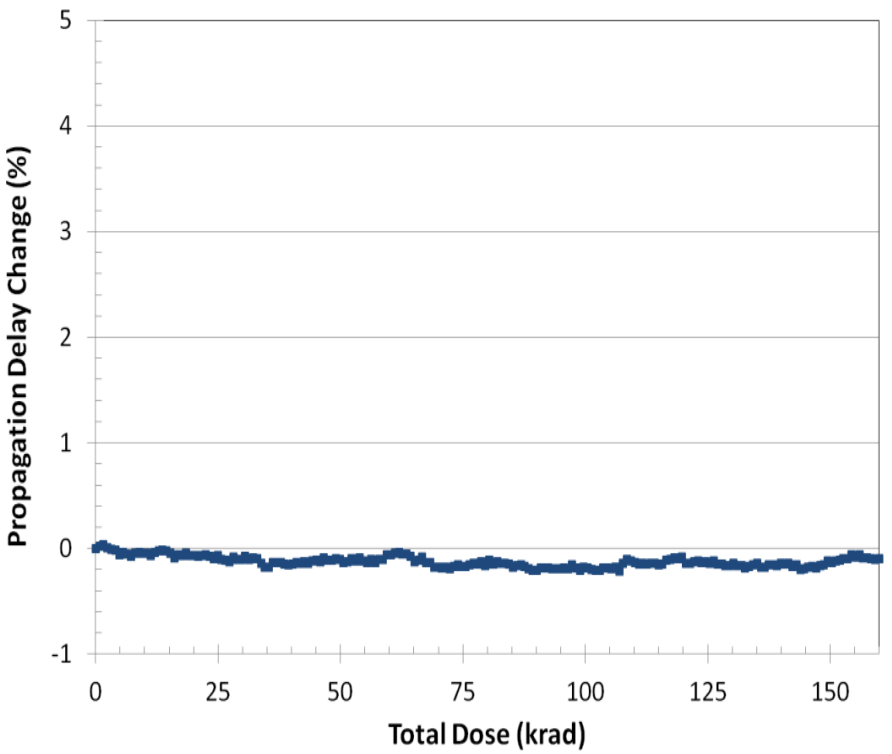
TID induced effect in RTG4 : Propagation Delay

- Propagation delay measured on an inverter-string design with 7200 stages programmed into the FPGA

SmartFusion2

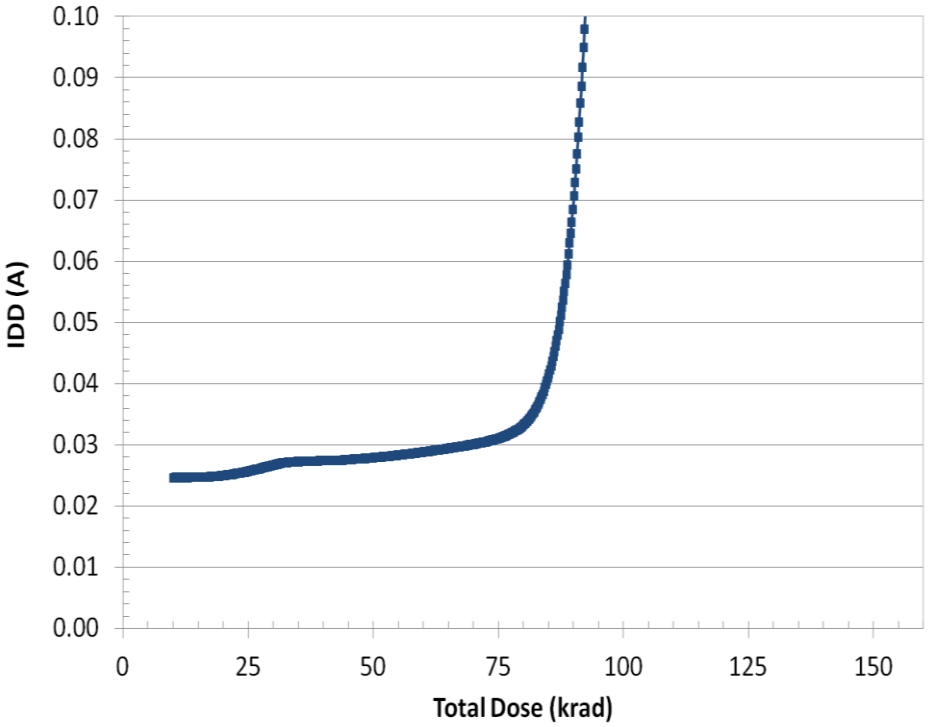


RTG4

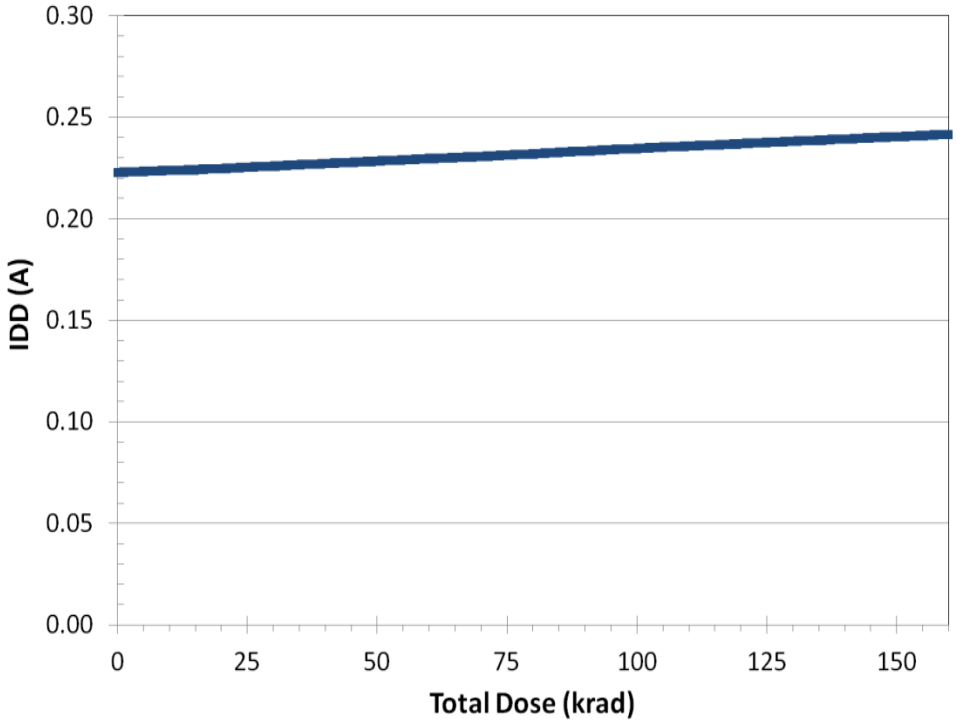


TID induced effect in RTG4 : Core power supply current

SmartFusion2

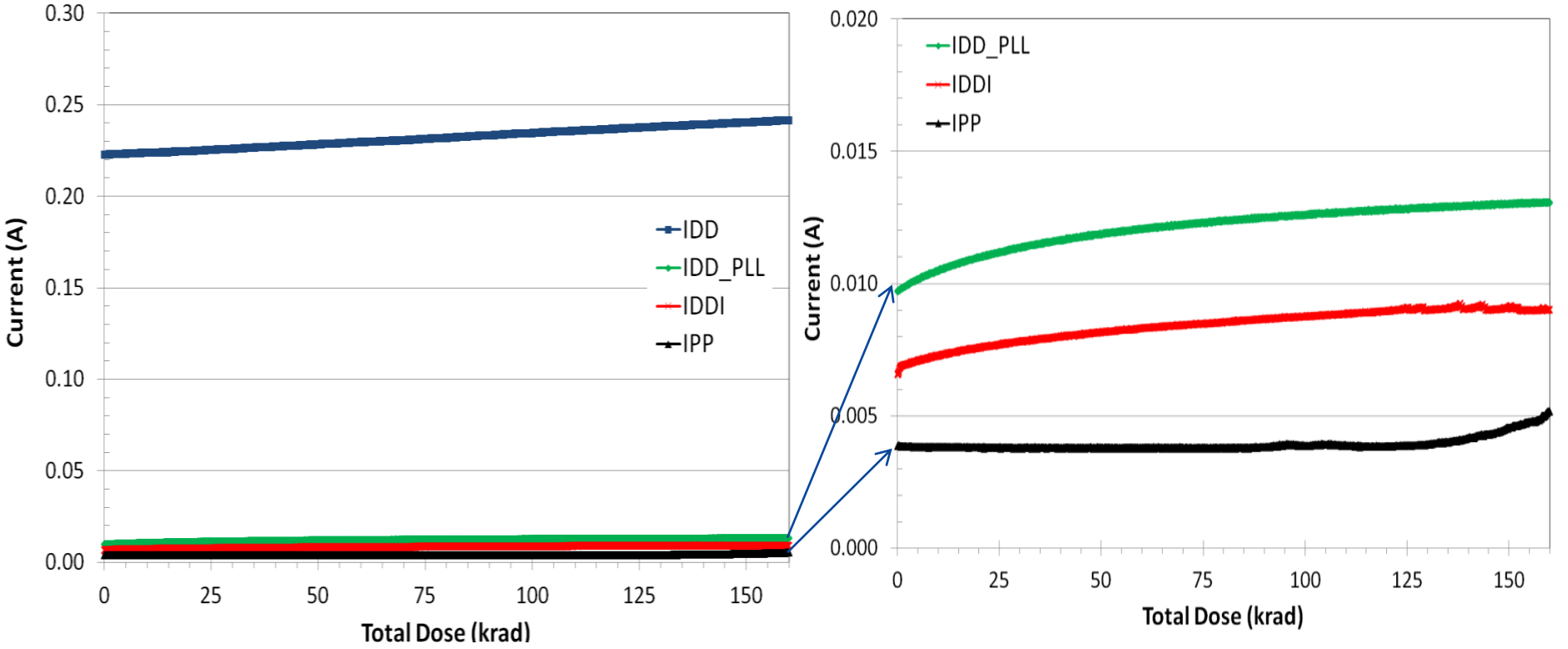


RTG4



- IDD: core power supply current
- 10% increase of the RTG4 power supply current

TID induced effect in RTG4 : Power supply current



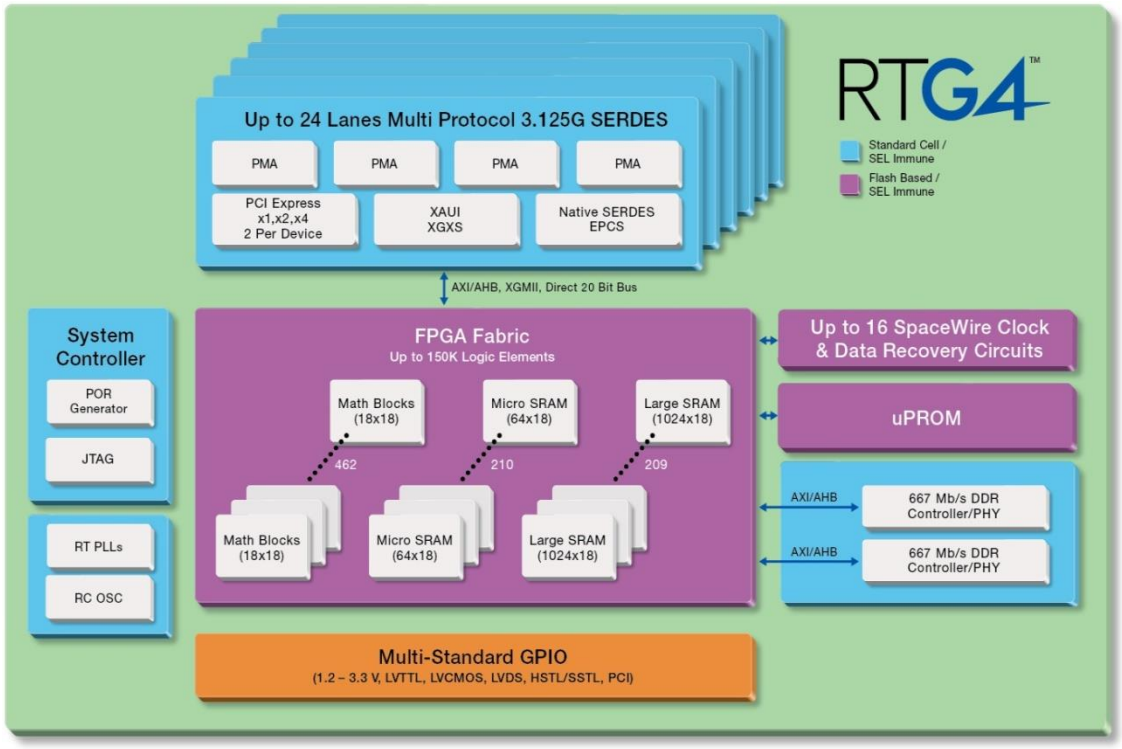
- IDD: core power supply current
- IDD_PLL : PLL power supply current
- IDDI : I/O bank power supply current
- IPP : Charge pump (programming circuit) power supply current

Single Event Effect Results

Outline

- RTG4 flash-based FPGA overview
- Testing condition and silicon preparation
- SEE Test Results
  - SEE in configuration Flash switch
  - SEL
  - SEU data in RT4G150
    1. Flip-Flop
    2. LSRAM
    3. µSRAM
  - MBU and MCU
- SEU simulation
  - Correlate SRAM data with 3D TCAD simulation
- Reprogramming
- Summary

RTG4 Flash-based FPGA



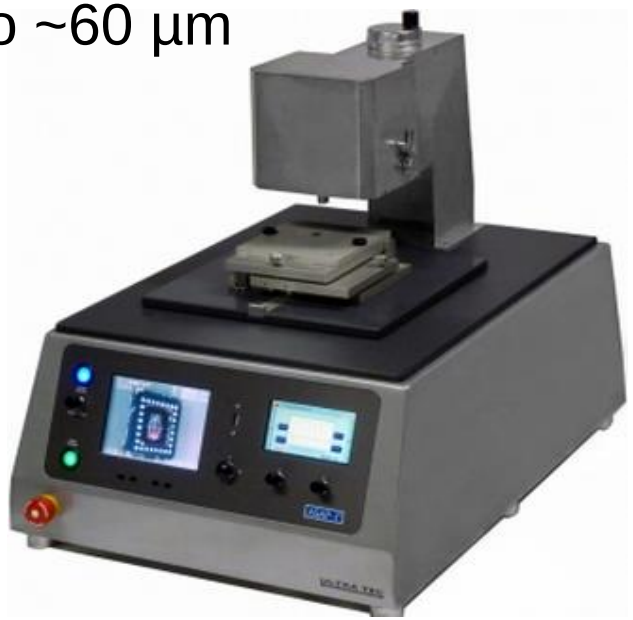
- RTG4 is a new radiation tolerant flash-based FPGA manufactured in UMC 65 nm technology
- Blocks configured and connected by Flash switches
- Functional Blocks
  - Fabric
    - Logic element (4LUT + carry chain + **STMR FF**)
    - Math block (DSP)
    - **EDAC LSRAM and µSRAM**
  - **SpaceWire clock**
  - **SERDES**
  - µPROM
  - RT PLLs, oscillators, CCCs

SEE Testing Conditions

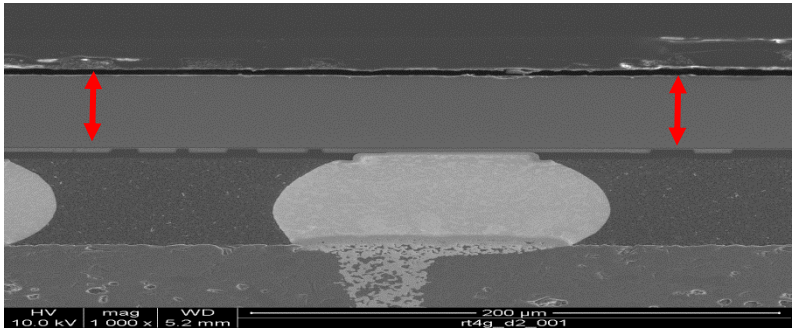
- **Lawrence Berkeley National Laboratory (LBNL)**
  - 16 MeV/nucleon cocktail, vacuum chamber
  - LETs Tested: 1.16 to 69.72 MeV.cm^2/mg (LET = 90.32 w/ Tilting and Si thickness adjustment)
  - Temperature: Room for SEU, 100 ºC for SEL
  - Bias: Nominal for SEU, Nominal+5% for SEL
  - Tilting -45, 0, +45
- **Texas A&M University (TAMU)**
  - 15 MeV, vacuum chamber for ion penetration
  - LET Tested: 9.8 to 103 MeV.cm^2/mg
  - Temperature: Room for SEU, 100 ºC for SEL
  - Bias: Nominal for SEU, Nominal+5% for SEL
  - Tilting -30, 0, +30

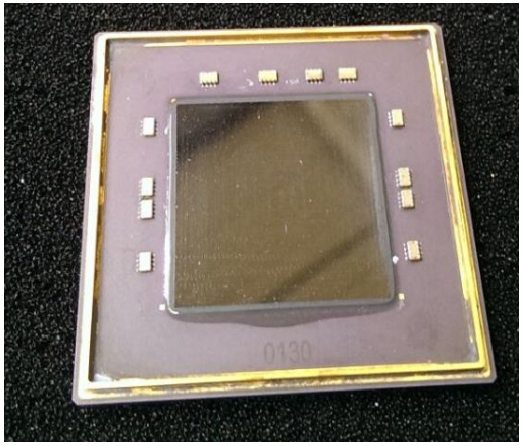
Preparation of Silicon

- Need to back-grind Flip-Chip from 675 µm to ~60 µm
- Special Considerations
  - Die size is very large (>2cm x 2cm)
  - Back grind silicon to ensure beam penetration
- Things learned
  - Take it slow when grinding, 6-8 hours per part
  - Use fresh fine diamond coated bits per chip
  - Edge cracks if too much force is applied (100 gr)
  - Thermal relaxation reduces center to edge variance
  - Verification of die thickness is important (SEM)



Measured Die thickness at center and edge. <10µm difference





Single Event Latchup

Temperature	LET (MeV.cm^2/mg)	SEL	Fluence (ions/cm^2)
Room Temp	9.8	0	2.00×10^7
	13.74	0	2.00×10^7
	26.9	0	6.51×10^7
	31.06	0	5.00×10^7
	89	0	5.00×10^6
	103	0	2.60×10^7
100 ºC	58	0	4.00×10^7
	89	0	8.94×10^7
	103	0	7.58×10^7

- Single event latchup testing performed at room temperature and 100 ºC, Nominal+5% bias
- No SEL is observed up to LET = 103 MeV.cm^2/mg @ 100 ºC

RTG4 Flash Configuration Cell

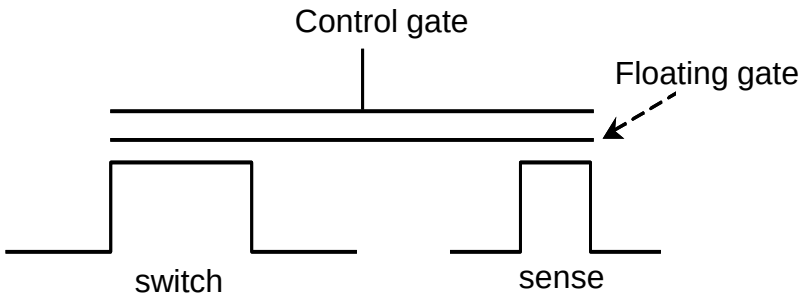
LET (MeV.cm^2/mg)	Configuration Upset	Total fluence (ions/cm^2)
1.16 to 103	0	5.02x10^8

- Functionality of the FPGA was continuously monitored during radiation exposure
- No configuration upsets were detected in the 10 parts tested at LBNL and TAMU up to LET = 103 MeV.cm^2/mg
- **RTG4 flash configuration cell is SEU immune**

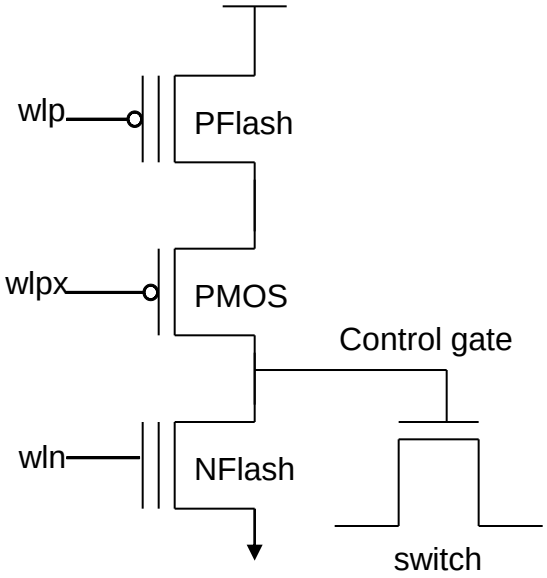
RTG4 Flash Configuration Cell

- 2 parameters contribute to RTG4 Push-Pull cell SEU immunity
  - Microsemi FPGA flash cells larger than std. flash memory cells
  - Switch transistor in RTG4 Push-Pull data path is indirectly coupled to the floating gate

SmartFusion2 : Sense Switch bit cell

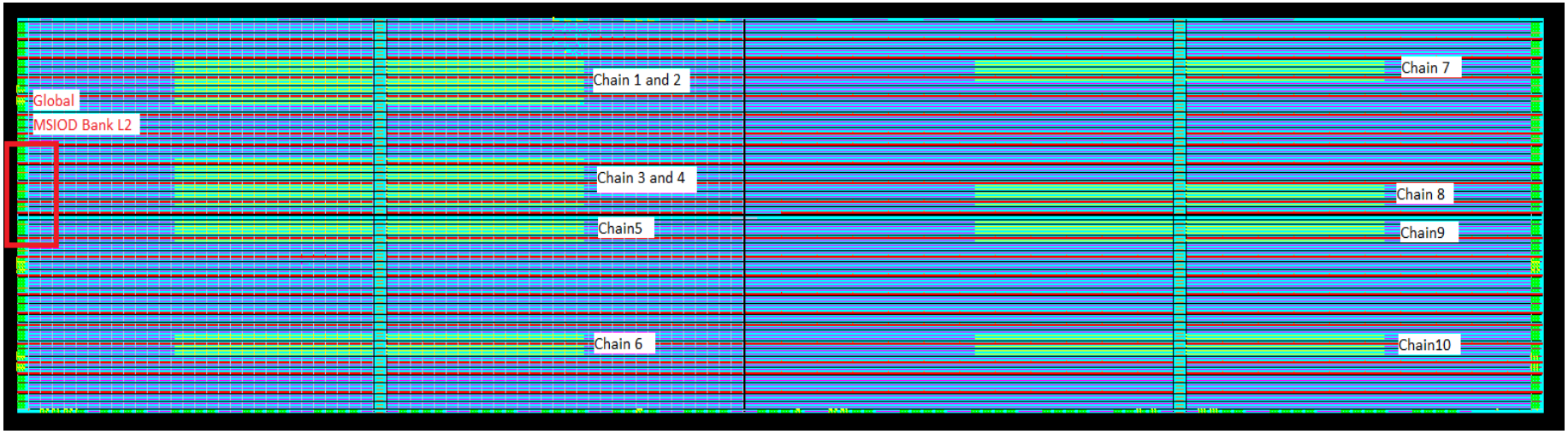


RTG4 : 4T Push-Pull bit cell

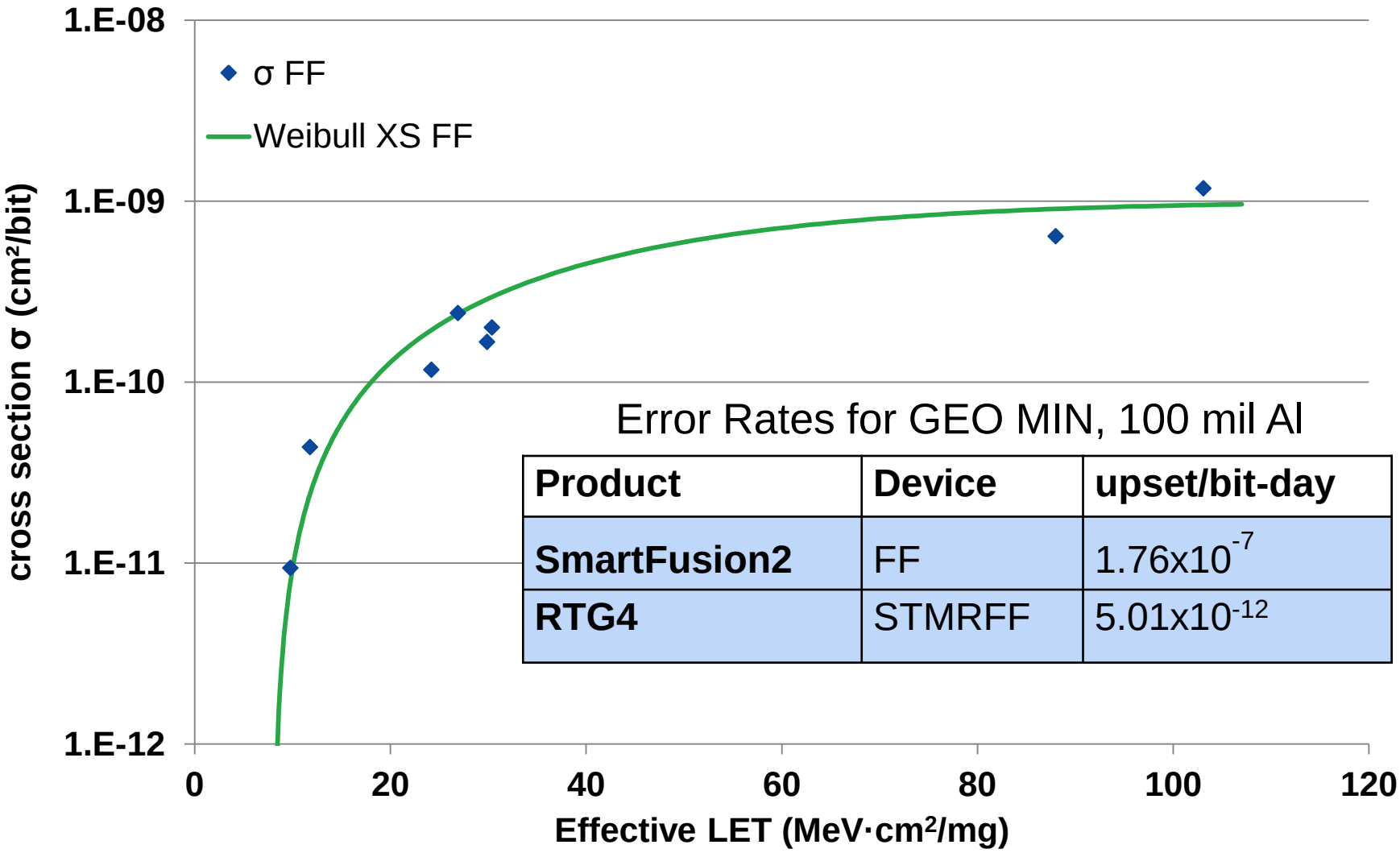


Flip-Flop Physical Placement

- STMRFF
  - RTG4 features built in STMR into each FF
- 2000x10 FF chains
  - 400 FF per row x 5 rows = 2000 FF per chain
  - Total of 10 chains, 20000 FFs for statistics
- Global
  - Manually placed to identify global upsets in Quadrant, Half, Full Fabric



RTG4 Flip-Flop Cross Section

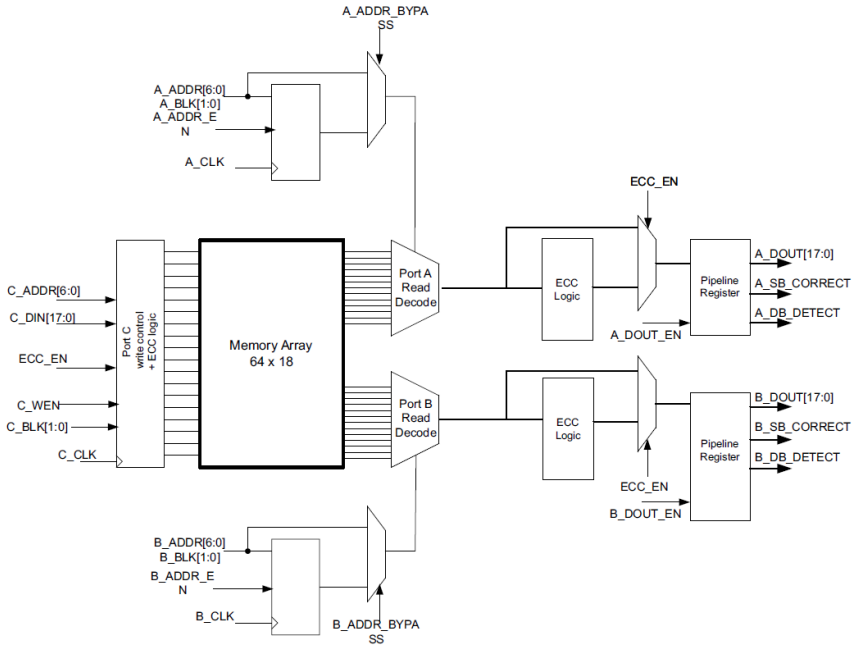


Error Rates for GEO MIN, 100 mil Al

Product	Device	upset/bit-day
SmartFusion2	FF	1.76×10^{-7}
RTG4	STMRFF	5.01×10^{-12}

SRAM blocks in RTG4 FPGA fabric

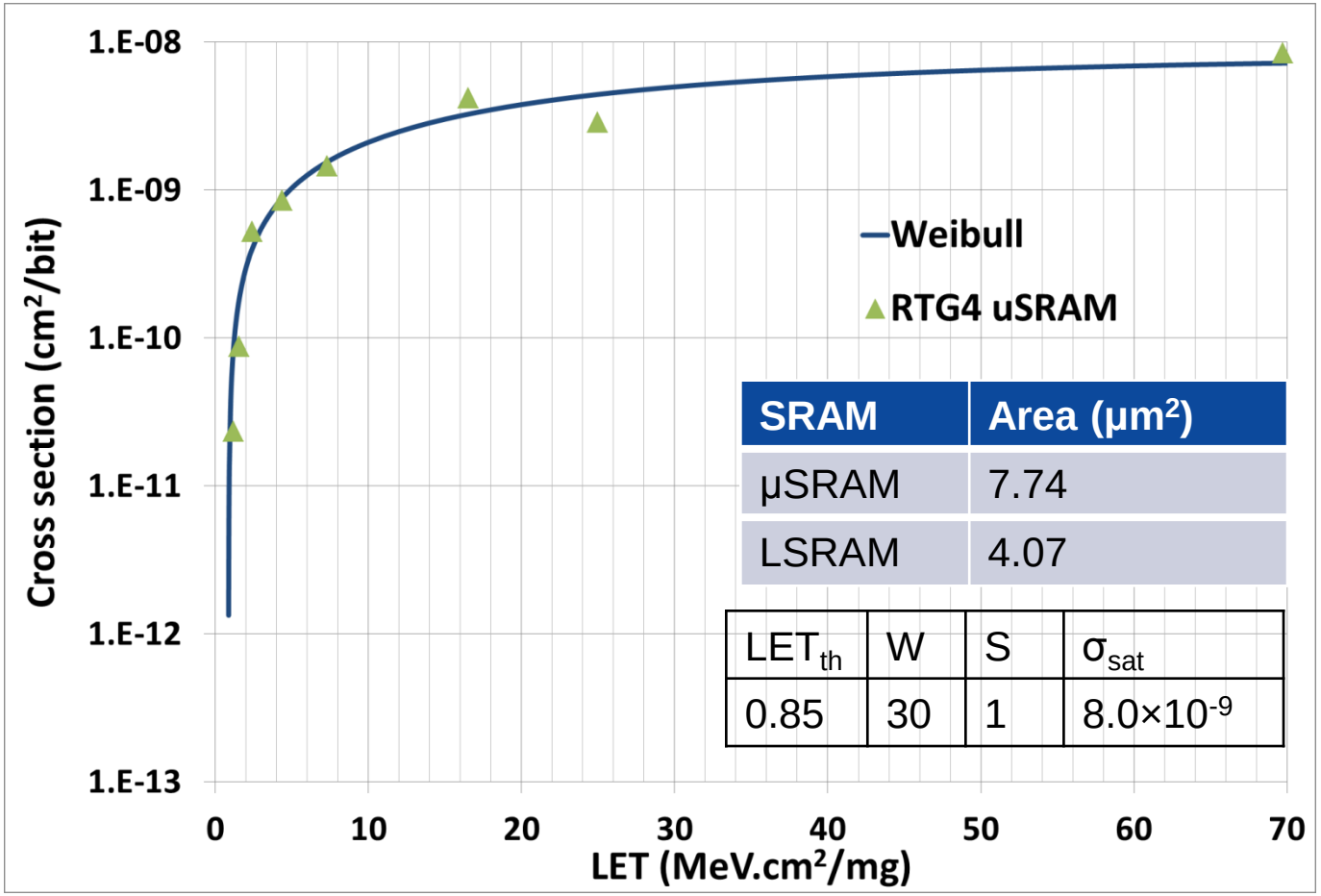
- µSRAM can be used as register file in state machine and µcontroller
- LSRAM can be used as cache memory
- Circuit design and layout techniques are used to mitigate SET affects
  - All registers in the data path employ STMR FF
- Built-in EDAC with SECDED code



Simplified Functional Block Diagram of µSRAM

SRAM	Configuration	#Tx/bit cell	Area (µm^2)	size	RT4G150 blocks
µSRAM	2 read port and 1 write port	14	7.74	1.5 Kb	210
LSRAM	Dual port and two-port	8	4.07	24.5 Kb	209

µSRAM single bit cross section

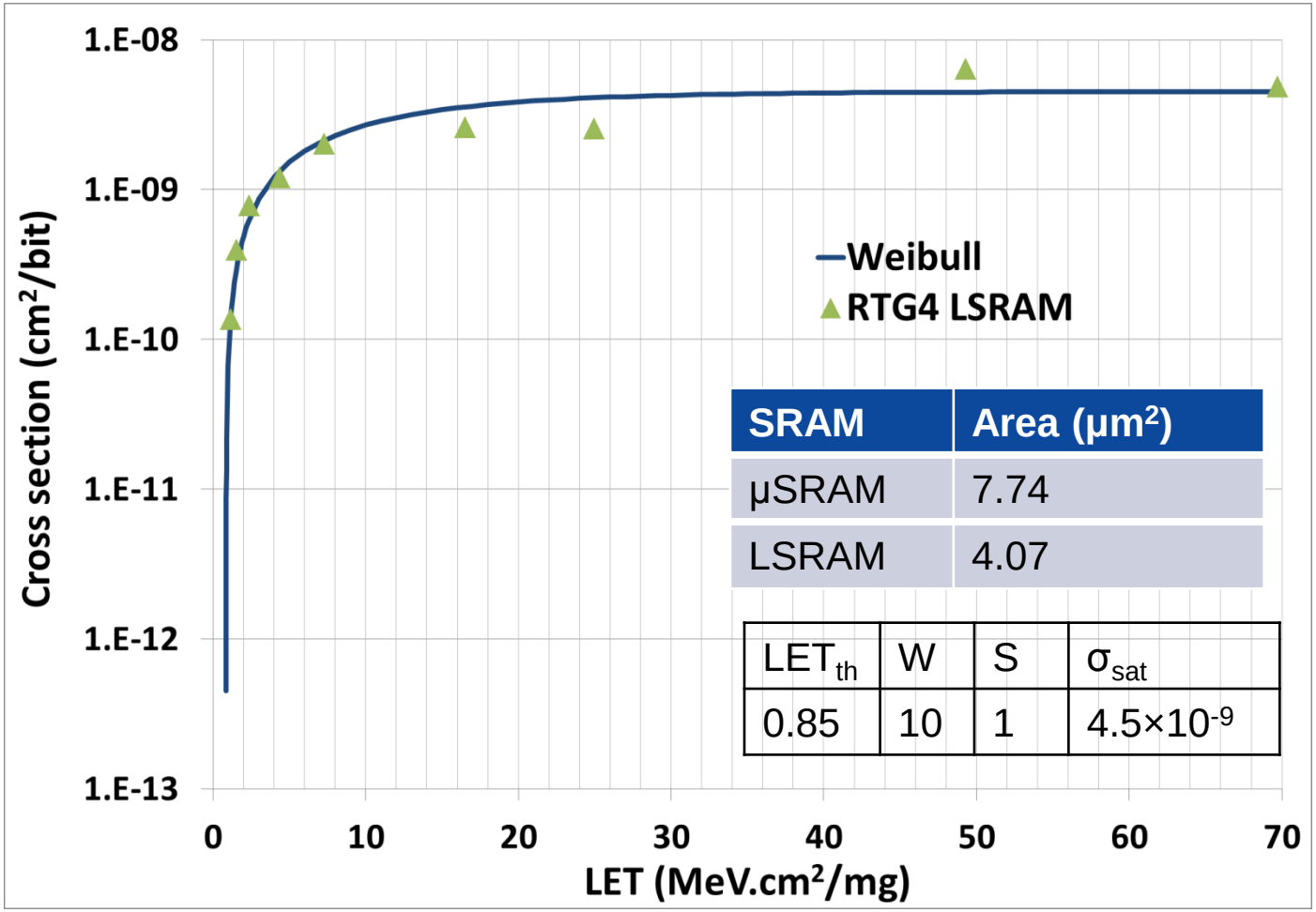


SRAM	Area (µm²)
µSRAM	7.74
LSRAM	4.07

LET_{th}	W	S	σ_{sat}
0.85	30	1	8.0×10^{-9}

- µSRAM SEU rate = 3.33×10^{-8} upset/bit-day for GEO MIN, 100 mil Al

LSRAM single bit cross section



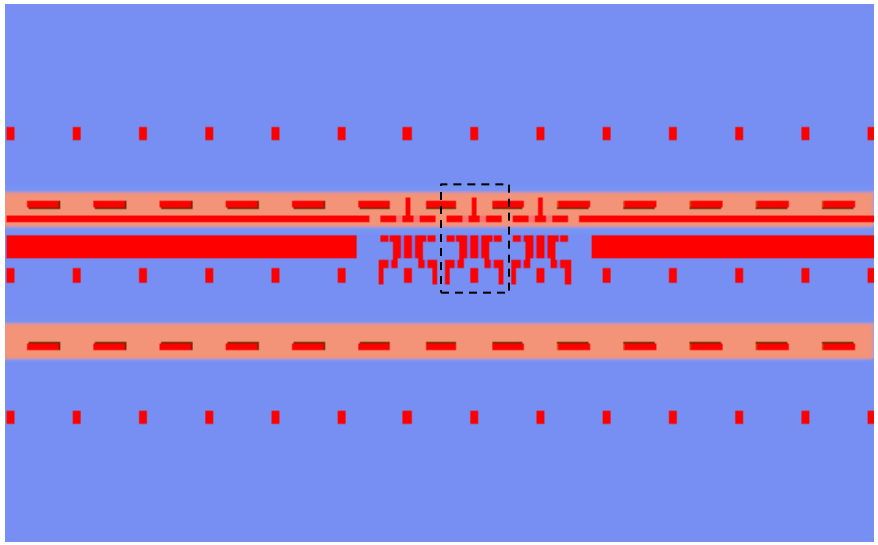
SRAM	Area (µm²)
µSRAM	7.74
LSRAM	4.07

LET_{th}	W	S	σ_{sat}
0.85	10	1	4.5×10^{-9}

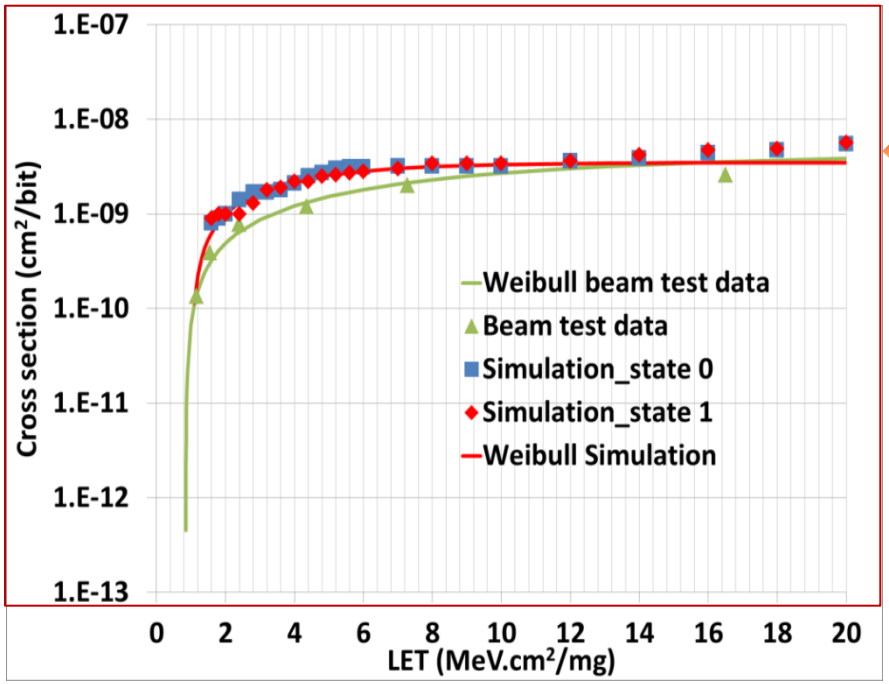
- LSRAM SEU rate = 4.03×10^{-8} upset/bit-day for GEO MIN, 100 mil Al

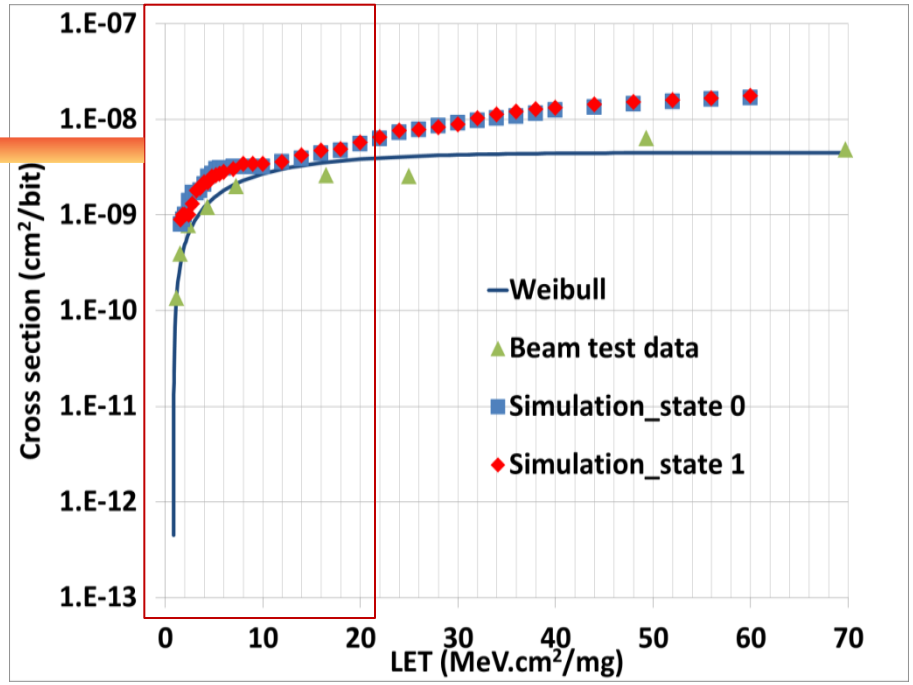
LSRAM SEU TCAD simulation

- 3D TCAD simulations using RCI tools are performed to compare and calibrate with beam test results
- The 3D structure includes three LSRAM cell and “source-ties” to account for the SRAM’s neighboring cells
  - “source-ties” are additional junctions tied to V_{dd} and ground, to accurately simulate charge collection
  - The dashed lines represent the targeted LSRAM cell boundary



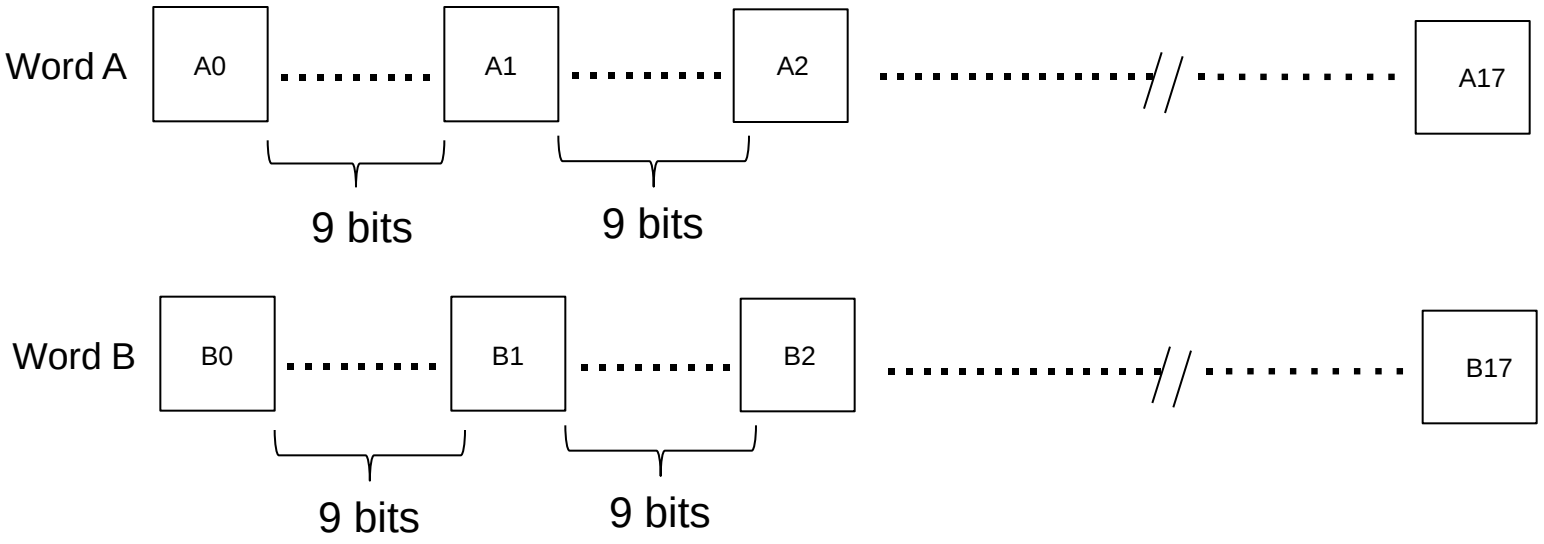
Correlate Beam Test Data with TCAD





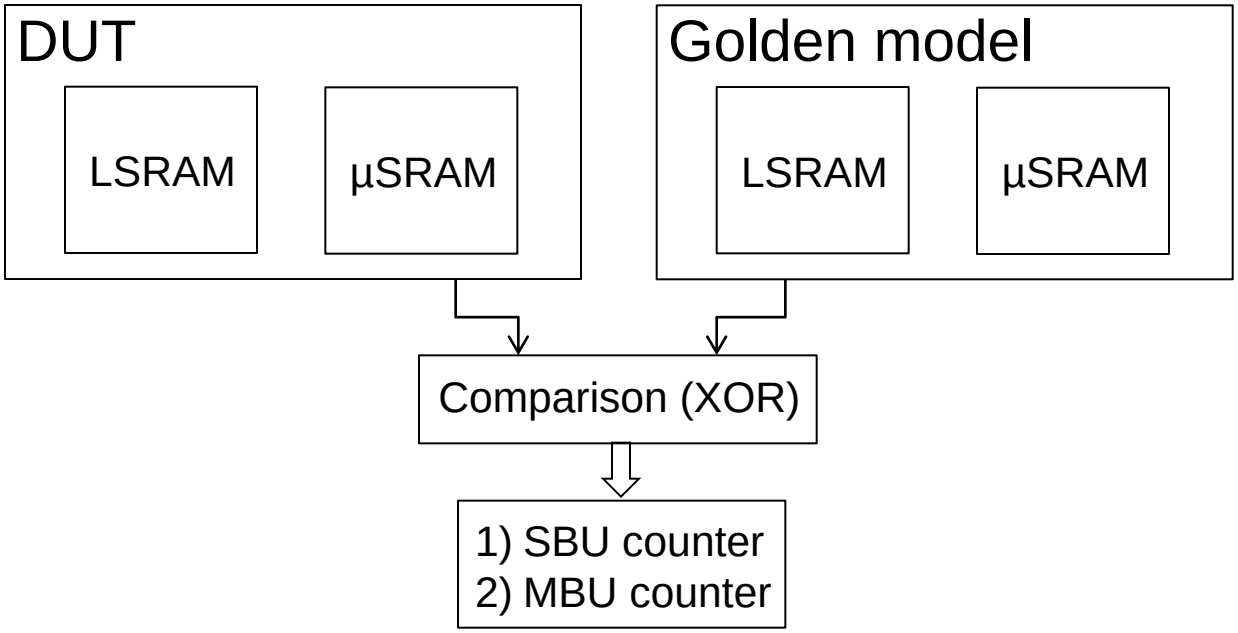
- The simulation results show a good correlation with beam test data at lower LET
  - At higher LETs the simulations deviate from testing data (results under investigation)
- The cross sections only deviate at higher LET and doesn't affect error rate prediction
  - The LET spectrum in space is dominated by low LET ions
- The upset rates using the simulated cross section and beam test data are very close
  - 4.03×10^{-8} upset/bit-day for beam test data
  - 4.67×10^{-8} upset/bit-day for the simulations

Mitigation of MBU in RTG4



- MBUs are mitigated by the interleaving of logical bits in the physical memory blocks in RTG4
- In RTG4 logically adjacent bits are separated by 9 physical bits

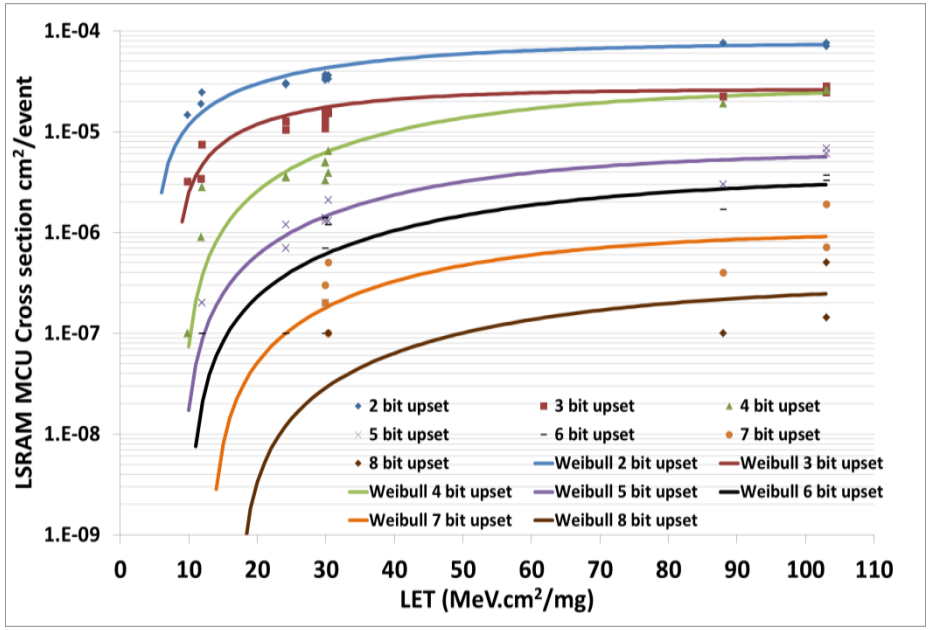
Fabric SRAM MBU detection

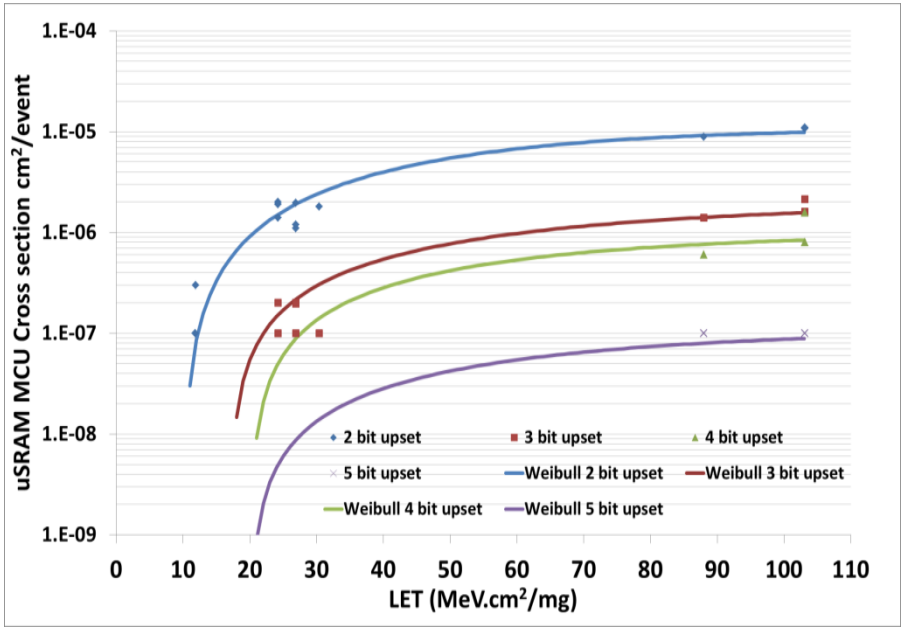


- The post-irradiation state of the SRAMs is compared to the “golden” SRAMs pre-irradiation state
- Readback of the SRAM is executed and processed to determine the number of SBU, MBU and MCU count
- Testing performed at low flux and refresh period is optimized to allow full read of the memory
  - The probability of multiple ion strikes in the time it takes to read the memory is negligible

MBU and MCU results

LET (MeV.cm²/mg)	Total Fluence (ions/cm²)	Flux (ions/cm²/s)	MBU
9.8 to 103	1.72×10^8	1×10^4 to 5×10^4	0





- Zero MBU are observed with RTG4 built-in interleaving
- MCU size 2 to 8 are observed but can be corrected with EDAC

Reprogramming

- Preliminary data shows reprogramming successful up to 106 krad from Heavy-Ion Irradiation

DUT Name	Total Dose from Heavy Ion	Reprogram Passed	Functional
RTG4_S07	80 krad	Yes	Yes
RTG4_S08	47 krad	Yes	Yes
RTG4_S09	48 krad	Yes	Yes
RTG4_S10	106 krad	Yes	Yes

Summary

- RTG4 Push-Pull Flash configuration cell is SEU immune
- No SEL observed at 100 ºC and LET > 100 MeV.cm^2/mg
- SEU Error Rate at Geo Min
  - STMRFF error rate : 5.01x10^{-12}
  - LSRAM (No EDAC) bit error rate : 4.03x10^{-8}
  - µSRAM (No EDAC) bit error rate : 3.33x10^{-8}
- 3D TCAD simulations allow good error rate prediction
- Zero MBU observed for LSRAM or µSRAM
- MCU are observed but can be corrected with EDAC

RTG4 Test Plan

RTG4 Radiation Test Plan

July 1st & Oct 6th SEE@LBNL	Aug 18th TID@NASA	Sept 14th TID@VU
RT4G150 : **1. SEU** - SRAM with EDAC **2. SET** - Fabric logic - Mathblock - Global clock - SpaceWire - MSIO & MSIOD **3. SEFI** - SERDES/PCIe - PLL - DDR controller **4. Re-programming in beam**	**RT4G150 :** **1. Functionality** **2. Power Supply Current** **3. Input Logic Threshold (VIL/VIH)** **4. Output Drive Voltage (VOL/VOH)** **5. Propagation Delay** **6. Transition Time** **7. Reprogramming**	**RT4G150 :** **1. X-ray comparison**

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