IGLOO2/SmartFusion2

Clock Conditioning Circuit with PLL Configuration

Microsemi

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Introduction

The Fabric Clock Conditioning Circuit (CCC) Configurator enables you to configure the CCC/PLL blocks available on IGLOO2/SmartFusion2 devices (Figure 1).

The Fabric CCC can condition up to eleven input clocks to generate up to four clocks. Each of the four output clocks can directly drive the global network and/or the local routing network.

Each of the four output clocks can be driven by:

- One of eight PLL output phases
- One of four General Purpose Divider (GPD) outputs
- One of eleven input clocks

The reference clock of the PLL can be driven by one of eleven input clocks.

Each of the four GPDs can be driven by either one of eleven input clocks or one of eight PLL output phases. Refer to the Microsemi SmartFusion2 Clocking Resources User Guide for details on the CCC architecture. The configuration of the CCC can be broken down into the following three major blocks:

- Output Clocks GLx/Yx configuration
    - Clock source selection
    - Clocks frequency and phase configurations
    - Secondary clock selection if dynamic glitchless multiplexing is used
- PLL configuration
    - PLL clock generation configuration including external feedback support
    - Spread Spectrum Modulation configuration
- General Purpose Divider (GPD) configuration

The Fabric Clock Conditioning Circuitry (CCC) is configured using flash cells based on the selections made in this configurator.
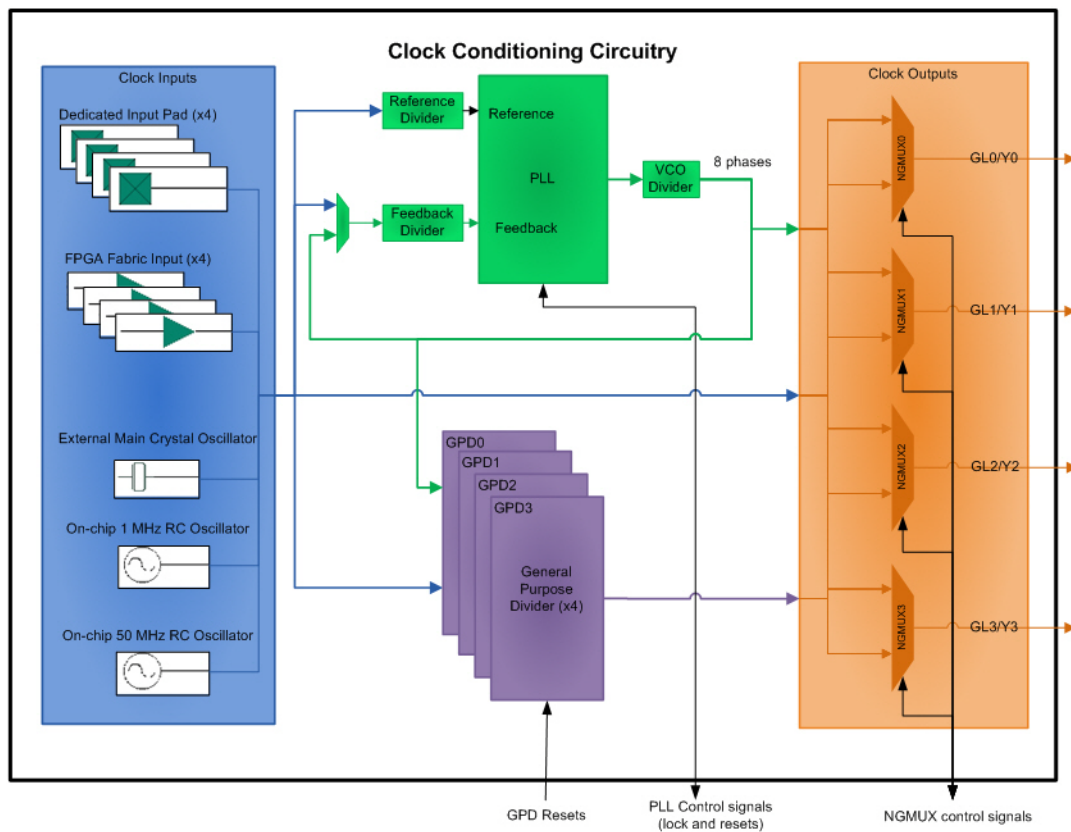
Figure 1 • Clock Paths Overview

1 – Configuration Options

Basic Configuration

Microsemi recommends the following flow to configure the clock generated by the CCC for basic use cases:

1. Select the number of desired output clocks (up to four)
2. For each selected output clock, set the required output frequency
3. Configure the CCC/PLL reference clock source and frequency

In basic configuration, the PLL is always used to generate the output frequency. The feedback of the PLL is internal to the CCC.

Actual output frequencies achieved by the CCC configurator are shown in the Actual column of the basic tab, as in Figure 1-1.
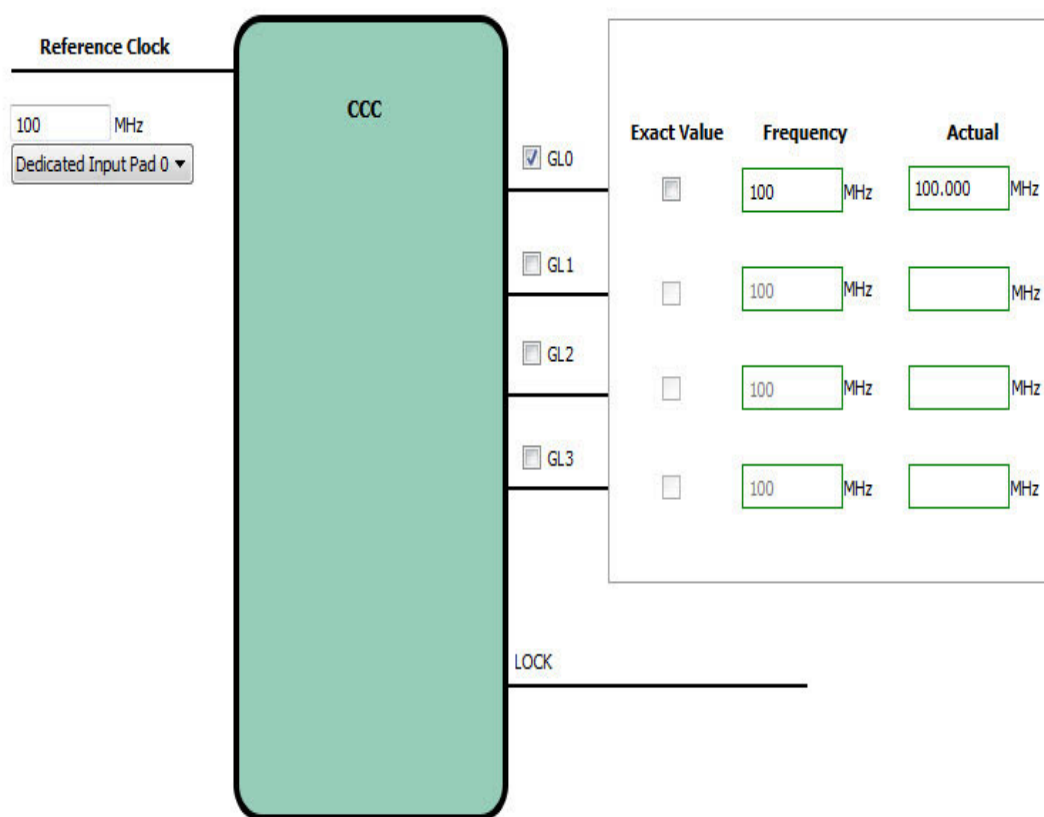

Figure 1-1 • **Basic CCC Configuration Tab**

Advanced Configuration

For advanced use-cases, Microsemi recommends using the following flow to configure the clock generated by the CCC (flow proceeds from right to left in the GUI):

1. Select the number of desired output clocks (up to four).
2. For each selected output clock, set the required output frequency.
3. For each selected output clock, select the desired reference (input) clock from which the output will be derived. It can be either:
   – One of CCC input clocks (PLL bypass mode).
   – One of 8 PLL output phases.
4. If required for each output, configure the glitchless MUX secondary output frequency and reference (input) clock from which it will be derived. It can be either:
   – One of CCC input clocks
   – One of the 8 PLL output phases
5. If required:
   – Select the PLL reference clock source and frequency
   – Select the PLL feedback source
6. Enter the frequency of each selected source clock(s) (either as the PLL reference or direct source for the output). The configurator uses those frequencies to compute the division factor of the PLL reference and feedback dividers as well as the GPD dividers.
7. Configure advanced options, such as Output synchronization configuration and Spread Spectrum.

The configurator automatically tries to compute a configuration that meets the frequency requirements and all the internal CCC/PLL constraints. If the configurator is unable to find an exact solution for all requirements, it finds a configuration that globally minimizes the error between the required and actual frequency.

Actual data (divider settings, PLL output frequency, and actual outputs frequencies) are shown in the advanced dialog in blue (Figure 1-2).
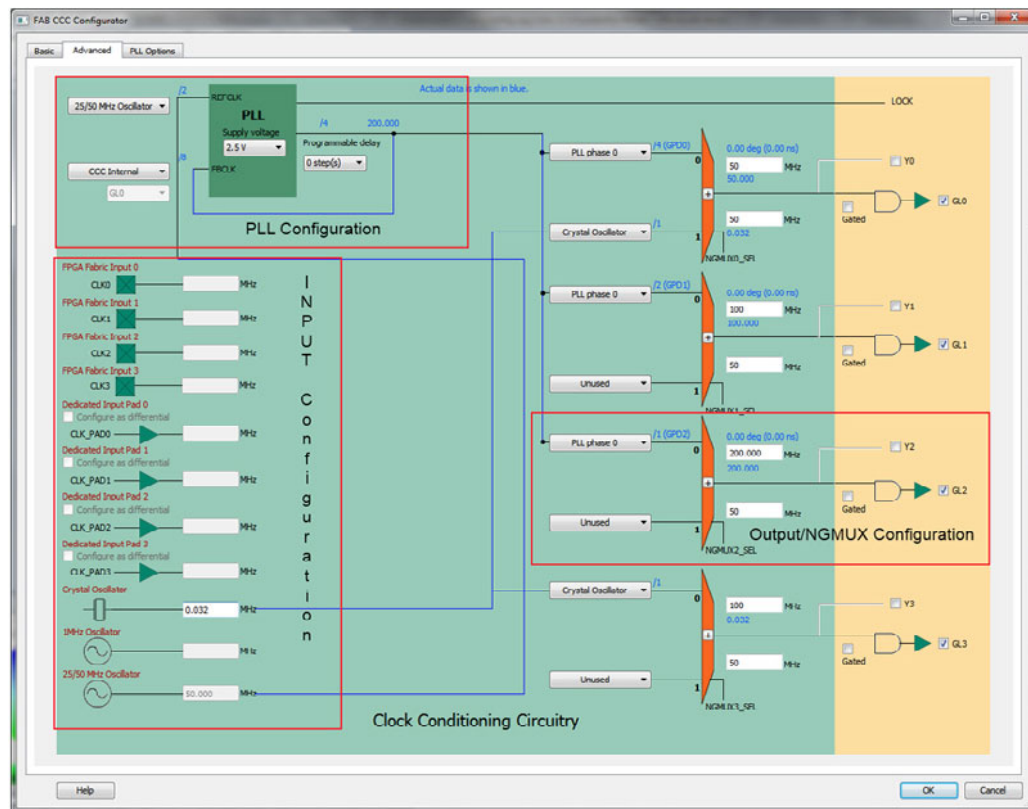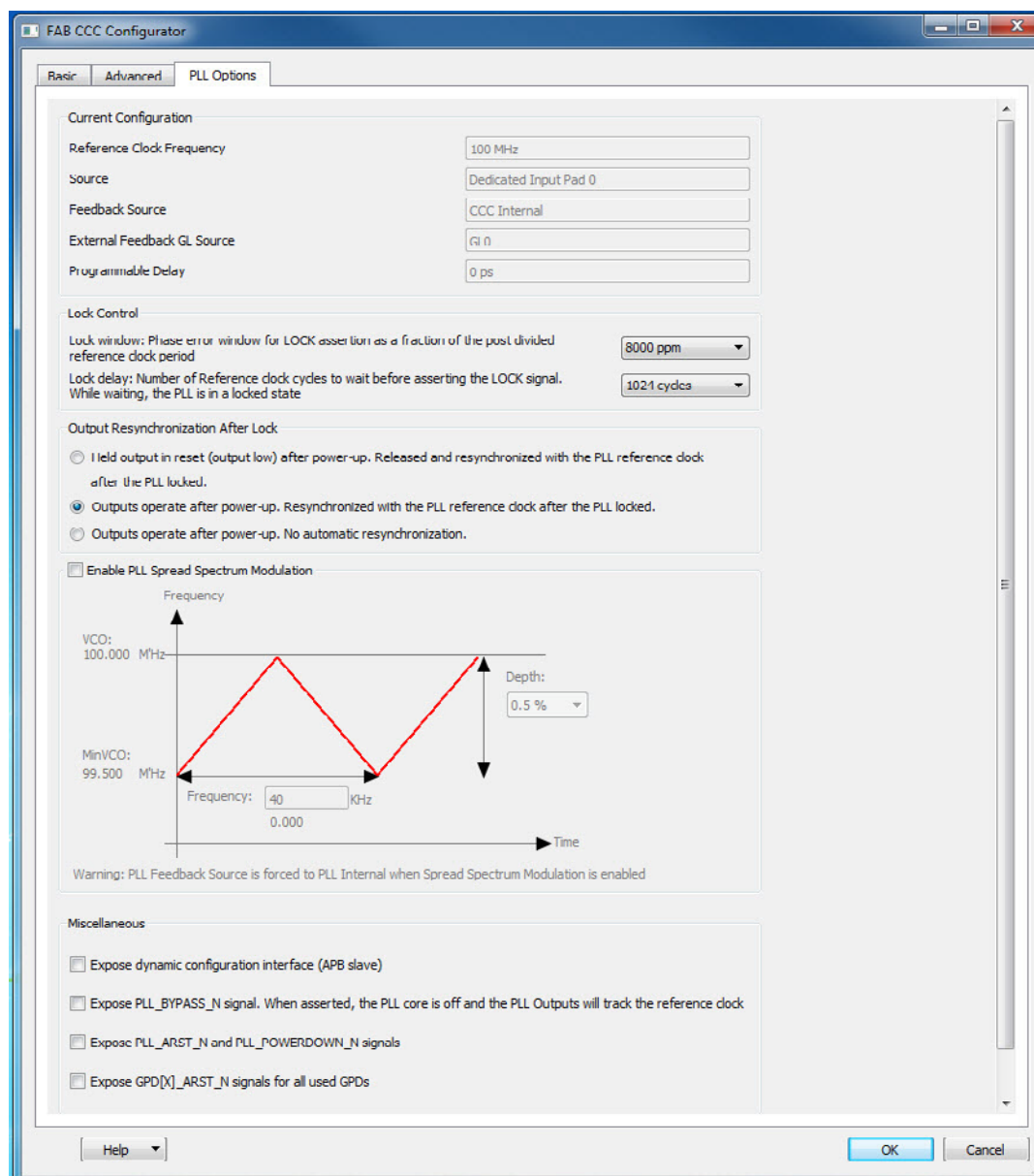

Figure 1-2 • **Advanced CCC Configuration Tab**

Figure 1-3 • Advanced PLL Options

Basic Tab

Output Clocks Selection

You must select at least one of the output clocks (Figure 1-4). The GL0, GL1, GL2 and GL3 output clocks drive a global network in the FPGA fabric.

Figure 1-4 • **Output Clocks Selection**

Output Clock Frequency

You must specify the required output clock frequency (Figure 1-5). Those frequencies are used by the CCC configurator to compute the configuration of the CCC dividers and PLL to meet the requirements. Actual column displays the actual value the configurator was able to achieve.

Figure 1-5 • **Output Clock Frequency**

PLL Reference Clock Source and Frequency

The following sources are available from the reference clock pull-down menu.

Dedicated Input Pad - The clock source is one of the four regular FPGA I/Os that have a dedicated path to the CCC.

Fabric Input - The clock source is one of the four signals coming from the FPGA Fabric:

- FPGA Fabric Input 0
- FPGA Fabric Input 1
- FPGA Fabric Input 2
- FPGA Fabric Input 3

Oscillators - The source is from one of the three oscillators:

- **Crystal Oscillator** - The source is an external Crystal or an external RC circuit connected to the main crystal oscillator external pins. Refer to the Microsemi SmartFusion2 Clocking Resources User Guide for details about how the external crystal must be connected on the board to the IGLOO2/SmartFusion2 device.
- **1MHz RC Oscillator** - The source is the on-chip 1 MHz oscillator.
- **25/50MHz RC Oscillator**: The source is the on-chip 50 MHz oscillator.

Advanced Tab

The advanced configuration tab inherits settings from the basic tab. Modifying a parameter in the Advanced tab that cannot be reflected in the Basic tab results in a warning in the Basic tab.

Output Clocks

You must select at least one of the output clocks. The GL0, GL1, GL2 and GL3 clocks drive a global network in the FPGA fabric; Y0, Y1, Y2 and Y3 drive local routing resources in the FPGA fabric.

Primary Clock Source Selection
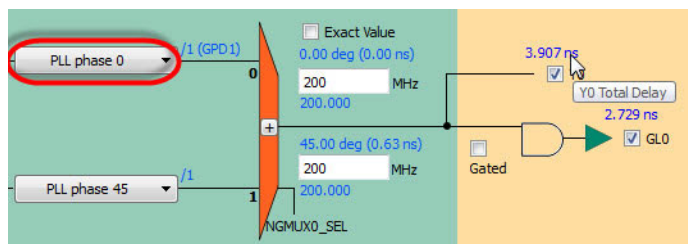
Figure 1-6 • **Primary Clock Source Selection**

The source of the GLx/Yx clocks (Figure 1-6) can be:

PLL - The PLL block offers eight phases (0 deg to 315 deg in 45 deg steps). The actual phases and resulting delays are highlighted in blue on the configurator UI. The actual phase is not the same as the selected phase if the output divider is not 1 (actual_phase = selected_phase / output_divider).

Dedicated Input Pad - The clock source is one of the four regular FPGA I/O's that has a dedicated path to the CCC.

FPGA Fabric Input - The clock source is one of the four fabric input signals coming from the FPGA Fabric.

Oscillators - The source is from one of the three oscillators:

- **Crystal Oscillator** - The source is an external Crystal or an external RC circuit connected to the main crystal oscillator external pins. Refer to the Microsemi SmartFusion2 Clocking Resources User Guide for details about how the external crystal must be connected on the board to the IGLOO2/SmartFusion2 device.
- **1MHz RC Oscillator** - The source is the on-chip 1 MHz oscillator.
- **25/50MHz RC Oscillator** - The source is the on-chip 50 MHz oscillator.

Secondary Clock Source Selection (Glitchless Multiplexer NGMUX0/1/2/3_SEL)
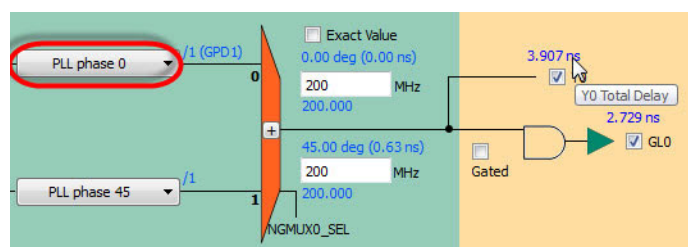
Figure 1-7 • **Secondary Clock Source Selection**

Each output can be configured to use a secondary output clock source (Figure 1-7). Selecting a secondary output exposes the input signal NGMUXx_SEL (with x = 0, 1, 2, 3). This signal can be used to dynamically transition between the primary and secondary output. The transition between the primary and secondary clock is guaranteed to be glitchless

The source of the GLx/Yx secondary clocks can be:

Unused (default)

PLL - The PLL block offers 8 phases (0 deg to 315 deg by 45 deg steps). The actual phases and resulting delays are highlighted in blue on the configurator UI. The actual phase is not the same as the selected phase if the output divider is not 1 (actual_phase = selected_phase / output_divider).

Dedicated Input Pad - The clock source is one of the four regular FPGA I/Os that has a dedicated path to the CCC

FPGA Fabric Input - The clock source is one of four fabric input signals coming from the FPGA Fabric.

Oscillators - The source is from one of the three oscillators:

- **Crystal Oscillator** - The source is an external Crystal or an external RC circuit connected to the main crystal oscillator external pins. Refer to the Microsemi SmartFusion2 Clocking Resources User Guide for details about how the external crystal must be connected on the board to the IGLOO2/SmartFusion2 device.
- **1MHz RC Oscillator** - The source is the on-chip 1 MHz oscillator.
- **25/50MHz RC Oscillator** - The source is the on-chip 50 MHz oscillator.

Output Clock Frequency

You must specify the required primary output clock frequency as well as the required secondary output clock frequency if used. Those frequencies are used by the CCC configurator to compute the configuration of the CCC dividers and PLL to meet the requirements. The dividers and their names are highlighted in blue in the UI (Figure 1-8).
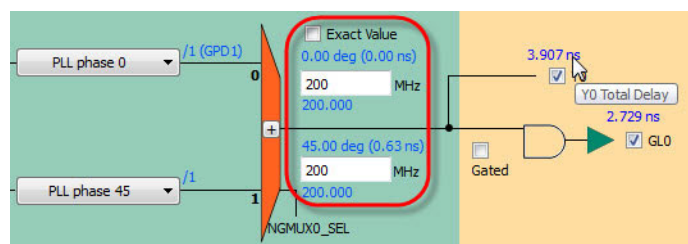
Figure 1-8 • **Output Frequency**

Gated Clock Configuration

For GLx only, you may choose to have an enable (GLx_EN) signal that can turn off the entire global clock network (Figure 1-9). Refer to the Microsemi SmartFusion2 Clocking Resources User Guide for details about the global and clock architecture of the IGLOO2/SmartFusion2 device.
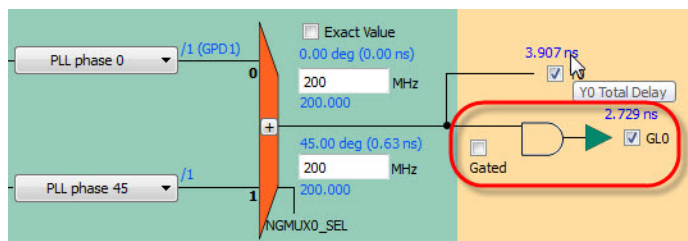
Figure 1-9 • **Gated Clock Configuration**

Inversion Configuration

Each output can be inverted if required (Figure 1-10). The inversion affects both the primary and secondary clock. Click the + sign of NGMUX0_SEL to get the inverted output.
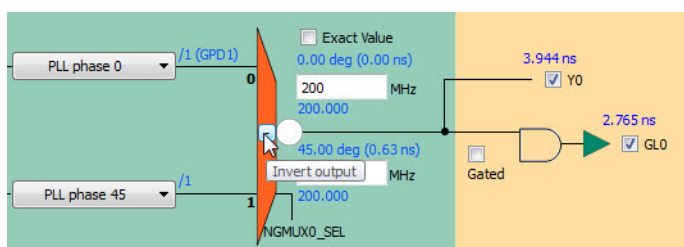
Figure 1-10 • **Inverted Configuration**

Total Output Delay

The CCC Configurator automatically computes the total input to output delay of Y0/1/2/3 and GL0/1/2/3 and display the delay number (ns) in blue (Figure 1-11).
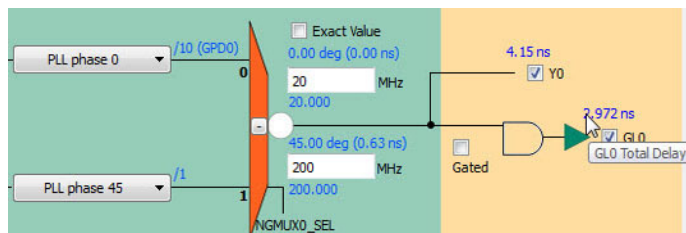
Figure 1-11 • **Total Delay**

PLL Configuration

PLL Reference Clock Source

The following sources are available from the reference clock pull-down menu (Figure 1-12):

Dedicated Input Pad - The clock source is one of the four regular FPGA I/Os that has a dedicated path to the CCC.

FPGA Fabric Input - The clock source can be one of the four input signals coming from the FPGA Fabric.

Oscillators - The source is from one of the three oscillators:

Crystal Oscillator - The source is an external Crystal or an external RC circuit connected to the main crystal oscillator external pins. Refer to the Microsemi SmartFusion2 Clocking Resources User Guide for details about how the external crystal must be connected on the board to the IGLOO2/SmartFusion2 device.
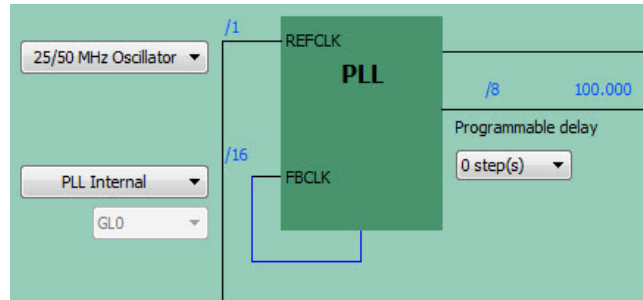
1MHz RC Oscillator - The source is the on-chip 1 MHz oscillator.

25/50MHz RC Oscillator - The source is the on-chip 50 MHz oscillator.

Figure 1-12 • **PLL Reference Clock Source**

PLL Feedback Source

If you use the PLL you can choose to use an internal or an external feedback loop depending on your system level requirements (Figure 1-13):

CCC Internal - Default value

PLL Internal - This is a shorter feedback path integrated into the PLL. You must use the PLL internal feedback when using Spread Spectrum Modulation or if the reference clock frequency is 32 KHz. Note: Programmable delay and output synchronization are not available in this mode.

Dedicated Input Pad - The clock source is one of the four regular FPGA I/Os that has a dedicated path to the CCC

FPGA Fabric Input - The clock source can one of the four input pad signals coming from the FPGA Fabric.
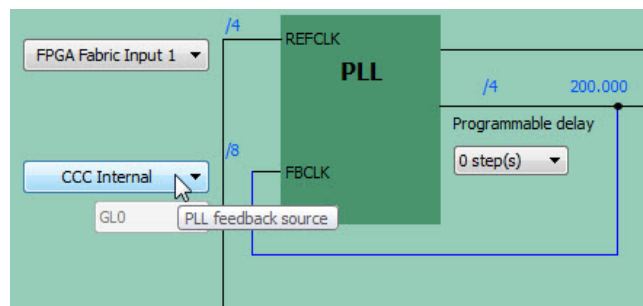
Figure 1-13 • **PLL Feedback Source**

PLL External Feedback Source

If you use the PLL with an external feedback source, all engine computations are based on the assumptions that the external feedback is driven from the selected GLx/Yx fabric CCC output whether through the fabric or externally to the chip (Figure 1-14).

Figure 1-14 • **PLL External Feedback Source**

Programmable Delay Line

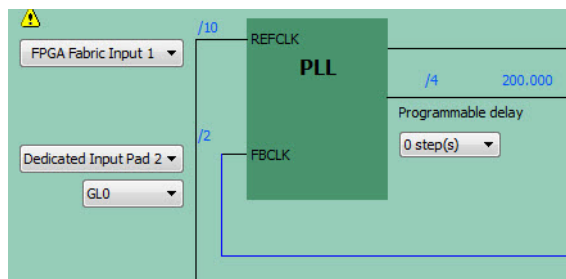The programmable delay line enables you to delay (or advance) the PLL output clock with respect to the PLL reference clock by applying a delay to the reference clock path (or feedback path), as in Figure 1-15.
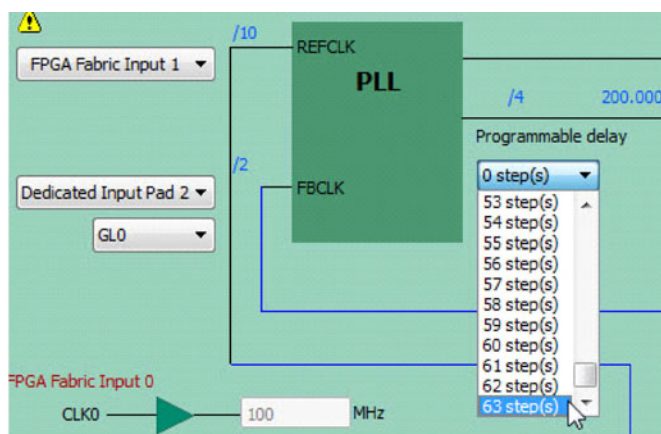
Figure 1-15 • **Programmable Delay Line**

The programmable delay has 64 positive steps when applied to the PLL reference clock path and 64 negative steps when applied to the PLL feedback clock. The programmable delay steps are approximately 100ps in typical conditions. Refer to the Microsemi IGLOO2/SmartFusion2 Datasheet or the timing analysis for the actual value of each step. The programmable delay steps are not Process, Voltage, Temperature (PVT) compensated.

The programmable delay line is not available when using the PLL internal feedback mode.

CCC Input Configuration

You must enter the clock frequency each CCC input used in the configuration as the PLL reference clock, PLL feedback clock or Output direct connection (Figure 1-1). Those frequencies are used to compute the PLL configuration and divider configuration that meet the output frequencies requirements.
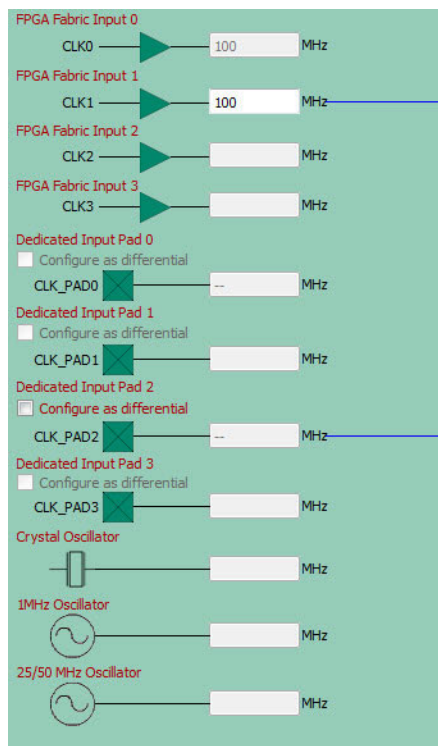
Figure 1-1 • **CCC Input Configuration**

Dedicated Input Pad - Some of the dedicated inputs to the CCC can be configured to use a differential I/ O technology. The location, I/O technology and attributes available for each CCC dedicated input pad is described in the Microsemi IGLOO2/SmartFusion2 Datasheet.

2 – PLL Options

The PLL Options enable you to configure advanced PLL/CCC options, such as Spread-Spectrum, output resynchronization, and reset signals.

The PLL Options summarizes your PLL configuration (Figure 2-1).

Figure 2-1 • **PLL Configuration Summary**

Lock Control

Lock Window - Enables you to configure the maximum phase error allowed for the PLL to indicate it has locked. The lock window is expressed as part per million of the post divided reference clock period.

Lock Delay - Enables you to set the number of Reference REFCLK clock cycles to wait before asserting the LOCK signal. While waiting, the PLL is in a locked state.

Spread Spectrum Modulation

When enabled, the output frequency of the PLL is down-spread over time. Depending on your design requirements you can control the period of the modulation as well as the depth (Figure 2-2).
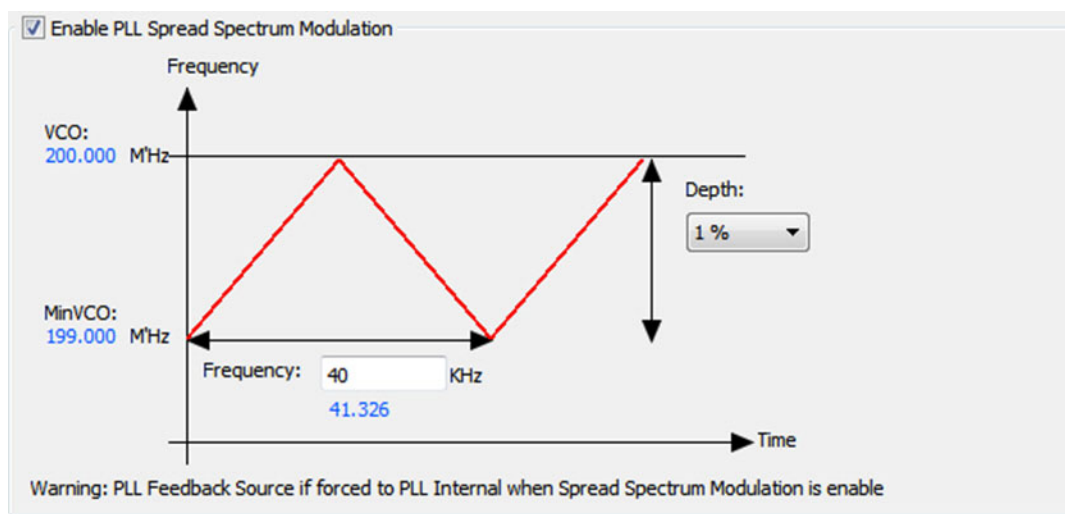

Figure 2-2 • **Spread Spectrum Modulation**

- Depth - Specify the depth of the modulation as a percentage of the PLL output frequency.

- Frequency - Specify the modulation frequency of the PLL output. The modulation frequency must be at least 100 times less than the PLL reference clock frequency. The modulation frequency must be between 20 and 50 KHz

You must use PLL internal feedback to enable spread spectrum modulation.

Spread spectrum modulation is not available if the PLL reference clock frequency is 32 KHz.

Refer to the Microsemi SmartFusion2 Clocking Resources User Guide for details on the Spread Spectrum Modulation feature.

Output Resynchronization After Lock Configuration

SmartFusion 2 CCC contains four General Purpose Dividers (GPD). These dividers' source and division settings are automatically configured based on the frequency requirement you specified in the CCC configurator. GPDs can be used as the source of any outputs. For example, GPD0 can be used on a path to the GL1 output. Microsemi recommends that you re-synchronize GPDs driven by the PLL output clock after the PLL locks to ensure that the first edge of each GPD is aligned with the PLL reference clock and with each other.

There are three different resynchronization options for GPDs/outputs:

Held in reset (output low) after power up. Released and resynchronized with the PLL reference clock after the PLL locked

- If enabled, GPD(s) (driven by the PLL) are held in reset low after power-up. Hence the output(s) (GLx/Yx) connected to those GPD(s) are held low (or high if inverted) after power-up.
- After the PLL lock, the GPD(s) reset are released synchronously with the PLL reference clock.
- The CCC configurator automatically inserts a GPD on each GL/Y output driven by the PLL even if the division factor is 1. This ensures the GL/Y driven by the PLL is held in reset at power-up.
- Does not apply to the output(s)/GPD(s) on the PLL external feedback path (if any).
- Does not apply for the output(s)/GPD(s) not driven by one of the PLL 8 phases output.
- Mode is not available when the PLL feedback source is PLL Internal.

Operate after power up. Released an resynchronized with the PLL reference clock after the PLL locked

- If enabled, GPD(s) (driven by the PLL) output are operational after power-up. Hence the output(s) (GLx/Yx) connected to those GPD(s) are operational after power-up.
- After the PLL lock, the GPD(s) is synchronously reset with the PLL reference clock.
- Does not apply to the output(s)/GPD(s) on the PLL external feedback path (if any).
- Does not apply for the output(s)/GPD(s) not driven by one of the PLL 8 phases output.
- Mode is not available when the PLL feedback source is PLL Internal.

Operate after power-up. No automatic resynchronization

- If enabled, the corresponding GPD(s) output is operating after power-up. Hence the outputs (GLx/Yx) connected to this GPD are operating after power-up.
- There is no resynchronization after the PLL lock.
- All GPD(s) directly connected to one of the eleven input clocks (bypassing the PLL) are configured in this mode.

Refer to the Microsemi SmartFusion2 Clocking Resources User Guide for details on the GPD synchronization timing diagram.

Miscellaneous Options

Expose dynamic configuration interface (APB Slave) - When selected, an APB slave interface is exposed to the FPGA fabric. This interface can be used to read or modified the CCC configuration register from the FPGA fabric. Refer to the Microsemi SmartFusion2 Clocking Resources User Guide for the list of CCC configuration registers.

Expose PLL_BYPASS_N signal - When selected, the input signal PLL_BYPASS_N is exposed to the FPGA Fabric. When this signal is asserted, the PLL core is turned off and the PLL outputs track the reference clock. This signal is active low.

Expose PLL_ARST_N and PLL_POWERDOWN_N signals - When selected, the signals PLL_ARST_N and PLL_POWERDOWN_N are exposed to the FPGA Fabric. When PLL_ARST_N is asserted, the PLL core is turned off and the PLL outputs are low. When PLL_POWERDOWN_N is asserted, PLL is off and is in the lowest power consumption mode. The PLL outputs are low. Both signals are active low.

Expose GPD[x]_ARST_N signal for all used GPDs- When selected, the input signals GPD[x]_ARST_N (with x = 0, 1, 2, 3 depending on which GPD is used in the configuration, see the advanced tab to find out which GPD is used) are exposed to the FPGA Fabric. When asserted, the corresponding GPD output is held low.

Clock Frequency Requirements

You must specify the clock source frequency. Note the following frequency requirements:

- The On-chip 1MHZ Oscillator clock frequency is fixed to 1 MHz and cannot be changed.
- The On-chip 25/50MHZ Oscillator clock frequency is fixed to 50 MHz when the core voltage is 1.2V and 25 MHz when the core voltage is 1.0V and cannot be changed.
- Crystal Oscillator frequency must be between 0.032 MHz and 20 MHz.
- PLL reference clock frequency must be between 1 MHz and 200 MHz or 32KHz*
- Output clock frequencies must be less than 400 MHz.
- Input used in bypass mode frequency must be less than 400 MHz

32 KHz reference clock frequency is not available on all CCC/PLL. Refer to the Microsemi IGLOO2/ SmartFusion2 Datasheet for details.

Output Clock Frequency Below 78 KHz

The lowest output frequency from the CCC when using the PLL is 78 KHz. This is a silicon limitation. To get an output frequency lower than 78 KHz, you must use the Advanced tab of the CCC Configurator to bypass the PLL.

1. On the Basic tab, enter the desired frequency

2. Ignore the Actual Frequency Number displayed in red (Figure 2-3).
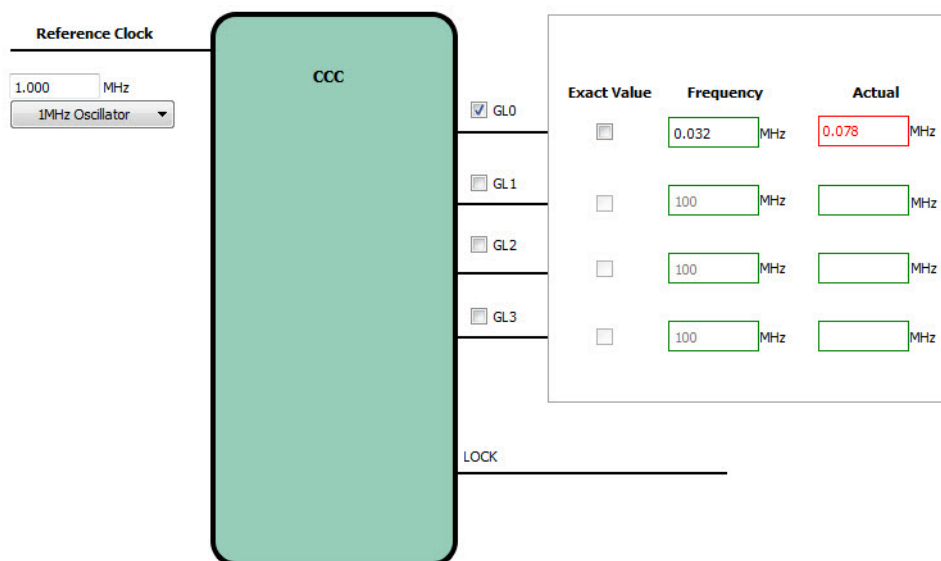
Figure 2-3 • **Actual Frequency Number**

3. In the Advanced tab, de-deselect PLL (to bypass the PLL) and select any one of the following as the clock source (Figure 2-4):
   – Dedicated Input
   – Fabric Input
   – Oscillators

   Your desired frequency is displayed in black as a valid CCC output.
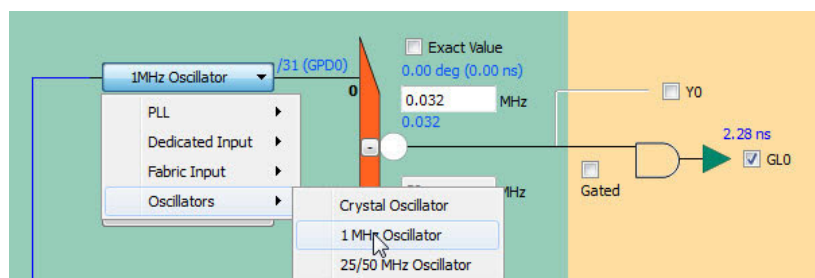
Figure 2-4 • **Bypassing PLL as the Reference Clock Source**

3 – Port Description

Table 3-1 • **Port Description**

Port Name	Direction	PAD?	Description
CLK0_PAD	In	Yes	Input clock when using **Dedicated Input Pad 0** configured as single ended I/O
CLK1_PAD	In	Yes	Input clock when using **Dedicated Input Pad 1** configured as single ended I/O
CLK2_PAD	In	Yes	Input clock when using **Dedicated Input Pad 2** configured as single ended I/O
CLK3_PAD	In	Yes	Input clock when using **Dedicated Input Pad 3** configured as single ended I/O
CLK0_PADP	In	Yes	Input clock when using **Dedicated Input Pad 0** configured as differential I/O. P side
CLK1_PADP	In	Yes	Input clock when using **Dedicated Input Pad 1** configured as differential I/O. P side
CLK2_PADP	In	Yes	Input clock when using **Dedicated Input Pad 2** configured as differential I/O. P side
CLK3_PADP	In	Yes	Input clock when using **Dedicated Input Pad 3** configured as differential I/O. P side
CLK0_PADN	In	Yes	Input clock when using **Dedicated Input Pad 0** configured as differential I/O. N side
CLK1_PADN	In	Yes	Input clock when using **Dedicated Input Pad 1** configured as differential I/O. N side
CLK2_PADN	In	Yes	Input clock when using **Dedicated Input Pad 2** configured as differential I/O. N side
CLK3_PADN	In	Yes	Input clock when using **Dedicated Input Pad 3** configured as differential I/O. N side
CLK0	In	No	Input clock from FPGA core when using **FPGA Fabric Input 0**
CLK1	In	No	Input clock from FPGA core when using **FPGA Fabric Input 1**
CLK2	In	No	Input clock from FPGA core when using **FPGA Fabric Input 2**
CLK3	In	No	Input clock from FPGA core when using **FPGA Fabric Input 3**
RCOSC_25_50MHZ	In	No	Input clock when using **25/50 MHz Oscillator**
RCOSC_1MHZ	In	No	Input clock when using **1 MHz Oscillator**
XTLOSC	In	No	Input clock when using **Crystal Oscillator**'
GL0	Out	No	Generated clock driving FPGA fabric global network 0

Table 3-1 • **Port Description (continued)**

Port Name	Direction	PAD?	Description
GL1	Out	No	Generated clock driving FPGA fabric global network 1
GL2	Out	No	Generated clock driving FPGA fabric global network 2
GL3	Out	No	Generated clock driving FPGA fabric global network 3
GL0_ENABLE	In	No	Enable signal for the clock driving FPGA fabric global network 0
GL1_ENABLE	In	No	Enable signal for the clock driving FPGA fabric global network 1
GL2_ENABLE	In	No	Enable signal for the clock driving FPGA fabric global network 2
GL3_ENABLE	In	No	Enable signal for the clock driving FPGA fabric global network 3
Y0	Out	No	Generated clock driving FPGA fabric local routing resource
Y1	Out	No	Generated clock driving FPGA fabric local routing resource
Y2	Out	No	Generated clock driving FPGA fabric local routing resource
Y3	Out	No	Generated clock driving FPGA fabric local routing resource
LOCK	Out	No	PLL Lock indicator signal. This signal is asserted (lock) high.
PLL_BYPASS_N	In	No	Shutdown the PLL core when 0. In that case, the PLL outputs are tracking the reference clock.
PLL_ARST_N	In	No	Hold the PLL and the PLL reference and feedback divider in reset. PLL outputs are low.
PLL_POWERDOWN_N	In	No	Shutdown the PLL for the lowest quiescent current. PLL outputs are low.
NGMUX0_SEL	In	No	Output 0 (GL0/Y0) NGMUX selection signal. Glitchlessly switches from the primary to the secondary clock. 0: Primary clock 1: Secondary clock
NGMUX1_SEL	In	No	Output 1 (GL1/Y1) NGMUX selection signal. Glitchlessly switches from the primary to the secondary clock. 0: Primary clock 1: Secondary clock
NGMUX2_SEL	In	No	Output 2 (GL2/Y2) NGMUX selection signal. Glitchlessly switches from the primary to the secondary clock. 0: Primary clock 1: Secondary clock
NGMUX3_SEL	In	No	Output 3 (GL3/Y3) NGMUX selection signal. Glitchlessly switches from the primary to the secondary clock. 0: Primary clock 1: Secondary clock
NGMUX0_HOLD_N	In	No	Output 0 (GL0/Y0) NGMUX hold signal. Synchronously set the NGMUX output low when 0.

Table 3-1 • Port Description (continued)

Port Name	Direction	PAD?	Description
NGMUX1_HOLD_N	In	No	Output 1 (GL1/Y1) NGMUX hold signal. Synchronously set the NGMUX output low when 0.
NGMUX2_HOLD_N	In	No	Output 2 (GL2/Y2) NGMUX hold signal. Synchronously set the NGMUX output low when 0.
NGMUX3_HOLD_N	In	No	Output 3 (GL3/Y3) NGMUX hold signal. Synchronously set the NGMUX output low when 0.
NGMUX0_ARST_N	In	No	Output 0 (GL0/Y0) NGMUX reset signal. Asynchronous reset signal. Can be used to clear NGMUX error state
NGMUX0_ARST_N	In	No	Output 1 (GL1/Y1) NGMUX reset signal. Asynchronous reset signal. Can be used to clear NGMUX error state
NGMUX0_ARST_N	In	No	Output 2 (GL2/Y2) NGMUX reset signal. Asynchronous reset signal. Can be used to clear NGMUX error state
NGMUX0_ARST_N	In	No	Output 3 (GL3/Y3) NGMUX reset signal. Asynchronous reset signal. Can be used to clear NGMUX error state
GPD0_RESET_N	In	No	GPD 0 reset signal. The GPD is held in reset when this signal is low.
GPD1_RESET_N	In	No	GPD 1 reset signal. The GPD is held in reset when this signal is low.
GPD2_RESET_N	In	No	GPD 2 reset signal. The GPD is held in reset when this signal is low.
GPD3_RESET_N	In	No	GPD 3 reset signal. The GPD is held in reset when this signal is low.

A – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at **www.microsemi.com**.

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