Power Matters

Microsemi

Technology Roadmap for Digital Space Flight Products

Microsemi Space Forum Russia – November 2013

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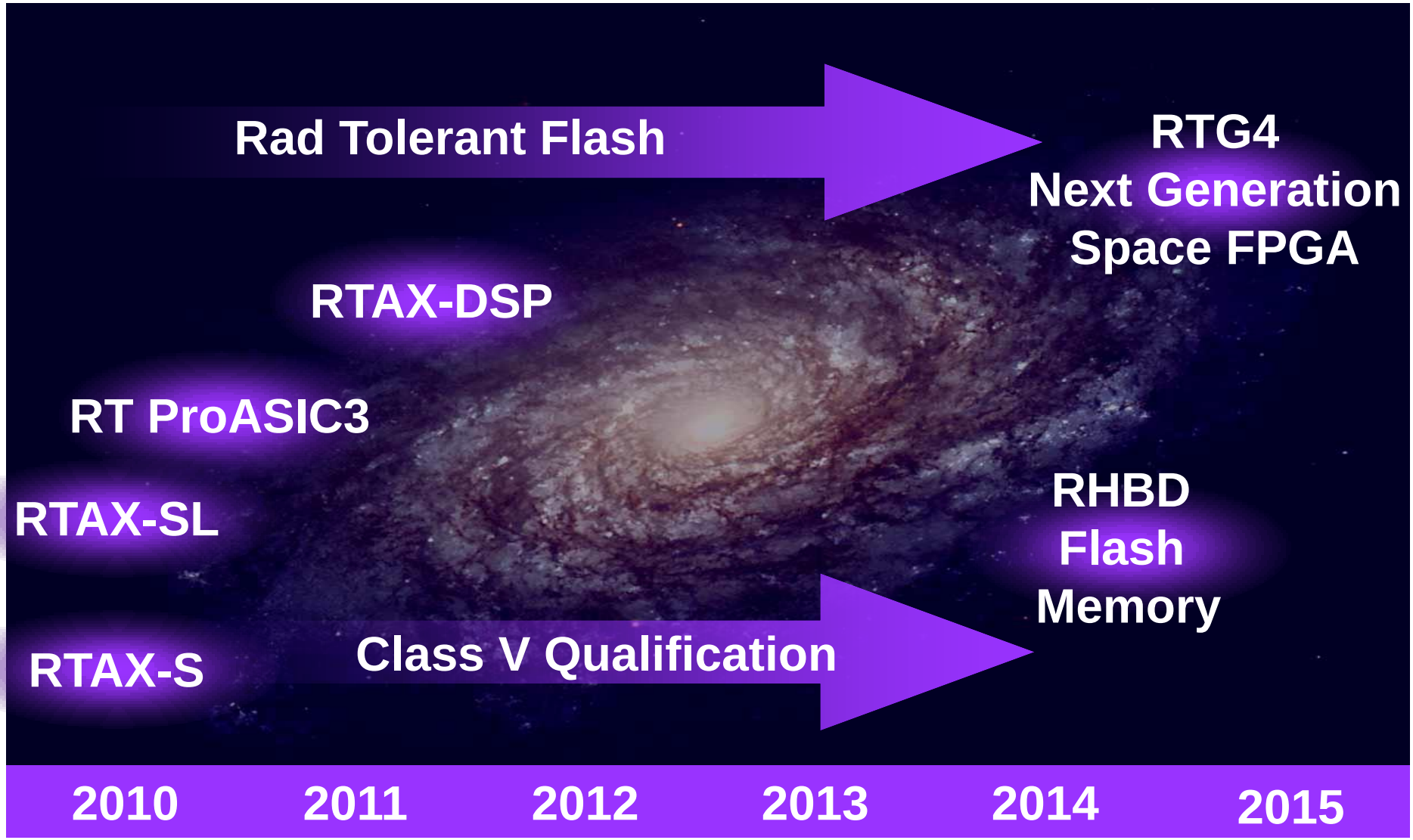
Roadmap for Space-Flight FPGAs



Agenda

- RTG4 – Next Generation FPGAs for Space Flight
- RHBD Flash Memory for Space
- Space System Managers

Next Generation Space FPGAs

- Designed for high-bandwidth data processing in payload applications
  - Abundant high-performance programmable logic fabric
  - Embedded high speed multiply-accumulate blocks
  - Ample on-board memory with fast access time, two block sizes
  - High performance I/Os – SERDES, LVDS, DDR2, …
- Based on 65nm Flash low power process
  - Naturally resistant to configuration upsets
  - Non-volatile configuration – live at power-up, no external boot memory needed
  - Low static power
- RTG4 – radiation enhanced for GEO and deep space
  - Total ionizing dose, Single event effects, Latch-up immunity

RTG4

RTG4 Family Resources

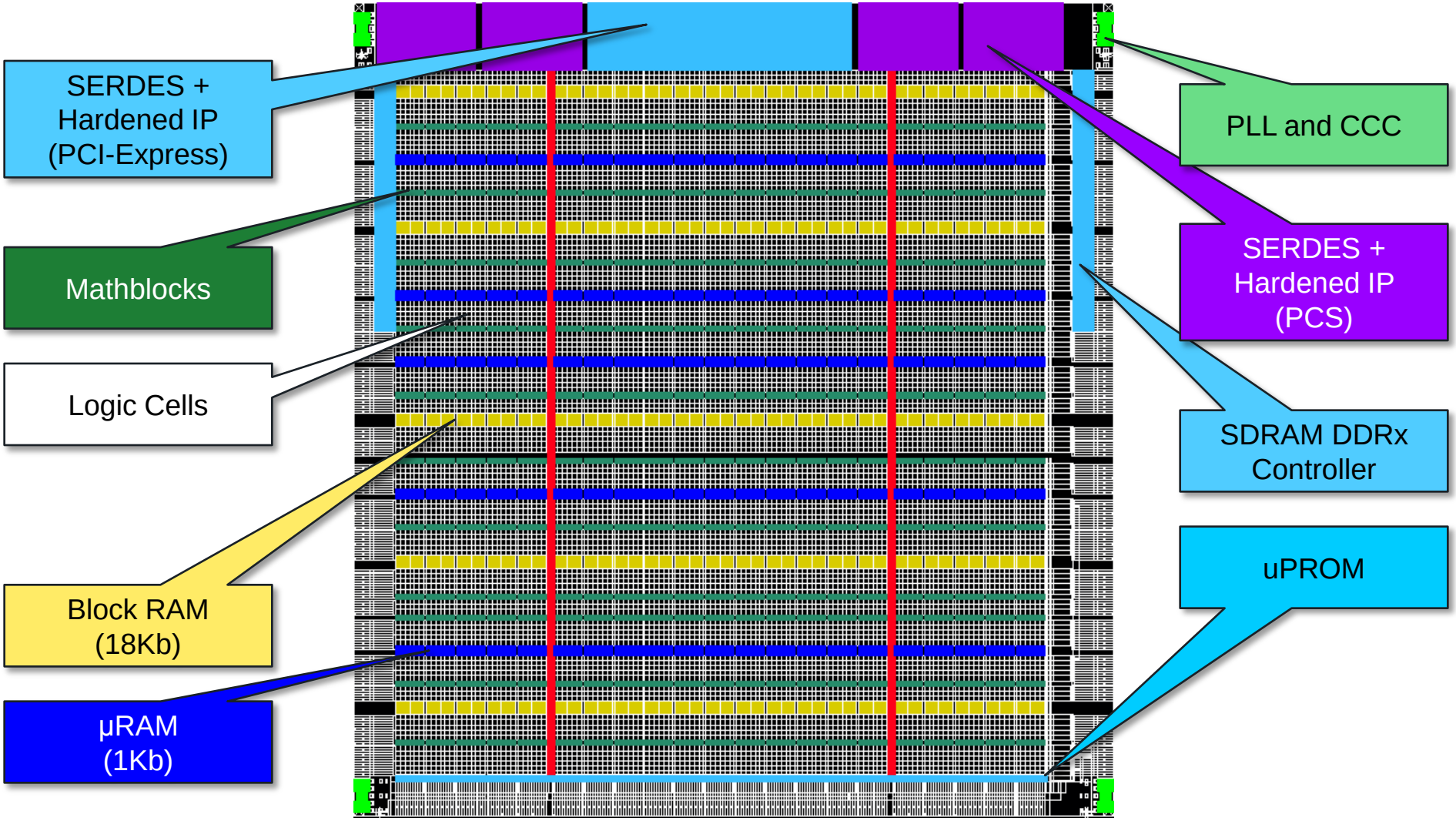
	RT4G075	RT4G150	RT4G200
LUT4 + TMR/SET FF	77,616	151,728	203,400
User IO (non-SERDES)	528	720	816
RAM18K Blocks	111	209	269
uRAM1K Blocks	112	210	270
RAM Mbits	2.1	3.9	5.0
UPROM Kbits	254	381	417
18x18 Multiply-Accumulate Blocks	224	462	594
SERDES lanes	16	24	32
DDR2/3 SDRAM Controller (with ECC)	2x32	2x32	2x32
Globals	24	24	24
PLLs (Rad Tolerant)	8	8	8
Spacewire Interfaces	16	16	16
PCI Express Endpoints	2	2	2
Packages			
CG1432	✓		
CG1657	✓	✓	
CG2092		✓	✓

Radiation Specifications

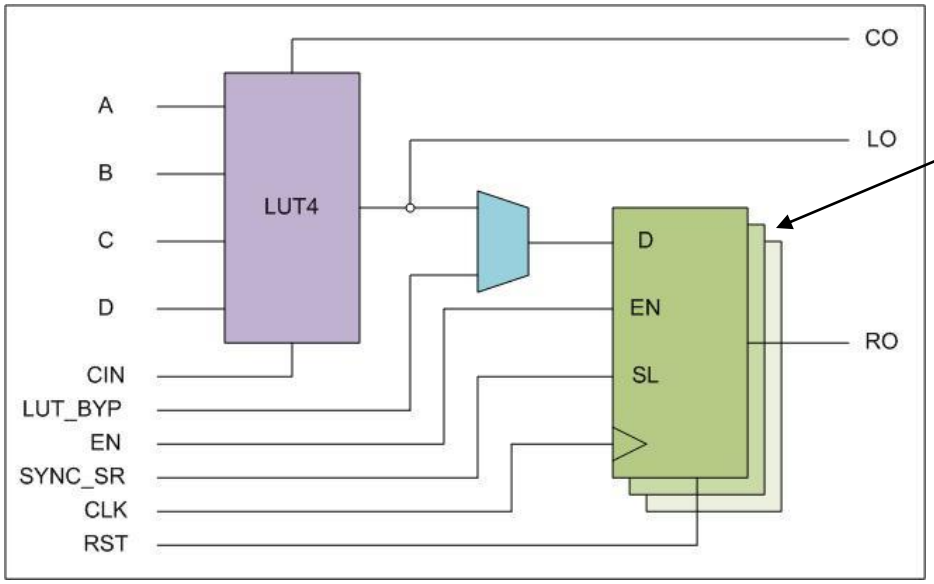
- Total Dose
  - > 100 KRad TID

- Single Event Effects
  - ***No configuration failures*** (to be tested to > 110 MeV-cm^2/mg)
  - No single event latch-up (to be tested to > 110 MeV-cm^2/mg)
  - Mitigation for single event upsets
    - Flip-flops with TMR and asynchronous self-correction (LET_{TH} > 37 MeV-cm^2/mg)
      - Flip-flops in the logic fabric
      - Flip-flops in embedded features – Mathblocks etc
    - On-chip SRAM (RAM18K and uRAM1K)
      - Built-in EDAC
      - 1E-10 errors/bit-day, GEO solar min
  - Mitigation of single event transients
    - Logic cells hardened with SET filter
      - SET filter can be individually enabled / disabled for higher performance
    - Target 1E-8 errors/bit-day, GEO solar min

Flexible Chip Architecture (RT4G150)



RTG4 Logic Module

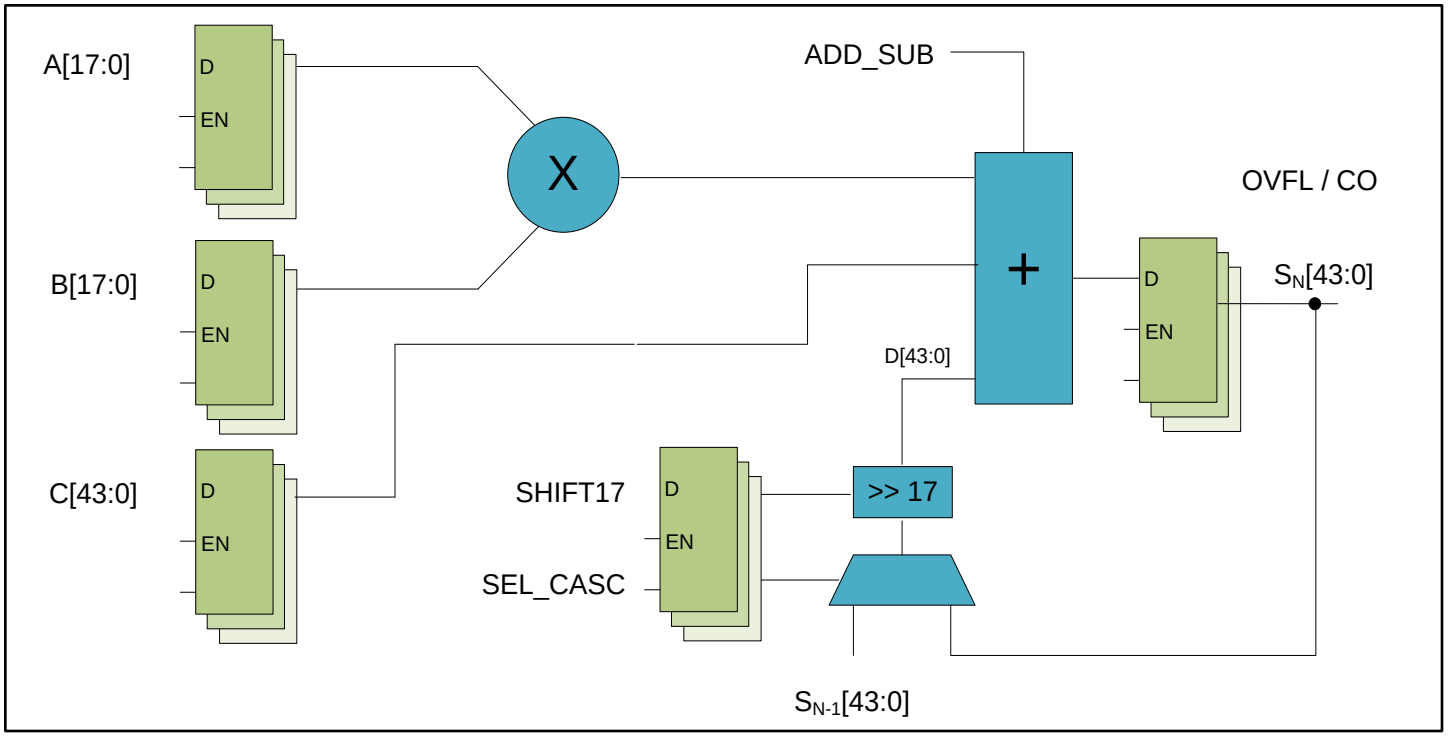


TMR Protected

Simplified Diagram

- Dedicated Flip-flop to enable efficient TMR hardening
  - With enable, global asynchronous set/reset, and local synchronous set/reset
- Fast carry chain to complement Mathblock performance
  - Arithmetic functions (add/subtract)
  - Target 300 MHz for 32-bit functions (no SET filter)
  - Target 250 MHz for 32-bit function (SET filter deployed)
- Industry standard LUT4 for efficient synthesis
- High utilization
  - LUT4 and flip-flop in same module can be used independently
  - Hierarchical routing architecture enables >95% module utilization

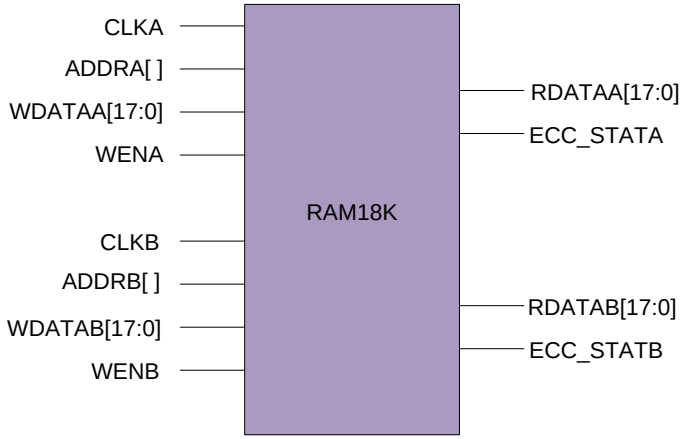
RTG4 Mathblock

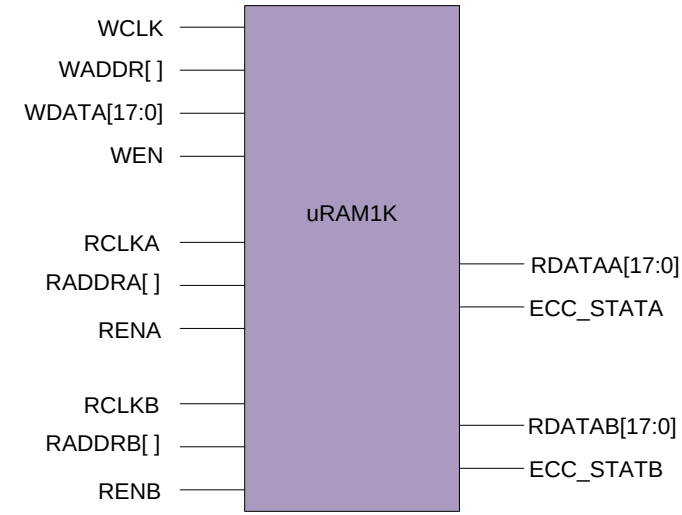


- 18 x 18 multiplier with advanced accumulate
  - New 3-input adder function: (C + D) +/- (A * B)
- High performance for signal processing throughput
  - 250 MHz with SET mitigation
  - 300 MHz without SET mitigation
- Optional SEU-protected registers on inputs and outputs (including C input)

RTG4 Memory Blocks

- Radiation Tolerant
  - Resistant to multi-bit upset
  - Built-in EDAC (SECDED)
- LSRAM18K
  - Dual-port and two-port options
  - High performance synchronous operation
  - Example usage
    - Large FFT memory
- uRAM1K
  - Three Port Memory
    - Synchronous Write Port
    - Two Asynchronous or Synchronous Read Ports
  - Example usage
    - Folded FIR filters and FFT twiddle factors
- Mixed port sizes
  - Write and read port sizes can be different
- 300 MHz performance





RTG4 Memory Organization

- 18-bits data + 6-bits EDAC

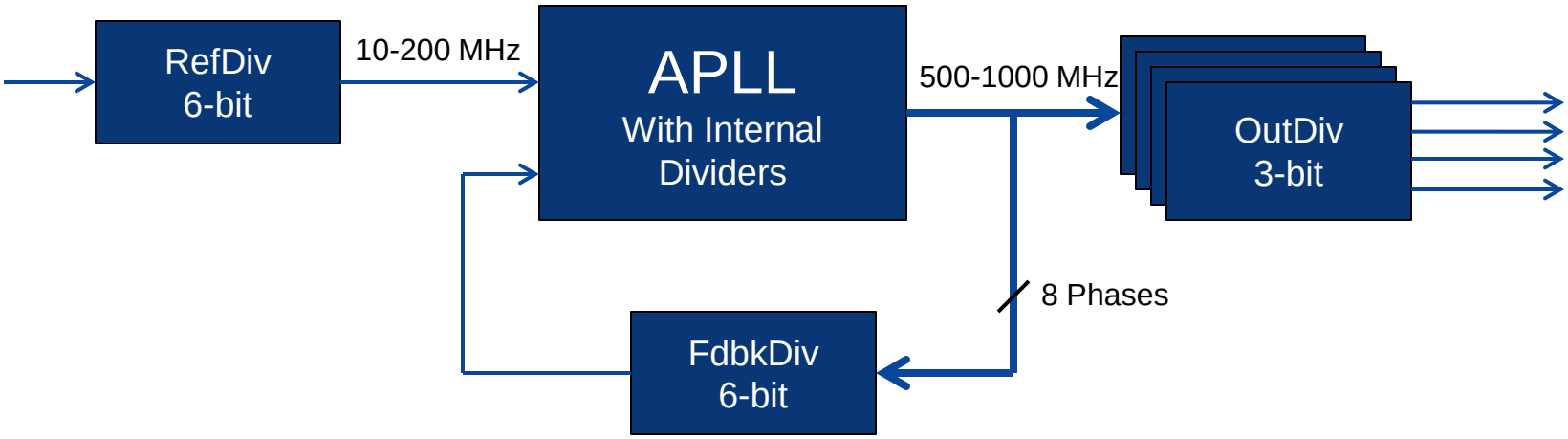
- LSRAM Configuration Options
  - 512 x 36-bits (Optional EDAC)
  - 1024 x 18-bits (Optional EDAC)
  - 2048 x 12-bits (No EDAC)
  - 2048 x 9-bits (No EDAC)

- uRAM1K Configuration Options
  - 64 x 18-bits (Optional EDAC)
  - 128 x 12-bits (No EDAC)
  - 128 x 9-bits (No EDAC)

- Block enables permit concatenation of multiple blocks
  - Deeper and wider configurations

RTG4 APLL / CCC

8 PLL's Per Device



Global Clock Network

- 24 per device
- Frequency range: 0 – 400 MHz

uPROM Non-volatile Memory

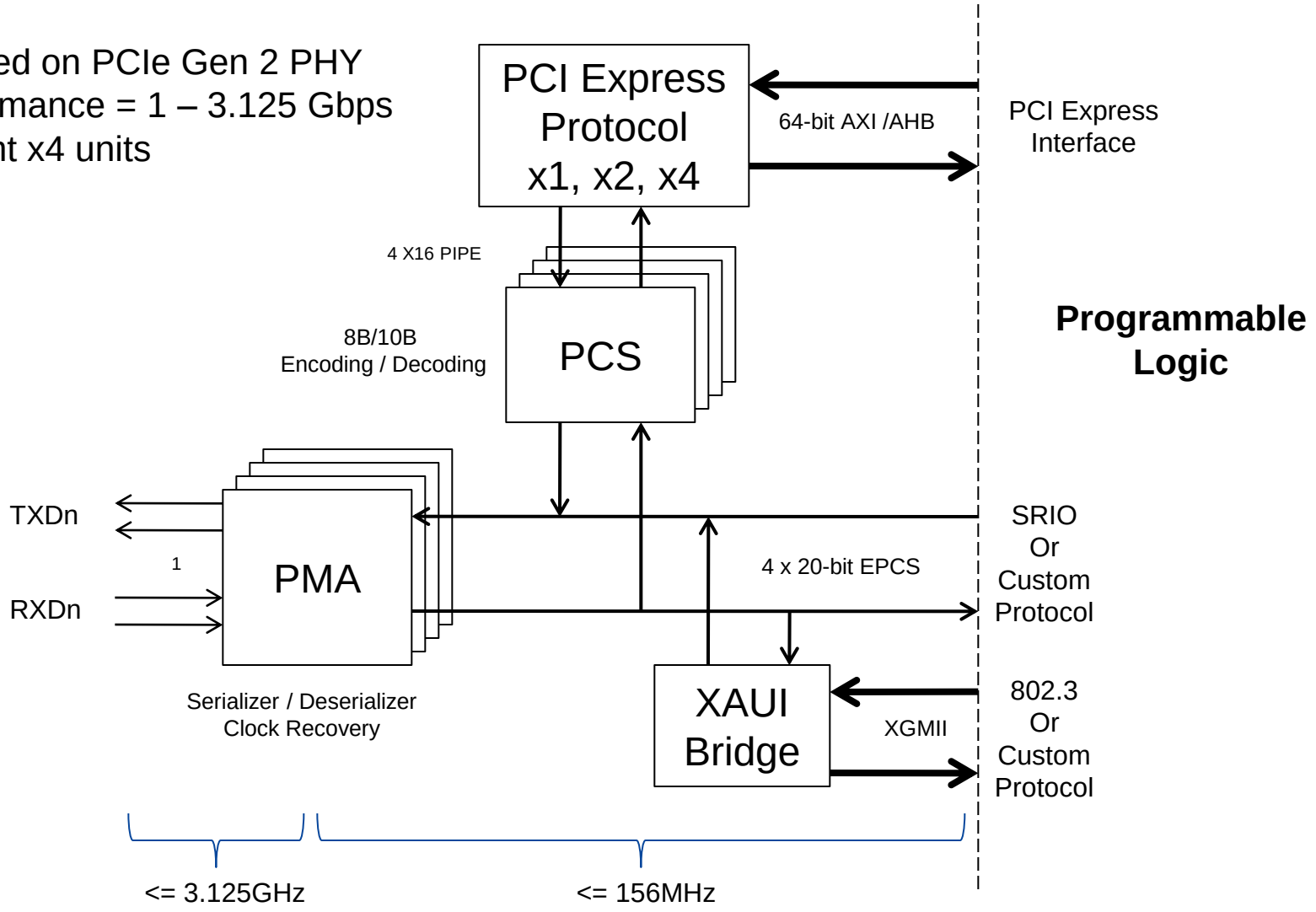
- Non-volatile memory based on FPGA configuration cell
  - Configuration upset immune
  - TID >= 100 Krad
- 254 Kbits to 417 Kbits storage for DSP coefficients
- Initialize RAMs and embedded IP from uPROM
  - Power-on initialization
  - Modification of coefficients during normal operation
- Read performance of 25 MHz x 32-bits

General Purpose IO

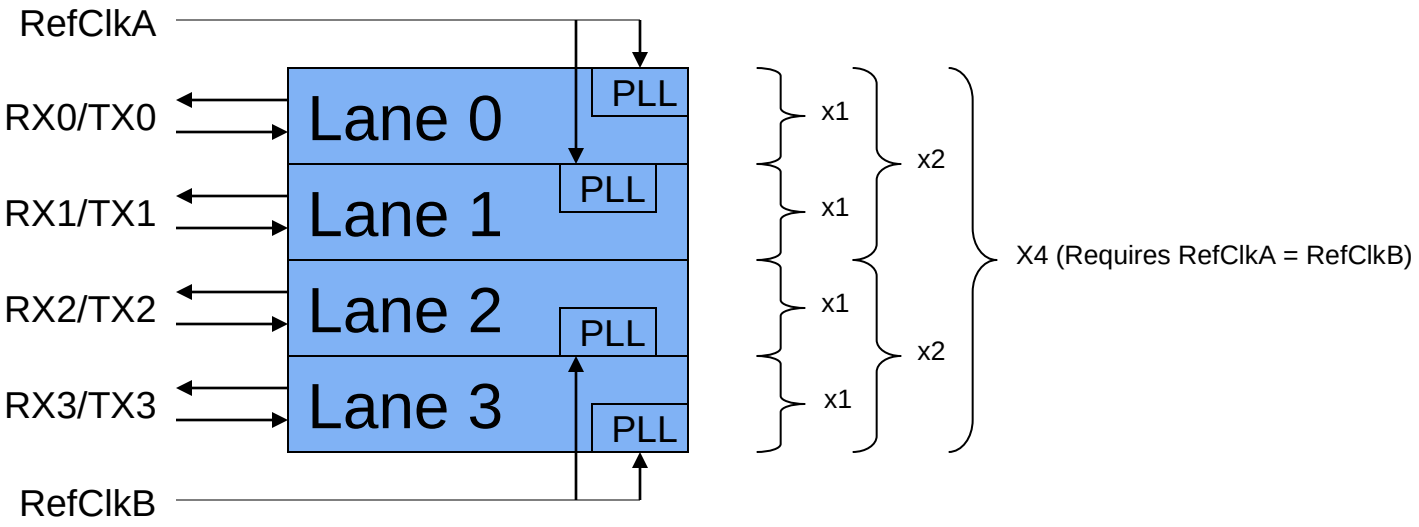
- Single ended standards
  - LVCMOS from 1.2V to 3.3V
  - LVTTL
  - PCI
- Voltage reference standards (600+ Mbps)
  - Includes on-chip termination
  - SSTL2, SSTL18 and SSTL15
    - For DDR2/DDR3 SDRAM memories
  - HSTL18 and HSTL15
    - For SRAM memories
- Differential I/O standards
  - Includes on-chip termination
  - True LVDS (600+ Mbps)
  - Mini-LVDS, M-LVDS, RSDS, LVPECL

3.125Gbps SERDES

PMA Based on PCIe Gen 2 PHY
RT Performance = 1 – 3.125 Gbps
Up to eight x4 units



SERDES Ganging Options



DDRx Controller

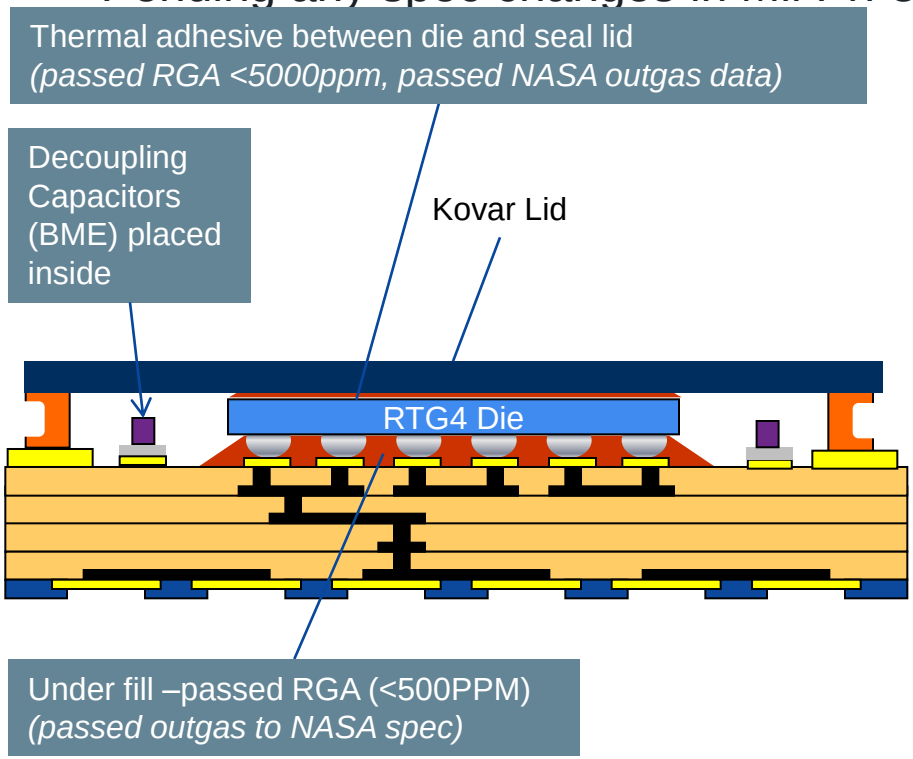
- Built-in DDR Controller
- 8/16/32-bit External Data Bus
- High Performance
  - Operation speed to 667 Mbps (333 MHz Clock)
  - Support for DDR2 and DDR3
- ECC Options
  - X16 and X32 widths

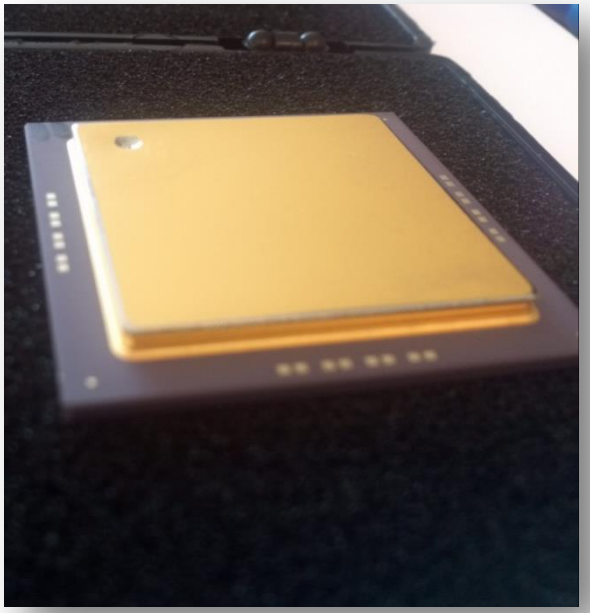
Performance Summary

- General purpose logic
  - 250 MHz system performance with SET mitigation deployed
  - 300 MHz system performance without SET mitigation
  - 300 MHz DSP support performance (adders, delays, etc.)
- Mathblock
  - 250 MHz pipelined performance with SET mitigation deployed
  - 300 MHz pipelined performance without SET mitigation
- RAM18K and uRAM1K
  - > 300 MHz
- IO
  - > 600 Mbps LVDS and 667 Mbps DDRx SDRAM data
  - SERDES to 3.125 Gbps
- Overall
  - 250 MHz general system performance with SET mitigation deployed
  - 300 MHz signal processing performance without SET mitigation

RTG4 Packaging Summary

- Flip chip assembly
- Hermetically sealed cavity
- Internally-mounted BME decoupling capacitors
- Expect that this is qualifiable as Class V
  - Pending any spec changes in Mil Prf 38535 rev K





RTG4 Product Availability

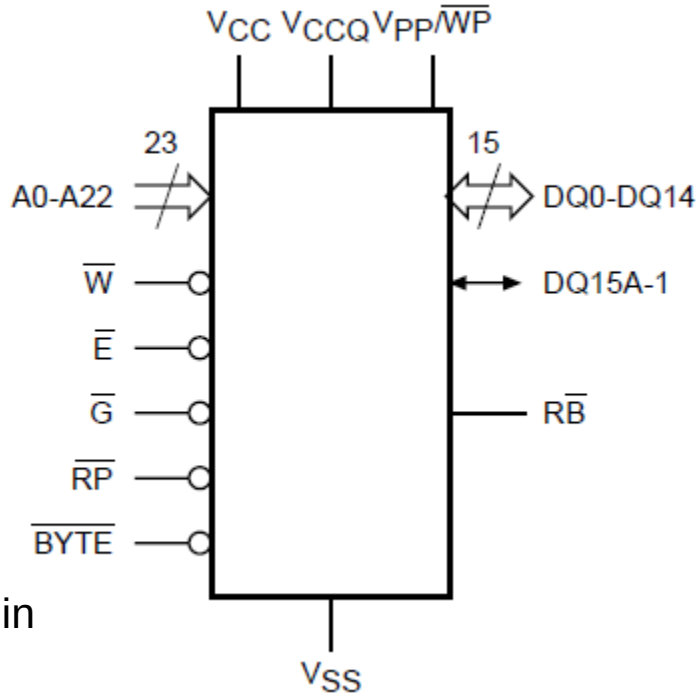
- Non-RT ***SmartFusion2*** and ***Igloo2*** for emulation and development
  - Not footprint compatible with RTG4, no SEU hardening, timing differences
  - Software general availability: ***NOW***
  - Commercial device availability: ***NOW***

- RT devices for space flight applications
  - Initial device: RT4G150
  - Early SW access: End 2013
  - Sample RT4G150 silicon: 2015
  - 883B flight units: 2016
  - QML qualification: 2016

Rad Hard By Design Flash Memory for Space

RHBD Non-Volatile Memory for Space

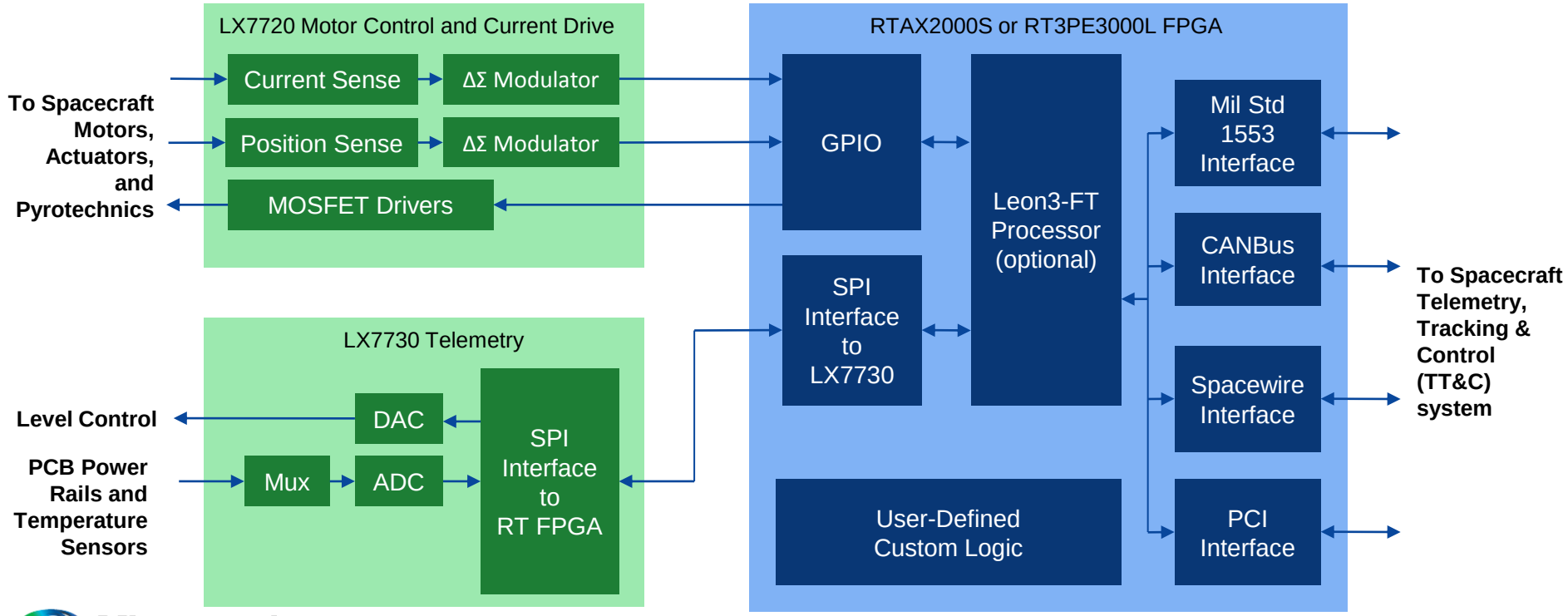
- 128 Mbit Flash memory
  - NOR-flash architecture
  - Parallel user interface – address bus, data bus
  - JTAG user interface for read and write
  - 30 nsec read / write access time
- Radiation hardened by design
  - TID hard to 300Krad
  - SEL immune
  - SEU protected to LET_{TH} > 37 MeV-cm^2/mg
    - Orbital error rate <1E-10 errors/bit-day, GEO solar min
  - This is NOT upscreened commercial product
- Space-grade manufacturing and packaging
  - Mil Std 883 Class B, QML class Q, QML class V
  - Hermetic packaging, planning for 100-pin CQFP
- Availability of flight-qualified parts expected 2015



Space System Managers

Space System Managers

- Standard off-the-shelf solutions for telemetry and motor control in space
- Microsemi mixed signal standard ASICs
  - LX7720 current sense, rotary position sense and MOSFET drivers
  - LX7730 voltage, current and temperature telemetry
- Microsemi RT FPGAs implement digital interface with satellite control bus



Space System Manager Concept

- Space System Manager (SSM) is a combination of an FPGA with a special purpose analog or power companion IC
- The Companion IC integrates circuits that control or monitor typical application oriented interfaces but has minimal hard coded internal logic
- Using HDL modules the FPGA can be configured to customize the SSM for specific applications
- The Companion IC is a standard part that is space qualified and immediately available
- The SSM solution is scalable by selecting one or more companion ICs for an application and selecting an FPGA model number with a sufficient number of gates

Summary

Summary

- Microsemi is dedicated, focused, and investing in space products and capabilities
- Microsemi has been in the space business as a partner with our customers for more than 55 years
- Microsemi has the system, circuit, and production experience in space to be a long term supplier of state-of-the-art products for long life cycles
- Microsemi uses a system view of applications, and a broad range of technology and design experience to build the best-in-class products for space

Microsemi

Thank You