Interfacing SmartFusion2 SoC FPGA with External LPDDR Memory through MDDR Controller - Libero SoC v11.4

Demo Guide

Microsemi

Revision History

Date	Revision	Change
22nd August, 2014	1	First Release

Confidentiality Status

This document is a Non-Confidential.

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Preface

About this document

This demo guide is for SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) devices. It provides instructions on how to use the corresponding reference design.

Intended Audience

The following designers using the SmartFusion2 devices:

- FPGA designers
- System-level designers
- Embedded designers

References

Microsemi® Publications

- *SmartFusion2 SoC FPGA High Speed DDR Interfaces User Guide*
- *SmartFusion2 System Builder User Guide*
- *SmartFusion2 SoC Evaluation Kit User Guide*

Refer to the following web page for a complete and up-to-date listing of SmartFusion2 SoC device documentation: *http://www.microsemi.com/index.php?option=com_content&id=2034&lang=en&view=article#documents*.

Interfacing SmartFusion2 SoC FPGA with External LPDDR Memory through MDDR Controller

Introduction

This demo shows that the high performance memory subsystem (HPMS) DDR controller accessing the external DDR SDRAM memories in the SmartFusion2 SoC devices. The demo has two parts:

- Demo using simulation
- Demo using the SmartFusion2 SoC Evaluation Kit

In the demo design, the AXI Master in the FPGA Fabric accesses the Low Power DDR (LPDDR) memory present in the SmartFusion2 SoC Evaluation Kit board using the MDDR Controller. A utility, `SF2_MDDR_Demo` is provided along with the demo deliverables. Using the utility, you can drive the AXI Master logic. The AXI Master converts the commands from the utility to AXI transactions for the MDDR Controller to perform the read/write operations on the LPDDR memory.

Table 1 • **Design Requirements**

Design Requirements	Description
Hardware Requirements	
SmartFusion2 SoC Evaluation Kit has: • FlashPro4 programmer • 12 V adapter • USB A to Mini-B cable	Rev C or later
Host PC or Laptop	Any 64-bit Windows Operating System
Software Requirements	
Libero® System-on-Chip (SoC)	v11.4
FlashPro programming software	v11.4
Microsoft .NET Framework 4	-
Host PC Drivers	USB to UART drivers

Demo Design

Introduction

The demo design files are available for download from the following path in the Microsemi website:

http://soc.microsemi.com/download/rsc/?f=SF2_MDDR_Demo_11p4_DF

Design files include:

- Demo_utility
- Libero_project
  - SF2_MDDR_Demo
- Programming_file
- Source_files
- readme.txt

Figure 1 shows the top level structure of the design files. For further details, refer to the `readme.txt` file.

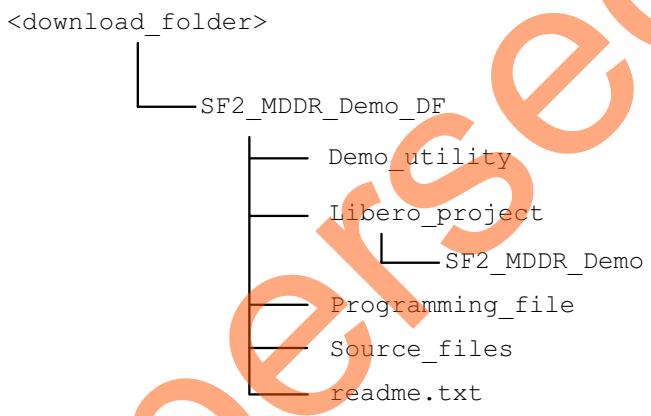

***Figure 1* • Demo Design Files Top Level Structure**

Figure 2 on page 7 shows the top level view of demo design.

In the demo design, the AXI Master implemented in the FPGA Fabric accesses the LPDDR memory present in the SmartFusion2 Evaluation Kit board using the MDDR Controller. The AXI Master logic communicates to the MDDR controller through CoreAXI interface and the DDR_FIC interface.The read/write operations initiated by the `SF2_MDDR_Demo` utility are sent to the UART_IF block using the UART protocol. The AXI Master receives the address and the data from the UART_IF block. During a write operation, the UART_IF block sends the address and data to the AXI Master logic.

During a read operation, the UART_IF block sends the address to the AXI Master and stores the read data in TPSRAM. When the read operation is complete, the read data is sent to the Host PC through UART.

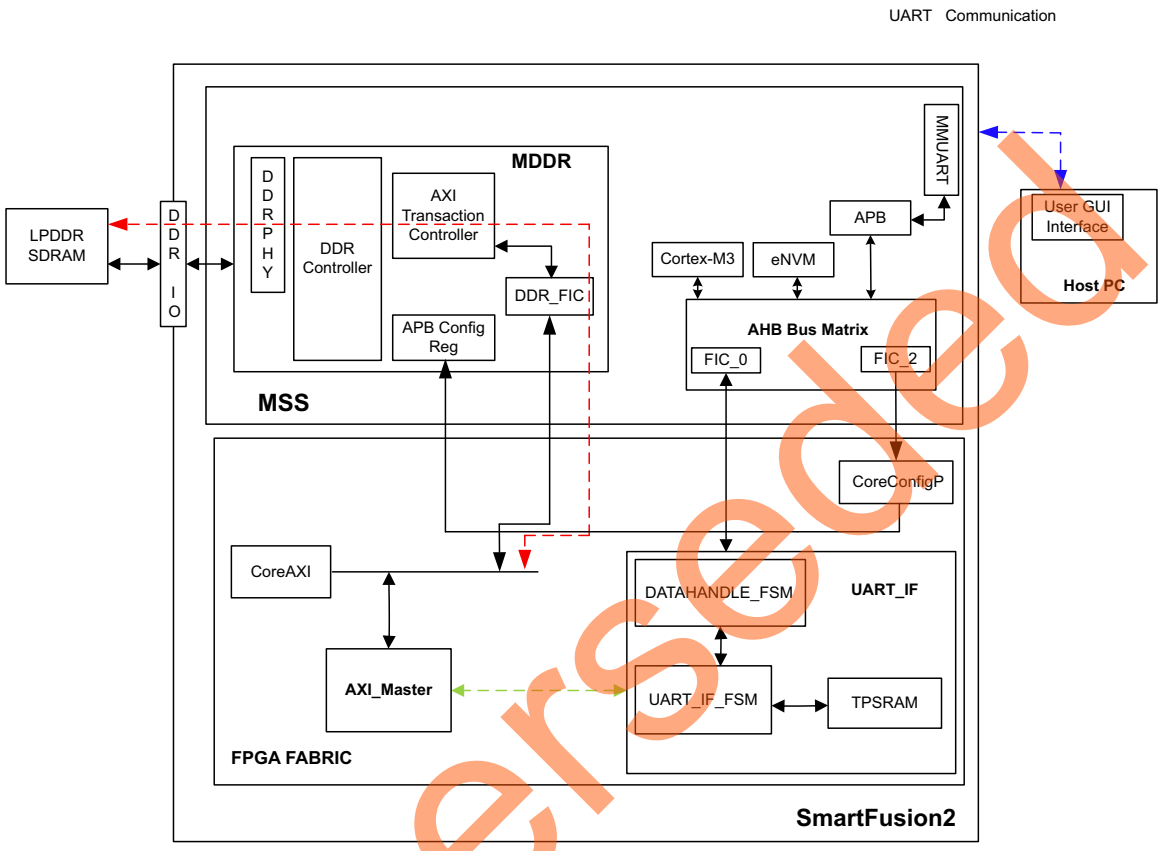

***Figure 2* • SmartFusion2 MDDR Demo Block Diagram**

In this demo design, different blocks are configured as shown below:

- MDDR Controller is configured for LPDDR memory available in the SmartFusion2 Evaluation Kit board. The LPDDR memory is a Micron DRAM part (part number MT46H32M16LF)
- DDR_FIC is configured for AXI bus interface.
- AXI clock is configured for 80 MHz and LPDDR clock is configured for 160 MHz.
- TPSRAM IP has the following configuration:
  - Write port depth: 256
  - Write port width: 64
  - Read port depth: 2048
  - Read port width: 8

Refer to "Appendix A: Configuring the MDDR Controller" on page 28 for information on how to configure the DDR controller.

Demo Design Features

The SF2 MDDR demo design has the following features:

- Single AXI read/write transactions
- 16-beat burst AXI read/write transactions
- LPDDR memory model simulation using SmartDesign testbench
- Design validation using the SmartFusion2 SoC Evaluation Kit board that has the LPDDR memory
- Initiation of the read/write transactions using `SF2_MDDR_Demo` utility

Demo Design Description

The demo design consists of the following SmartDesign components:

- **MDDR_Demo_top_0**: This SmartDesign handles the data transactions between the MDDR controller and LPDDR SDRAM.
- **UART_IF_0**: This SmartDesign handles the communication between the Host PC and the SmartFusion2 SoC Evaluation Kit Board.

Figure 3 shows the MDDR_Demo_top_0 and UART_IF_0 connection.

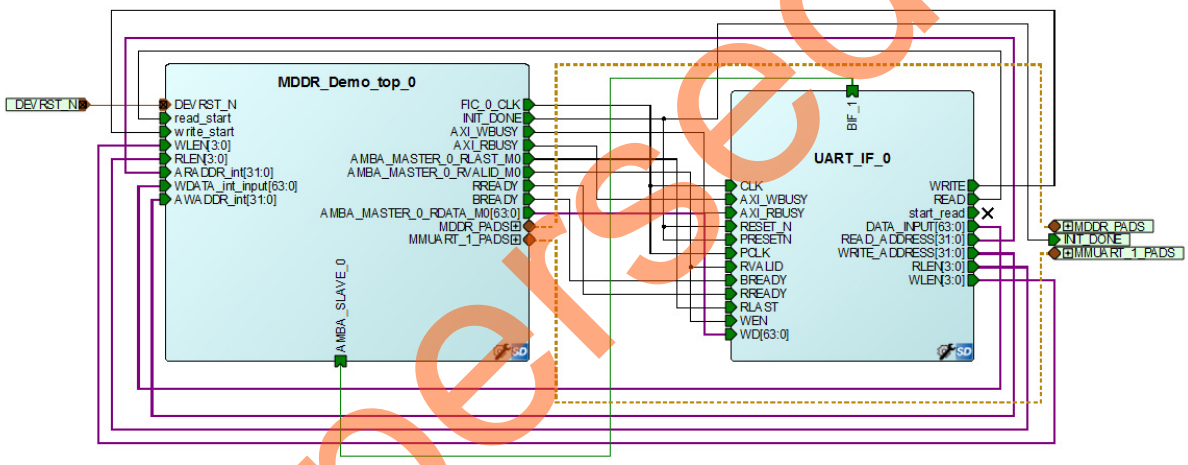

***Figure 3* • SF2_MDDR_Demo SmartDesign**

MDDR_Demo_top_0

This consists of the MDDR_Demo_0 subsystem generated using the System Builder and the AXI_IF_0 master logic. The AXI_IF_0 master logic is an RTL code that implements the AXI read and write transactions. It receives the read/write operations, burst length (RLEN and WLEN), address and data as inputs. Based on inputs received, it communicates with the LPDDR memory through the MDDR controller.

Figure 4 shows the MDDR_Demo_top_0 SmartDesign component.

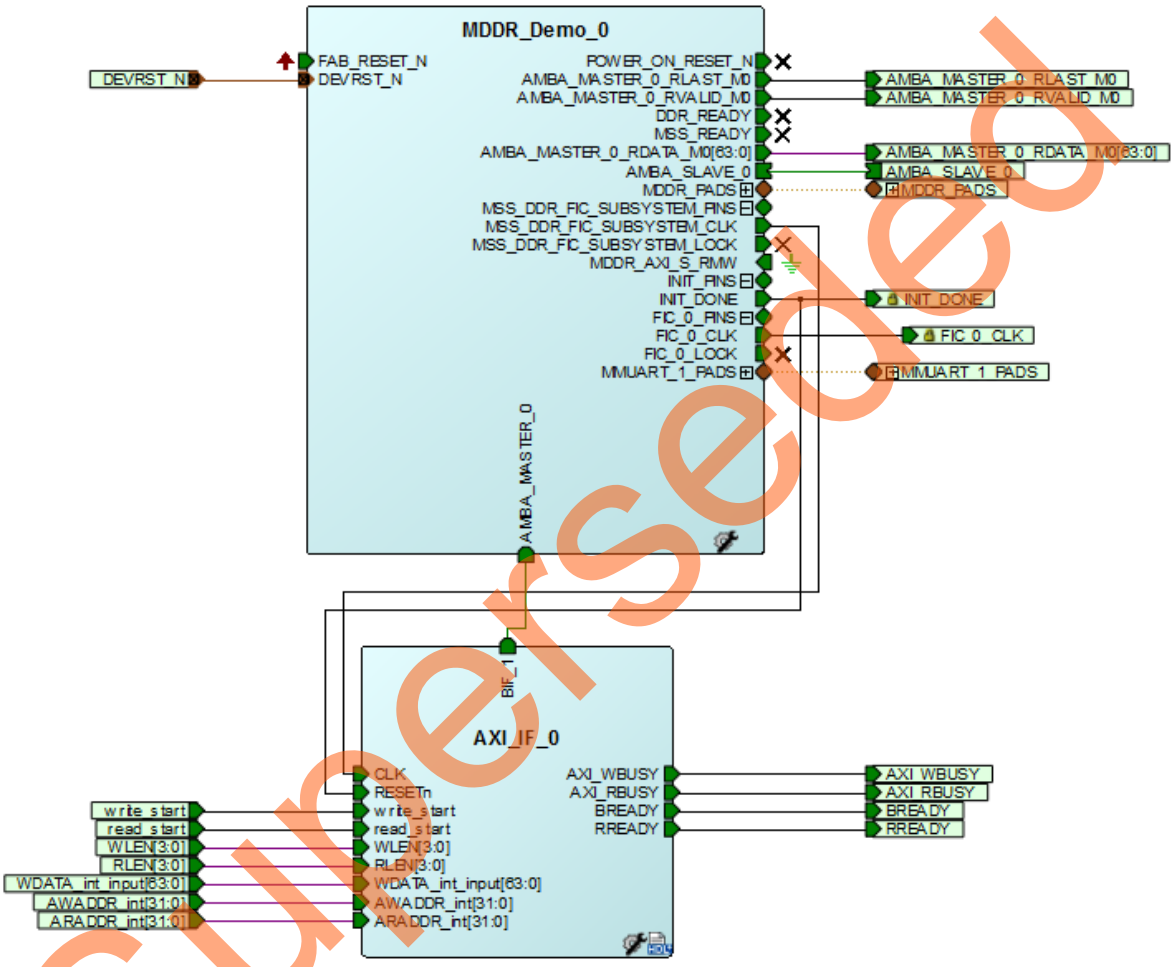

Figure 4 • **MDDR_Demo_top_0 SmartDesign Component**

UART_IF_0

The UART_IF_0 SmartDesign component handles the communication between Host PC demo utility and the AXI Master logic. The MMUART_1 block present in the MSS subsystem receives the UART signals from the Host PC user interface, the Cortex-M3 processor sends this user data to the DATAHANDLE_FSM block present in the FPGA fabric using the FIC_0 APB slave interface. DATAHANDLE_FSM is an APB slave wrapper, which sends the received data to the UART_IF_FSM_0 block.

For a single write operation, the UART_IF_FSM_0 wrapper receives the address and data from the demo utility. For a burst write operation, the address and data are received from the demo utility and the subsequent incremental data are provided by the UART_IF_FSM_0 wrapper.

For a burst read operation, UART_IF_FSM_0 collects the address from the demo utility and sends that to the AXI_IF_0 master logic. It then receives the read data from the AXI_IF_0 master logic and stores it in the TPSRAM_0. After completion of the read burst transactions, the Cortex-M3 processor reads the TPSRAM_0 buffer through DATAHANDLE_FSM (APB wrapper) block. The received data is sent to the Host PC using the MMUART_1 block.

Figure 5 shows the UART_IF_0 SmartDesign component.

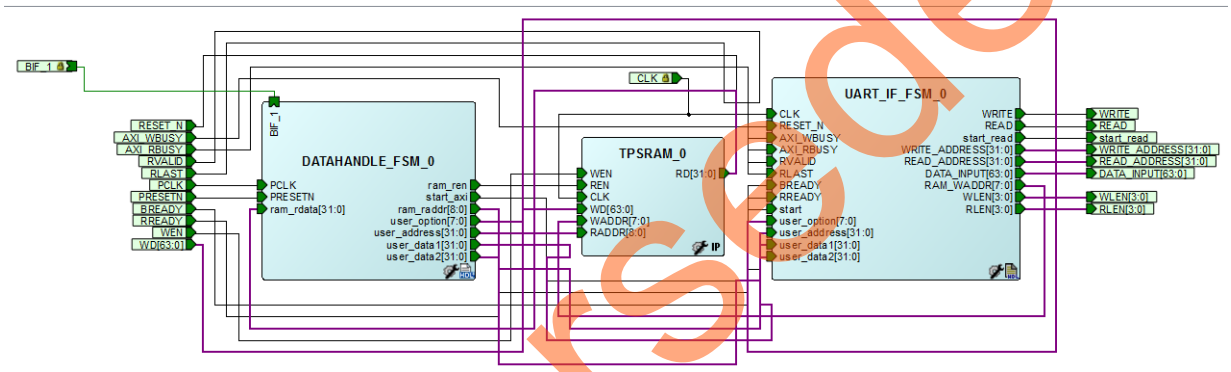

***Figure 5* • UART_IF_0 SmartDesign Component**

Running the Demo using Simulation

Introduction

The demo design can be simulated using SmartDesign Testbench and the LPDDR memory model (MT46H32M16LF with 512 Mb density).

The simulation is set to run the following:

- Single AXI write and read operation
- 16-beat AXI burst write and read operation

Figure 6 shows the AXI_LPDDR_Simulation SmartDesign Testbench. The AXI_testbench provides the read/write operations, burst length, address, and data to the MDDR_Demo_top_0 SmartDesign component.

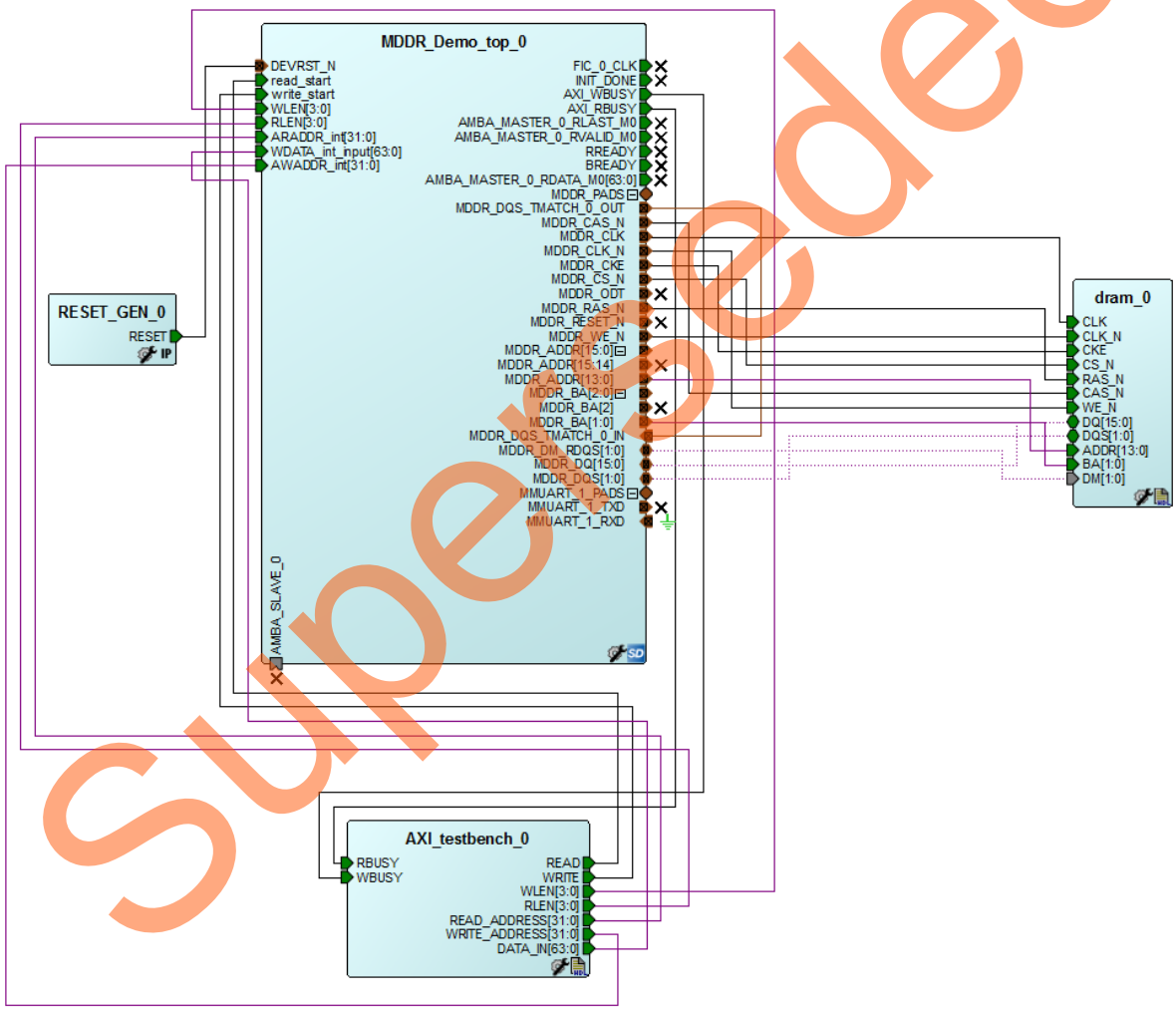

***Figure 6* • AXI_LPDDR_Simulation SmartDesign Testbench**

To run simulation, ensure that the following files are present in the Libero SoC project:

- dram.v
- dram_parameters.vh
- AXI_testbench.v

The default location of the above mentioned files is,

<Download folder>\SF2_MDDR_Demo_DF\Libero_project\SF2_MDDR_Demo\stimulus

Simulation

Simulation setup configuration can be set properly by using the following steps:

1. Launch the Libero SoC software.
2. Browse the *SF2_MDDR_Demo* project provided in the design file.
3. Go to **Project** > **Project Settings** > **Simulation Options**.
4. Ensure that the **DO File** tab has the configuration as shown in Figure 7.

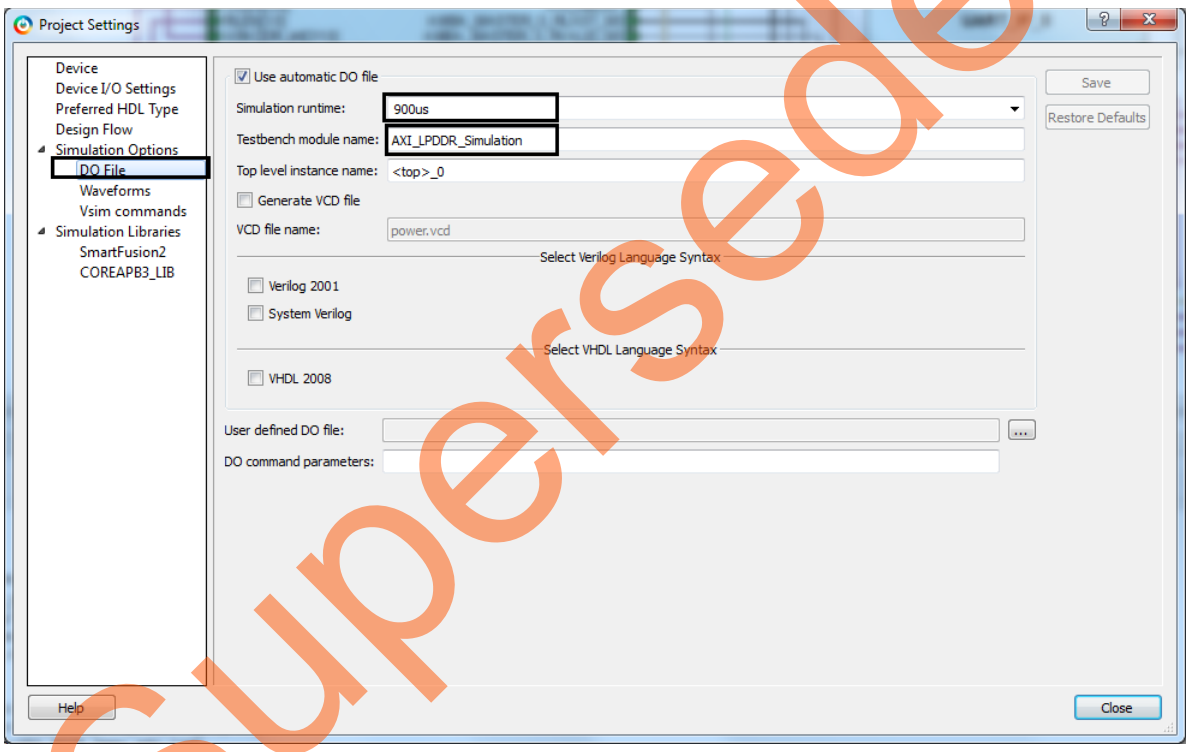

Figure 7 • DO File Settings

5. Ensure that the **Waveforms** tab has the configuration as shown in Figure 8.

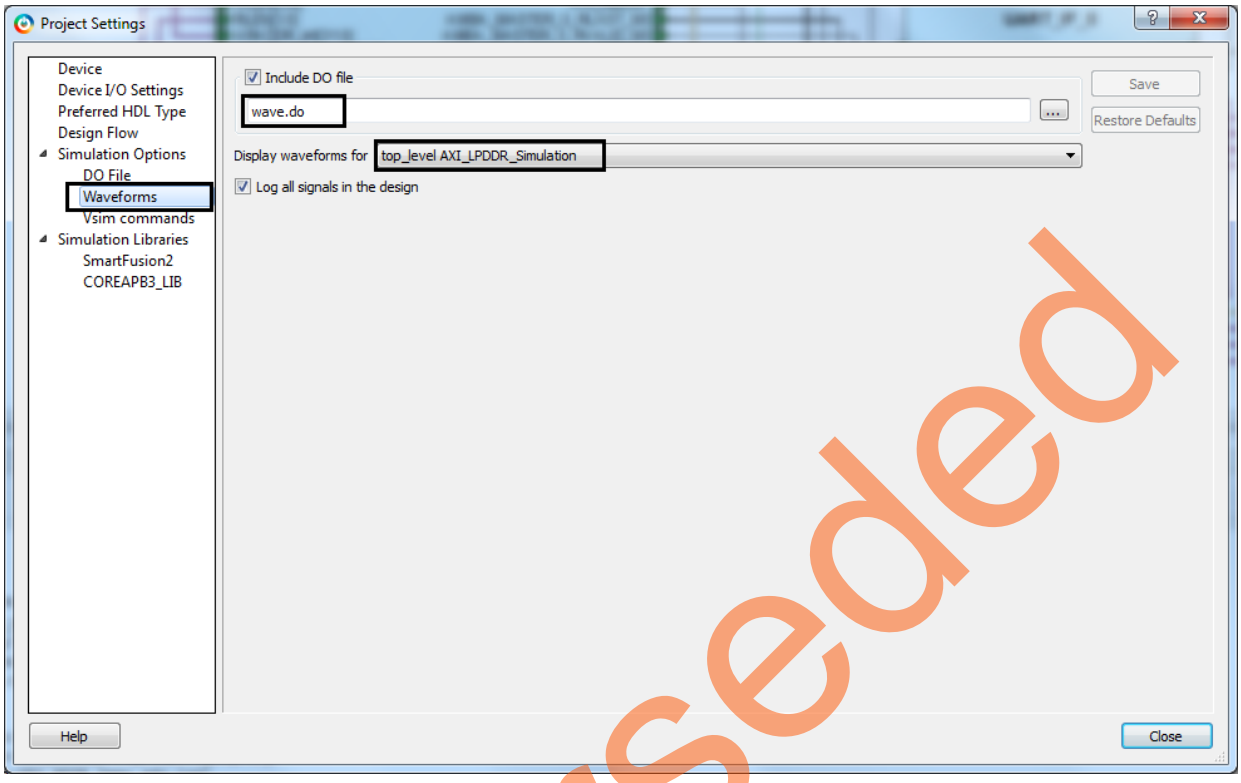

Figure 8 • **Waveforms Settings**

6. Go to **Design Flow** tab.
7. Right click **Simulate** under **Verify – Pre synthesized Design** and then select, **Organize Input Files** > **Organize Stimulus Files**.

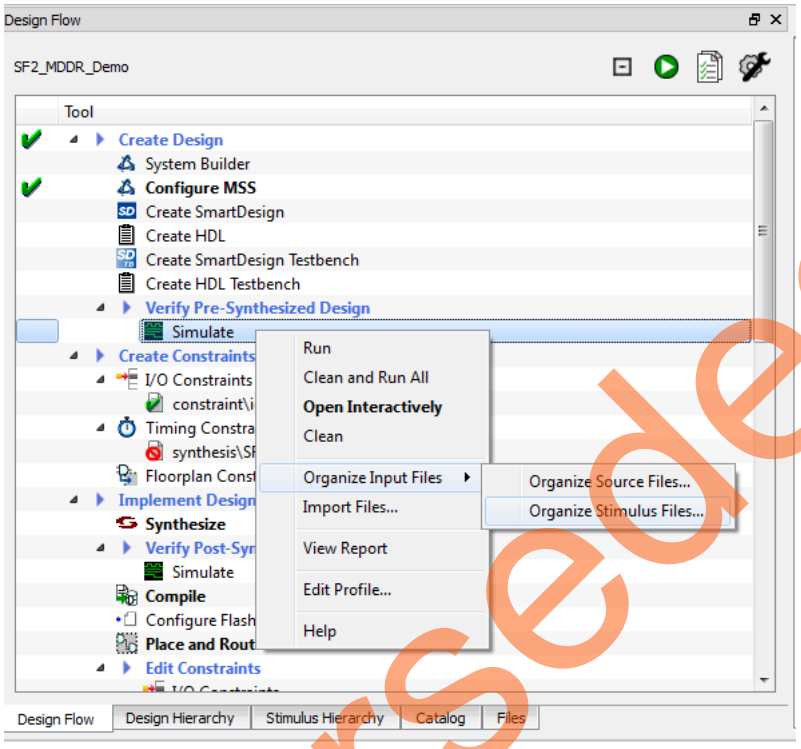

***Figure 9* • Invoking Organize Stimulus Files Window**

8. Ensure that the **Organize Stimulus files** window has the configuration as shown in Figure 10.

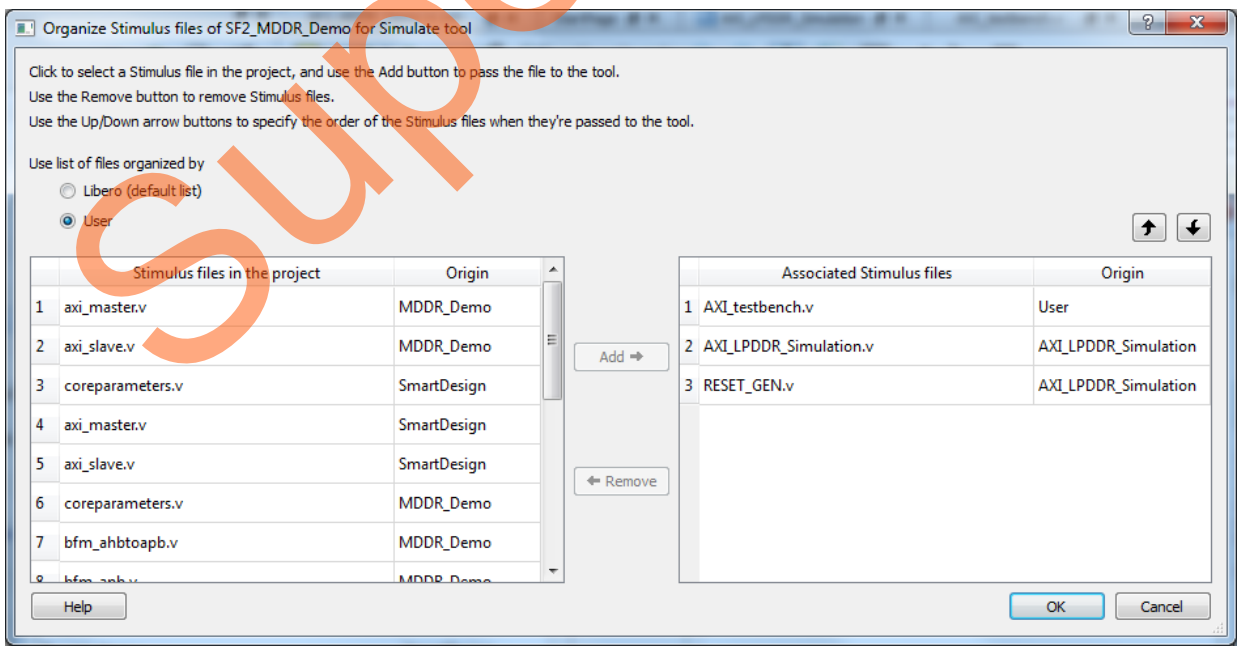

***Figure 10* • Organize Stimulus Files Window**

Running the Simulation

1. Right click **Simulate** under **Verify – Pre Synthesized Design**.
2. Click **Open Interactively**.
3. Simulation requires 900us to complete as mentioned in the 3rd point under "Simulation" section on page 12.

Figure 11 shows the transcript window of the simulation.

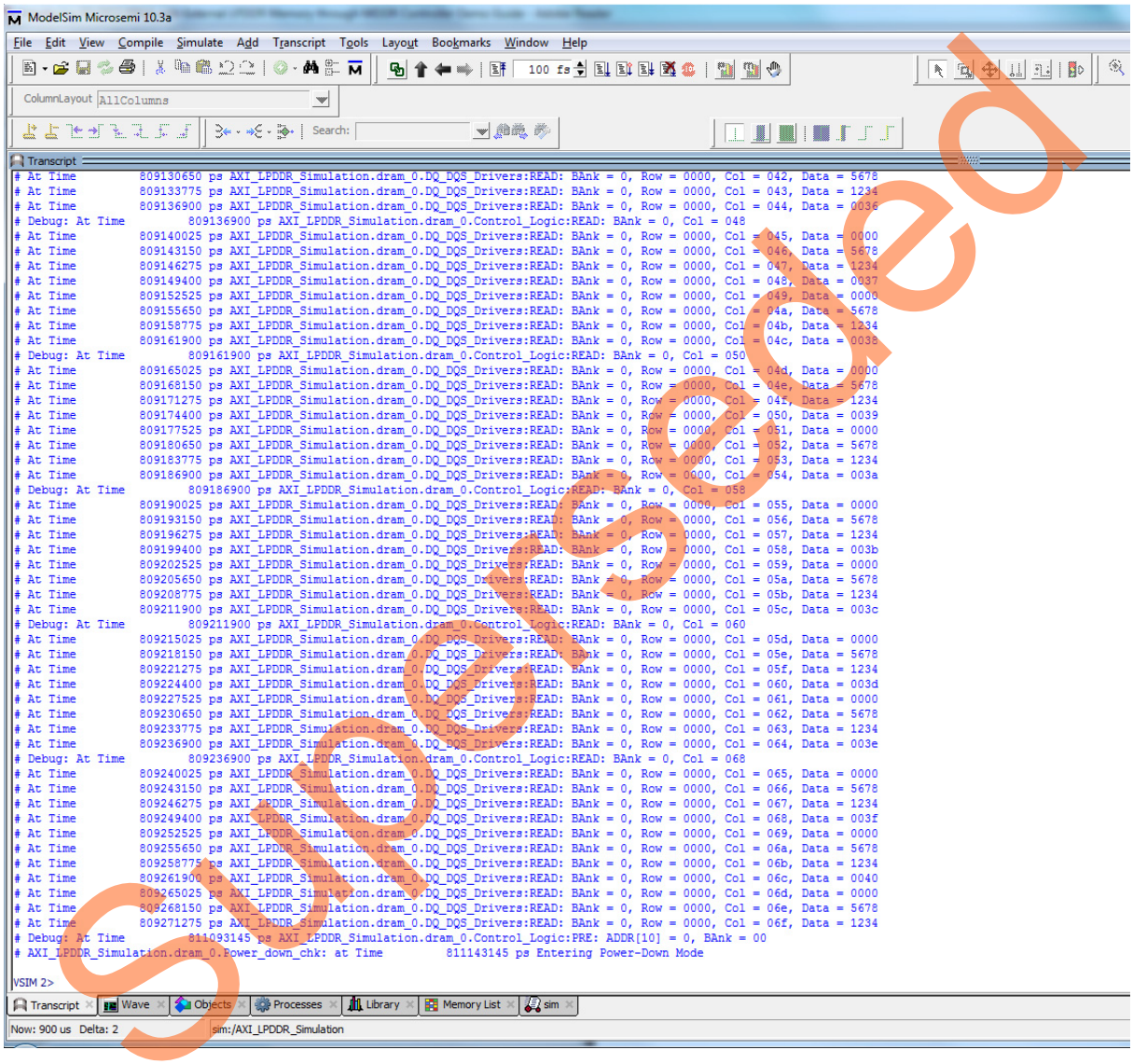

***Figure 11* • Simulation Completed**

Figure 12 shows the single AXI write and AXI read operation.

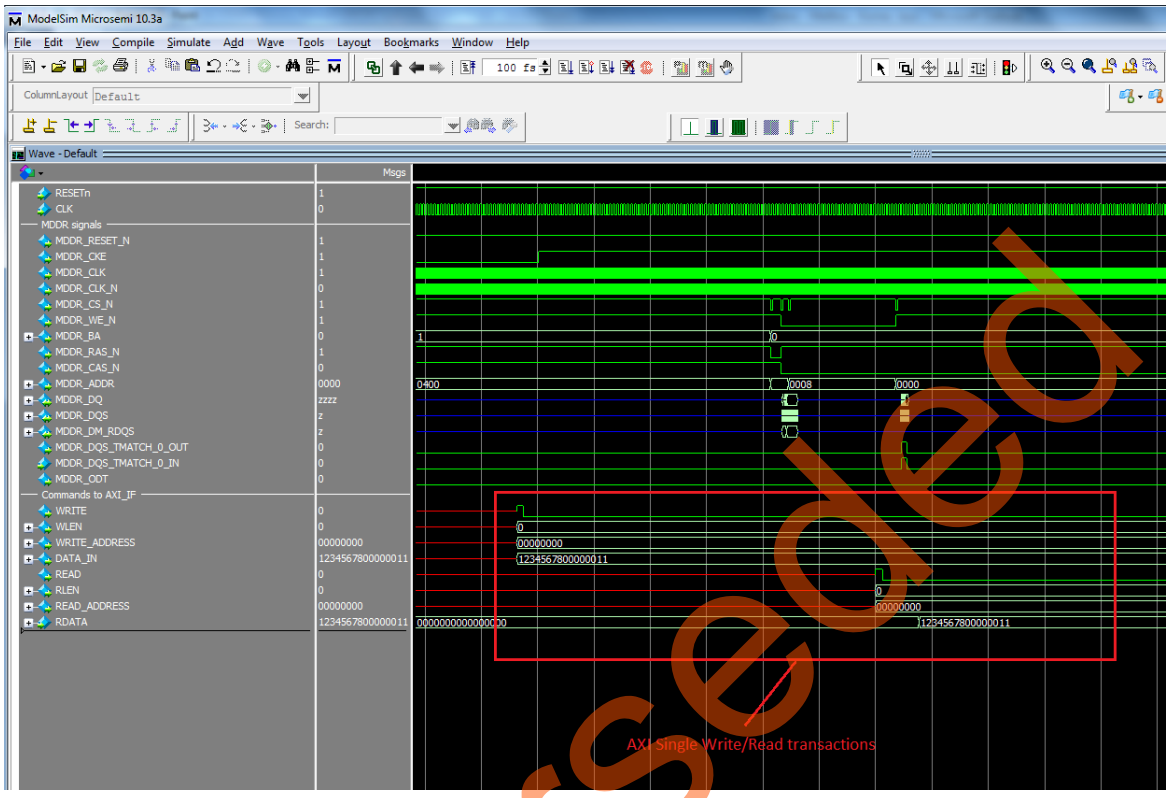

Figure 12 • **Single Write and Read Operation**

Figure 13 shows the 16-beat AXI burst write and read operation.

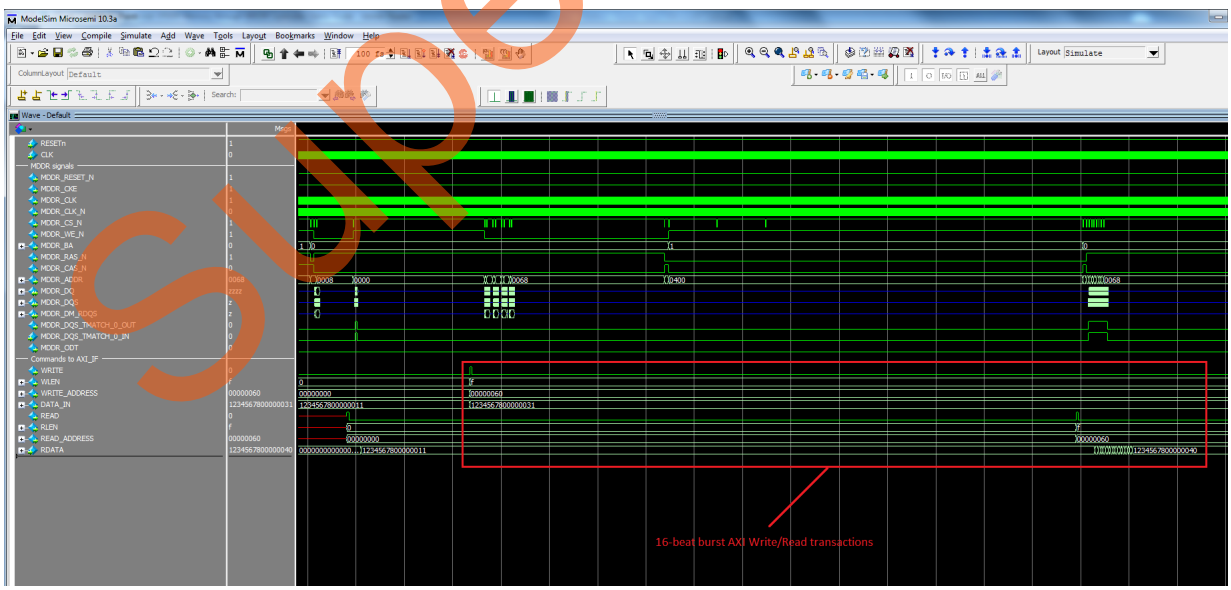

Figure 13 • **16-Beat AXI Burst Write and Read**

Setting up the Hardware Demo

Use the following steps to setup the hardware demo:

1. Connect the jumpers on the SmartFusion2 SoC Evaluation Kit as shown in Table 2.

Table 2 • **SmartFusion2 SoC FPGA Evaluation Kit Jumper Settings**

Jumper	Pin (from)	Pin (to)	Comments
J22	1	2	Default
J23	1	2	Default
J24	1	2	Default
J8	1	2	Default
J3	1	2	Default

CAUTION: While making the jumper connections, the power supply switch **SW7** must be switched off.

2. Connect the Power supply to the J6 connector, switch on the power supply switch, **SW7**.
3. Connect the FlashPro4 programmer to the J5 connector of the SmartFusion2 Evaluation Kit.
4. Connect the Host PC USB port to the SmartFusion2 Evaluation Kit board's J18 USB connector using the USB mini-B cable.

Figure 14 shows the board setup for running the SmartFusion2 MDDR demo on the SmartFusion2 Evaluation Kit.

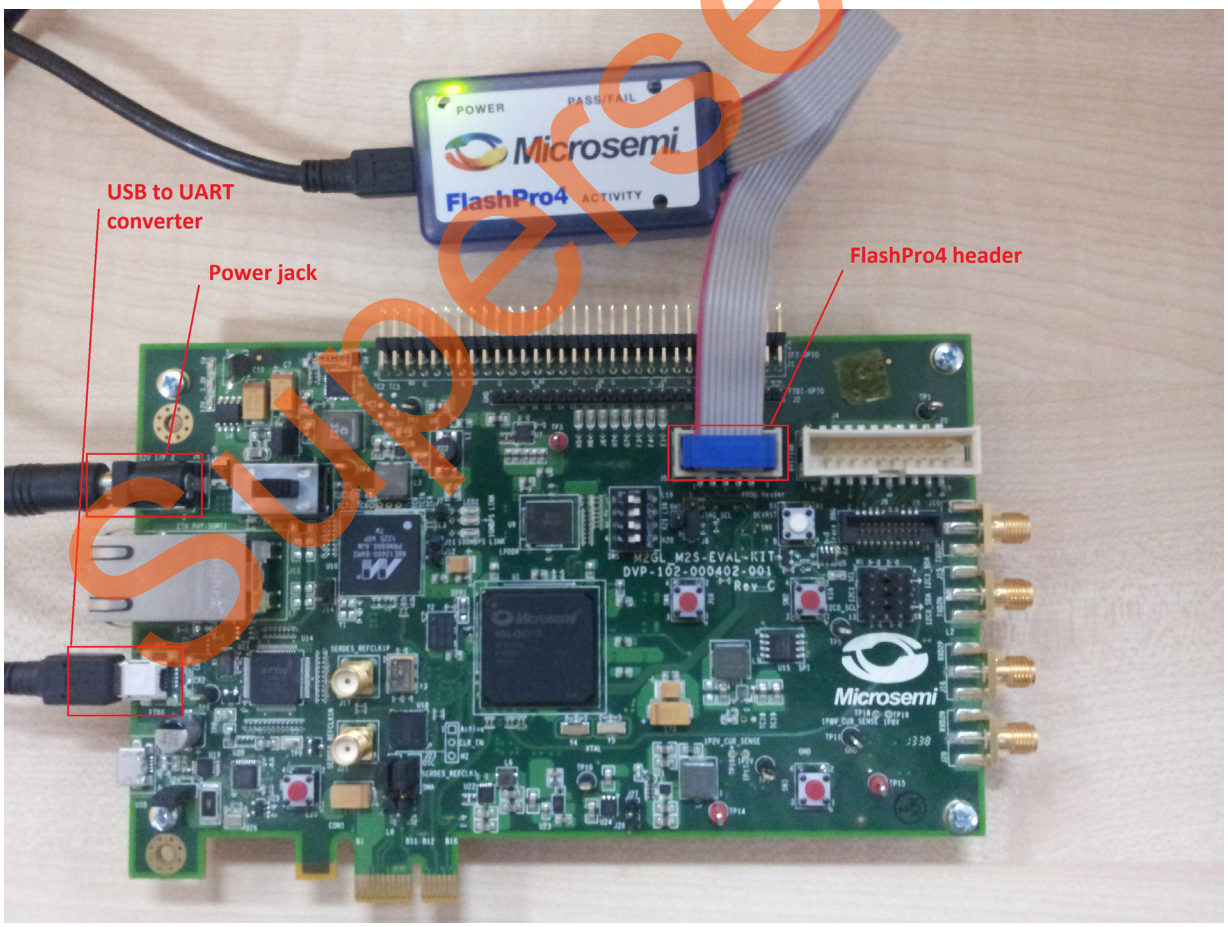

Figure 14 • **SmartFusion2 Evaluation Kit**

5. Ensure that the USB to UART bridge drivers are automatically detected. This can be verified in the **Device Manager** of the Host PC. The FTDI USB to UART converter enumerates four COM ports. For USB 2.0, note down the USB Serial Converter D COM port number to use it in the GUI. Figure 15 shows the USB 2.0 Serial port properties. As shown in Figure 15, COM7 is connected to USB Serial Converter D. Refer to "Appendix B: Finding the Correct COM Port Number When Using the USB 3.0" on page 32 for finding the correct COM port in USB 3.0.

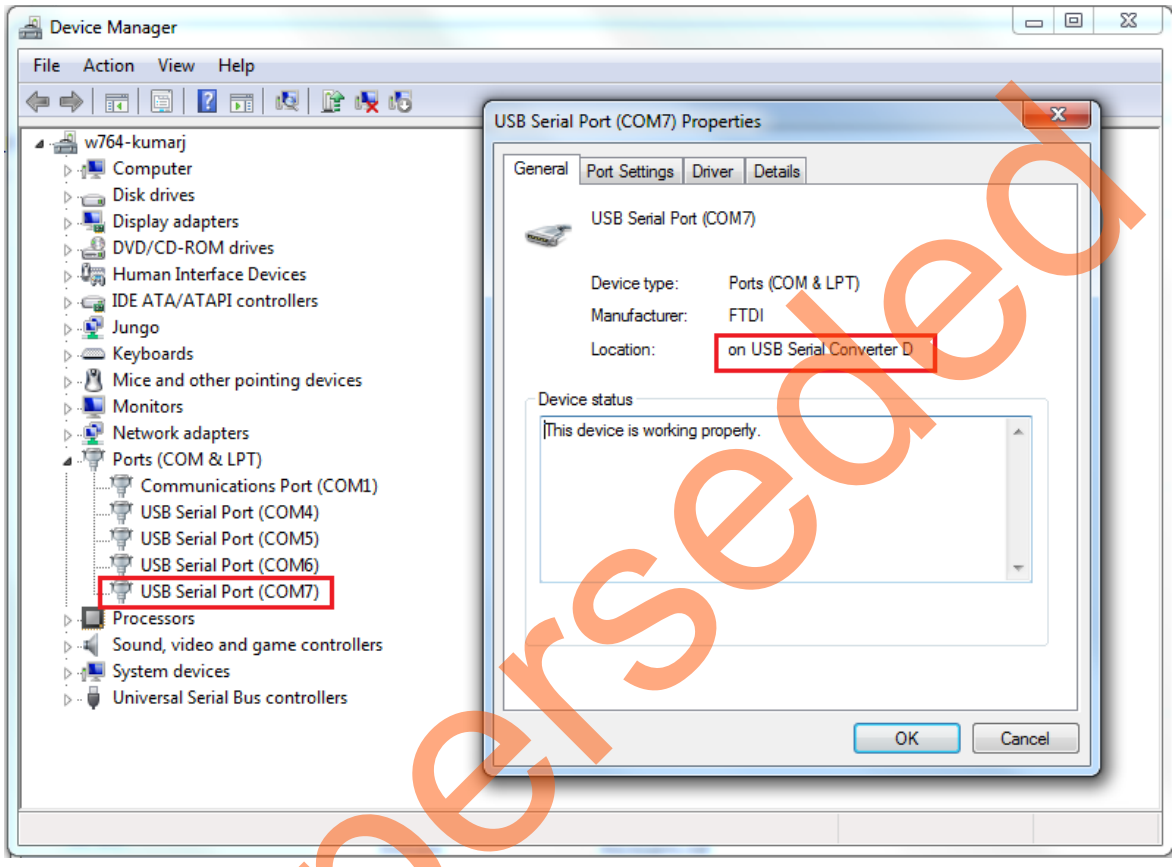

***Figure 15* • USB Serial 2.0 Port Properties**

6. If the USB to UART bridge drivers are not installed, download and install the drivers from *www.microsemi.com/soc/documents/CDM_2.08.24_WHQL_Certified.zip*.

Programming the Demo Design

Use the following steps to program the demo:

1. Download the demo design from: *http://soc.microsemi.com/download/rsc/?f=SF2_MDDR_Demo_11p4_DF*
2. Switch **ON** the SW7 power supply switch.
3. Launch the FlashPro software.
4. Click **New Project**.
5. In the **New Project** window, type the project name as `SF2_MDDR_Demo`.

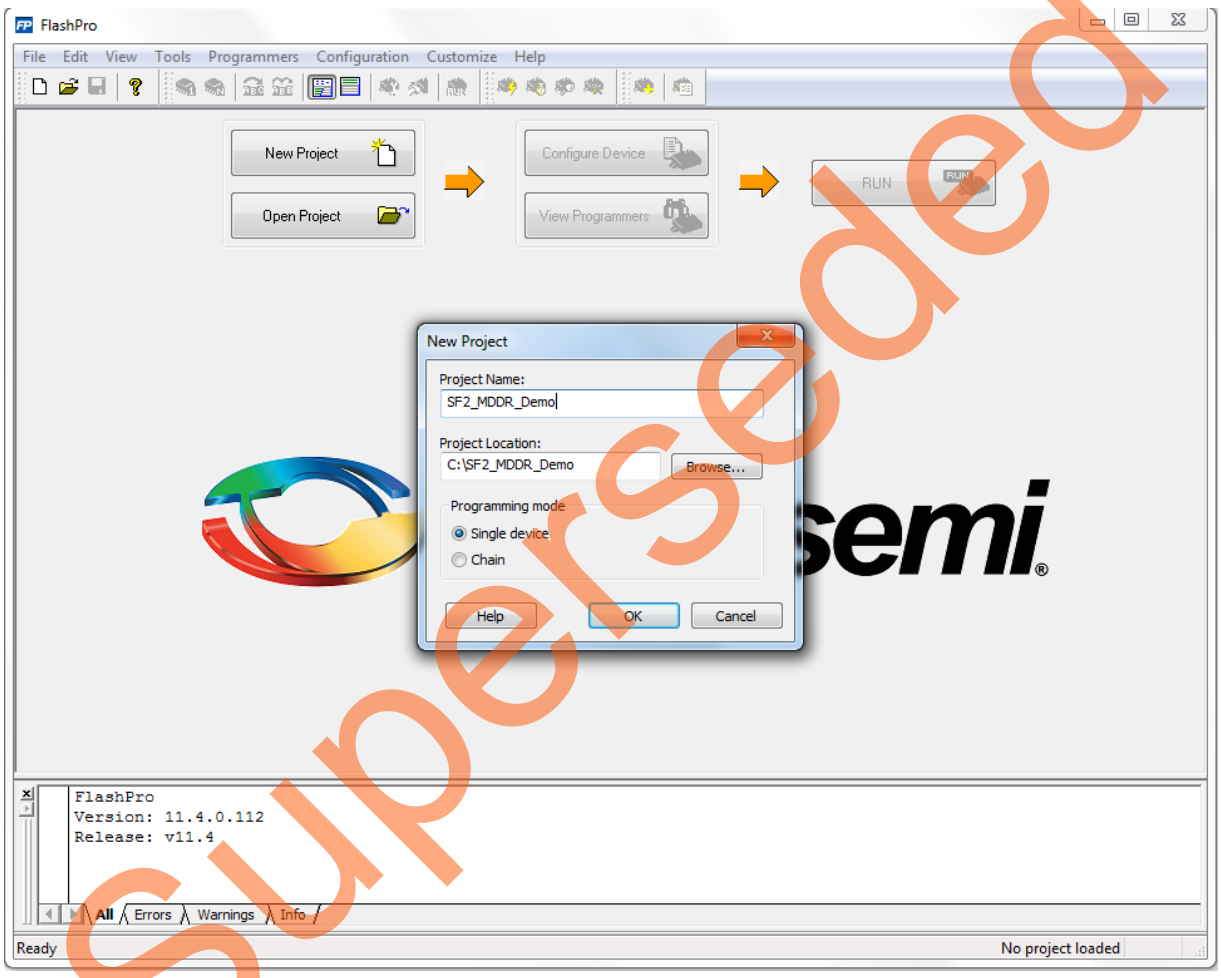

***Figure 16* • FlashPro New Project**

6. Click **Browse** and navigate to the location where you want to save the project.
7. Select **Single device** as the **Programming mode**.
8. Click **OK** to save the project.

Setting up the Device

Use the following steps to configure the device:

1. Click **Configure Device** on the FlashPro GUI.
2. Click **Browse** and navigate to the location where the SF2_MDDR_Demo.stp file is located and select the file. The default location is: *<download_folder>\SF2_MDDR_Demo_DF\Programming_file*.
3. Click **Open**. The required programming file is selected and is ready to be programmed in the device.

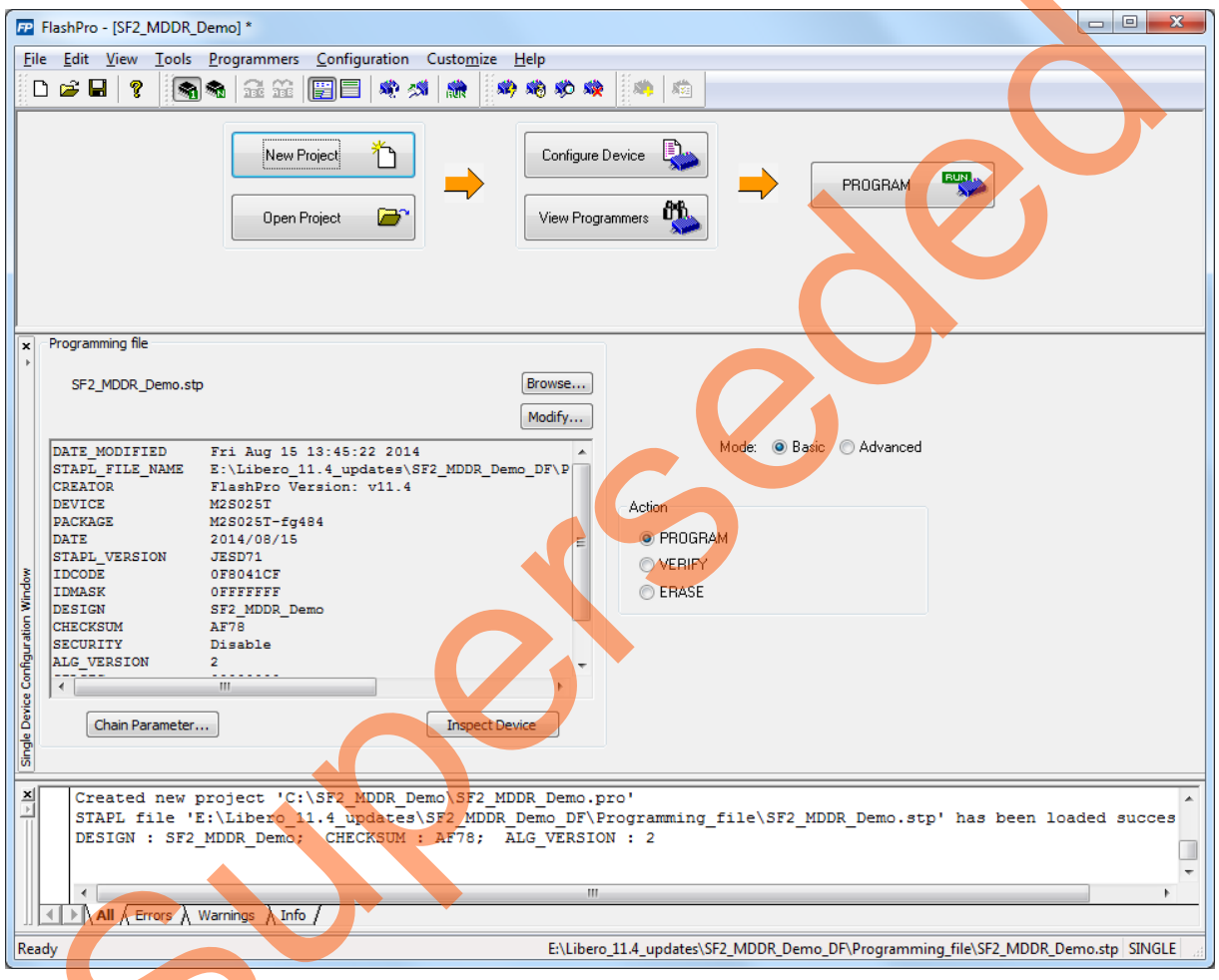

Figure 17 • **FlashPro Project Configured**

Programming the Device

Use the following steps to start programming the device:

1. Click **PROGRAM** to start programming the device. Wait until you get a message indicating that the **PROGRAM PASSED**.

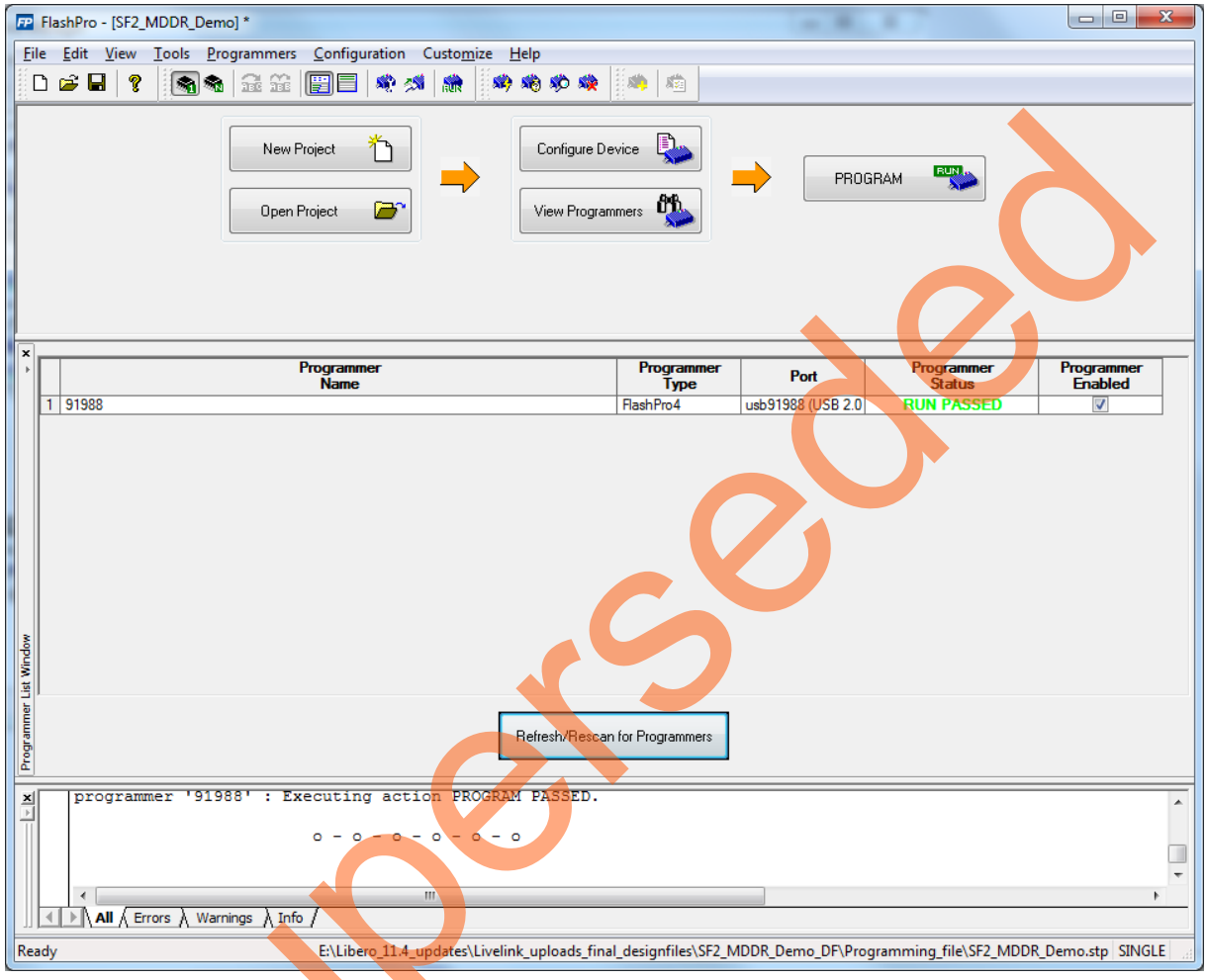

Figure 18 • **FlashPro Program Passed**

Running the Hardware Demo

The SmartFusion2 SoC MDDR demo comes with utility, `SF2_MDDR_Demo` that runs on the Host PC to communicate with the SmartFusion2 SoC Evaluation Kit. The UART protocol is used as the underlying communication protocol between the Host PC and the SmartFusion2 SoC Evaluation Kit. Figure 19 shows the initial screen of the `SF2_MDDR_Demo` utility.

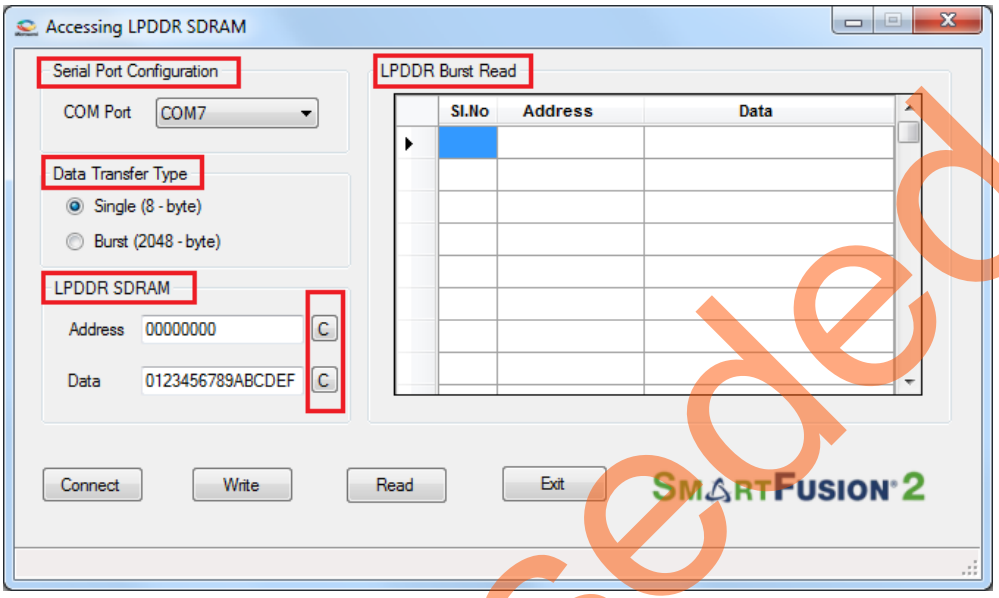

***Figure 19* • SF2_MDDR_Demo Utility**

The SF2_MDDR_Demo utility has the following sections:

- **Serial Port Configuration**: Displays the serial port. Baud rate is fixed at 115200.
- **Data Transfer Type**: Single or Burst.
- **LPDDR SDRAM**: Provides Address and Data.
- **LPDDR Burst Read**: Displays the Burst Read Values for the corresponding address.
- **C:** Clears the existing data.

Steps to run the GUI

1. Launch the utility. The default location is: *<download_folder>\\SF2_MDDR_Demo_DF\Demo_Utility\SF2_MDDR_Demo.exe*.
2. Select the appropriate COM port from drop down menu. In this case, it is COM 7.
3. Click **Connect**. The connection status along with the COM Port and Baud rate is shown in the left bottom corner of the screen. Figure 20 shows the connection status of the utility.

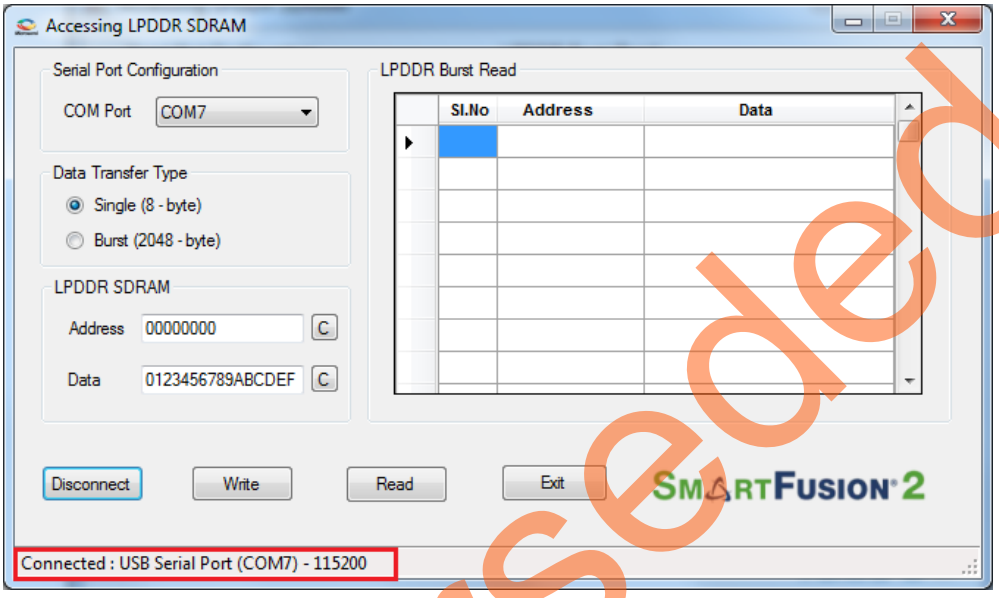

***Figure 20* • SF2_MDDR_Demo – Connection Status**

Performing a Single Data Transfer

For a single write or read operation, the AXI Master logic is configured to transfer a burst length of 1 (that is, 8 bytes). For a write operation, the utility sends a 32-bit address and 64-bit (8 bytes) data. The data is then written to the LPDDR SDRAM. For a read operation, the utility sends a 32-bit address and receives 64-bit data from LPDDR and is displayed in the utility.

To perform a single data transfer, follow the below mentioned steps:

1. Select the **Data Transfer Type as Single (8 bytes)**.
2. A 64-bit aligned address is required in the address field. Enter a 32-bit HEX Address in the range 0x00000000 - 0x03FFFFF8. When a non 64-bit aligned address is provided, the GUI converts it to 64-bit aligned address and performs the write/read. Refer to "Appendix C: Performing Write/Read Operation When Non 64-Bit Aligned Address is Provided" on page 34 to perform write/read when non 64-bit aligned address is provided.
3. In the **Data** field, enter a 64-bit data in HEX format.
4. Click **Write**. The entered data is written to the LPDDR memory.

5. Figure 21 shows the **Address** and **Data** values entered for a Single Write operation.

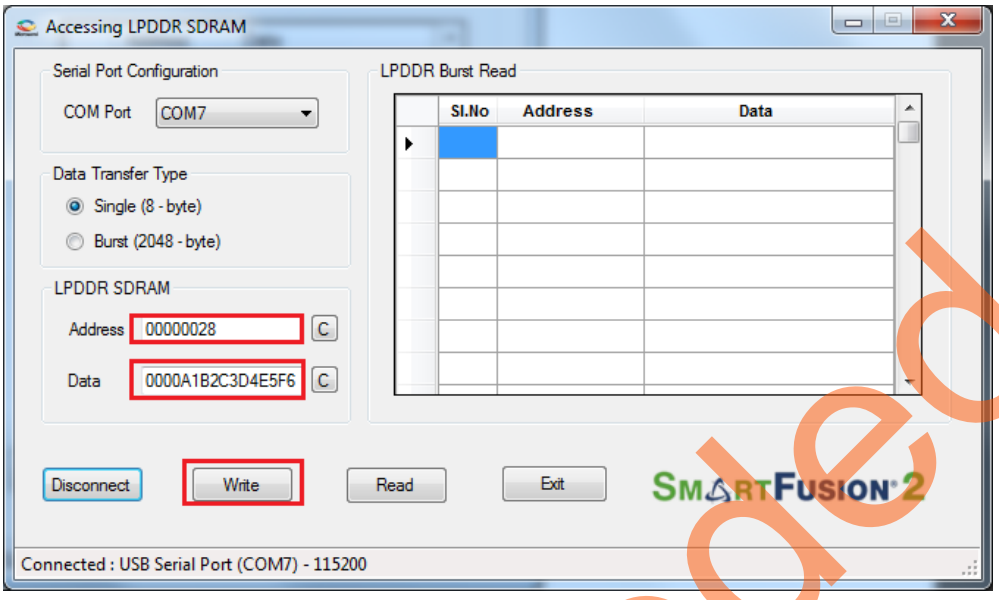

Figure 21 • **Single Write Operation**

6. To verify the write operation, perform a read operation to the same address where the data was written.
7. Press **C** to clear the data present in the **Data** field. Figure 22 highlights the Clear button, C.

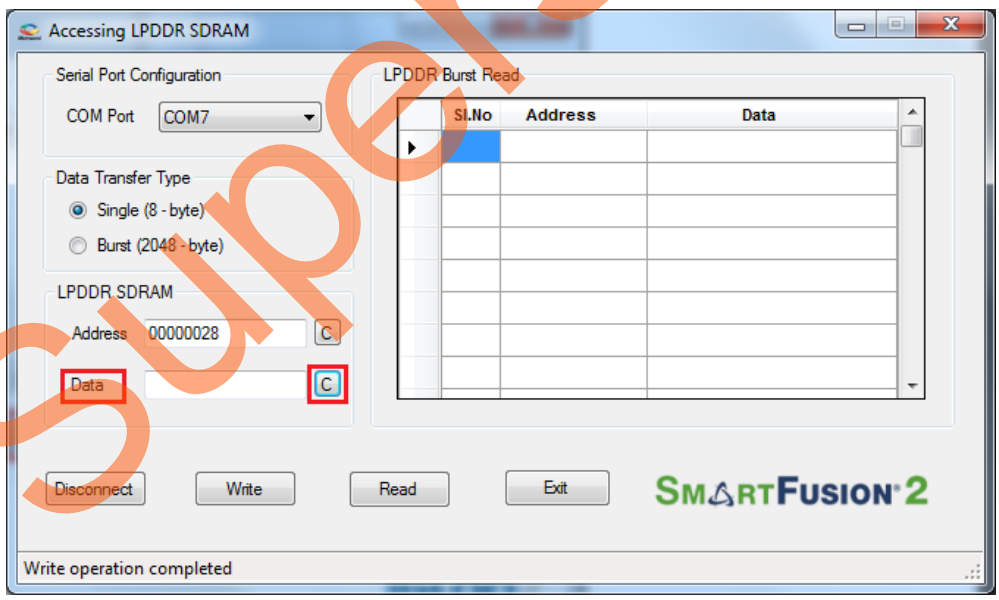

Figure 22 • **Clear the Data Field**

8. Click **Read** to read the data from the LPDDR SDRAM.

Figure 23 shows the data read from the LPDDR SDRAM.

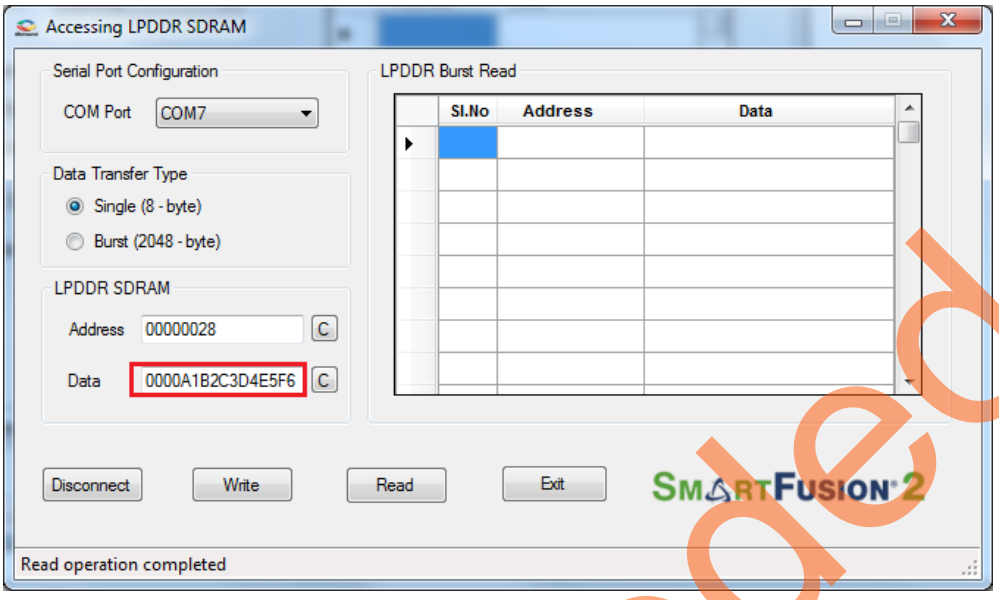

***Figure 23* • Single Read Operation**

9. Compare the read and write data. The write and read data being same establishes that the write and read operations to the LPDDR SDRAM were successful.

Performing Burst Data Transfer

For a burst write or read operation, the AXI Master logic is configured to transfer a burst length of 16 (that is, 128 bytes). In this demo, 16 transfers of 16-beat burst operations is implemented, that is, 16 (transfers) x 16-beat burst data = 2048 bytes data). For a write operation, the utility sends a 32-bit initial address and 64-bit (8 bytes) initial data. After the initial write operation, incremental data is written. For a read operation, the utility sends a 32-bit address and receives 2048 bytes of data from the LPDDR SDRAM and the data is displayed in the utility.

To perform a burst data transfer, follow the below mentioned steps:

1. Select the **Data Transfer Type** as **Burst (2048 bytes)**.
2. A 64-bit aligned address is required in the address field. Enter a 32-bit HEX Address in the range 0x00000000 - 0x03FFF7F8. When a non 64-bit aligned address is provided, the GUI converts it into 64-bit aligned address and performs the write/read operation. Refer to "Appendix C: Performing Write/Read Operation When Non 64-Bit Aligned Address is Provided" on page 34 to perform write/read when non 64-bit aligned address is provided.
3. In the **Data** field, enter a 64-bit data in HEX format.
4. Click **Write**. The entered data is written to the Address location specified in the Address filed and then the data is incremented by 1 and written to the next address location. This is repeated 256 times to write all the 2048 bytes of data.

5. Figure 24 shows the **Address** and **Data** values entered for a Burst Write operation.

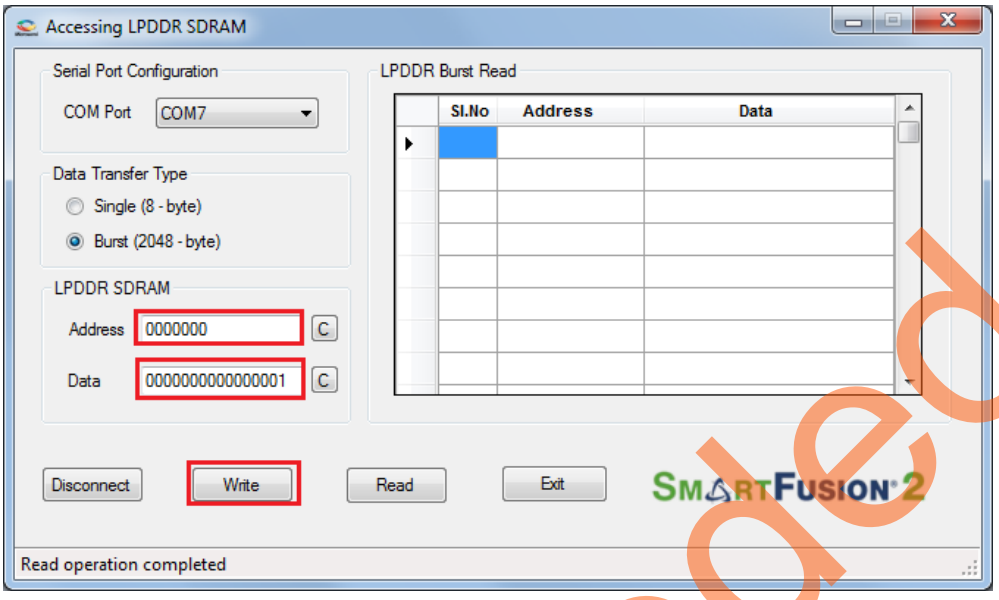

***Figure 24* • Burst Write operation**

6. To verify the write operation, perform a read operation to the same address where the data was written.
7. Click **Read**. All the 2048 bytes of data that was written to the LPDDR was read and the read data was displayed in the **LPDDR Burst Read** panel. Figure 25 shows the burst read data.

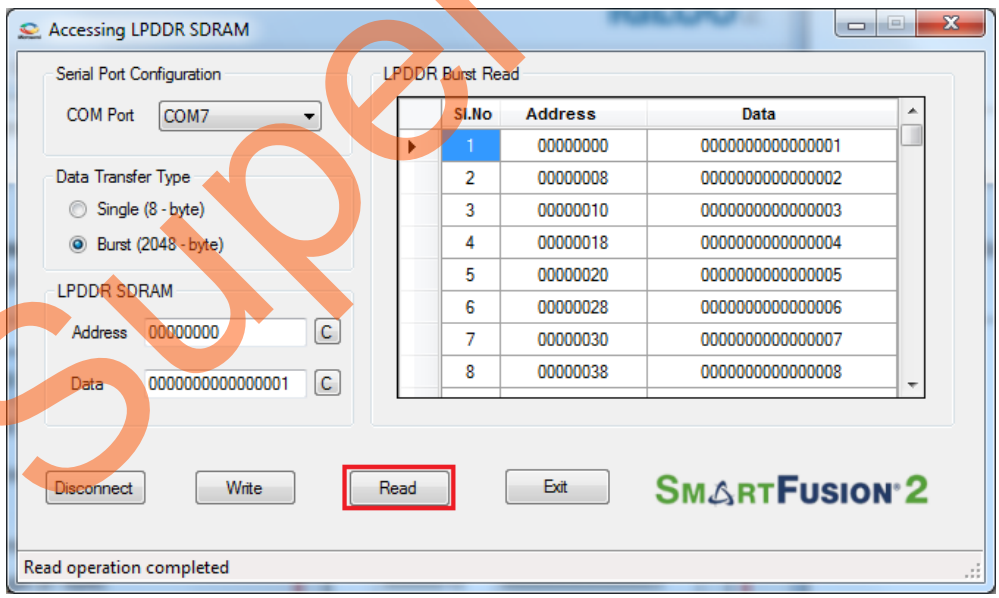

***Figure 25* • Burst Read Operation**

8. Click **Exit** to exit the utility.

Conclusion

This demo shows how to perform Read/Write operations to LPDDR SDRAM using SmartFusion2 SoC MDDR controller. Options are provided to simulate the design using a SmartDesign testbench and validate the design on the SmartFusion2 SoC Evaluation Kit using a GUI interface.

Appendix A: Configuring the MDDR Controller

This section describes how to configure the MDDR Controller registers using Libero SoC. Configuration options for MDDR are available at the **MDDR** tab of the **Memories** tab in System Builder. Figure 26 shows the **MDDR** tab.

The SmartFusion2 SoC Evaluation Kit has the LPDDR memory from Micron. All values provided here are from the Micron datasheet, part number, MT46H32M16LF.

Note: The *Automotive Mobile Low-Power DDR SDRAM* datasheet is available for download from Micron website.

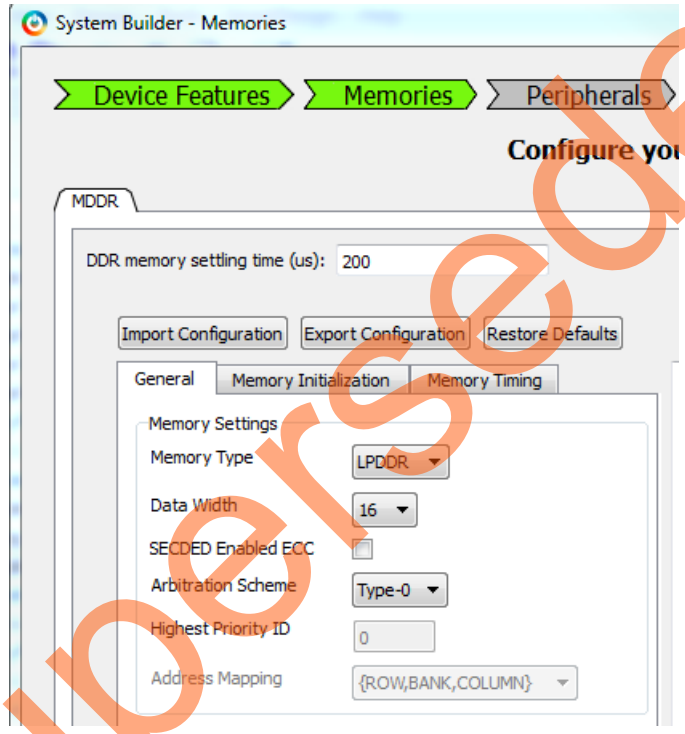

***Figure 26* • System Builder - Memories - MDDR Tab**

MDDR Configuration Tab

When using an external memory, the memory controller must wait for the memory to initialize (settling time) before accessing it. Since the SmartFusion2 SoC Evaluation Kit is using the LPDDR memory, the DDR Controller has to wait at least 200us. Provide 200 as the value for the field, **DDR memory settling time (us)**.

Note: All the values provided here are from the Micron datasheet. The parameters can be configured according to the user's requirements.

General

This section shows the configurations of the **General** tab.

- **Memory Type**: LPDDR
- **Data Width**: 16

Figure 27 shows the **General** tab after configuration parameters are set.

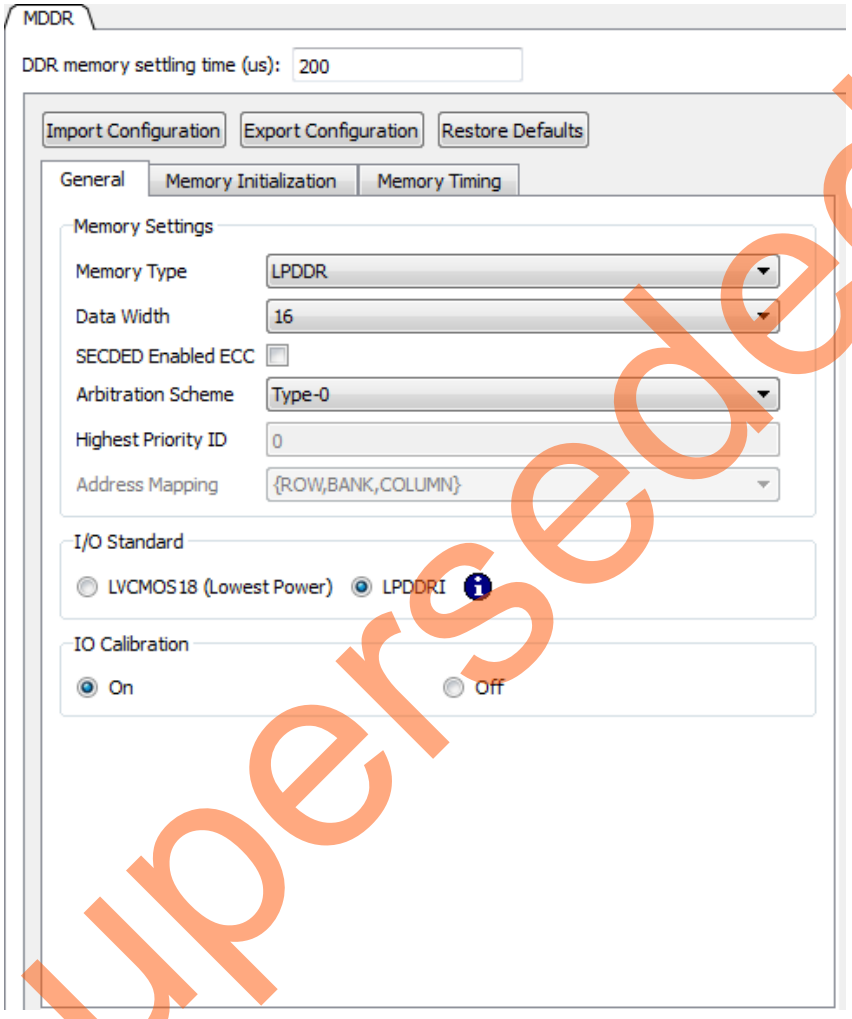

***Figure 27* • System Builder MDDR Configuration – General Tab**

Memory Initialization

This section shows the configurations of the **Memory Initialization** tab.

- **Burst length**: 8
- **Burst Order**: Sequential
- **Timing Mode**: 1T
- **CAS Latency**: 3
- **Self Refresh Enabled**: NO
- **Auto Refresh Burst Count**: 8
- **Power Down Enabled**: YES
- **Stop the clock:** NO
- **Deep Power Down enabled**: NO
- **No Activity clocks for Entry**: 320

Figure 28 shows the **Memory Initialization** tab after configuration parameters are set.

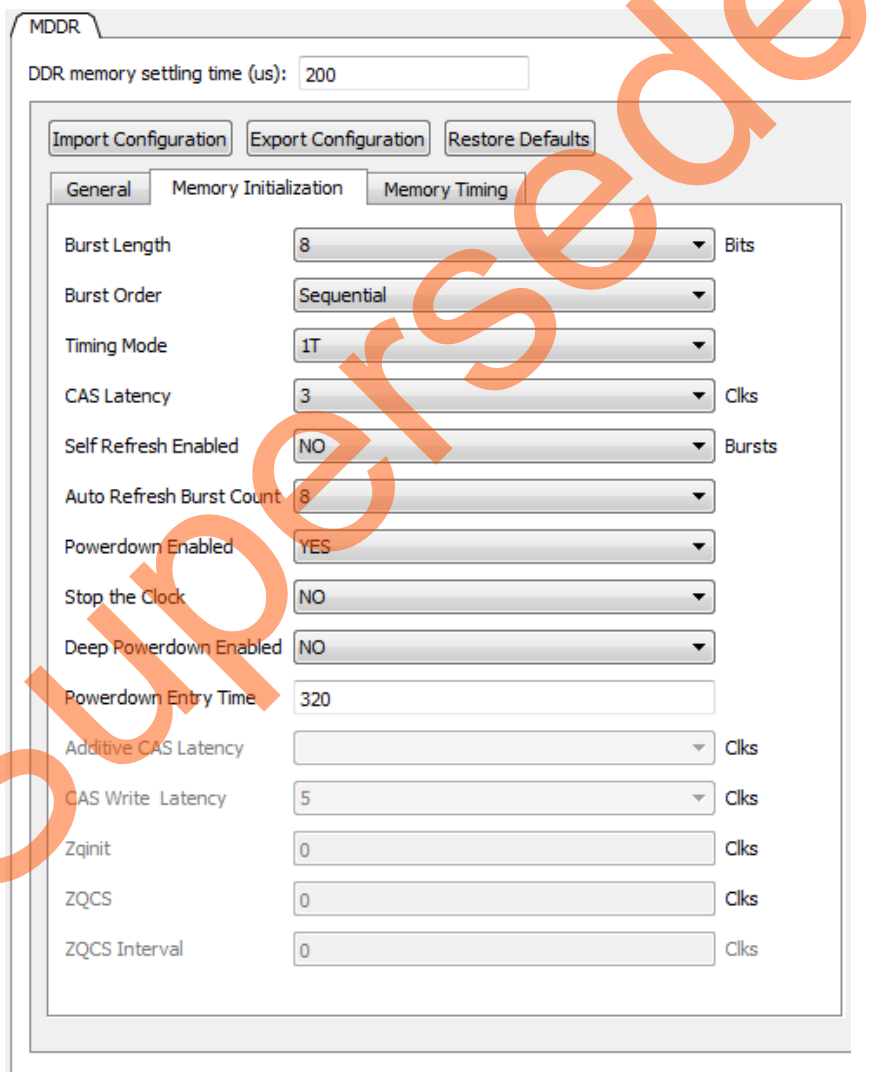

***Figure 28* • System Builder MDDR Configuration – Memory Initialization Tab**

Memory Timing:

This section shows the configurations of the **Memory Timing** tab.

- **Time To Hold Reset Before INIT** – 0 clks
- **MRD**: 4 clks
- **RAS (Min)**: 8 clks
- **RAS (Max)**: 8192 clks
- **RCD**: 6 clks
- **RP**: 7 clks
- **REFI**: 3104 clks
- **RC**: 3 clks
- **XP**: 3 clks
- **CKE**: 3 clks
- **RFC**: 79 clks
- **FAW**: 0 clks

Figure 29 shows the **Memory Timing** tab after configuration parameters are set.

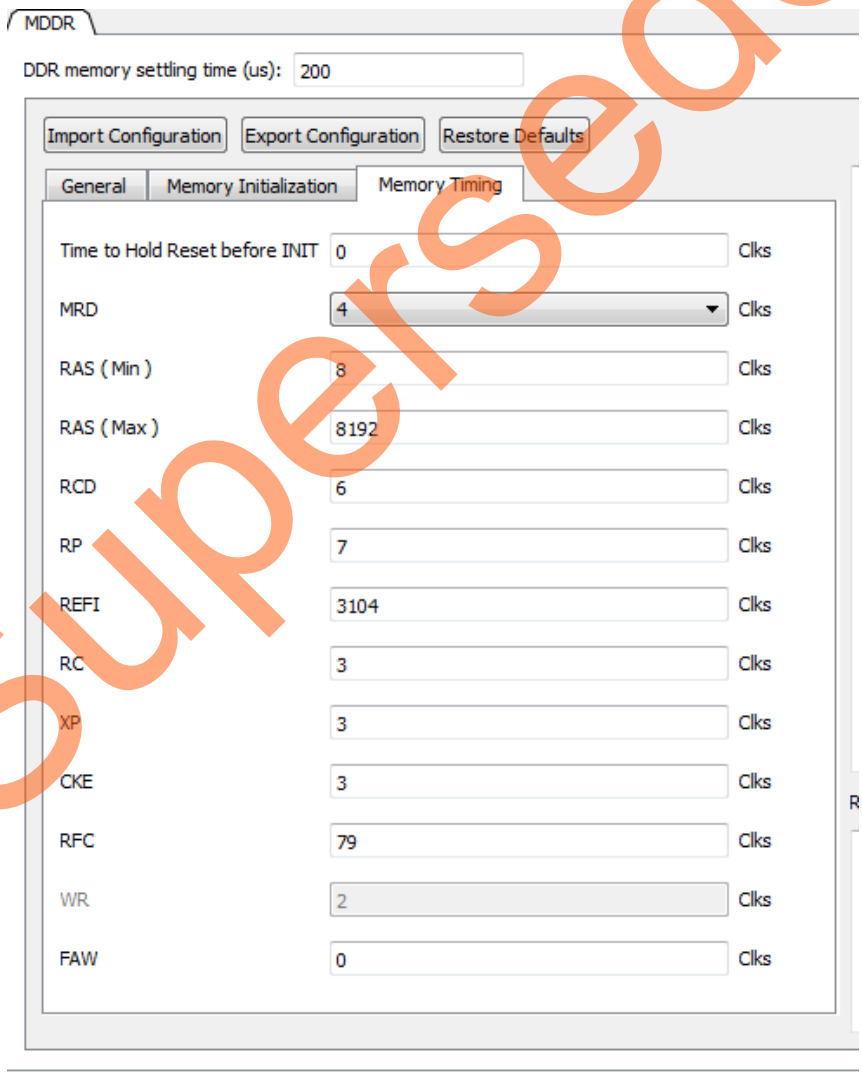

***Figure 29* • System Builder MDDR Configuration – Memory Timing Tab**

Appendix B: Finding the Correct COM Port Number When Using the USB 3.0

FTDI USB to UART converter enumerates the four COM ports. In USB 3.0, the four available COM ports are in Location 0. Figure 30 shows the USB 3.0 Serial port properties.

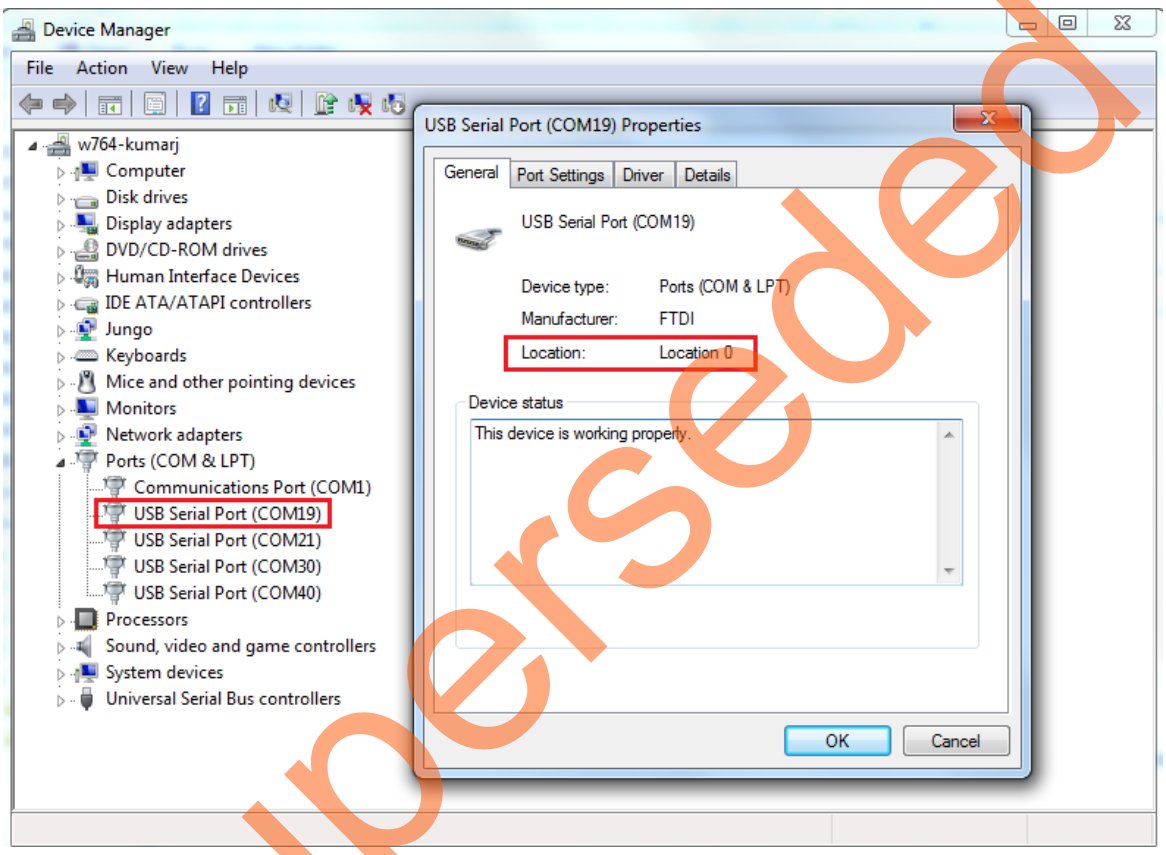

Figure 30 • **USB 3.0 Serial Port Properties**

To find out the correct COM port, program the SmartFusion2 SoC Evaluation Kit board with provided programming file. Connect each available COM port and click **Write**. If wrong COM port is selected, the GUI displays the read error. Try with all four available COM ports until this message disappears. Figure 31 shows the read error message.

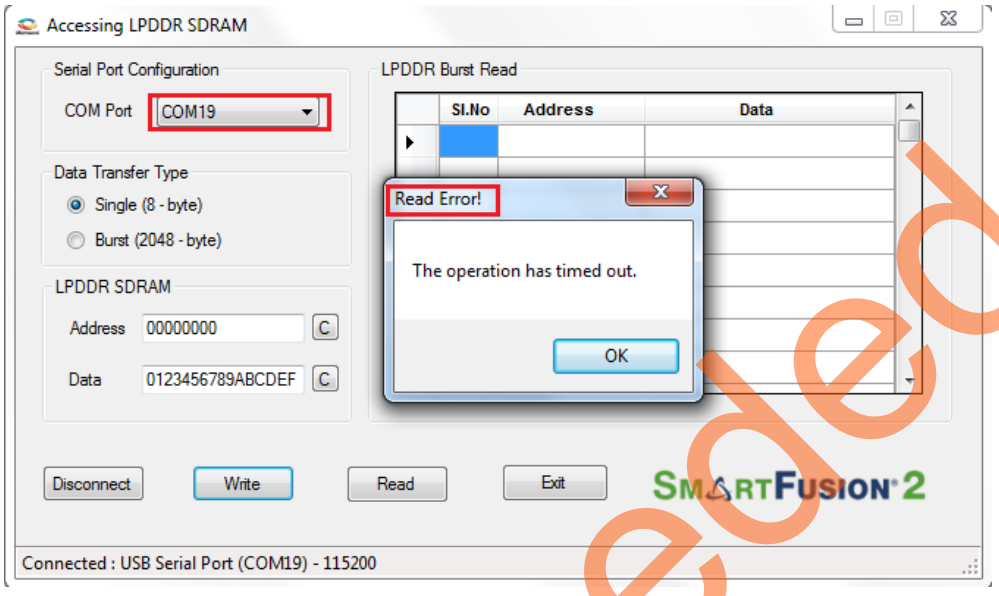

***Figure 31* • Read Error**

Appendix C: Performing Write/Read Operation When Non 64-Bit Aligned Address is Provided

When a non 64-bit aligned address is provided in the GUI, the GUI converts it into the 64-bit aligned address (0, 8,10,18,20,28,30,38 …) and performs the write/read operation.

1. Enter the non 64-bit aligned 32-bit address in HEX format.
2. Enter the 64-bit data in HEX format.

Figure 32 shows the non 64-bit aligned address entered in the GUI.

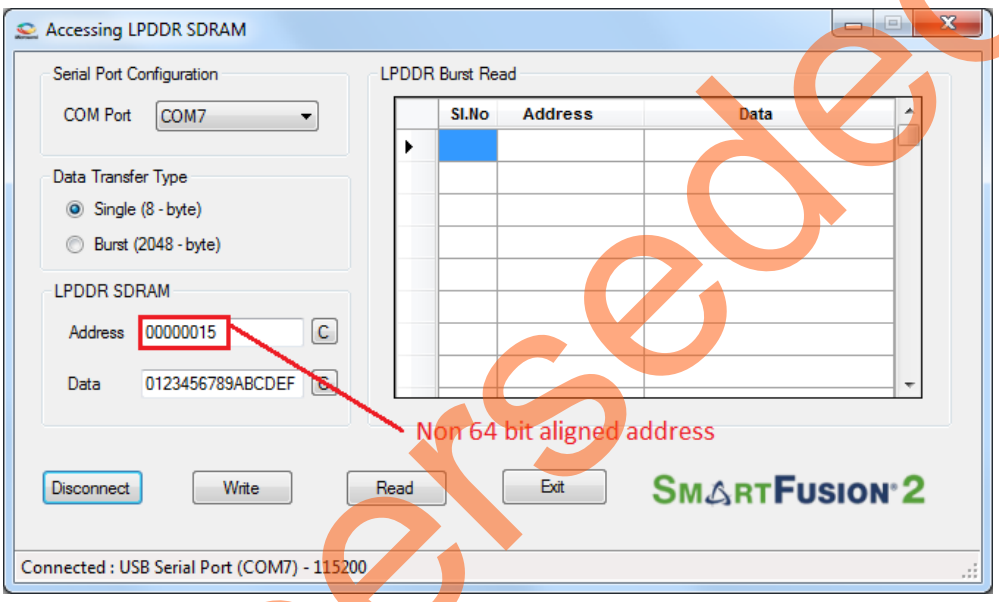

***Figure 32* • Non 64-Bit Aligned Address**

3. Click **Write** to perform write operation. GUI converts the address into 64-bit aligned address and performs the write operation.

Figure 33 shows the GUI pop up information message and converted 64-bit aligned address.

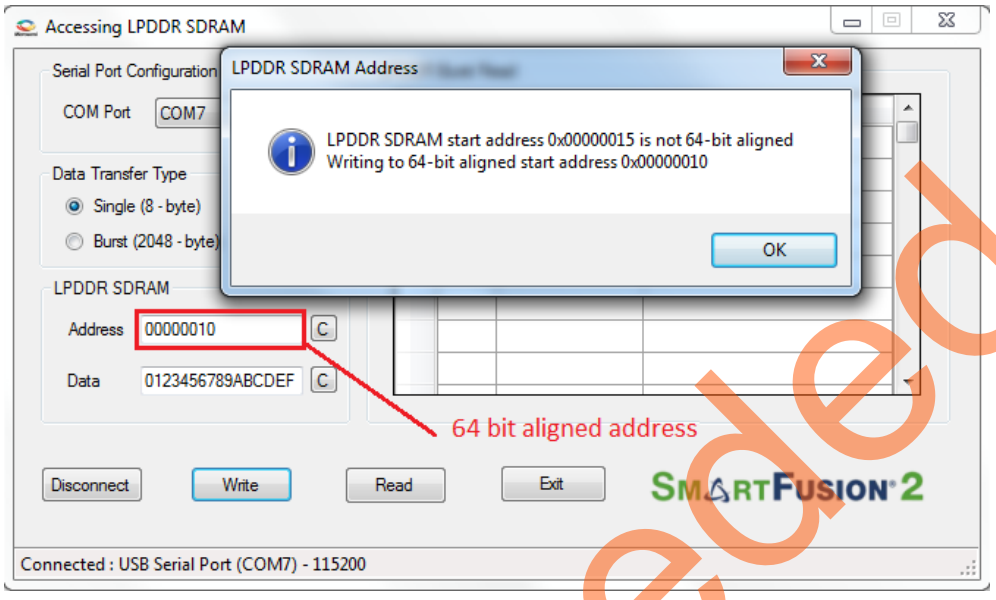

***Figure 33* • Converted 64-Bit Aligned Address**

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

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Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

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Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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