IGLOO2 FPGA PCIe Control Plane with Device Serial Number - Libero SoC v11.4

Demo Guide

August 2014

Microsemi

Revision History

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07 August 2014	3	Third Release
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Confidentiality Status

This is a non-confidential document.

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Preface

About this document

This demo is for IGLOO®2 field programmable gate array (FPGA) devices. It provides instructions on how to use the corresponding reference design.

Intended Audience

The following designers use the IGLOO2 devices:

- FPGA designers
- System-level designers

References

Microsemi Publications

- IGLOO2 FPGA High Speed Serial Interfaces User Guide
- Implementing PCIe Control Plane Design - Libero SoC Flow Tutorial for IGLOO2 FPGA
- IGLOO2 FPGA System Controller User Guide

See the following web page for a complete and up-to-date listing of IGLOO2 device documentation: http://www.microsemi.com/products/fpga-soc/fpga/igloo2-fpga

IGLOO2 FPGA PCIe Control Plane with Device Serial Number Demo

Introduction

The IGLOO2 FPGA devices integrate a fourth-generation flash-based FPGA fabric and high-performance communication interfaces on a single chip. The IGLOO2 high speed serial interface (SERDES) provides a fully hardened PCI®express (PCIe) endpoint (EP) implementation and is compliant with PCIe Base Specification Revision 2.0 and 1.1. For more details, refer to the *IGLOO2 FPGA High Speed Serial Interfaces User Guide*.

This demo shows how the embedded PCIe feature of IGLOO2 FPGA devices can be used as a low bandwidth control plane interface. This demo also demonstrates device serial number (DSN) feature embedded in the IGLOO2 device. A sample design is provided to access IGLOO2 PCIe EP from Host PC. This demo can run on both windows and RedHat Linux operating system (OS). A GUI installer, Host PC drivers for windows OS and a Linux PCIe application for Linux OS are provided for reading and writing to the IGLOO2 PCIe configuration and memory space.

Figure 1 shows the top-level block diagram of the PCIe control plane demo. The demo design uses an IGLOO2 PCIe interface with a link width of x1 lane to interface with a Host PC PCIe Gen2 slot. The CoreGPIO IP controls the LEDs and switches on the IGLOO2 Evaluation Kit board through the PCIe interface. The Host PC can also read and write to the IGLOO2 large SRAM (LSRAM). The Host PC can also be interrupted by using the push button on the IGLOO2 Evaluation Kit board. The Host PC can read the 128-bit DSN system service.

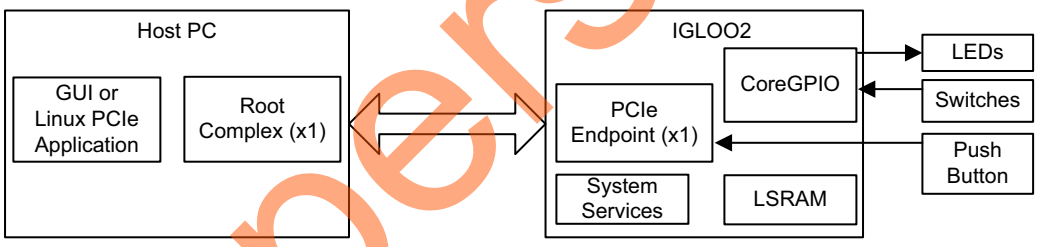

***Figure 1* • PCIe Control Plane Demo Top-Level Block Diagram**

Design Requirements

Table 1 • **Design Requirements**

Design Requirements	Description
Hardware Requirements	
IGLOO2 Evaluation Kit • 12 V adapter • FlashPro4 programmer • USB A to Mini-B cable	Rev C or later
Host PC or Laptop with an available PCIe 2.0 Gen 1 or Gen 2 compliant slot	64-bit Windows 7 OS or 64-bit Red Hat Linux OS (Kernel Version: 2.6.18-308)
Express Card slot and PCIe Express card adapter (for Laptop only)	-
Software Requirements	
Libero® System-on-Chip (SoC) for viewing the design files	v11.4
FlashPro Programming Software	v11.4
Host PC Drivers (provided along with the design files)	
GUI executable (provided along with the design files)	-
Note: PCIe Express card adapter is not supplied with the IGLOO2 Evaluation Kit	

Demo Design

Introduction

The design files for this demo can be downloaded from the Microsemi® website:
http://soc.microsemi.com/download/rsc/?f=M2GL-PCIE-Control-Plane-DSN-11p4-DF

Design files include:

1. Libero project
2. Programming files
3. Host PC drivers and GUI executable for Windows OS
4. Host PC drivers and PCIe application for Linux OS
5. Source files
6. Readme file

Figure 2 shows the top-level structure of the design files. For further details, refer to the readme.txt file.

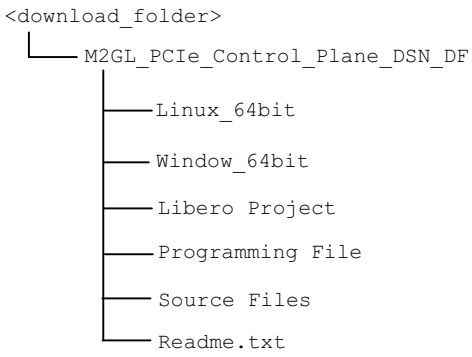

***Figure 2* • Demo Design Files Top-Level Structure**

Demo Design Features

The demo design performs the tasks listed below:

- Displays PCIe link enable/disable, negotiated link width, and the link speed.
- Controls the status of LEDs on the IGLOO2 Evaluation Kit board
- Displays the position of DIP switches on IGLOO2 Evaluation Kit board
- Enables read and write to LSRAM
- Accepts and displays interrupts from the push button on the IGLOO2 Evaluation Kit board
- Shows the IGLOO2 PCIe configuration space
- Reads DSN

Demo Design Description

The demo design helps to access the IGLOO2 PCIe EP from the Host PC.

Figure 3 shows a detailed block diagram of the design implementation.

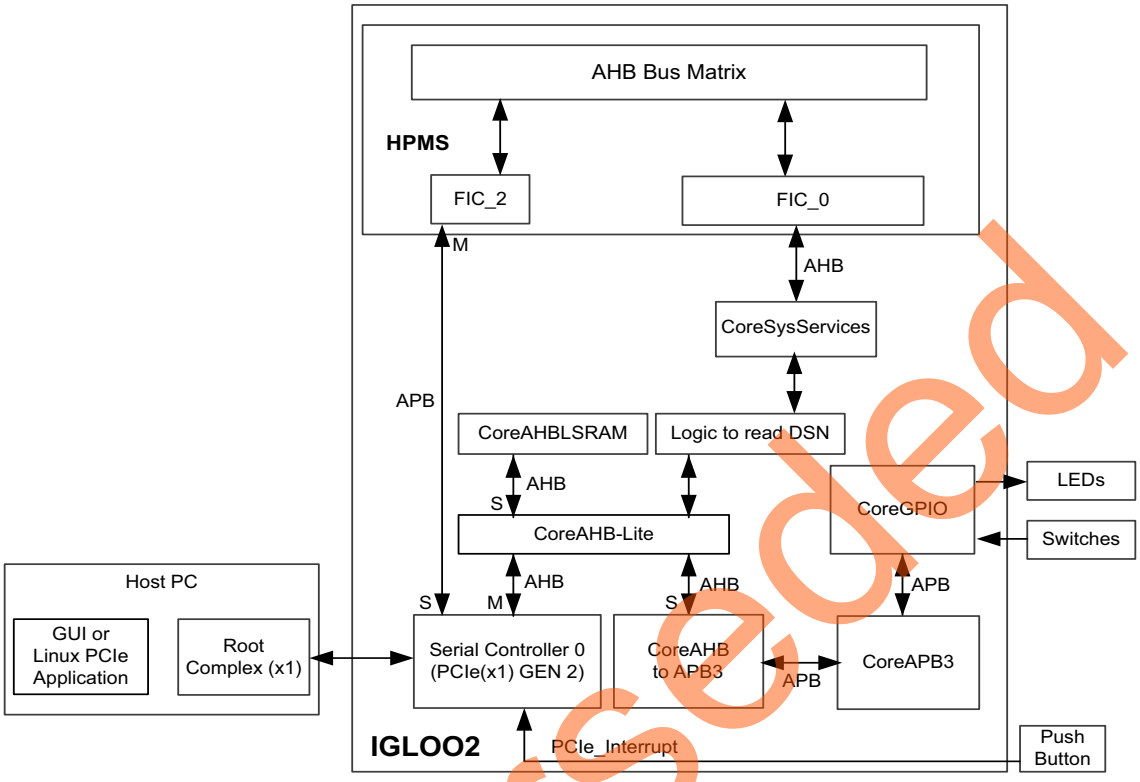

***Figure 3* • PCIe Control Plane Block Diagram**

The PCIe EP device receives commands from the Host PC through the GUI or Linux PCIe application and performs corresponding memory writes to the IGLOO2 fabric address space.

The SERDES_IF_0 is configured for a PCIe 2.0, x1 link width with GEN2 speed. The PCIe interface to the fabric uses an AMBA high-speed bus (AHB). The AHB master interface of SERDESIF is enabled and connected to the slaves CoreAHBLSRAM and CoreGPIO using CoreAHBLite, CoreAHBTOAPB, and CoreAPB3 bus interfaces.

SERDES_IF_0 is initialized by HPMS which is configured by the System Builder.

CoreSysServices Soft IP provides a user interface and AHB-Lite master interface to access the DSN System Service. This System Service fetches the 128-bit DSN. The DSN is unique to every device that is set during manufacturing. A simple Verilog logic is implemented to read the DSN using CoreSysServices IP and write the same to LSRAM.

For more details on System Services refer to the *IGLOO2 FPGA System Controller User Guide*.

The AXI master windows of the SERDESIF PCIe provide address translation for accessing one address space from another address space as the PCIe address is different from the IGLOO2 AHB bus matrix address space. The AXI master window 0 is enabled and configured to translate the BAR0 memory address space to the CoreGPIO address space to control the LEDs and DIP switches.

The AXI master window 1 is enabled and configured to translate the BAR1 memory address space to the CoreAHBLSRAM address space to perform read and write from PCIe.

The IGLOO2 PCIe BAR0 and BAR1 are configured in 32-bit mode.

CoreGPIO is enabled and configured as below:

- GPIO_OUT [8] connected to user logic to read the DSN
- GPIO_OUT [7:0] connected LEDs
- GPIO_IN[4] indicates that the device serial number is available in LSRAM to display
- GPIO_IN [3:0] connected to DIP switches

The PCIe interrupt line is connected to the **SW4** push button on the IGLOO2 Evaluation Kit board. The FPGA clocks are configured to run the FPGA fabric at 50 MHz and HPMS at 100 MHz.

Simulating the Design

The design supports the BFM_PCIe simulation level to communicate with the SERDESIF block through the master AXI bus interface. Although no serial communication actually goes through the SERDESIF block, this scenario allows to validate the fabric interface connections. The SERDESIF_0_user.bfm file under the *<Libero project>/simulation* folder contains the BFM commands to verify the read or write access to CoreGPIO and CoreAHBLSRAM.

BFM commands added in the `SERDESIF_0_user.bfm` file do the following:

- Write to GPIO_OUT[7:0]
- Write to LSRAM
- Read-check from LSRAM

To run the simulation, double-click **Simulate** under **Verify Pre-Synthesized Design** in the **Design Flow** window of Libero project. ModelSim runs the design for about **290 us**. The ModelSim transcript window displays the BFM commands and the BFM simulation completed with no errors, as shown in Figure 4.

***Figure 4* • SERDES BFM Simulation**

Figure 5 shows the waveform window with GPIO_OUT signals.

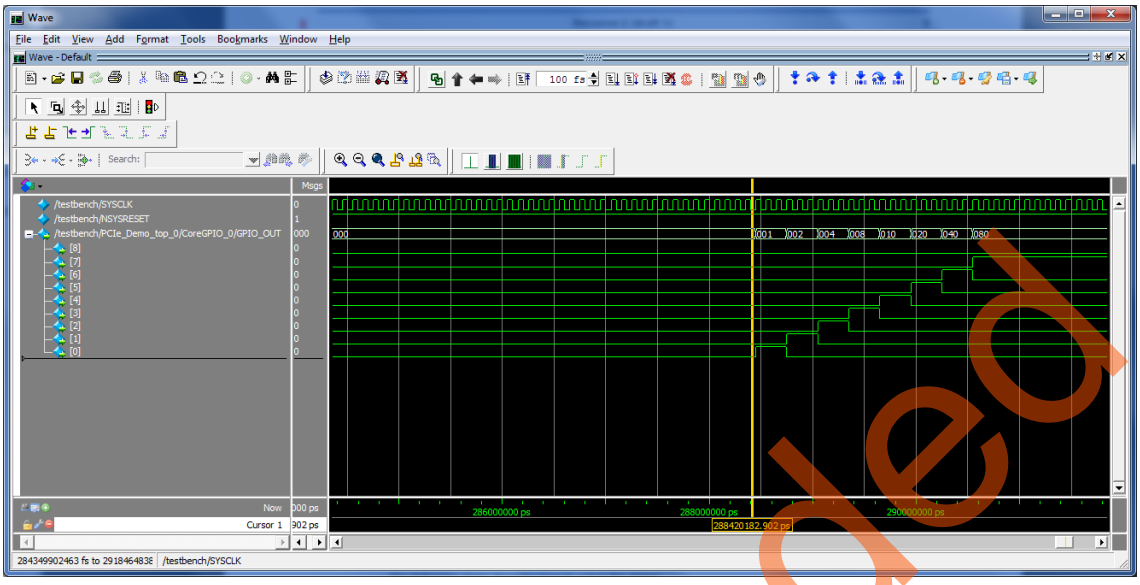

***Figure 5* • Simulation Result with GPIO_OUT Signals**

Setting Up the Demo Design

The following steps describe how to setup the demo:

1. Connect the **FlashPro4 programmer** to the J5 connector of the IGLOO2 FPGA Evaluation Kit board.
2. Connect the jumpers on the IGLOO2 FPGA Evaluation Kit board as shown in Table 2.

   CAUTION: While making the jumper connections, the power supply switch **SW7** on the board should be in **OFF** position.

***Table 2* • IGLOO2 FPGA Evaluation Kit Jumper Settings**

Jumper	Pin (from)	Pin (to)	Comments
J22	1	2	Default
J23	1	2	Default
J24	1	2	Default
J8	1	2	Default
J3	1	2	Default

3. Connect the power supply to the J6 connector.

Board Setup

Snapshots of the IGLOO2 Evaluation Kit board with the complete set up is given in the "Appendix 1: IGLOO2 Evaluation Kit Board" on page 39.

Programming the IGLOO2 Board

1. Download the demo design from: http://soc.microsemi.com/download/rsc/?f=M2GL-PCIE-Control-Plane-DSN-11p4-DF
2. Switch **ON** the **SW7** power supply switch.
3. Launch the **FlashPro** software.
4. Click **New Project**.
5. In the **New Project** window, type the project name as PCIe_Control_Plane.

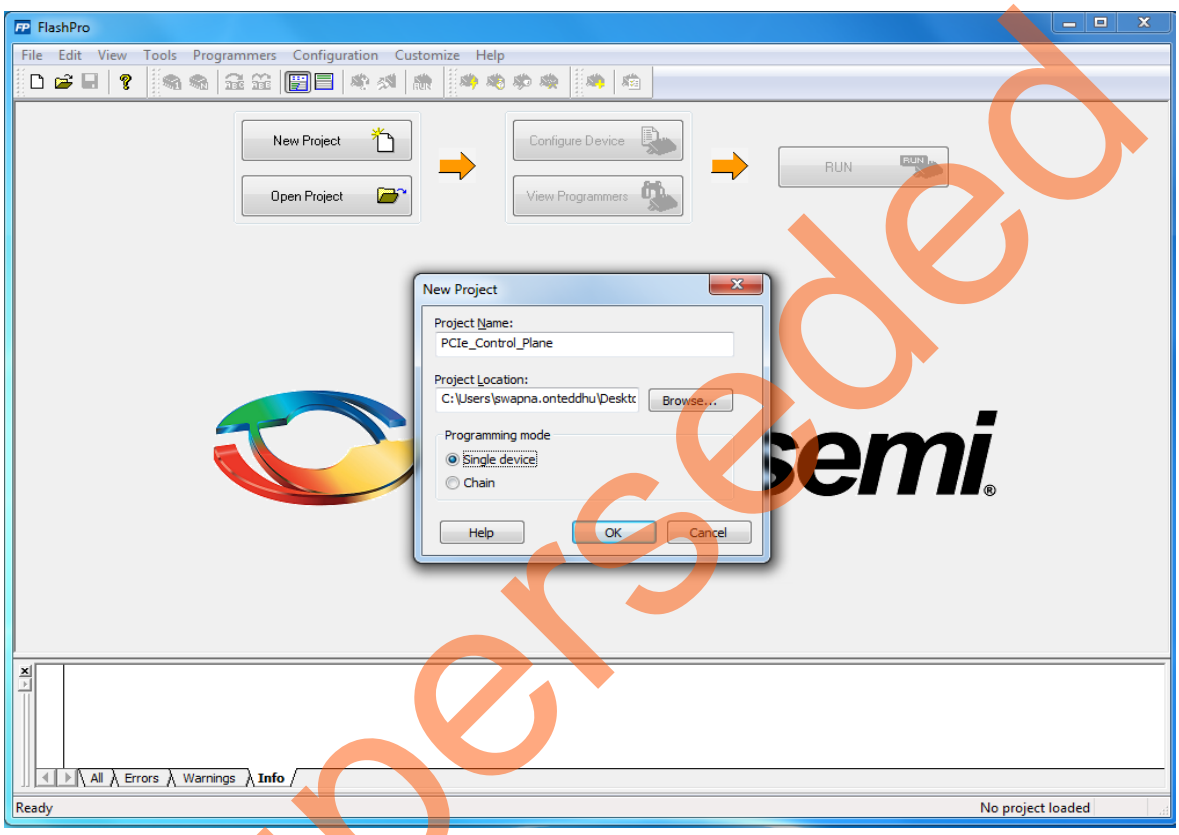

***Figure 6* • FlashPro New Project**

6. Click **Browse** and navigate to the location where you want to save the project.
7. Select **Single device** as the **Programming mode**.
8. Click **OK** to save the project.
9. Click **Configure Device** on the FlashPro GUI.
10. Click **Browse** and navigate to the location where the `PCIe_Demo_top.stp` file is located and select the file. The default location is: *<download_folder>\M2GL_PCIE_Control_Plane_DSN_DF\programming_file*.

11. Click **Open**. The required programming file is selected and is ready to be programmed in the device.

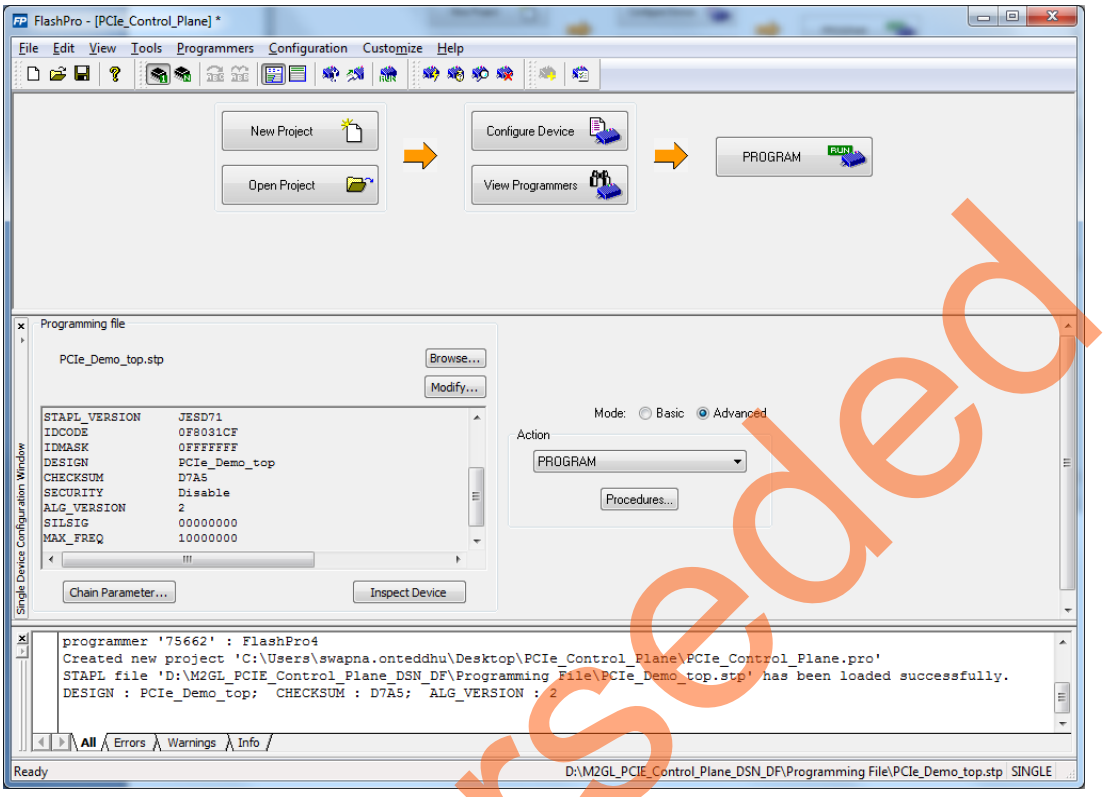

***Figure 7* • FlashPro Project Configured**

12. Click **PROGRAM** to start programming the device. Wait until you get a message indicating that the **PROGRAM PASSED**.

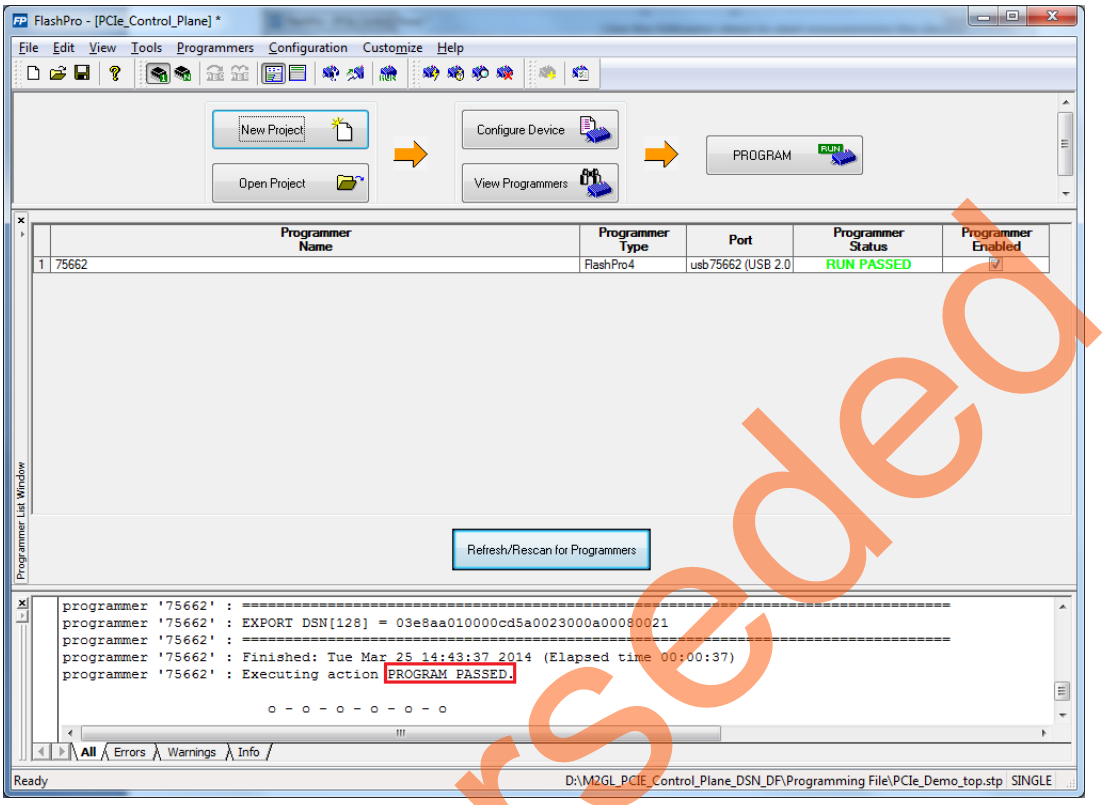

***Figure 8* • FlashPro Program Passed**

Connecting the Evaluation Kit Board to the Host PC

1. After successful programming, power **OFF** the IGLOO2 Evaluation Kit board and shut down the Host PC.
2. Use the below steps to connect the **CON1–PCIe Edge Connector** either to Host PC or laptop:

   a. Connect the **CON1–PCIe Edge Connector** to Host PC PCIe Gen2 slot or Gen1 slot as applicable. This tutorial is designed to run in any PCIe Gen2 compliant slot. If the Host PC does not support the Gen2 compliant slot, the design switches to the Gen1 mode.

   b. Connect the **CON1–PCIe Edge Connector** to the laptop PCIe slot using the express card adapter. If you are using a laptop, the express card adapters typically support only Gen1 and the design works on Gen1 mode.

Note: Host PC or laptop should be powered OFF while inserting the PCIe Edge Connector. If the system is not powered OFF, the PCIe device detection and selection of Gen1 or Gen2 do not occur properly. It is recommended that the Host PC or laptop should be powered OFF during the PCIe card insertion.

3. Figure 9 shows the board setup for the Host PC in which IGLOO2 Evaluation Kit board is connected to the Host PC PCIe slot. To connect the IGLOO2 Evaluation Kit board to the laptop using Express card adapter, refer to the "Appendix 2: IGLOO2 Evaluation Kit Board Setup for Laptop" on page 40.

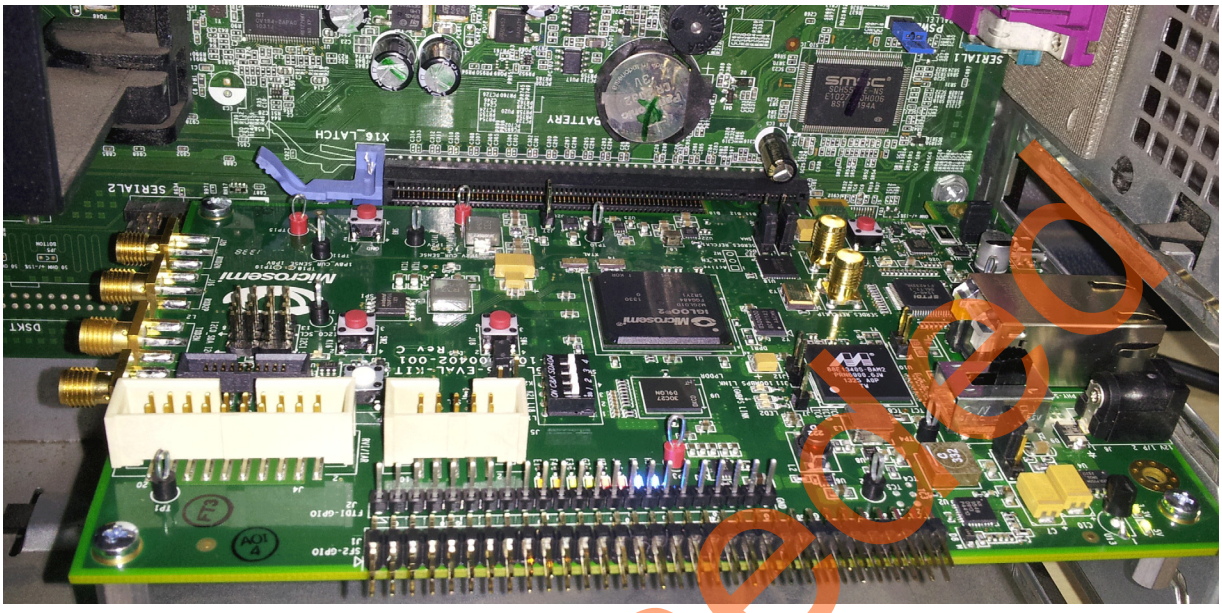

***Figure 9* • IGLOO2 Evaluation Kit Setup for Host PC**

Running the Demo Design

This demo can run on both windows and RedHat Linux OS.

- To run the demo on Windows OS GUI, Jungo drivers are provided. Refer to "Running the Demo Design on Windows" section on page 15.
- To run the demo on Linux OS, native RedHat Linux drivers and command line scripts are provided. Refer to "Running the Demo Design on Linux" section on page 27

Running the Demo Design on Windows

1. Switch **ON** the **SW7** power supply switch.
2. Power on the Host PC and open the host PC Device Manager for PCIe device as shown in Figure 10. If the PCIe device is not detected, power cycle the IGLOO2 Evaluation Kit board and click **scan for hardware changes** in Device Manager.

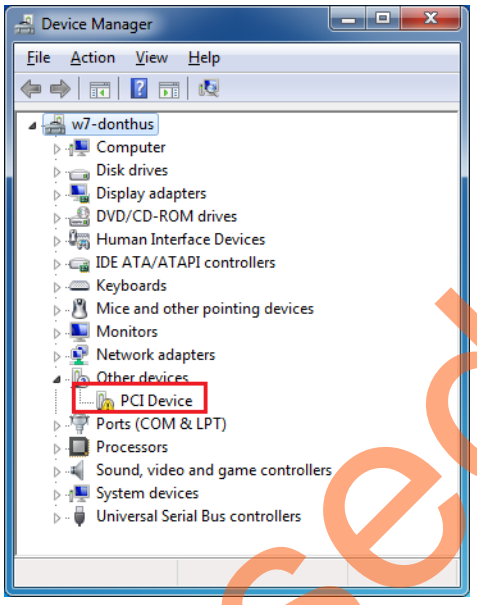

Figure 10 • **Device Manager**

Note: If the device is still not detected, check whether or not the BIOS version in Host PC is latest, and if PCIe is enabled in the Host PC BIOS.

If the Host PC has any other installed drivers (previous versions of Jungo drivers) for the IGLOO2 PCIe device, uninstall them. To uninstall previous versions of Jungo drivers follow steps a and b.

a. To uninstall previous Jungo drivers, go to device manager and right-click **DEVICE** and select **Uninstall** as shown in Figure 11.

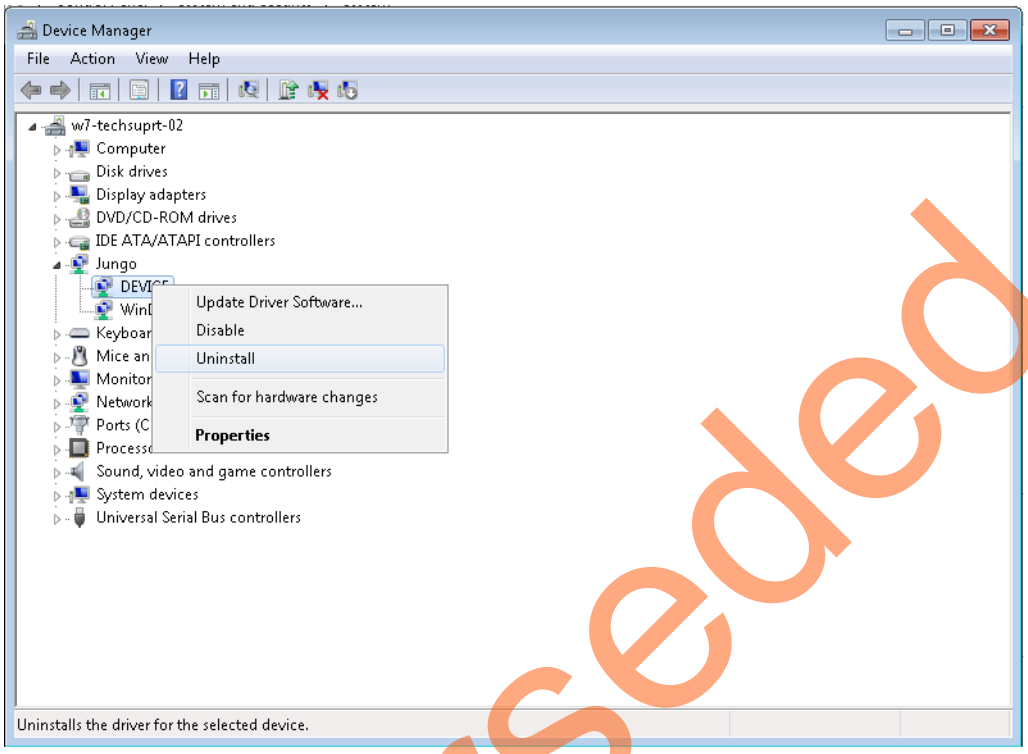

***Figure 11* • Device Uninstall**

b. The DEVICE uninstall window is displayed as shown in Figure 12. Select **Delete the driver software for this device**. After uninstalling previous Jungo drivers, make sure that the PCIe device is detected in the **Device Manager** window as shown in Figure 10.

***Figure 12* • Confirm Device Uninstall**

Drivers Installation

The PCIe demo uses a driver framework provided by Jungo WinDriverPro. To install the PCIe drivers on Host PC for IGLOO2 Evaluation Kit, use the following steps:

1. Extract the **PCIe_Demo.rar** to C:\ drive. The PCIe_Demo.rar is located in the provided design files:
   – M2GL_PCIE_Control_Plane_DSN_DF\Windows_64bit\Drivers\PCIe_Demo.rar

Note: Installing these drivers require Host PC administration rights.

2. Run the batch file ***C:\PCIe_Demo\DriverInstall\Jungo_KP_install.bat***
3. Click **Install** if the window is displayed as shown in Figure 13.

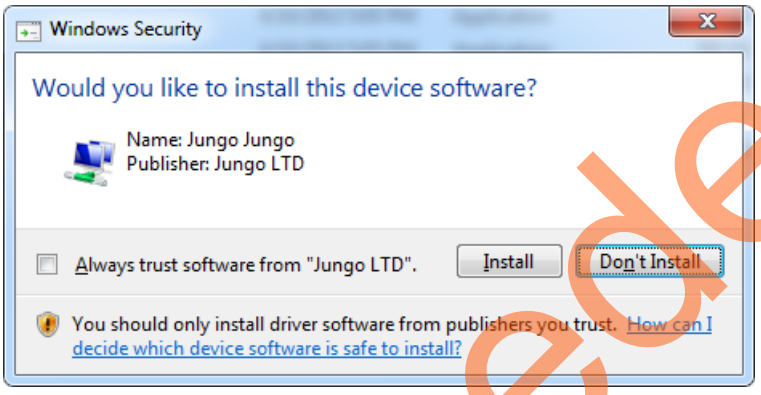

Figure 13 • **Jungo Driver Installation**

Note: If the installation is not in progress, right-click on the command prompt and select **Run as administrator**. Run the batch file ***C:\PCIe_Demo\DriverInstall\Jungo_KP_install.bat*** from command prompt.

4. Click **Install this driver software anyway** if the window appears as shown in Figure 14.

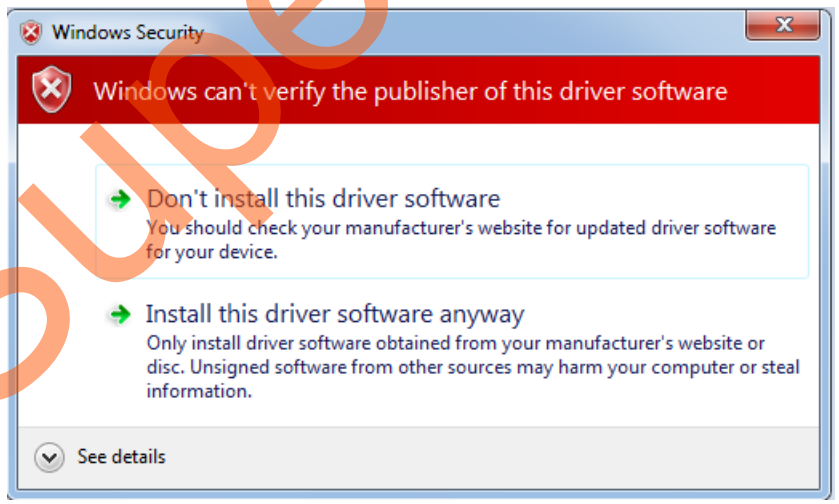

Figure 14 • **Windows Security**

PCIe Demo GUI Installation

IGLOO2 PCIe demo GUI is a simple GUI that runs on the Host PC to communicate with the IGLOO2 PCIe EP device. The GUI provides the PCIe link status, driver information, and demo controls. The GUI invokes the PCIe driver installed on the Host PC and provides commands to the driver according to the user selection.

Use the following steps to install the GUI:

1. Extract the **PCIe_Demo_GUI_Installer.rar** from the provided design files: *M2GL_PCIE_Control_Plane_DSN_DF\Windows_64bit\GUI*.
2. Double-click **setup.exe** in the provided GUI installation (*PCIe_Demo_GUI_Installer\setup.exe*). Apply default options as shown in Figure 15.

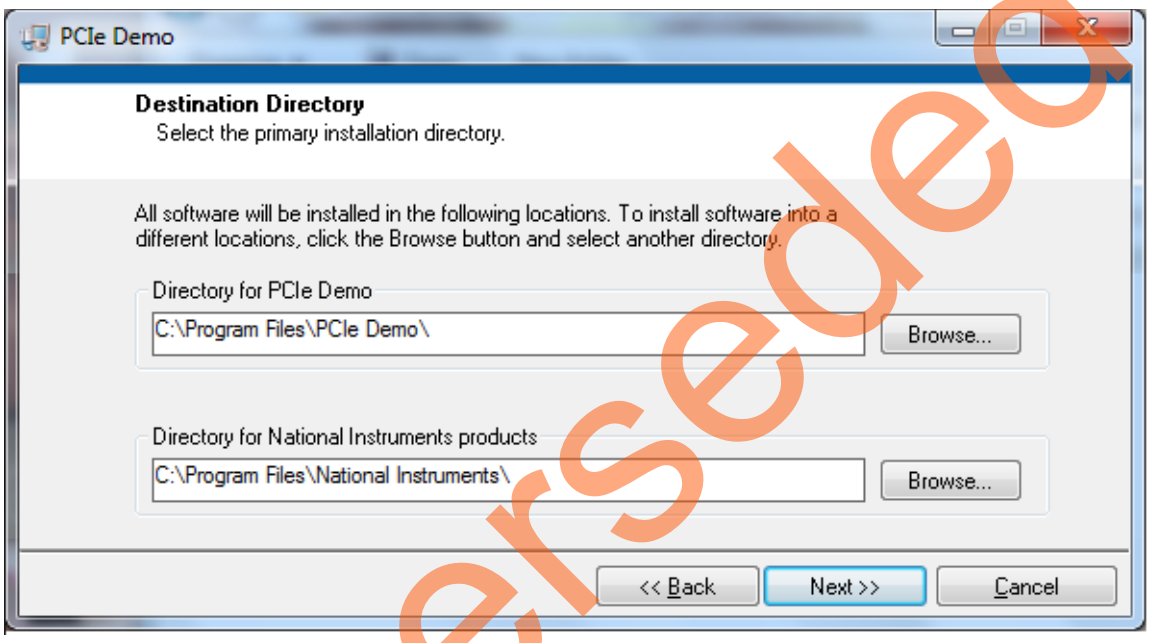

***Figure 15* • GUI Installation**

3. Click **Next** to complete the installation. After successful installation, the following window is displayed:

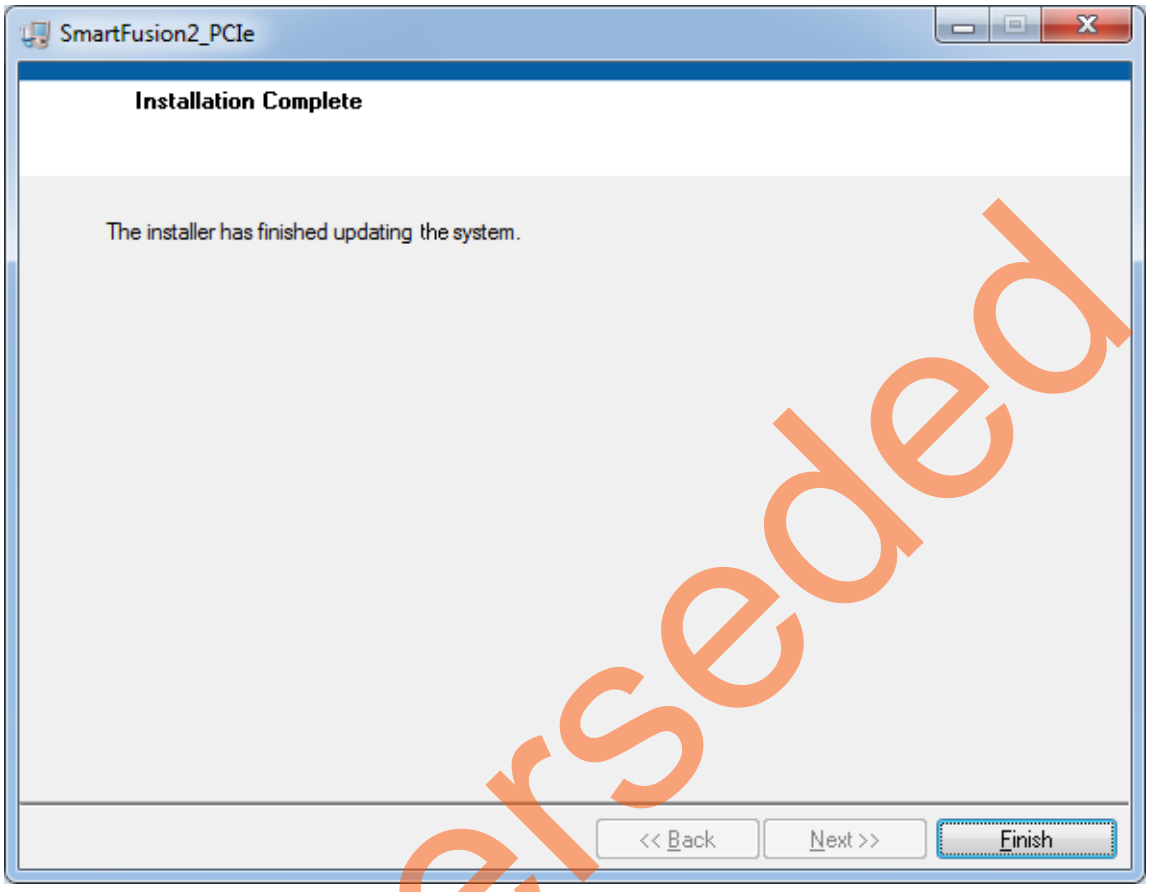

Figure 16 • **Sucessful GUI Installation**

4. Restart the Host PC.

Running the PCIe GUI

1. Check the Host PC **Device Manager** for the drivers. If the device is not detected, power cycle the IGLOO2 Evaluation Kit board and click **scan for hardware changes** in Device Manager. Make sure that the board is switched ON.

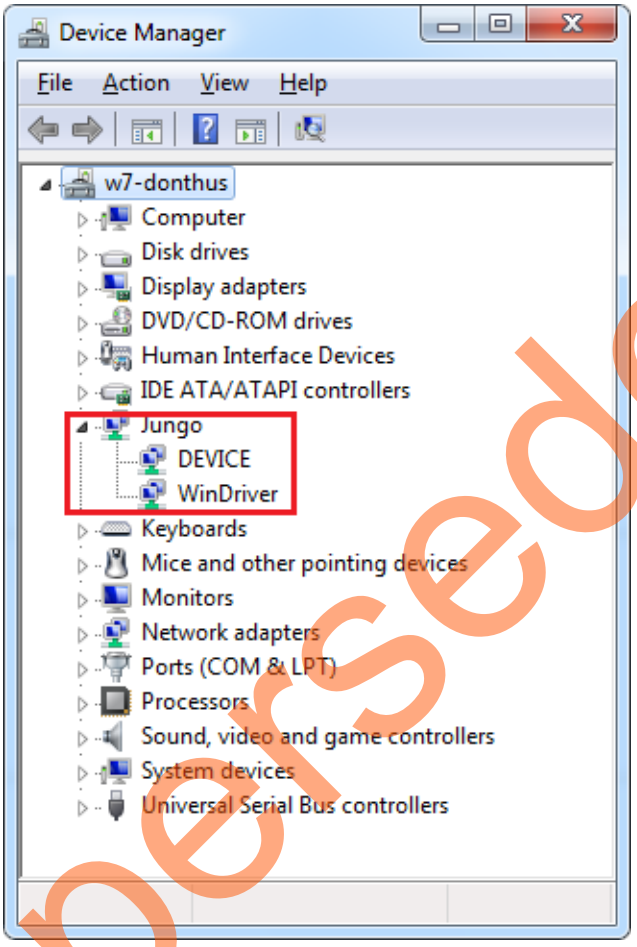

***Figure 17* • Device Manager - PCIe Device Detection**

Note: If a warning symbol is displayed on the **DEVICE** or **WinDriver** icons in the **Device Manager**, uninstall them and start from step1 of "Drivers Installation" on page 17.

2. Invoke the GUI from **ALL Programs > PCIeDemo > PCIe Demo GUI**. The GUI is displayed as shown in Figure 18.

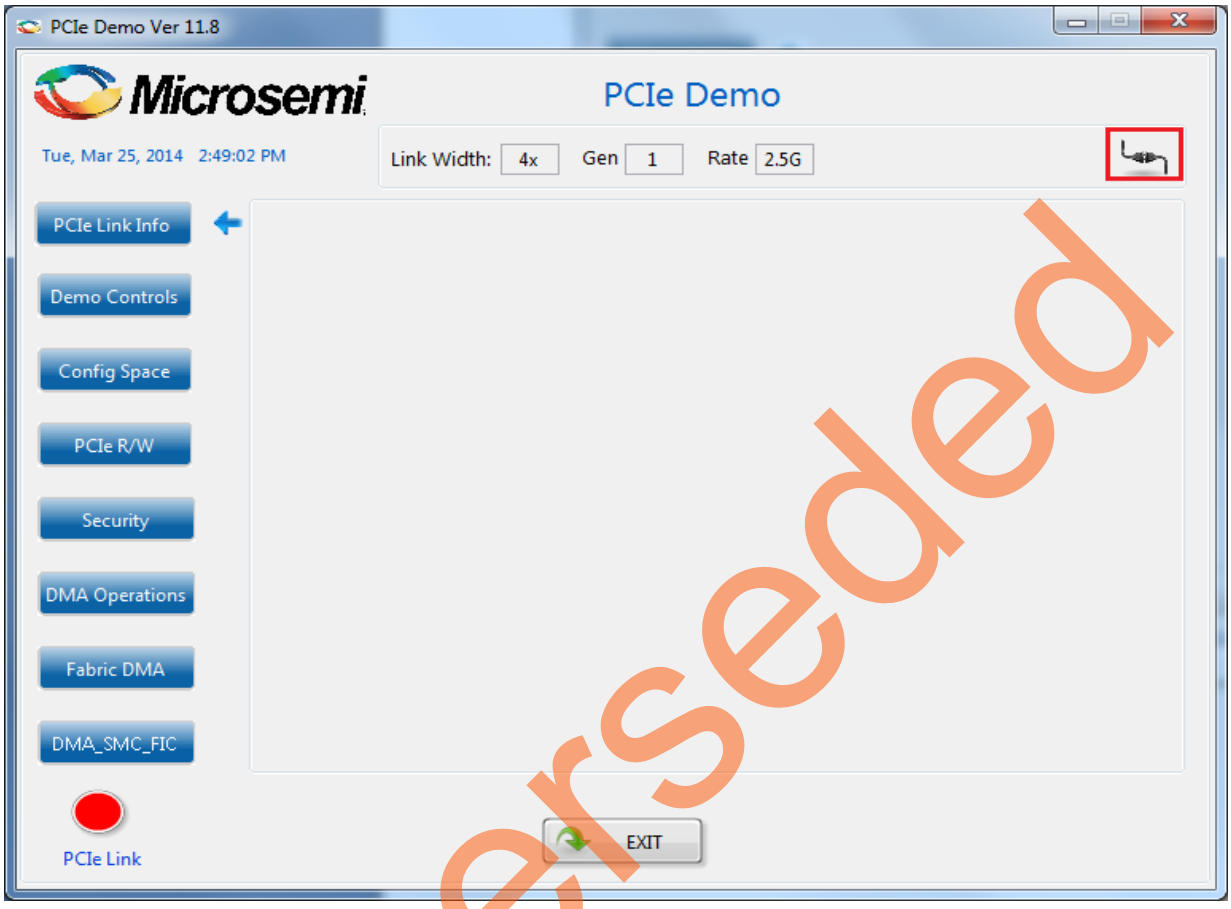

Figure 18 • **PCIe Demo GUI**

3. Click **Connect** at the top-right corner of the GUI. The messages are displayed on the GUI as shown in Figure 19.

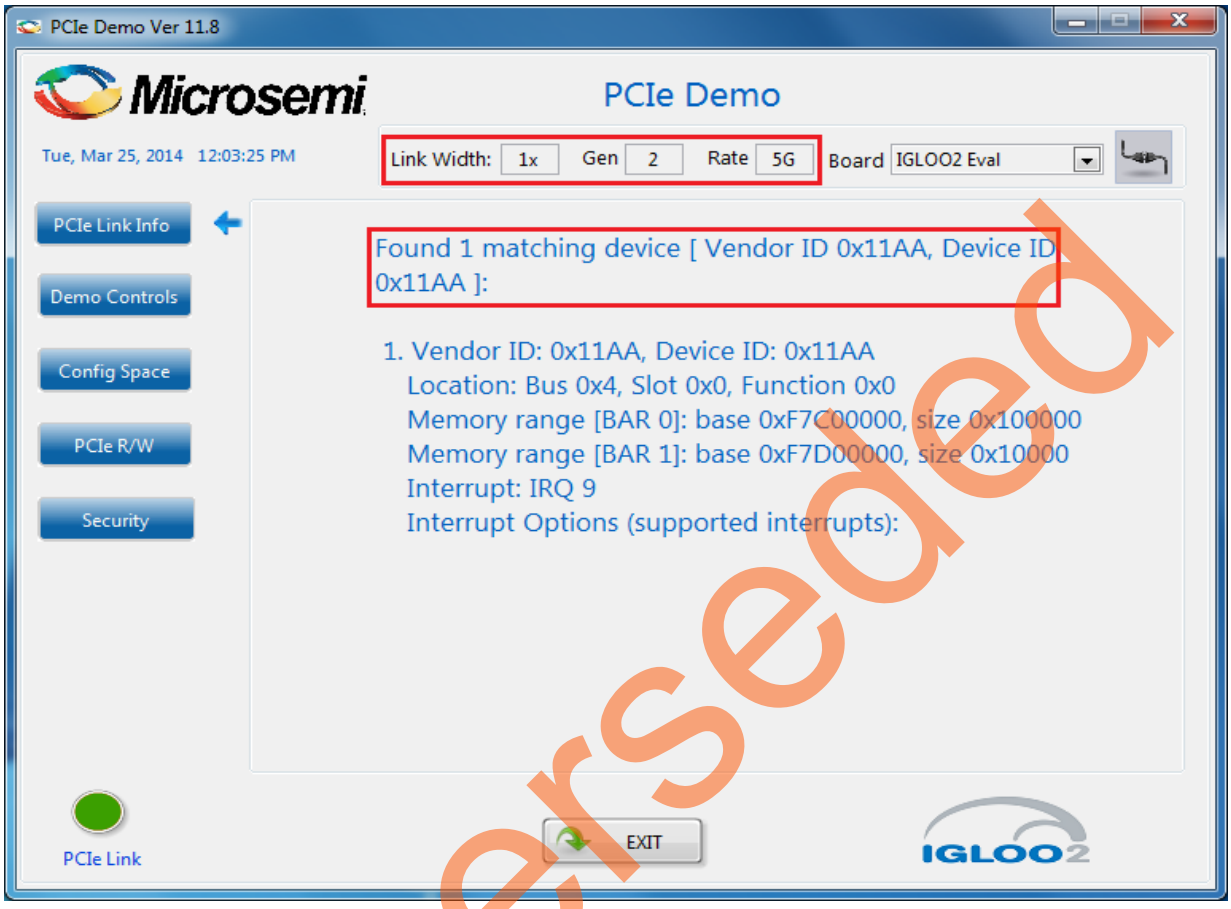

***Figure 19* • Version Information**

Note: If the Host PC does not support GEN2 slot, then this design will run at GEN1 speed.

4. Clicking **Demo Controls** in the GUI displays the LEDs options and DIP switch status as shown in Figure 20.

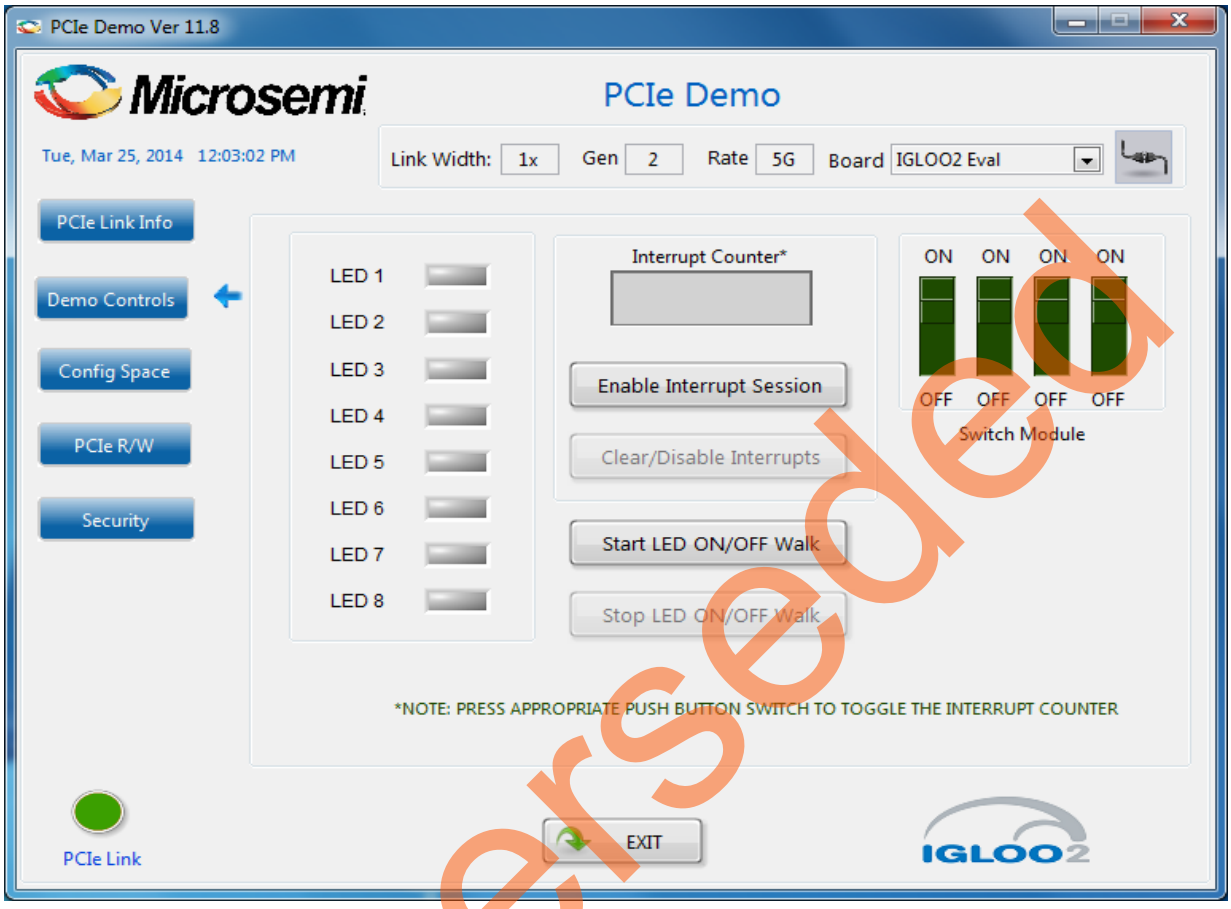

***Figure 20* • Demo Controls**

5. Click LEDs on GUI to **ON/OFF** the LEDs on the IGLOO2 Evaluation Kit board.
6. Click **Start LED ON/OFF Walk** to blink the LEDs on IGLOO2 Evaluation Kit board.
7. Click **Stop LED ON/OFF Walk** to stop the LEDs blinking.
8. Change the DIP switch positions on the IGLOO2 Evaluation Kit board (**SW5**) and observe the similar position of switches in **GUI SWITCH MODULE**.
9. Click **Enable Interrupt Session** to enable the PCIe interrupt.

10. Press the push button **SW4** on the IGLOO2 Evaluation Kit board and observe interrupt count on the **Interrupt Counter** field in GUI as shown in Figure 21.

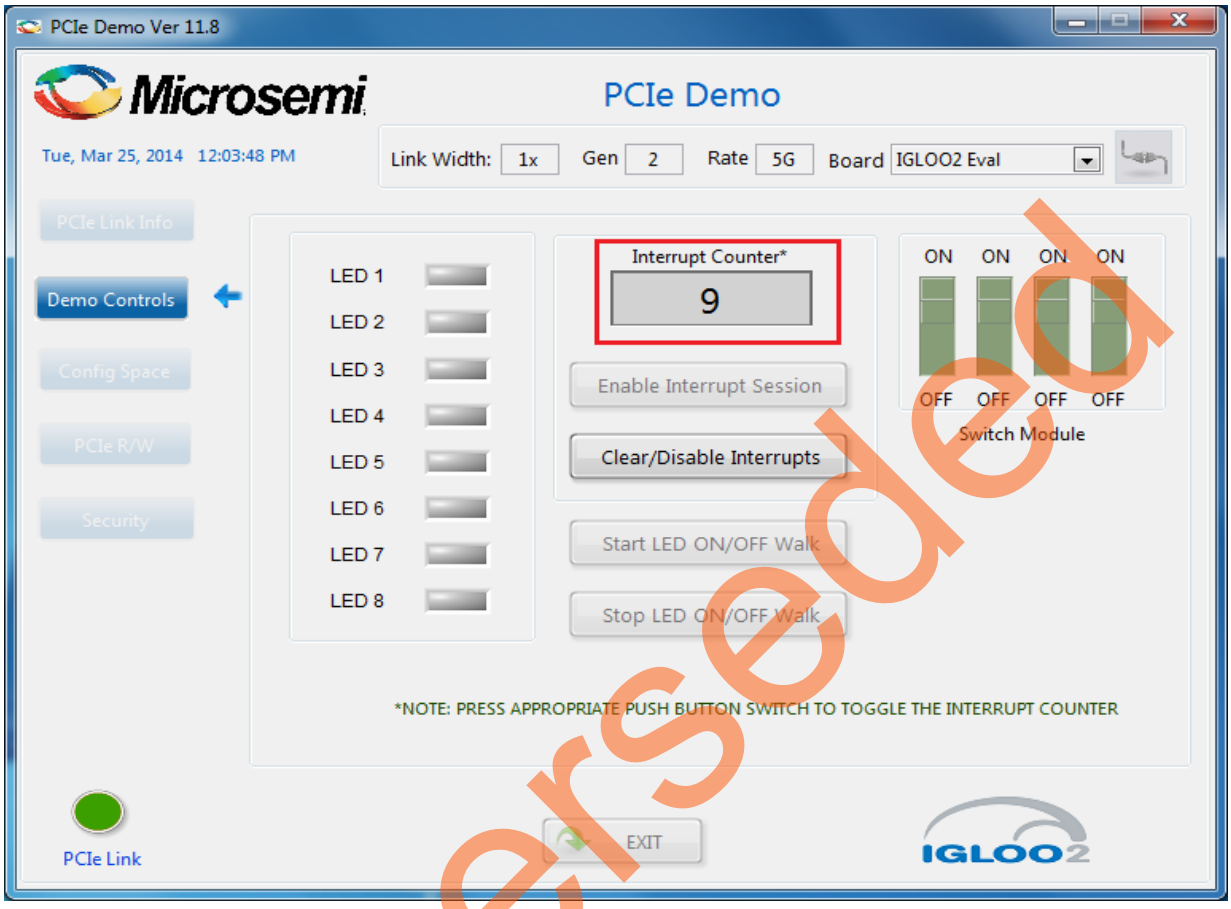

Figure 21 • **Interrupt Counter**

11. Click **Clear/Disable Interrupts** to clear and disable the PCIe interrupts.

12. Click **Config Space** to read details about the PCIe configuration space. Figure 22 shows the PCIe configuration space.

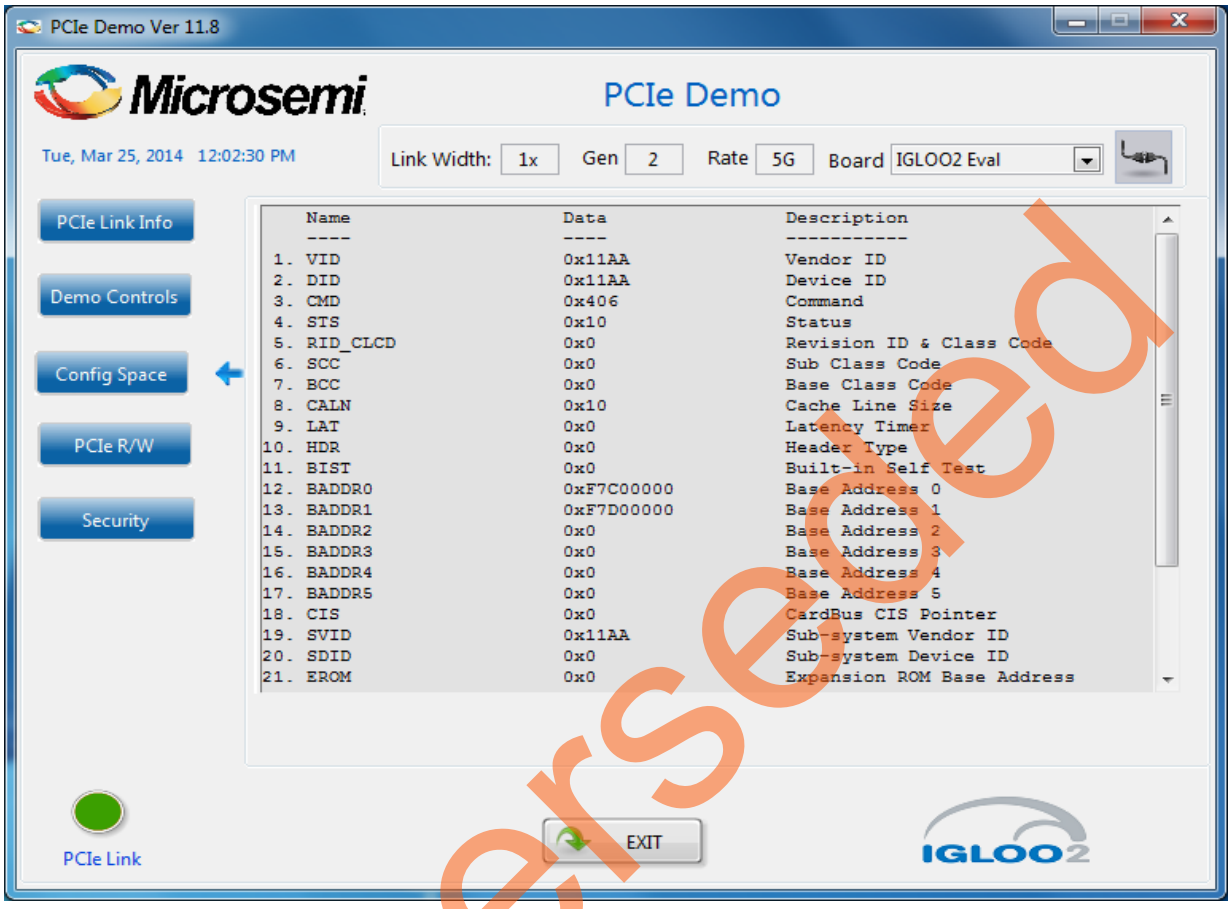

Figure 22 • **Configuration Space**

13. Click **PCIe R/W** to perform read and writes to LSRAM memory through **BAR1** space. Figure 23 shows the PCIe R/W window. Enter **Address** between 0x0000 to 0x7FFC.

14. Enter **Data**. The data field accepts a 32-bit hexadecimal value.

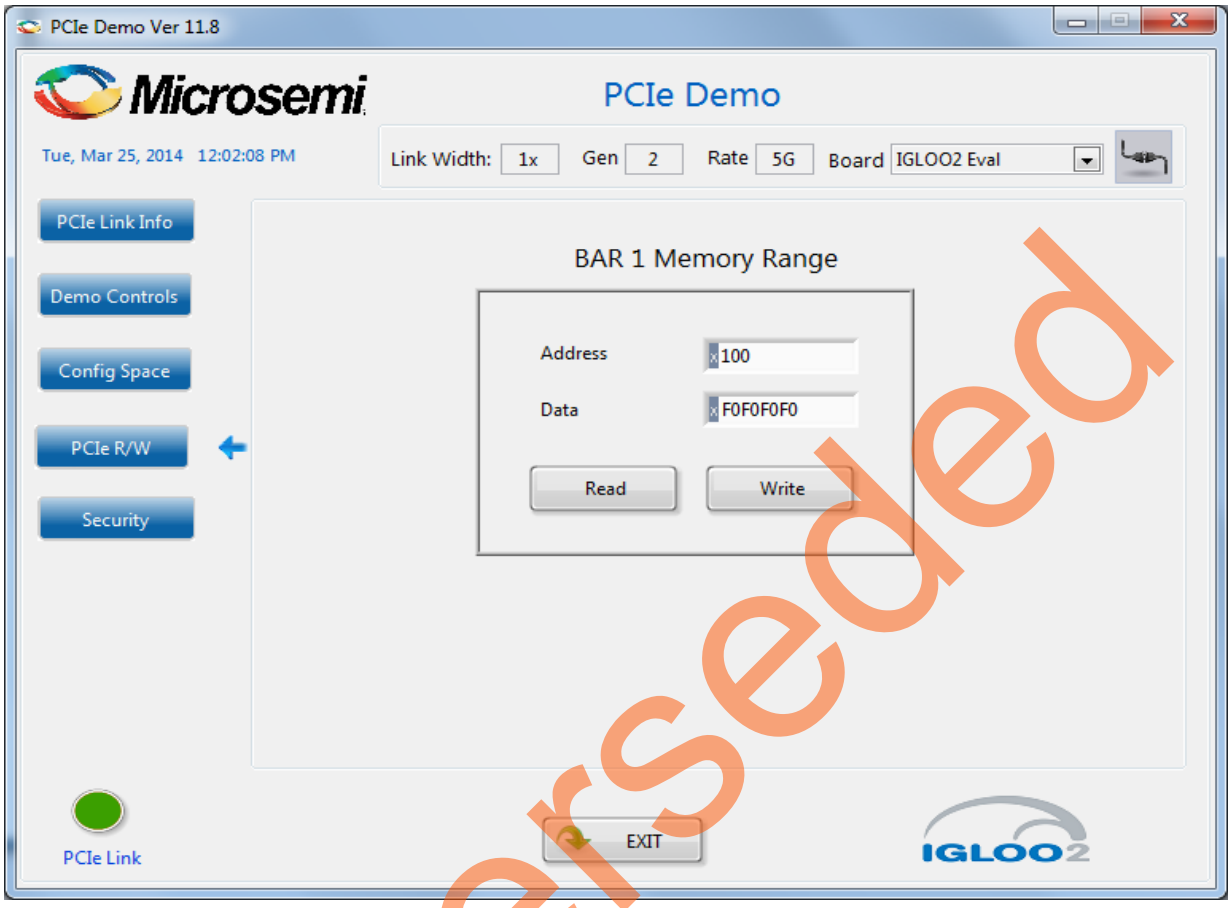

***Figure 23* • Perform Read and Write to LSRAM Using PCIe**

15. Click the **Security** tab and click **Read** to read the DSN. Figure 24 shows Security window.

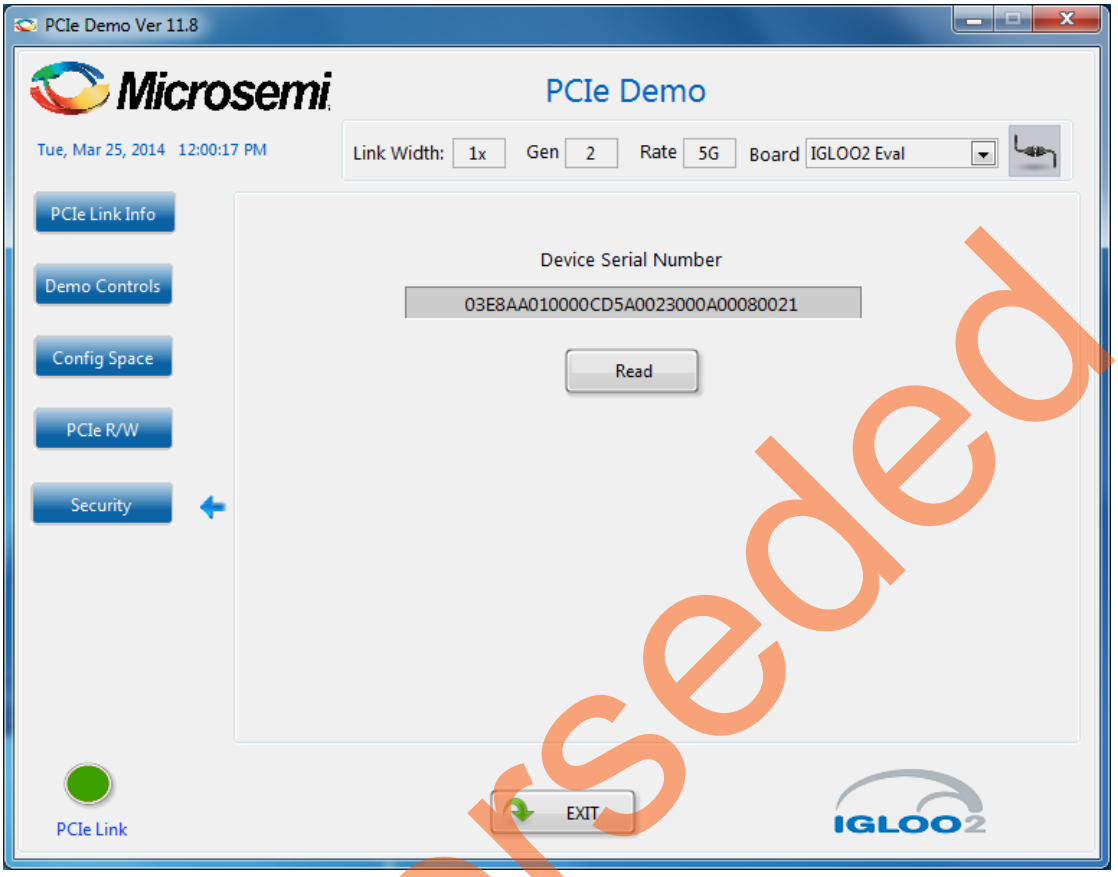

***Figure 24* • Reading Device Serial Number**

16. Click **Exit** to quit the demo.

Running the Demo Design on Linux

1. Switch **ON** the power supply switch on the IGLOO2 Evaluation Kit board.
2. Switch **ON** the Red Hat Linux Host PC.
3. Red Hat Linux Kernel detects the IGLOO2 PCIe end point as Actel Device.
4. On Linux Command Prompt Use `lspci` command to display the PCIe info.

```
# lspci
```

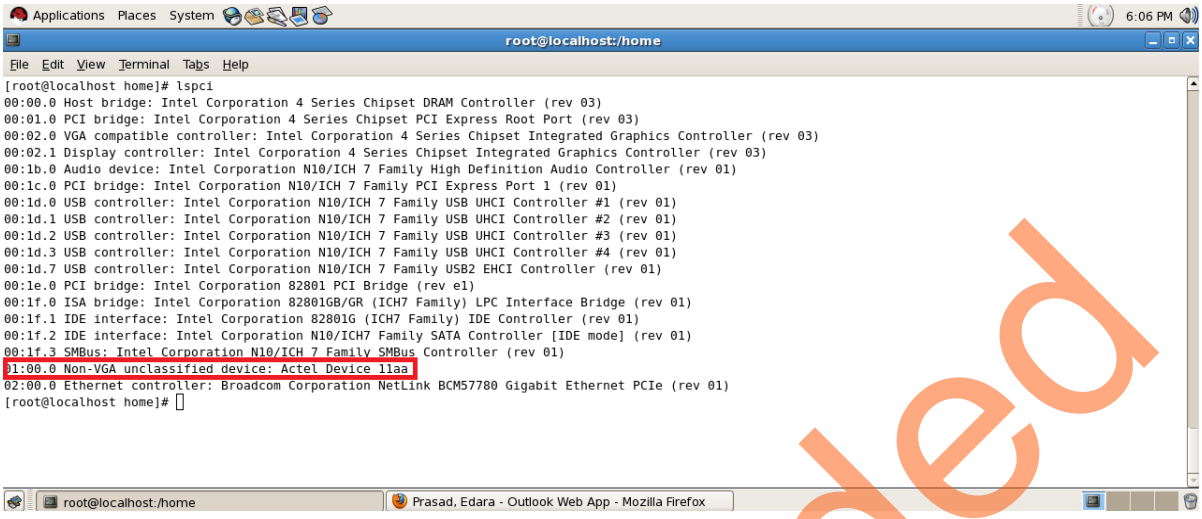

Figure 25 • **PCIe Device Detection**

Drivers Installation

Enter the following commands in the Linux command prompt to install the PCIe drivers:

1. Create the **igl2** directory under **home/**.

   ```
   # mkdir /home/igl2
   ```

2. Bring the *M2GL_PCIE_Control_Plane_DSN_DF/* design files folder under */home/igl2* directory, which contains the Linux PCIe device driver files and Linux PCIe application utility files.
3. Copy the Linux PCIe Device Driver file (`PCIe_Driver.zip`) from *M2GL_PCIE_Control_Plane_DSN_DF/* design files folder.

   ```
   # cp -rf
   /home/igl2/M2GL_PCIE_Control_Plane_DSN_DF/Linux_64bit/Drivers/PCIe_Driver.zip
   /home/igl2
   # unzip PCIe_Driver.zip
   ```

4. */home/igl2* directory must contain *PCIe_Driver/ inc/* folders.

   Execute `ls` command to display the contents of */home/igl2* directory.

   ```
   # ls
   ```

5. Change to *inc/* directory.

   ```
   #cd /home/igl2/inc
   ```

6. Edit the `board.h` file for IGLOO2 Evaluation Kit.

   ```
   #vi board.h
   #define IGL2
   #undef SF2
   ```

7. To save the selected file, perform `[:wq]`
8. To change the directory, use the following command:

   ```
   #cd /home/igl2/PCIe_Driver
   ```

9. To compile the Linux PCIe device driver code, execute make command on Linux Command Prompt.

   ```
   #make clean [To clean any *.o, *.ko files]
   #make
   ```

10. The kernel module, `pci_chr_drv_ctrlpln.ko` creates in the same directory.

11. To insert the Linux PCIe device driver as a module, execute `insmod` command on Linux Command Prompt.

    ```
    #insmod pci_chr_drv_ctrlpln.ko
    ```

Root Privileges are required to execute this command.

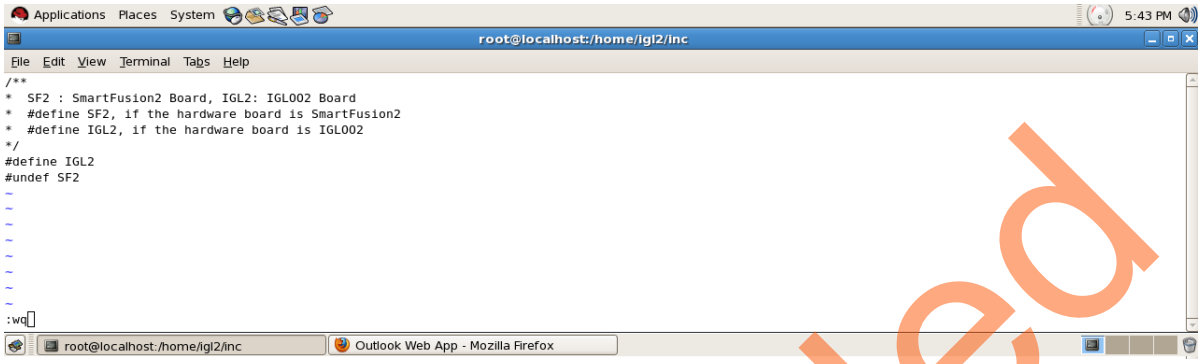

Figure 26 • **Edit board.h File**

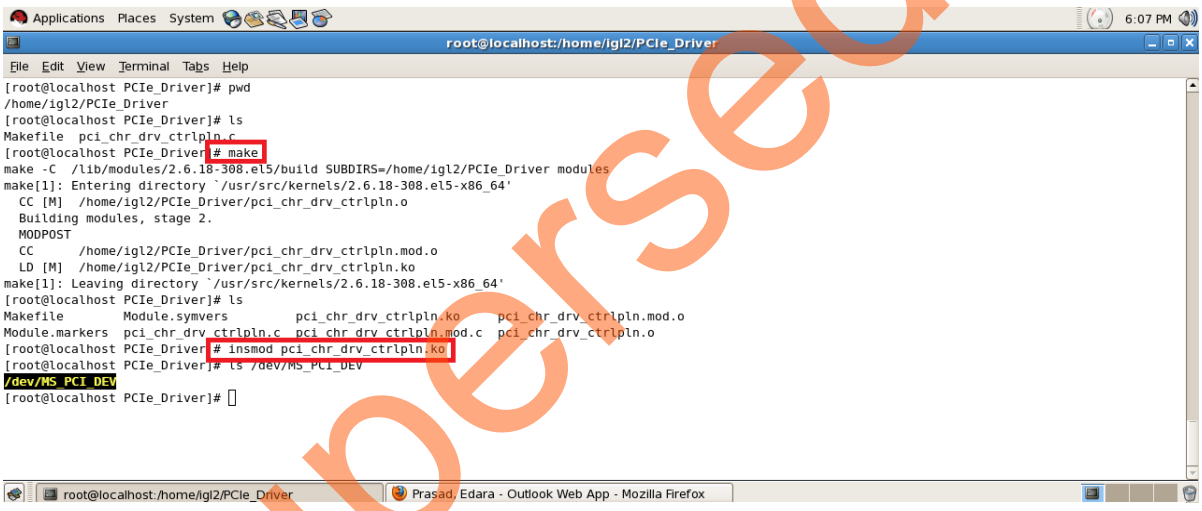

Figure 27 • **PCIe Device Driver Installation**

12. After successful Linux PCIe device driver installation, check `/dev/MS_PCI_DEV` got created by using the following Linux command:

    `#ls/dev/MS_PCI_DEV`

Note: `/dev/MS_PCI_DEV` interface is used to access the IGLOO2 PCIe end point from Linux user space.

Linux PCIe Application Compilation and PCIe Control Plane Utility Creation

1. Change to */home/igl2* directory.

   ```
   # cd /home/igl2
   ```

2. Copy the Linux PCIe application utility file (`PCIe_App.zip`) from *M2GL_PCIE_Control_Plane_DSN_DF/* design files folder.

   ```
   # cp -rf /home/igl2/M2GL_PCIE_Control_Plane_DSN_DF/Linux_64bit/UTIL/PCIe_App.zip
   /home/igl2
   # unzip PCIe_App.zip
   ```

3. */home/igl2* directory must contain *PCIe_App/* folder along with `led_blink.sh` and `pcie_config.sh` scripts. Execute `ls` command to display the contents in */home/igl2* directory.

   ```
   # ls
   ```

4. Compile the Linux user space application `pcie_appln_ctrlpln.c` in /home/igl2/PCIe_App folder by using gcc command.

   ```
   # cd /home/igl2/PCIe_App
   # gcc -o pcie_ctrlplane pcie_appln_ctrlpln.c
   ```

   After successful compilation, Linux PCIe application utility `pcie_ctrlplane` creates in the same directory.

5. On Linux Command Prompt, run the `pcie_ctrlplane` utility as:

   ```
   #./pcie_ctrlplane
   ```

   Help menu displays as shown in Figure 28.

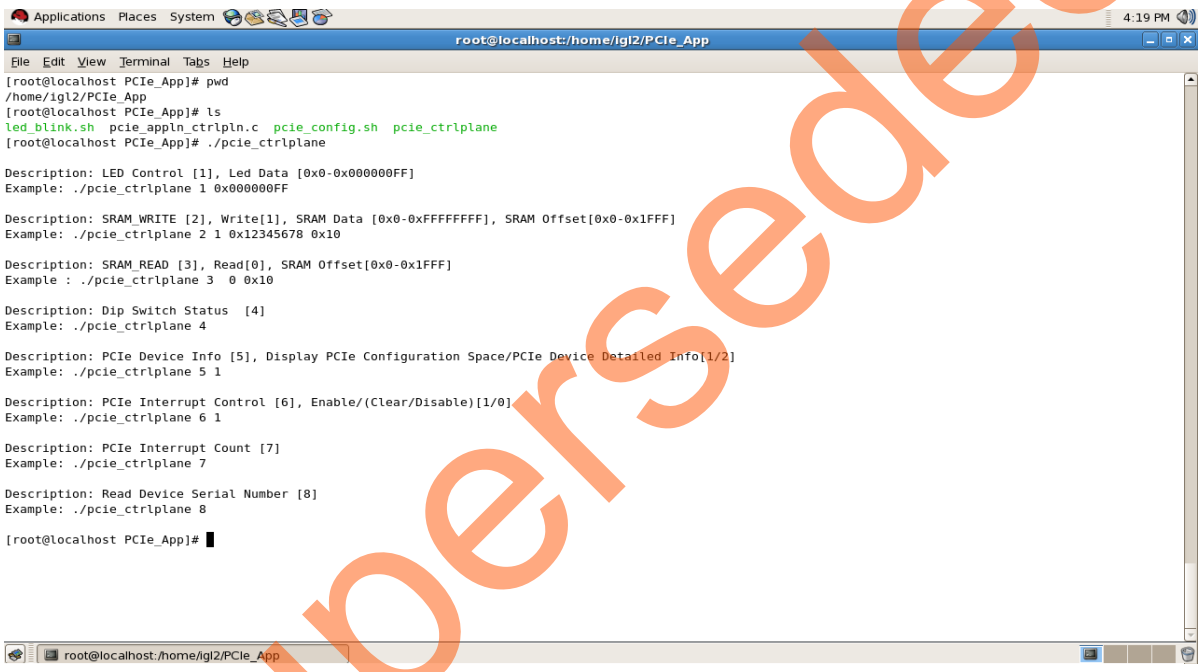

Figure 28 • **Linux PCIe Application Utility**

Execution of Linux PCIe Control Plane Features

LED Control

LED1 to LED8 is controlled by writing data to IGLOO2 LED control registers.

```
#./pcie_ctrlplane 1 0x000000FF [LED OFF]
#./pcie_ctrlplane 1 0x00000000 [LED ON]
```

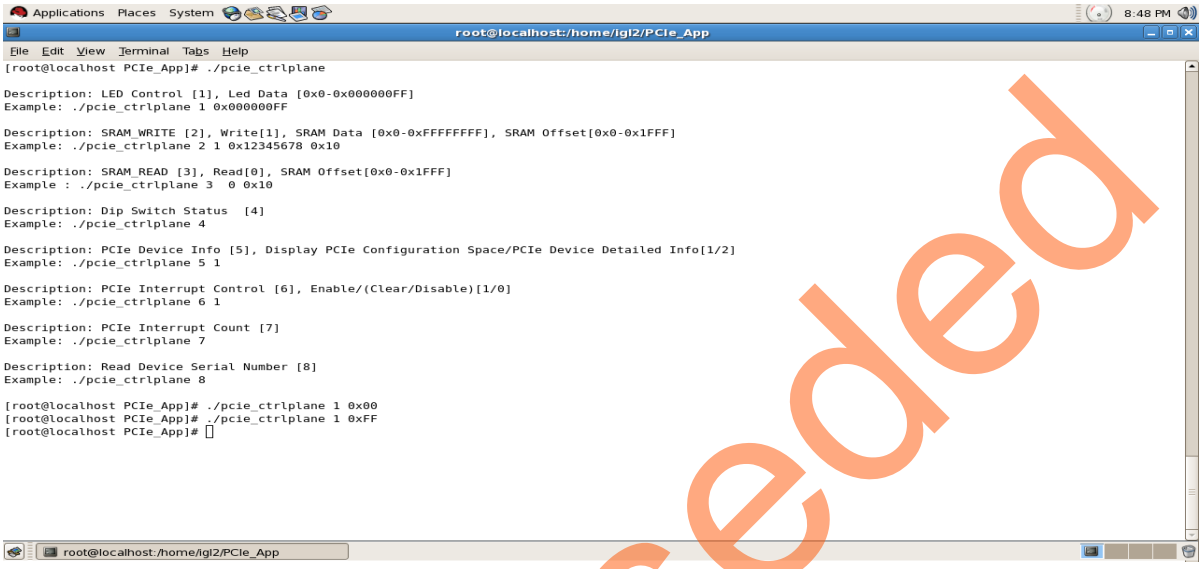

Figure 29 • **Linux Command - LED Control**

`led_blink.sh`, contains the shell script code to perform LED Walk ON where as `Ctrl+C` kills the shell script and LED Walk turns OFF.

```
#sh led_blink.sh
```

Run the led_blink.sh shell script using `sh` command.

SRAM Read/Write

32 KB SRAM is accessible for IGLOO2 Evaluation Kit.

```
#./pcie_ctrlplane 2 1 0xFF00FF00 0x1000 [SRAM WRITE]

#./pcie_ctrlplane 3 0 0x1000 [SRAM READ]
```

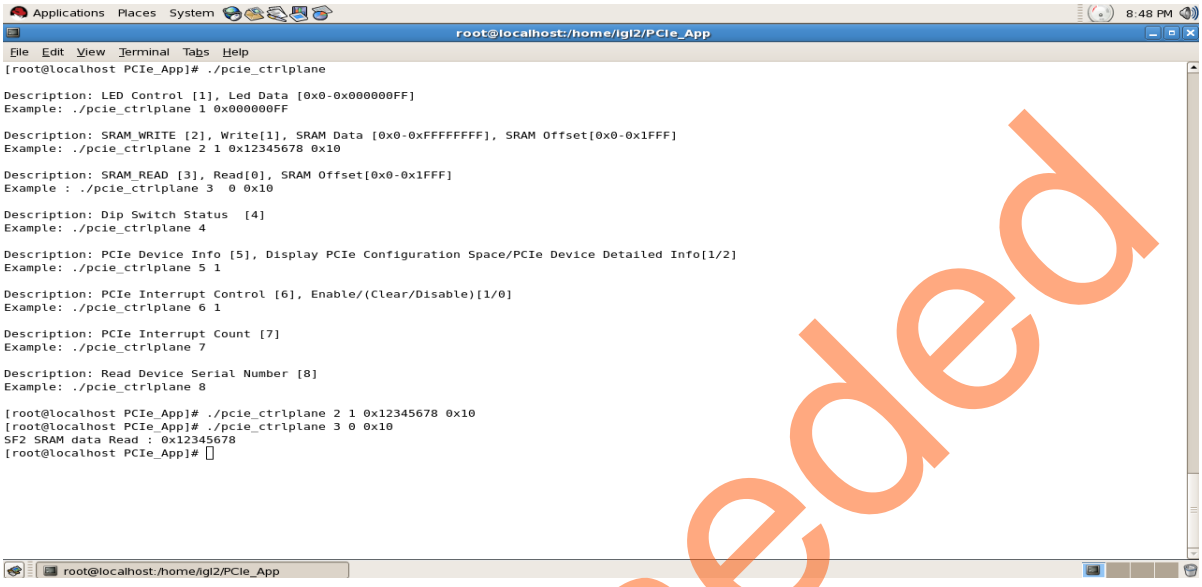

Figure 30 • **Linux Command - SRAM Read/Write**

DIP Switch Status

Dip switch on IGLOO2 Evaluation Kit board consists of 4 electric switches to hold the device configurations. Linux PCIe utility reads the corresponding switches (ON/OFF) state.

```
#./pcie_ctrlplane 4 [DIP Switch Status]
```

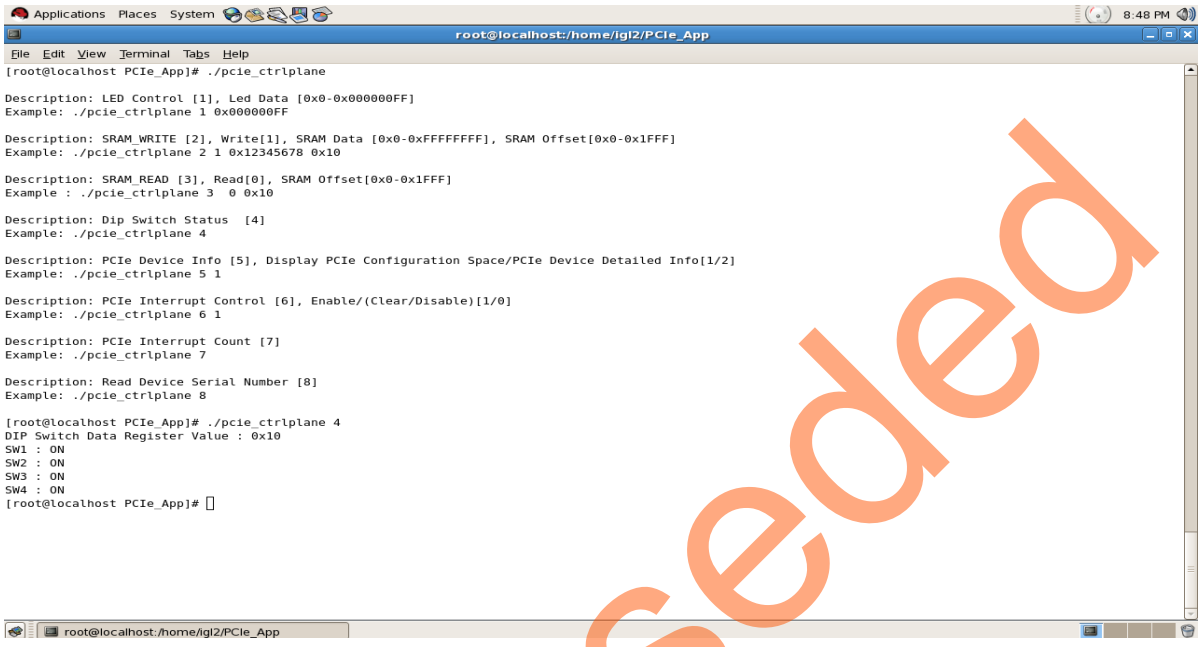

Figure 31 • **Linux Command - DIP Switch**

PCIe Configuration Space Display

PCIe Configuration Space contains the PCIe device data such as Vendor ID, Device ID, Base Address 0.

Note: Root Privileges are required to execute this command.

```
#./pcie_ctrlplane 5 1 [Read PCIe Configuration Space]
```

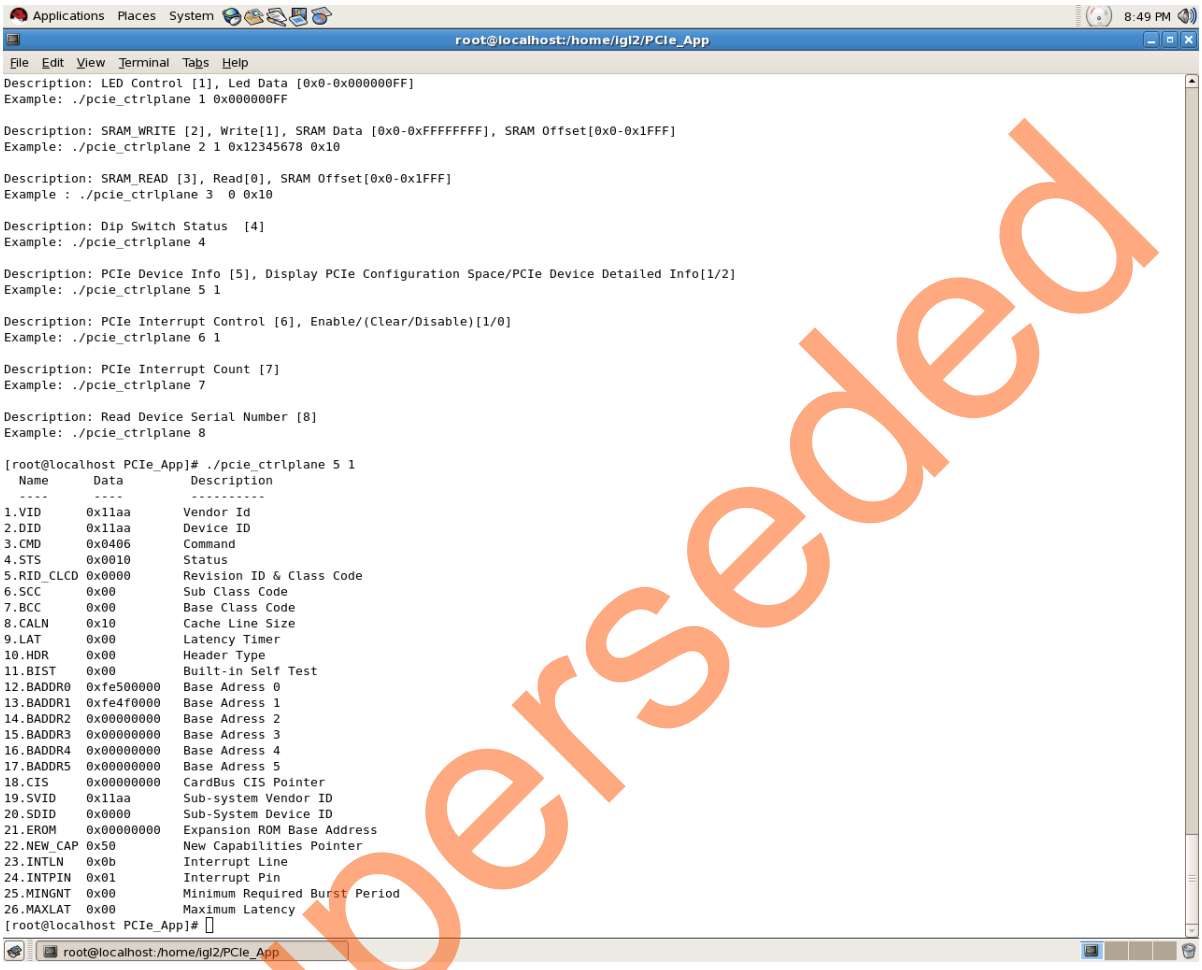

Figure 32 • **Linux Command - PCIe Configuration Space Display**

PCIe Link Speed and Width

Root Privileges are required to execute this command.

```
#./pcie_ctrlplane 5 2 [Read PCIe Link Speed and Link Width]
```

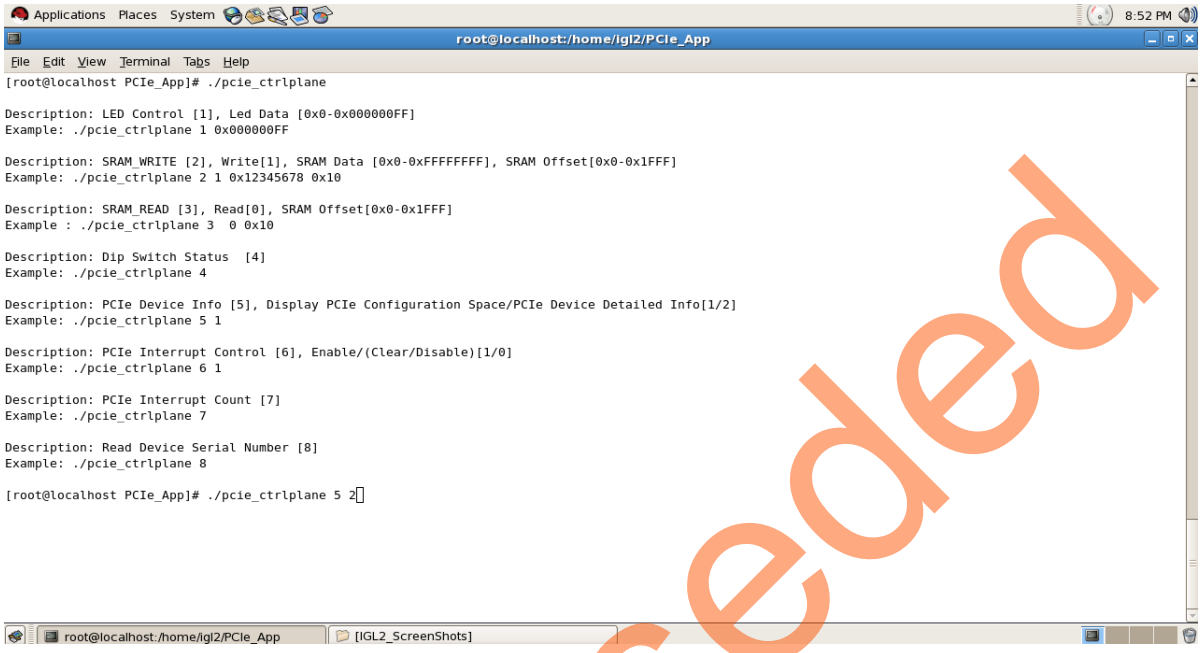

Figure 33 • **Linux Command - PCIe Link Speed and Width**

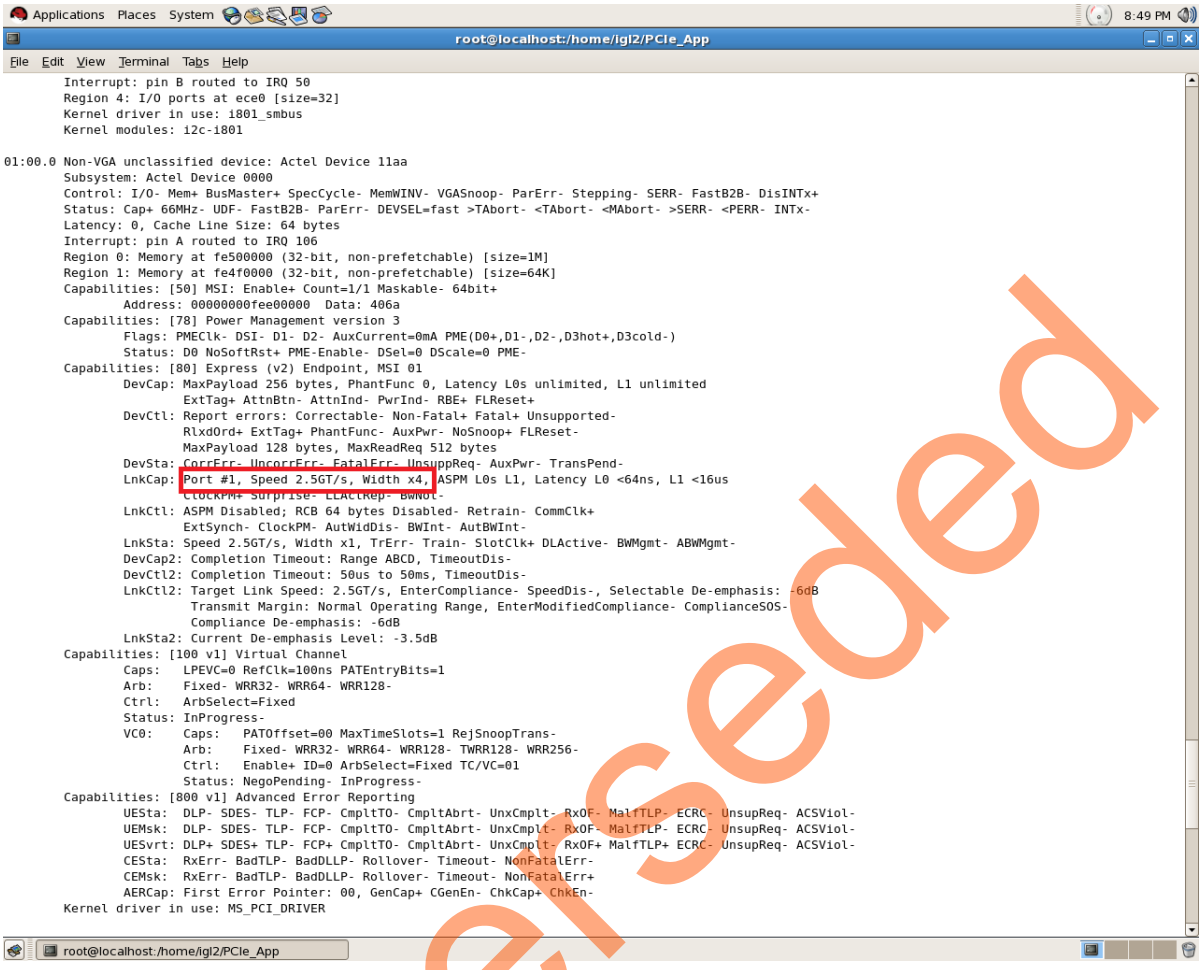

Figure 34 • **Linux Command - PCIe Link Speed and Width**

PCIe Interrupt Control (Enable/Disable) and Interrupt Counter

IGLOO2 Evaluation Kit enable/disable the MSI interrupts by writing data to its PCIe configuration space. Interrupt counter holds the number of MSI interrupts got triggered by pressing the **SW4** push button.

```
#. /pcie_ctrlplane 6 0 [Disable Interrupts]
#. /pcie_ctrlplane 6 1 [Enable Interrupts]
#. /pcie_ctrlplane 7 [Interrupt Counter Value]
```

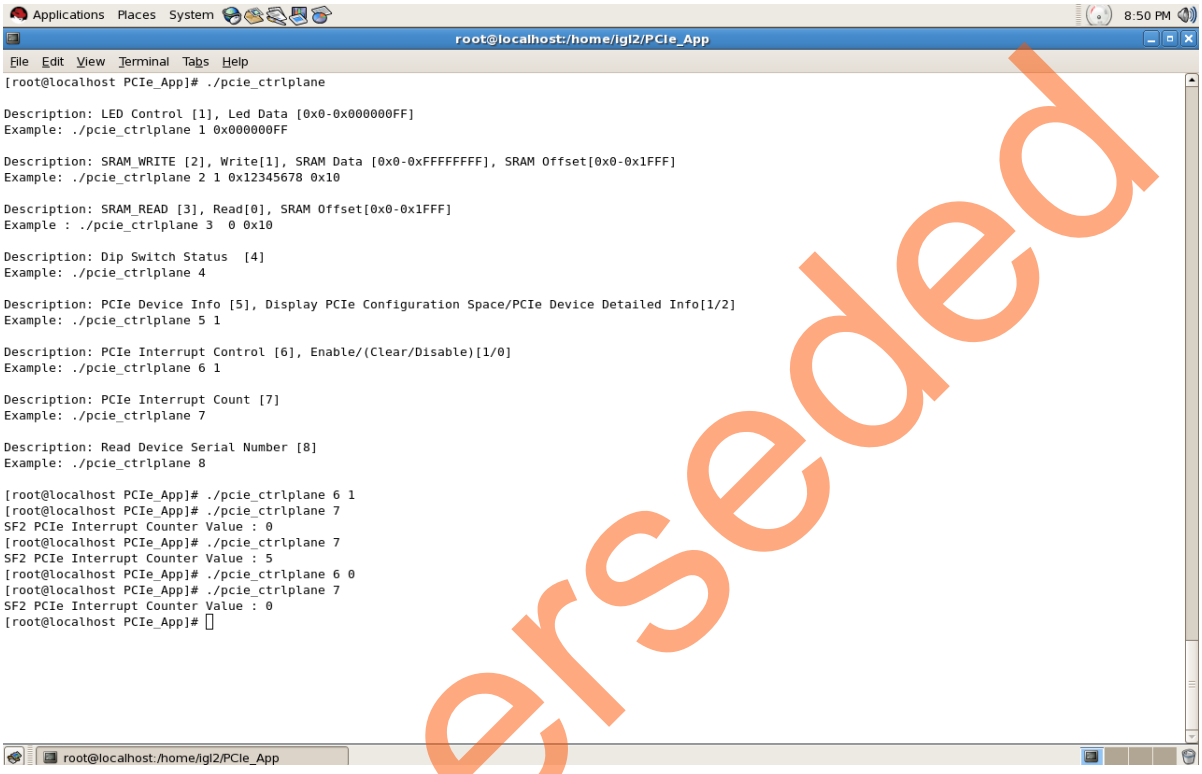

Figure 35 • **Linux Command - PCIe Interrupt Control**

Read Device Serial Number

IGLOO2 Evaluation Kit device serial number must be read by using the Linux PCIe application utility command.

```
#. /pcie_ctrlplane 8 [Read Device Serial Number]
```

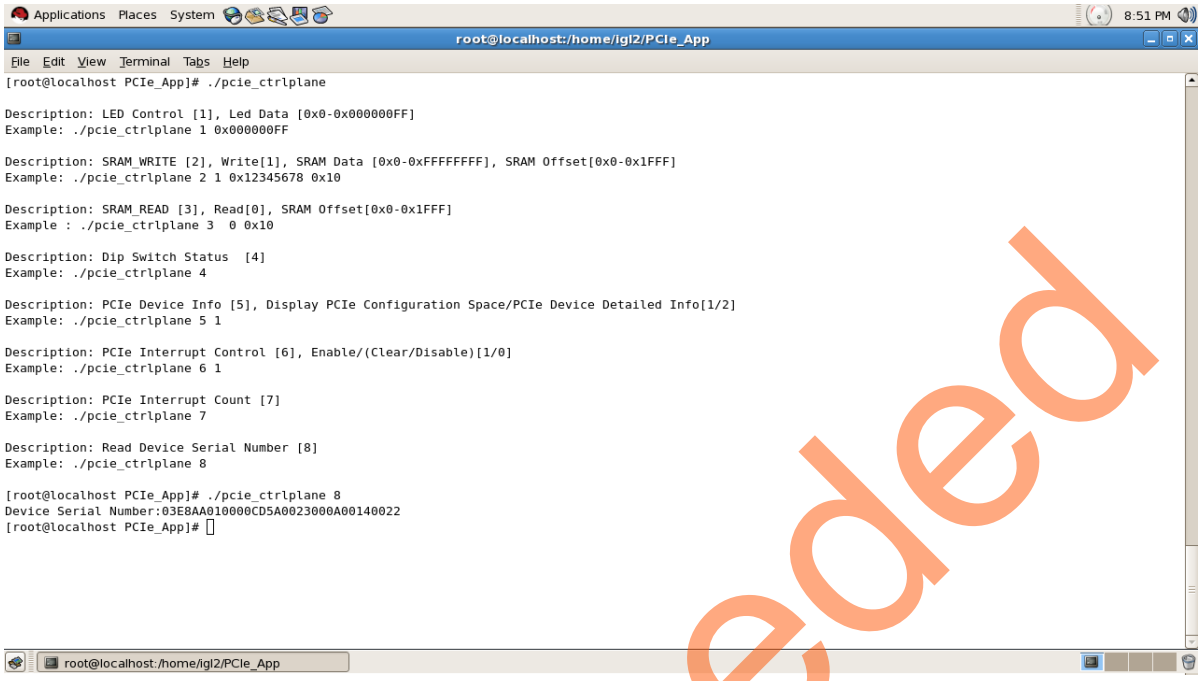

Figure 36 • **Linux Command - Read Device Serial Number**

Conclusion

This demo describes how to access the PCIe EP and display the device serial number feature of IGLOO2 by implementing a low bandwidth control plane design with BFM simulation. This demo provides a GUI for easy control of PCIe EP device through Jungo drivers for windows platform. This demo also provides a Linux PCIe application for easy control of PCIe EP device through Linux PCIe Device Driver.

Appendix 1: IGLOO2 Evaluation Kit Board

Figure 1 shows IGLOO2 Evaluation Kit board.

Figure 1 • **IGLOO2 Evaluation Kit Board**

Appendix 2: IGLOO2 Evaluation Kit Board Setup for Laptop

Figure 1 shows how to line up the IGLOO2 Evaluation Kit PCIe connector with the adapter card slot.

***Figure 1* • Lining up the IGLOO2 Evaluation Kit Board**

Note: The Notch (highlighted in red) does not go into the adapter card.

Figure 2 shows IGLOO2 Evaluation Kit PCIe connector inserted into the PCIe adapter card slot.

***Figure 2* • Inserting the IGLOO2 Evaluation Kit PCIe Connector**

Figure 3 shows the PCIe adapter card and the IGLOO2 Evaluation Kit connected to the laptop.

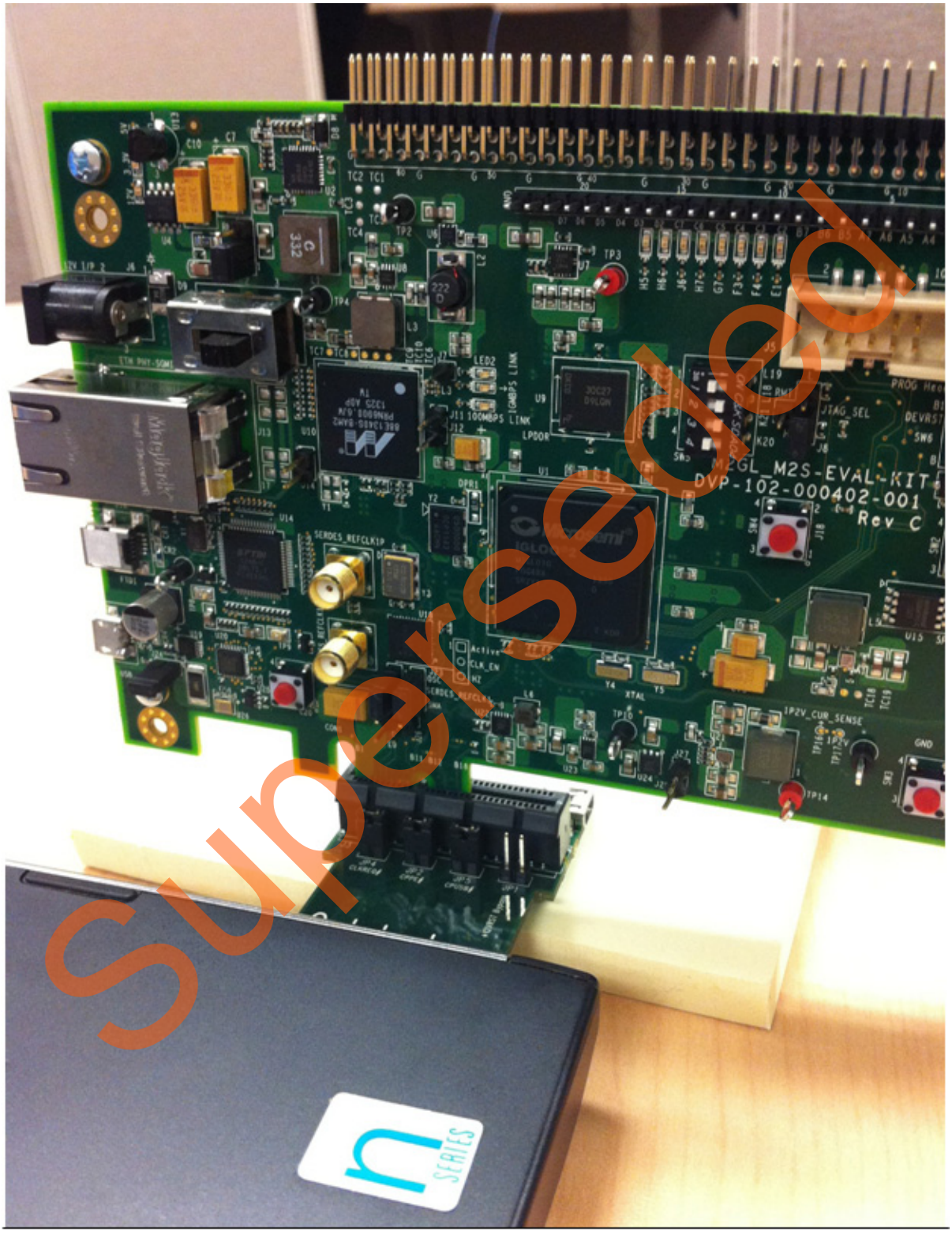

***Figure 3* • IGLOO2 Evaluation Kit Connected to the Laptop**

A – List of Changes

The following table lists critical changes that were made in each revision of the chapter in the demo guide.

Date	Changes	Page
Revision 3 (August 2014)	Updated the design files links.	NA
Revision 2 (July 2014)	Updated the document for Libero v11.4 software release (SAR 59586).	NA
Revision 1 (June 2014)	Initial release.	NA

B – Product Support

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From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (www.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

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You can browse a variety of technical and non-technical information on the SoC home page, at www.microsemi.com/soc.

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