SmartFusion2 M2S090(T,TS) and M2S150 (T,TS) Devices, Errata

v2.0 March 2015

This Errata sheet contains information about known Errata specific to the SmartFusion®2 M2S090(T,TS) and M2S150(T,TS) device families listed inTable 2 and provides available fixes and solutions.

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Table 1: **Revision History**

Date	Version	Changes
March 2015	2.0	Added M2S150 device. Updated Table 3: Summary of SmartFusion2 M2S090(T,TS) and M2S150(T,TS) Device Errata. Updated Errata descriptions based on fixes in new revisions of device. Added programming tables to separate different revisions of devices. Added item 11. Added item 12. Added item 13.
October 2014	1.2	Removed M2S090 Die Rev 1 devices. Added item 5.
September 2014	1.1	Added item 4.
July 2014	1.0	First revision

Table 2: **Device Status**

Silicon Devices	Revisions	Device Status
M2S090	Commercial/Industrial	Production
M2S150	Commercial/Industrial	Production

Errata for SmartFusion2 M2S090(T,TS) and M2S150(T,TS) Devices

Table 3 lists the specific device Errata and the affected SmartFusion2 M2S090 and M2S150 devices. Refer to the Marking Specification Details in the *SmartFusion2 SoC FPGAs Data Security Devices Product Brief* for this Die revision part marking specification.

Table 3: **Summary of SmartFusion2 M2S090(T,TS) and M2S150(T,TS) Device Errata**

No.	Errata	Silicon Revision(s) Affected							Software Errata
		M2S090(T,TS)				M2S150(T,TS)			
		Rev0	Rev1	Rev2	Rev3	Rev0	Rev1	Rev2	
1.	Power up digest is not supported	X				X			
2.	Updating eNVM from the MSS or the FPGA fabric requires changes to the NV_FREQRNG register	X	X	X		X			
3.	SYSCTRL_RESET_STATUS macro is not supported	X				X	X	X	
4.	Zeroization is not supported at this time.	X	X	X		X			
5.	Concurrent access of Cortex-M3 I-busses and D-busses are not allowed								X
6.	ECC Point-Multiplication Service and ECC Point-Addition System Service are not supported	X				X			
7.	The system controller RC oscillator runs at 25Mhz after a programming recovery operation	N/A	X	X	X	N/A			
8.	Programming M2S150 and M2S090 Silicon requires Cortex-M3 firmware code	X				X			
9.	Programming of the FPGA fabric can occur only at room temperature	X				X			
10.	Programming of the eNVM blocks needs to occur independently of the fabric	X				X			
11.	PCIe Hot Reset support requires a soft reset solution	X	X	X	X	X	X	X	
12.	Executing SRAM-PUF services fails while the Cortex-M3 code is executed from eNVM_1	X	X	X	X	X	X	X	
13.	After the successful completion of 2-step IAP or CM3 ISP, user design/logic cannot access the fabric SRAM (LSRAM and uRAM) blocks	X	X	X	X	X	X	X	

Notes:

- *An "X" means the errata exists for that particular device and revision number.*
- *A blank box means the errata does not exist for that particular device and revision number.*
- *N/A (Not Applicable) means the Programming Recovery mode is not available in this revision.*
- *Software Errata can be avoided by using Libero v11.4 SP1 or newer.*

Look at the new pin assignment and make sure that your board follows the new pin assignment. Contact Microsemi® SoC technical support if you have additional questions. To order a specific die, contact your local Microsemi sales office.

Errata Descriptions and Solutions

1. Power up digest is not supported

Workaround:

Use NVM Data Integrity Check System service after the device is powered up and then check the data.

2. Updating eNVM from the MSS or the FPGA fabric requires changes to the NV_FREQRNG register

When updating the eNVM from the FPGA fabric, the NV_FREQRNG register must be changed from the default value 0x07 to 0x0F; eNVM reads are not affected.

3. SYSCTRL_RESET_STATUS macro is not supported

Updated information will be available in a future version of the Errata document for the M2S150 devices.

4. Zeroization is not supported at this time.

5. Concurrent access of Cortex-M3 I-busses and D-busses are not allowed

A concurrent access of the Cortex®-M3 I-Bus and D-Bus may result in an invalid value returned to the internal registers from the cache; when both accesses are sourced by the cache while using a version of Libero® earlier than 11.4 SP1. For more details, refer to the Cache Controller Chapter of the *SmartFusion2 Microcontroller Subsystem User Guide.*

6. ECC Point-Multiplication Service and ECC Point-Addition System Service are not supported

7. The system controller RC oscillator runs at 25Mhz after a programming recovery operation

After a Programming Recovery event, the system controller will be running at 25 MHz, normally the system controller powers up running at 50 MHz after a programming recovery event.

Workaround:

If operating the system controller at 50 MHz is important to your design contact technical support.

8. Programming M2S150 and M2S090 Silicon requires Cortex-M3 firmware code

The eNVM needs to contain valid Cortex-M3 code. By default, SmartFusion2 SoC FPGA parts are shipped with a default boot up program stored at the eNVM address 0x60000000. If this default program is no longer valid or overwritten by the user and there is no valid user boot code, the Cortex-M3 won't execute to a valid state. This leads to unexpected behavior including programming lockout condition.

Workaround:

The firmware code must be programmed into the eNVM prior to re-programming a commercial device. A "while(1)" statement will work. Refer to Knowledge Base (KB) *SmartFusion2: Managing Cortex-M3, while accessing MSS from fabric, when there is no default or valid boot code for Cortex-M3 to execute* for details.

9. Programming of the FPGA fabric can occur only at room temperature

10. Programming of the eNVM blocks needs to occur independently of the fabric

11. PCIe Hot Reset support requires a soft reset solution

On SmartFusion2 SoC FPGA devices, a PCIe® Hot Reset requires a soft FPGA logic reset scheme which clears the sticky bits of the PCI configuration space.

Workaround:

The application note *Implementing PCIe Reset Sequence in SmartFusion2 and IGLOO2 Devices –Libero SoC v11.5* describes the PCIe Hot Reset reset scheme. However, this reset scheme causes PCIe violations in some cases.

- For the M2S090T(S) devices there are no violations
- For the M2S150T(S) devices at Gen1 rates there are no violations
- For the M2S150T(S) devices at Gen2 rates there are two PCIe CV violations.
  - Test case 1: TD_1_7 (Advanced Error Reporting Capability)
  - Test case 2: TD_1_41 (LinkCap2Control2Status2 Reg).

12. Executing SRAM-PUF services fails while the Cortex-M3 code is executed from eNVM_1

In the SmartFusion2 M2S090/M2S150 devices, the System Controller does not release the eNVM1 access after execution of the following SRAM-PUF system services:

- Create User AC (Activation Code) service
- Delete User AC service
- Create User KC for an Intrinsic Key service
- Create User KC for an Extrinsic Key service
- Delete User KC service

  The above system services get executed successfully but the eNVM1 becomes inaccessible to Cortex-M3 and also to fabric master
- Any subsequent access to eNVM1 after this point where eNVM1 is locked by the System Controller results in a stall, and Power on Reset (POR) is required to remove the stall

Workaround:

Execute "Get Number of the Key Code(GET_NUMBER_OF_KC)" SRAM-PUF system services immediately after the above services.

- The additional GET_NUMBER_OF_KC services release the eNVM1 access from the System Controller
- The firmware code for running SRAM-PUF services workaround must be executed from eNVM0, eSRAM, or DDR memories only, as Cortex-M3 can’t get access to the eNVM1 during that time

13. After the successful completion of 2-step IAP or CM3 ISP, user design/logic cannot access the fabric SRAM (LSRAM and uRAM) blocks

Workaround:

The user application must execute System Reset as soon as the IAP/ISP system service is completed. Otherwise user write and read accesses to LSRAM/uRAM will not be possible. The System Reset can be generated with the use of the tamper macro (availably in the Libero SoC Catalog). Immediately after the IAP/ISP service, the user logic checks the LSRAM/uRAM access. If access is denied, the user logic sends the reset request/interrupt to the system controller via the tamper macro (by enabling the RESET Function in the tamper macro configuration window) and then the system controller executes the system level reset. For more information, refer to the *SmartFusion2 Programming User Guide.*

The following application notes have more information and design examples on how to implement the workaround:

- *SmartFusion2 SoC FPGA - In-System Programming Using USB OTG Controller Interface - Libero SoC v11.5 Demo Guide*
- *SmartFusion2 SoC FPGA - In-System Programming Using UART Interface Demo - Libero SoC v11.5 Demo Guide*
- *SmartFusion2 SoC FPGA In-Application Programming Using PCIe Interface – Libero SoC v11.5 Demo Guide*

Usage Guidelines for SmartFusion2 M2S090(T,TS) and M2S150(T,TS) Devices

1. Programming support

Note that there may be package dependencies that may not expose certain programming interfaces. Refer to the product briefs for the device/package specific features.

Table 5: **Revision 1 and 2 Devices**

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2 Step IAP	Programming Recovery	M3 ISP
Programming Interface	JTAG	SC_SPI	SPI_0	SPI_0	SPI_0	SPI_0	N/A
M2S090(T),(TS)	Yes	Yes	Yes	Yes	Yes	Yes*	Yes
M2S150(T),(TS)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
*Refer to Errata item 7.							

Table 4: **Revision 0 Devices**

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2 Step IAP	Programming Recovery	M3 ISP
Programming Interface	JTAG	SPI_SC	SPI_0	SPI_0	SPI_0	SPI_0	N/A
M2S090(T),(TS)	Yes	Yes	No	No	No	Yes*	Yes
M2S150(T),(TS)	Yes	Yes	No	No	No	No	Yes
*Refer to Errata item 7.							

Table 6: **Revision 3 Devices**

Programming Mode	JTAG	SPI Slave	Auto Programming	Auto Update	2 Step IAP	Programming Recovery	M3 ISP
Programming Interface	JTAG	SPI_SC	SPI_0	SPI_0	SPI_0	SPI_0	N/A
M2S090(T),(TS)	Yes	Yes	Yes	Yes	Yes	Yes*	Yes
*Refer to Errata item 7.							

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