IGLOO2 FPGA Low Standby Power - Libero SoC v11.4

Demo Guide

August 2014

Microsemi

Revision History

Date	Revision	Change
August 20, 2014	1	First release

Confidentiality Status

This document is a non-confidential.

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Preface

About this document

This demo is for IGLOO®2 field programmable gate array (FPGA) devices. It provides instructions on how to use the corresponding reference design.

Intended Audience

The following designers using the IGLOO2 devices:

- FPGA designers
- System-level designers

References

Microsemi Publications

- *IGLOO2 Power Calculator User Guide*
- *IGLOO2 FPGA Low Power Design User Guide*
- *IGLOO2 FPGA Fabric User Guide*

IGLOO2 FPGA Low Standby Power - Libero SoC v11.4

Introduction

Microsemi® IGLOO2 FPGAs are designed to meet the demand of low power FPGAs. IGLOO2 devices exhibit lower power consumption in static and dynamic modes. This demo guide demonstrates how to implement standby power mode on IGLOO2 devices using SmartDesign and measure the standby power. The design drives the LEDs on the IGLOO2 Evaluation Kit with a pattern based on the state of the switches SW1 and SW3, as shown in Table 1.

Table 1 • **LEDs Pattern**

LED E1, F4, F3, G7 Behavior	Standby Entry (SW1)	Standby Exit (SW3)
LEDs toggle	Released	Released
LEDs on	Depressed and Released	Released
LEDs toggle	Depressed and Released	Depressed

This demo guide describes the following:

- Creating a Libero® System-on-Chip (SoC) project.
- Implementing standby power mode on IGLOO2 devices using SmartDesign.
- Importing a PDC file, running layout and programming the IGLOO2 silicon.
- Measuring standby power using a standard Digital Voltmeter (DVM)/Multimeter.

Design Requirements

Table 2 lists the design requirements.

Table 2 • **Design Requirements**

Design Requirements	Description
Hardware Requirements	
IGLOO2 Evaluation Kit: • 12 V adapter • FlashPro4 programmer	Rev C or later
Desktop or Laptop	Windows 64-bit Operating System
Software Requirements	
Libero® System-on-Chip (SoC)	11.4
ModelSim	ME 10.3a
Synplify Pro	ME I-2013.09MSP1-1
FlashPro Programming Software	11.4

Demo Design

Introduction

The demo design files are available for download from the following path in the Microsemi website:

http://soc.microsemi.com/download/rsc/?f=IGL2_Standby_tutorial_11p4_DF

The demo design files include:

- Libero SoC project
- Constraint file
- Programming file
- Source files
- Readme file

Refer to the Readme.txt file provided in the design files for the complete directory structure.

The design consists of a 32 kHz External Main Crystal Oscillator, Fabric CCC (FCCC), Standby power control logic and Fabric logic block. Figure 1 shows the block diagram of the design.

The FCCC is configured to provide 100 MHz clock to the Fabric logic. It is also configured with PLL power-down enabled. The 32 kHz External Main Crystal Oscillator is the reference clock source for the FCCC. The Lock signal is used as a reset signal to the Fabric logic. The standby power control logic consists of a clocked S-R latch which powers down the PLL of FCCC. The Fabric logic consists of 421 stages 18-bit loadable up-counters, 604 stages of shift registers, and 11 stages LSRAM and Math blocks. It also consists of a LED Driver block which is connected to a set of light-emitting diodes (LEDs) to monitor the state of the fabric while entering and exiting standby power mode.

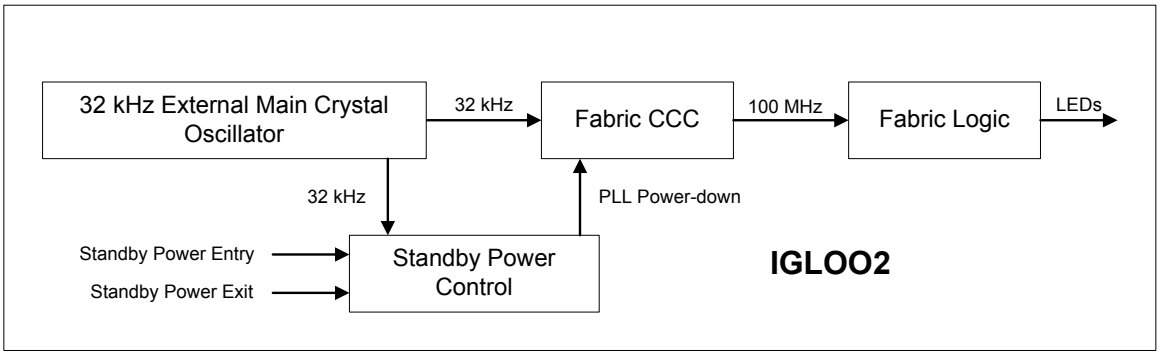


Figure 1 • **Design Block Diagram**

Extracting the Source Files

Extract *IGL2_Standby_tutorial_11p4_DF.zip* to extract the required lab files to the *<C:\ or D:\>Microsemi_prj* folder on the HDD of the PC. Confirm that a folder named *IGL2_Standby_tutorial* containing sub-folders named *Source_files* and *Constraints* are extracted.

Creating the Design

This section describes how to create the standby power mode enabled design using SmartDesign. Some source files are provided in the *Source_files* folder.

Launching Libero SoC

The following steps describe how to launch Libero SoC:

1. Click **Start > Programs > Microsemi Libero SoC v11.4 > Libero SoC v11.4,** or click on the shortcut icon on the PC. **Libero SoC Project Manager** window opens (see Figure 2).

Figure 2 • **Libero SoC Project Manager**

2. Create a new project by selecting **New** on the **Start Page** tab (highlighted in Figure 2), or by clicking **Project > New Project** from the Libero SoC menu. **New Project** dialog box opens (see Figure 3).
3. Enter the following information in the **New Project** dialog box:
   - Project Name: IGL2_Standby
   - Project Location: <C:\ or D:\>Microsemi_prj\IGL2_Standby_tutorial
   - Preferred HDL type: VHDL
   - Family: IGLOO2
   - Die: M2GL010T
   - Package: 484 FBGA
   - Speed: -1
   - Core Voltage (V): 1.2
   - Ramp rate: 100ms Minimum
   - Junction Temperature: COM
   - Core Voltage: COM
   - PLL Supply Voltage (V): 3.3
   - Use Design Tool: Un-checked (circled in Figure 3)

The PLL Analog Supply voltage can be either 2.5 V or 3.3 V. The voltage setting in the **New Project** dialog box must match with the PLL Analog supply voltage on the board to ensure that the PLL works

properly. The PLL Analog Supply voltage is connected to 3.3 V on the IGLOO2 Evaluation Kit. Therefore, the setting must be changed.

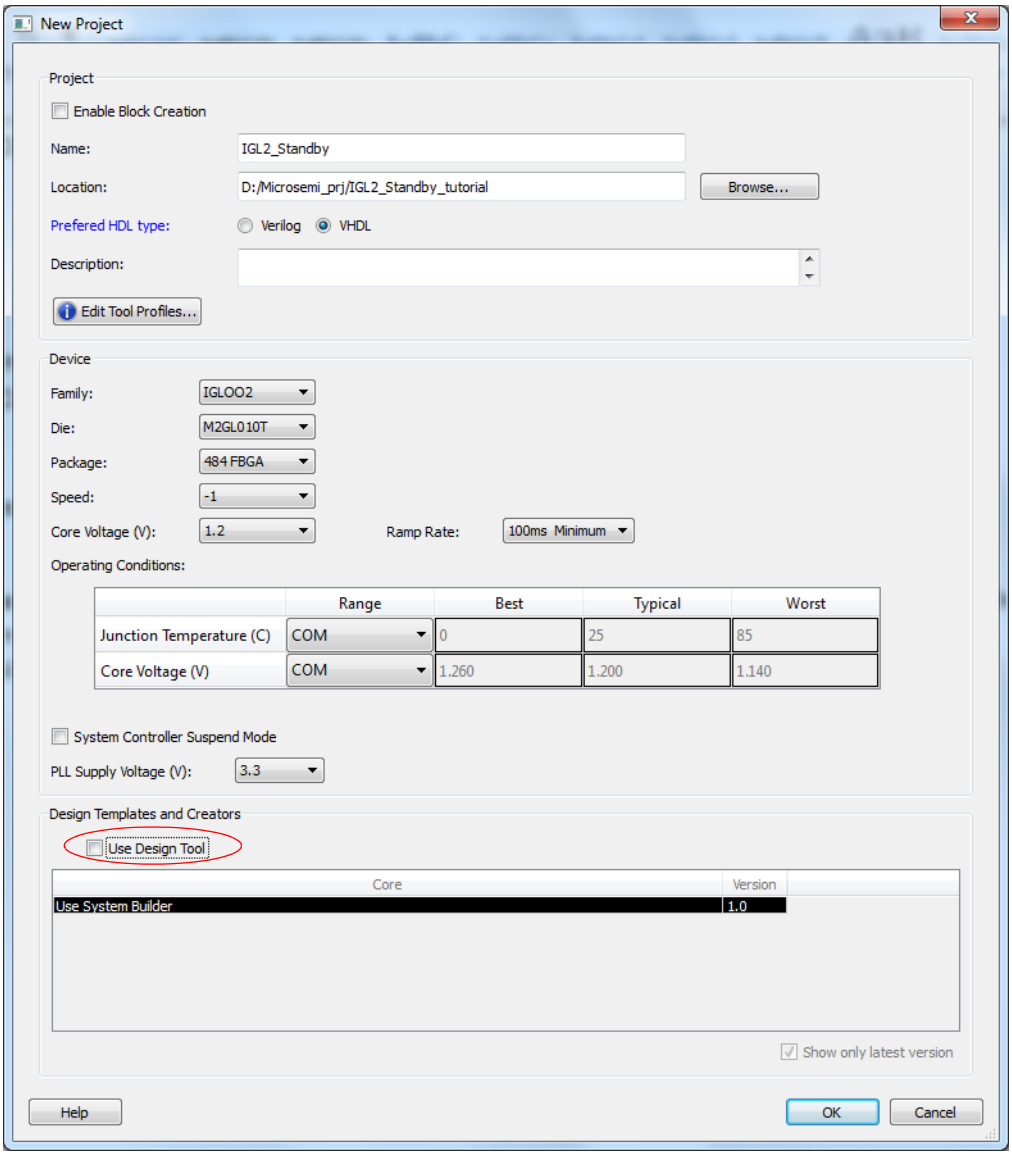


Figure 3 • **Libero SoC New Project Parameters**

4. Click **OK** and close the **New Project** dialog box.

5. Expand **Create Design** in the **Design Flow** tab as shown in Figure 4. Right-click **Create SmartDesign** and select **Run**.

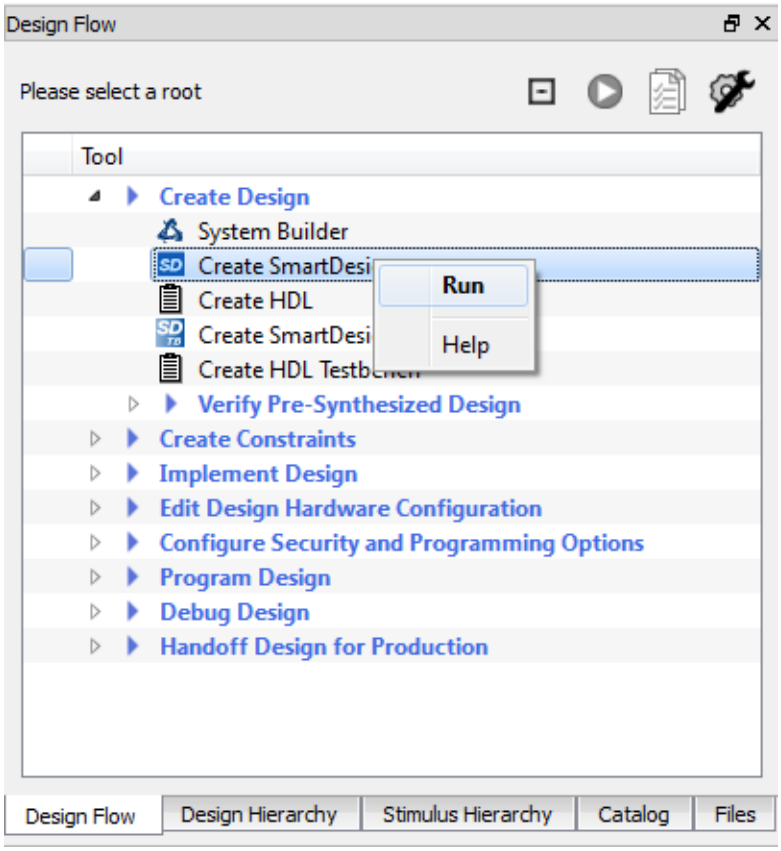


Figure 4 • **Creating SmartDesign**

6. Enter IGL2_Standby in the **Create New SmartDesign** dialog box and click **OK**. New SmartDesign canvas opens.

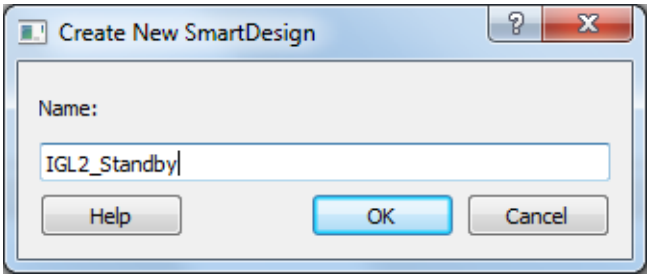


Figure 5 • **Entering SmartDesign Name**

7. This design uses a Fabric CCC to generate 100 MHz internal clock. The CCC reference clock is the 32 kHz external main crystal oscillator. Expand **Clock & Management** in the IP catalog.

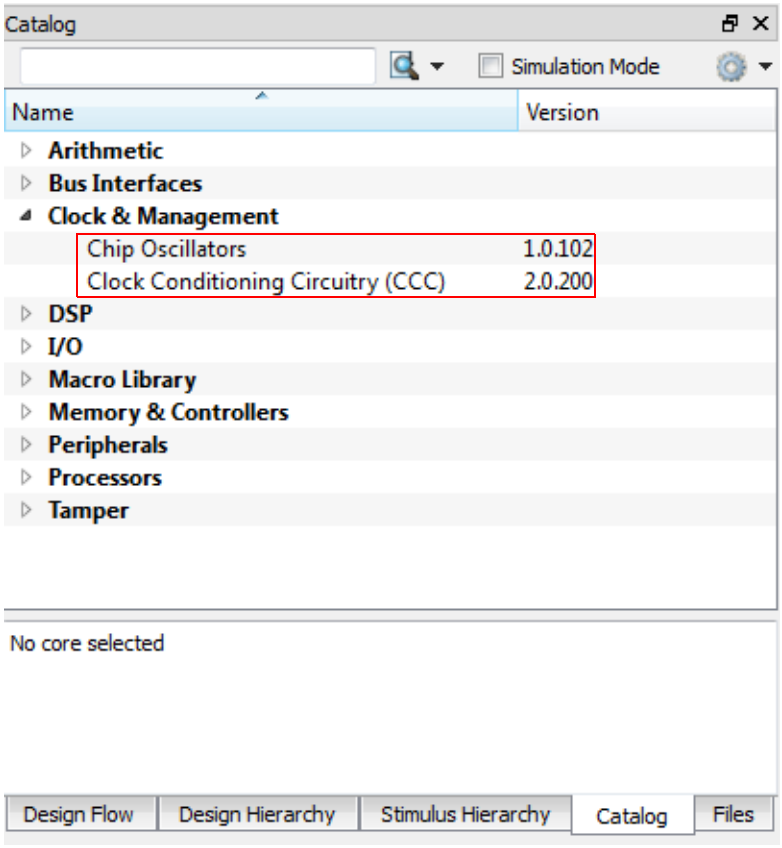


Figure 6 • **Clock & Management Category of Libero SoC IP Catalog**

8. Drag an instance of the Clock Conditioning Circuitry (CCC) v2.0.200 component into the SmartDesign canvas.
9. Double-click on the FCCC_0 component in the SmartDesign canvas and open the FAB CCC Configurator window as shown in Figure 6.
10. Click on **Basic** tab in the **FAB CCC Configurator** window (see Figure 6).
    Enter the following information:
    - Reference Clock Frequency: 0.032 MHz
    - Reference Clock: Select **Oscillators > Crystal Oscillator** from the pull-down menu
    - GL0: Checked; Frequency: 100 MHz

.

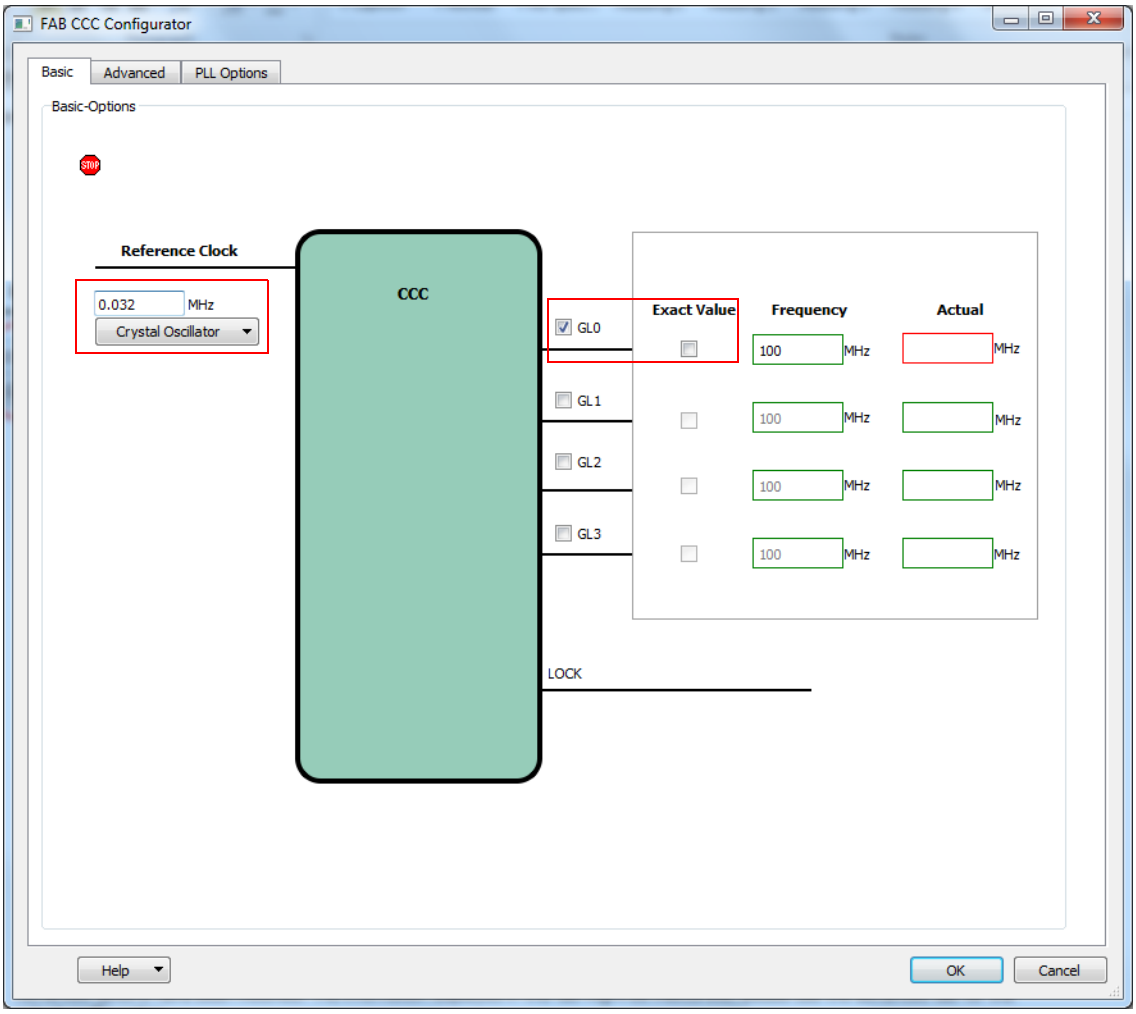


Figure 7 • **Configuring Fabric CCC**

11. Click on **Advanced** tab in the **FAB CCC Configurator** window and select **Internal > PLL Internal** from the pull-down menu as PLL feedback source, as shown in Figure 8.

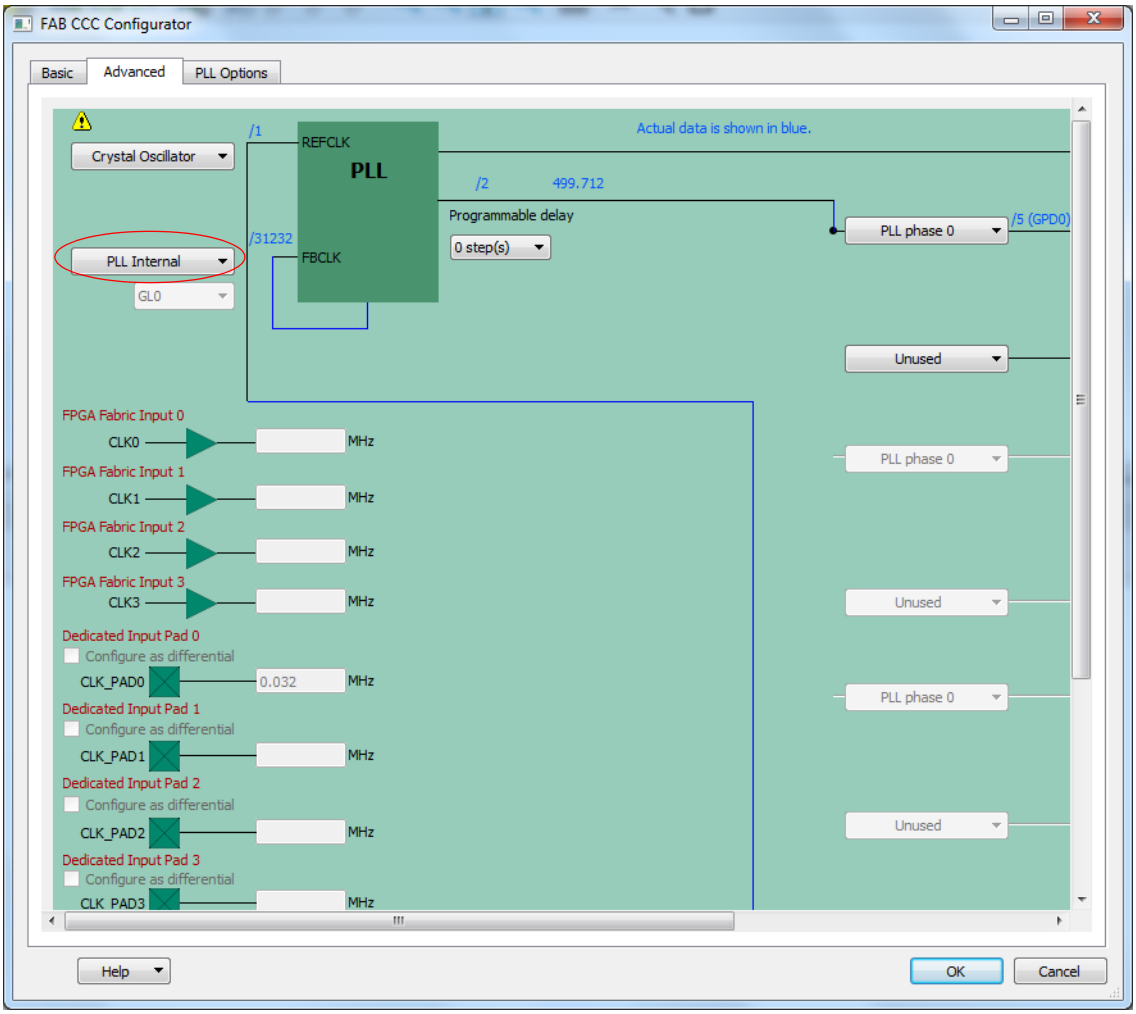


Figure 8 • **Configuring PLL Feedback Source**

12. Click on **PLL Options** tab in the **FAB CCC Configurator** window and check **Expose PLL_ARST_N and PLL_POWERDOWN_N signals** as shown in Figure 9.

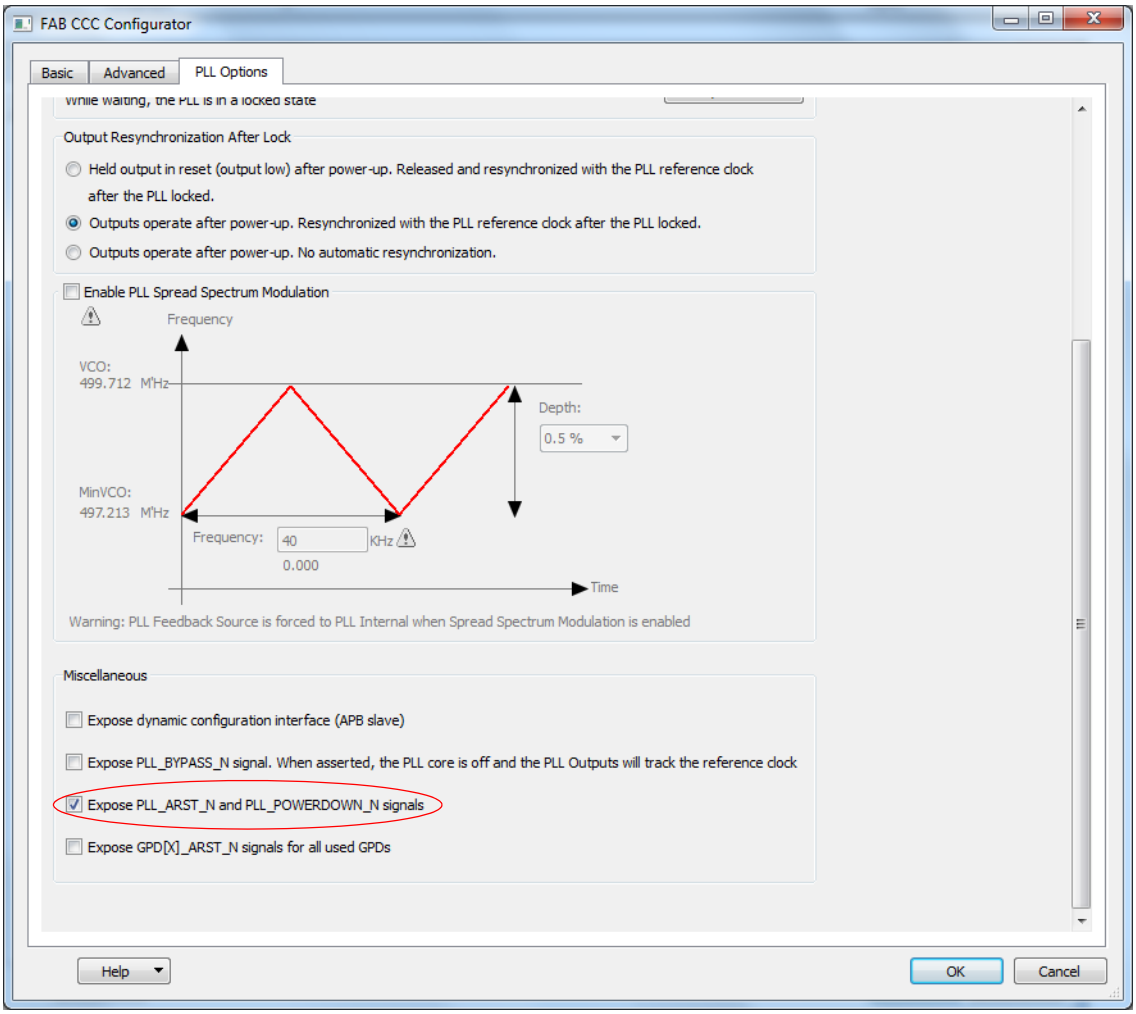


Figure 9 • **Configuring PLL Power-down Signal**

13. Click **OK** and close the **FAB CCC Configurator** window.
14. Drag an instance of the Chip Oscillators v1.0.102 component from the IP catalog into the SmartDesign canvas.
15. Double-click on the OSC_0 component in the SmartDesign canvas and open the **Chip Oscillators Configurator** window, as shown in Figure 10.
16. Configure the External Main Crystal Oscillator to drive FCCC and fabric logic.
    Enter the following information (see Figure 10):
    - External Main Crystal Oscillator: Checked
    - Source: Select **Crystal (32 KHz - 20 MHz)** from the pull-down menu
    - Frequency: 0.032 MHz
    - Drives Fabric CCC(s): Checked
    - Drives Fabric Logic: Checked

.

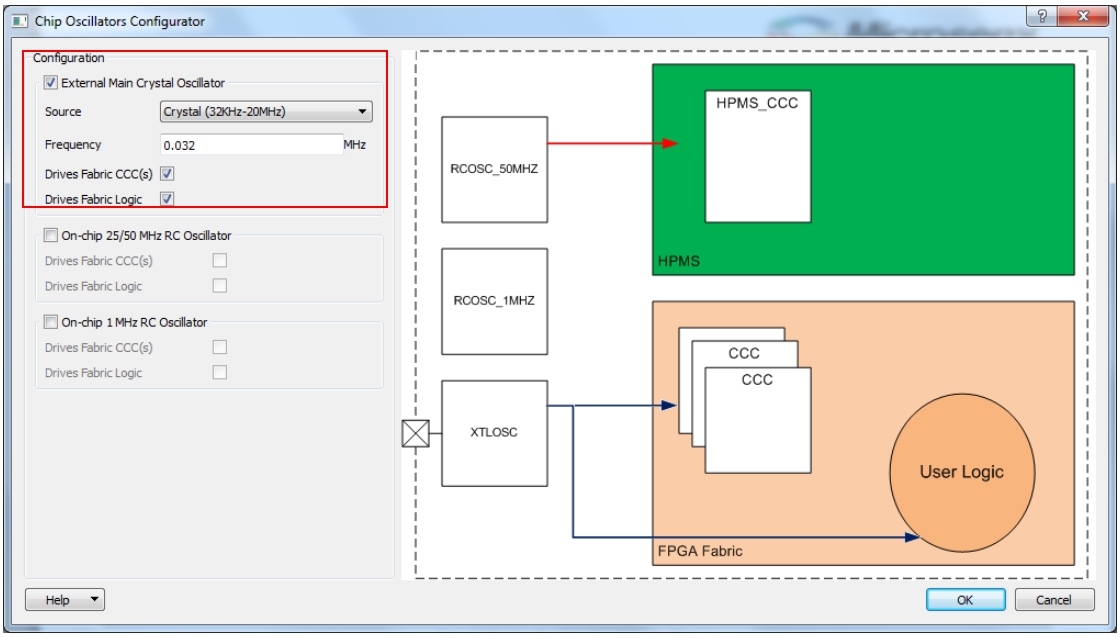


Figure 10 • **Configuring Chip Oscillators**

17. Click **OK** and close the **Chip Oscillators Configurator** window.

18. Import the VHDL source files into the project by selecting **Create HDL** under **Create Design** in the **Design Flow** tab. Right-click and select **Import Files…** (see Figure 11).

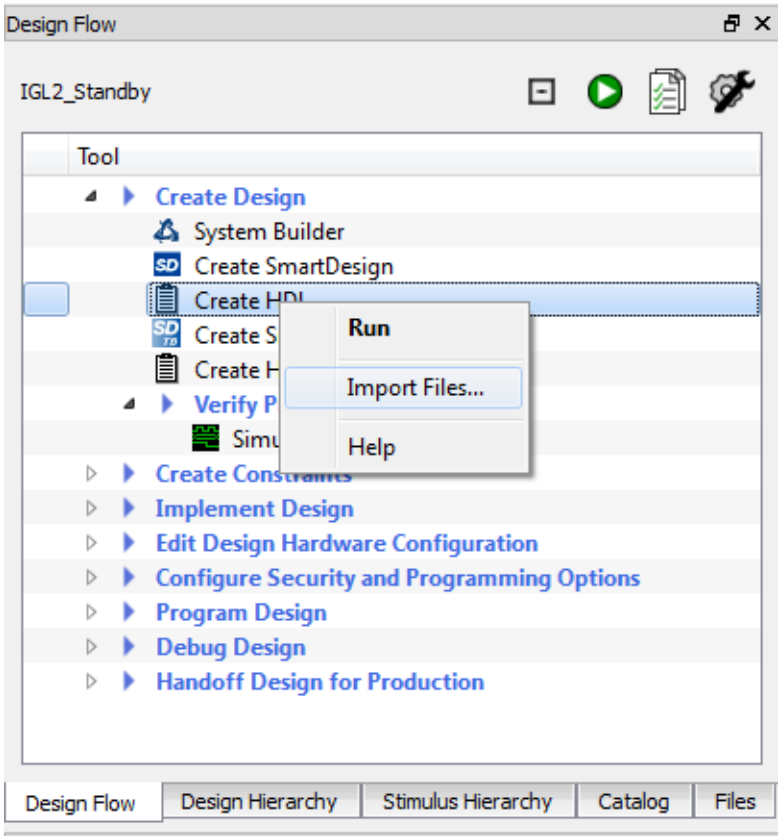


Figure 11 • **Importing HDL Source Files**

19. Enter the following in the **Import Files** dialog box and click **Open**:
    - Look in: *<C:\ or D:\>Microsemi_prj\IGL2_Standby_tutorial\Source_files*
    - Files of type: HDL Source Files (*.vhd *.v *.h)
    - File name: Select all files (click the first item and press Ctrl+A)

20. The files are visible on **Design Hierarchy** tab.

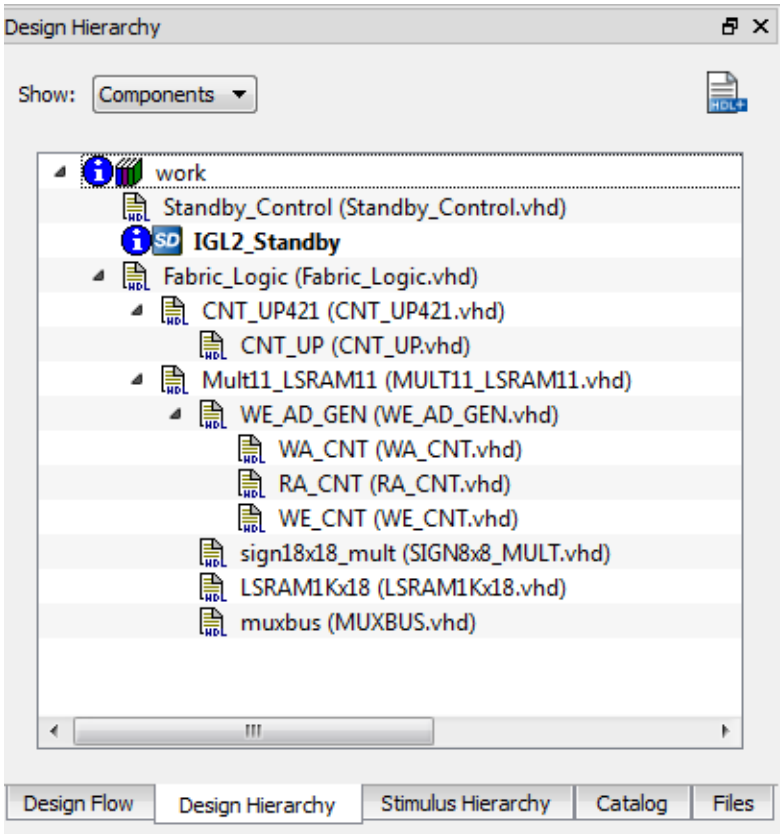


Figure 12 • **Design Hierarchy Tab with Imported Files**

21. Drag Standby_Control and Fabric_Logic components into the SmartDesign canvas.
22. After adding the components, the SmartDesign resembles Figure 13. Drag the components to improve the appearance of the canvas.

    Expand the canvas area by selecting **View > Maximize Work Area,** or click on  icon on the tool bar.

.

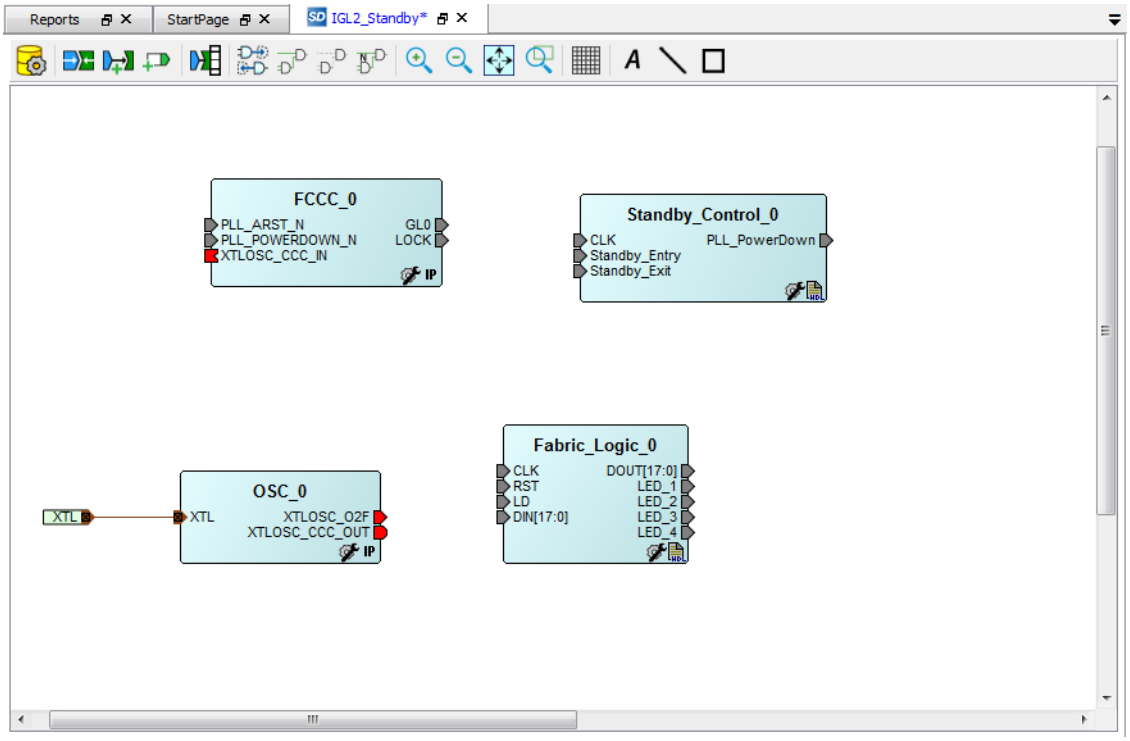


Figure 13 • **SmartDesign Canvas after Adding Components**

Connecting Components in the Canvas

SmartDesign in Libero SoC has a connection mode that supports click, drag, and release to connect the components.

Connect the components in the SmartDesign canvas using the following procedure:

1. Select **SmartDesign > Connection Mode** from the Libero SoC menu.
2. Connect the XTLOSC_CCC_OUT port of OSC_0 component to the XTLOSC_CCC_IN port of the FCCC_0 component as follows:
   - Click on the XTLOSC_CCC_OUT port of the OSC_0 component and hold the left mouse button.
   - Hold the left mouse button and drag the XTLOSC_CCC_IN port of FCCC_0 component.
   - Release the mouse button to connect.

Note: You can also connect the ports by selecting them using **CTRL** (Ctrl + click to select a port), right-clicking any of the selected ports, and selecting **Connect**.

3. Connect the other components in the SmartDesign canvas as per Table 3.

Table 3 • **Connections in Canvas**

From	To
OSC_0: XTLOSC_O2F	Standby_Control_0: CLK
Standby_Control_0: PLL_PowerDown	FCCC_0: PLL_ARST_N
	FCCC_0: PLL_POWERDOWN_N

Table 3 • **Connections in Canvas (continued)**

From	To
FCCC_0: GL0	Fabric_Logic_0: CLK
FCCC_0: LOCK	Fabric_Logic_0: RST

4. Select **SmartDesign > Connection Mode** from the Libero SoC menu to exit connection mode.
5. Promote the following ports to the top level (see Table 4). Click on the port, Right-click and select **Promote to Top Level**.

Table 4 • **Promote to Top Level**

Ports
Standby_Control_0: Standby_Entry
Standby_Control_0: Standby_Exit
Fabric_Logic_0: LD
Fabric_Logic_0: DIN[17:0]
Fabric_Logic_0: DOUT[17:0]
Fabric_Logic_0: LED_1
Fabric_Logic_0: LED_2
Fabric_Logic_0: LED_3
Fabric_Logic_0: LED_4

The SmartDesign canvas appears as shown in Figure 14. Drag the components or use the SmartDesign Auto Arrange feature to improve the appearance of the canvas.

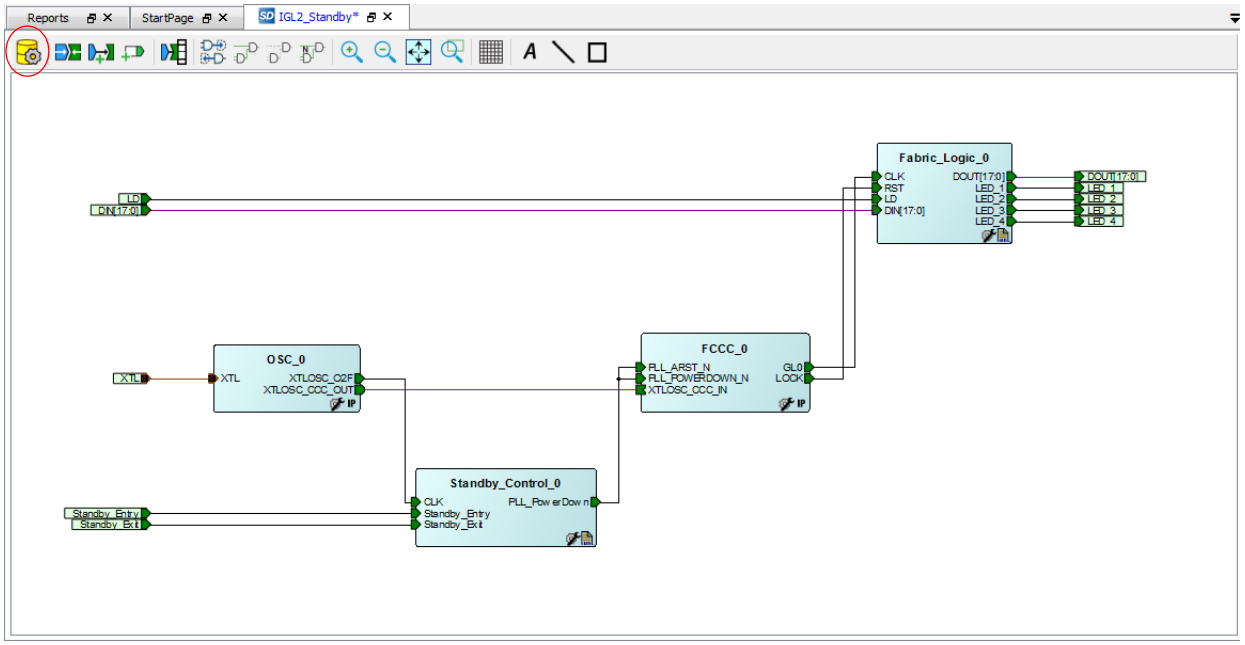


Figure 14 • **SmartDesign Canvas after Connections**

6. Save the design (**File > Save IGL2_Standby**).

7. Generate the design by selecting **SmartDesign > Generate Component,** or by clicking the **Generate Component** icon on the SmartDesign toolbar (circled in Figure 14).
8. Restore the work area (**View > Restore Work Area**) if you expanded the work area earlier.
9. Confirm that the message **IGL2_Standby was generated** appears in the Libero Log window.
10. Close the design (**File > Close IGL2_Standby**).

Importing Physical Constraint files

This section describes how to import a physical design constraint (PDC) file to make I/O attribute and pin assignments for the layout.

There are several ways to make I/O assignments:

1. Expand **Create Constraints** in the **Design Flow** tab. Right-click on **I/O Constraints** and select **Import Files...**.

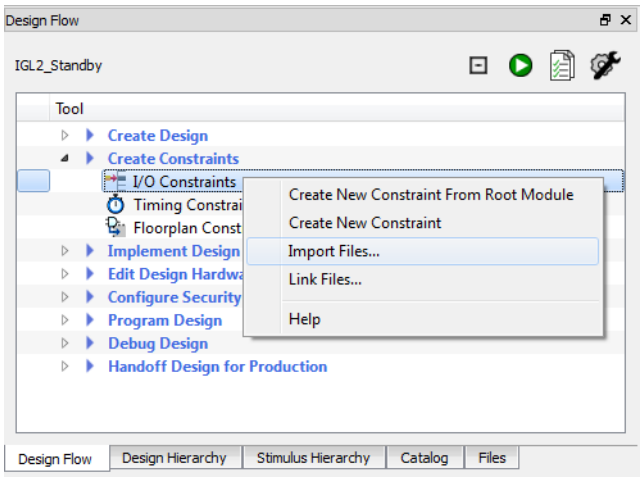


Figure 15 • **Importing I/O PDC Constraint File**

2. Enter the following in the **Import Files** dialog box then click **Open**:
   - Look in: *<C:\ or D:\>Microsemi_prj\IGL2_Standby_tutorial\Constraints*
   - Files of type: I/O Constraint Files (*.pdc)
   - File name: IGL2_Standby.pdc
3. Click **No** in the **Information** dialog box.

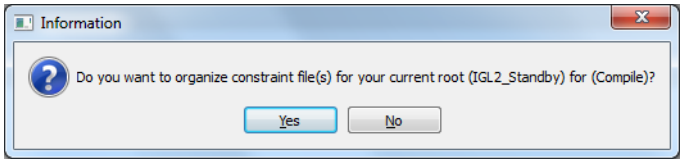


Figure 16 • **Information Dialog Box after Importing PDC Constraint File**

4. The file is visible on the Libero SoC Files tab under **constraint > io**.

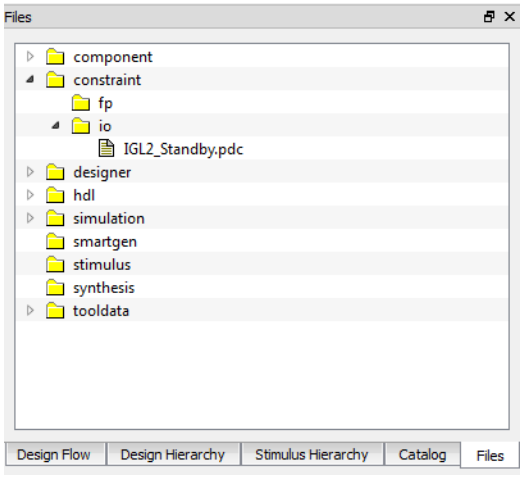


Figure 17 • **I/O PDC Constraint File in Libero SoC Project**

A description of the Designer PDC constraints is available in the Libero Help (**Help > Help Topics > Implement Design > Constrain Place and Route > Assigning Design Constraints > Design Constraints Guide > Reference > Constraints by File Format > PDC Command Reference**).

Synthesis and Layout

Use the push-button flow to synthesize the design with Synplify Pro, run layout and generate the programming file as mentioned below:

1. Expand **Create Constraints > I/O Constraints** in the Libero SoC **Design Flow** tab. Right-click **IGL2_Standby.pdc** under **Constraints.** Then, right-click and select **Use for Compile,** as shown in Figure 18. A green check mark appears next to the constraint file indicating that the file will be used.

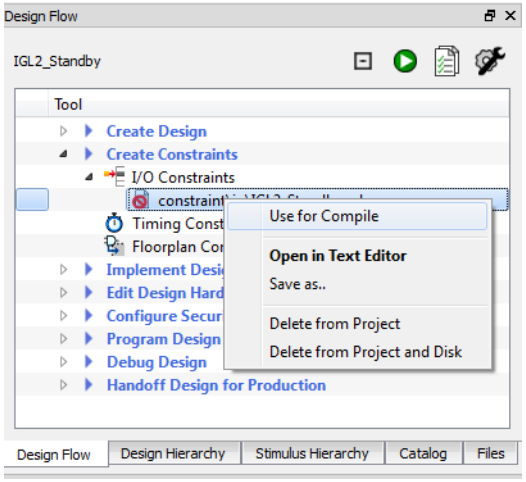


Figure 18 • **Selecting I/O PDC Constraint File in Design Flow Tab**

2. Click G**enerate Programming Data** icon in the **Design Flow** tab (circled in Figure 19), or select **Design > Generate Fabric Programming Data** to synthesize the design, run layout using the I/O constraints that are created and generate the programming file.

Figure 19 • **Generate Programming Data Icon**

The design implementation tools run in batch mode. Successful completion of a design step is indicated by a green check mark next to I**mplement Design** in the **Design Flow** tab (see Figure 20).

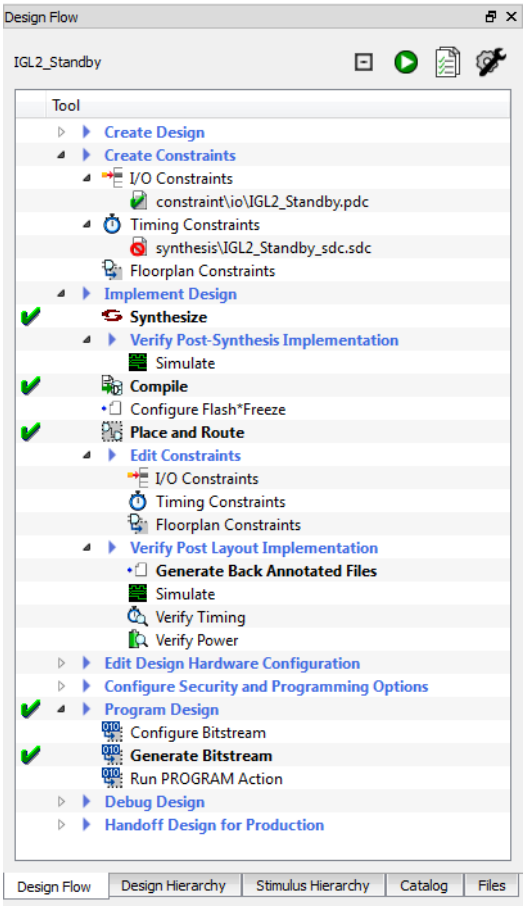


Figure 20 • **Successful Design Implementation**

3. Generate a power report by right-clicking **Verify Power** under **Verify Post Layout Implementation** in the **Design Flow** tab and selecting **Run**.

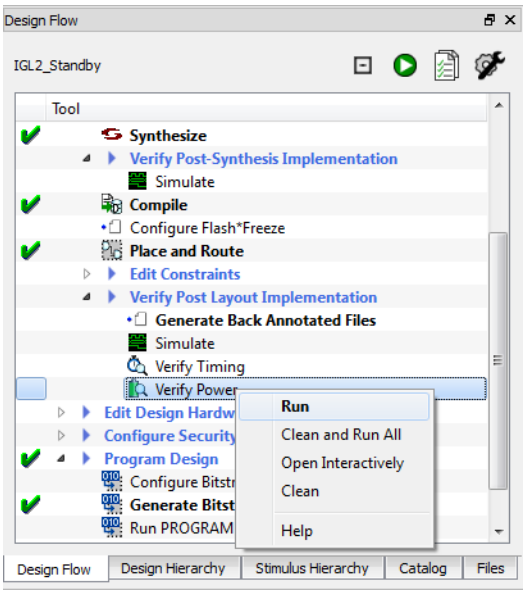


Figure 21 • **Generating Post Layout Power Report**

4. The **Reports** tab displays reports for the tools used to implement the design. Select **IGL2_Standby_power_report.xml** under **Verify Power** in the **Reports** tab to view the power consumption.

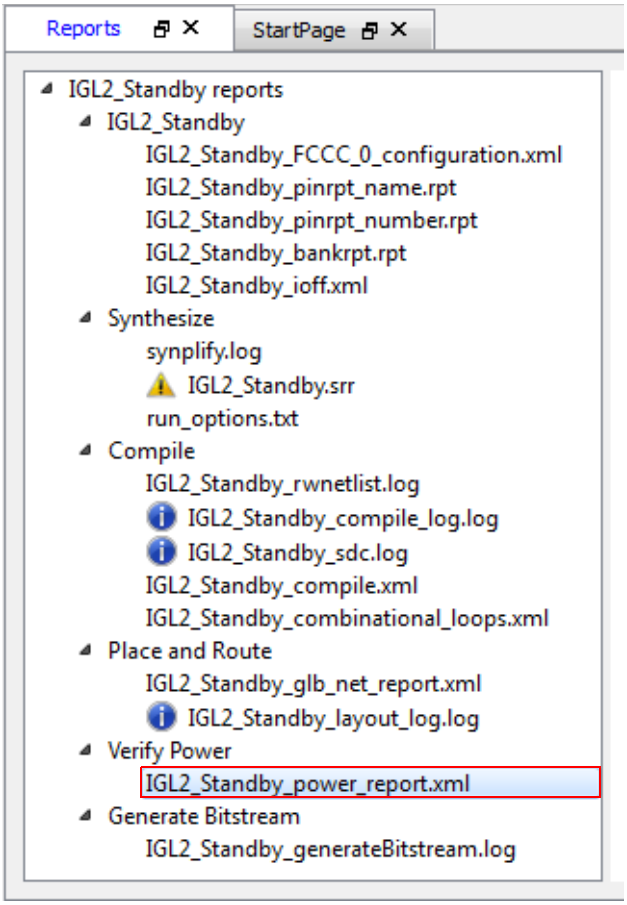


Figure 22 • **Reports Tab after Implementing Design**

The **Reports** tab displays the power report as shown in Figure 23.

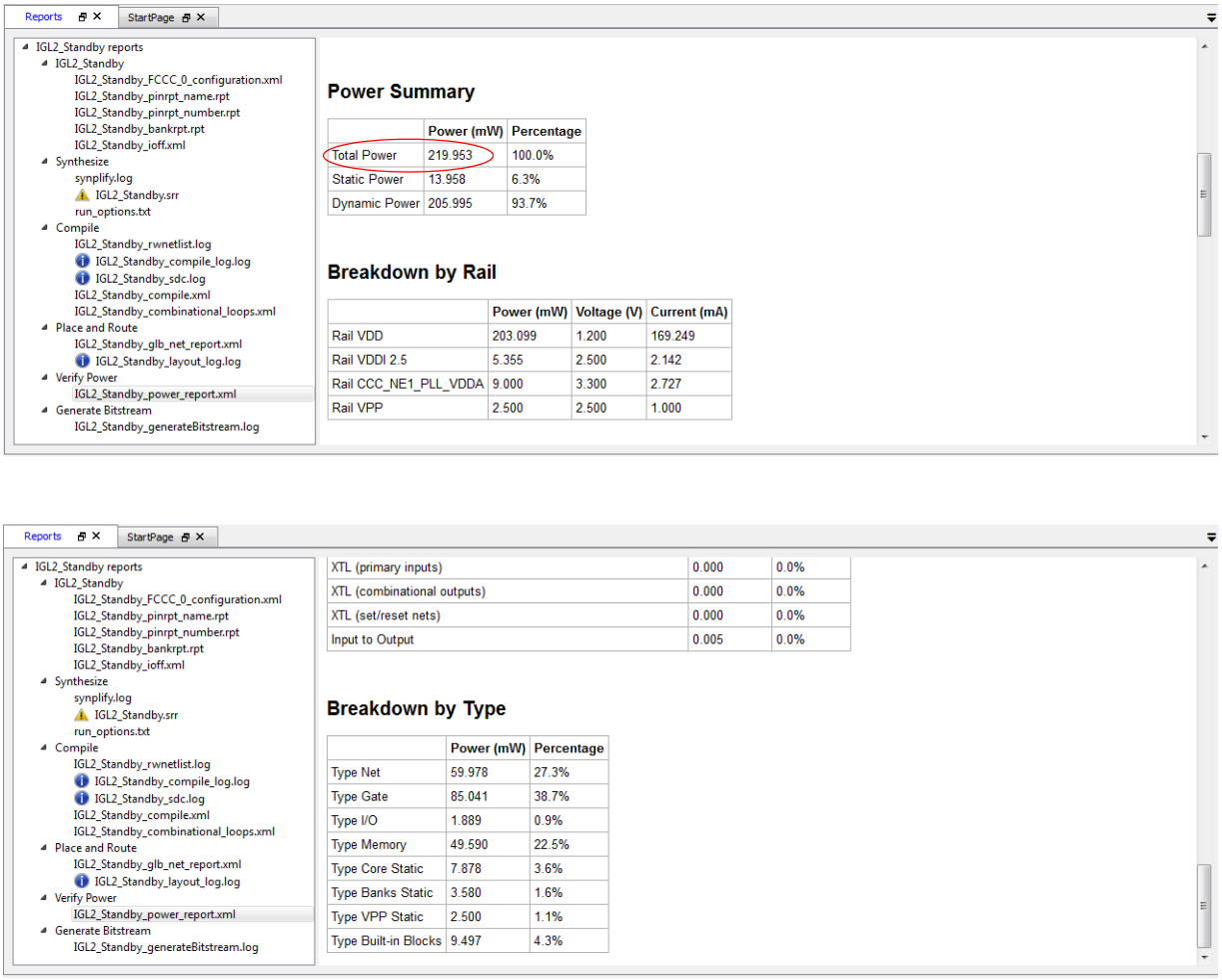


Figure 23 • **Power Report**

Programming

The following steps describe how to run FlashPro in batch mode and program the IGLOO2 M2GL010T on the IGLOO2 Evaluation Kit board:

1. Prior to programming (and powering up) the IGLOO2 Evaluation Kit board, ensure that the jumpers are positioned as shown in Table 5.

Table 5 • **Jumper Settings**

Jumper	Location	Setting
J3	Above the On/Off Switch in Figure 24	1-2 installed
J8	Below the JTAG Programming Header (J5) in Figure 24	1-2 installed

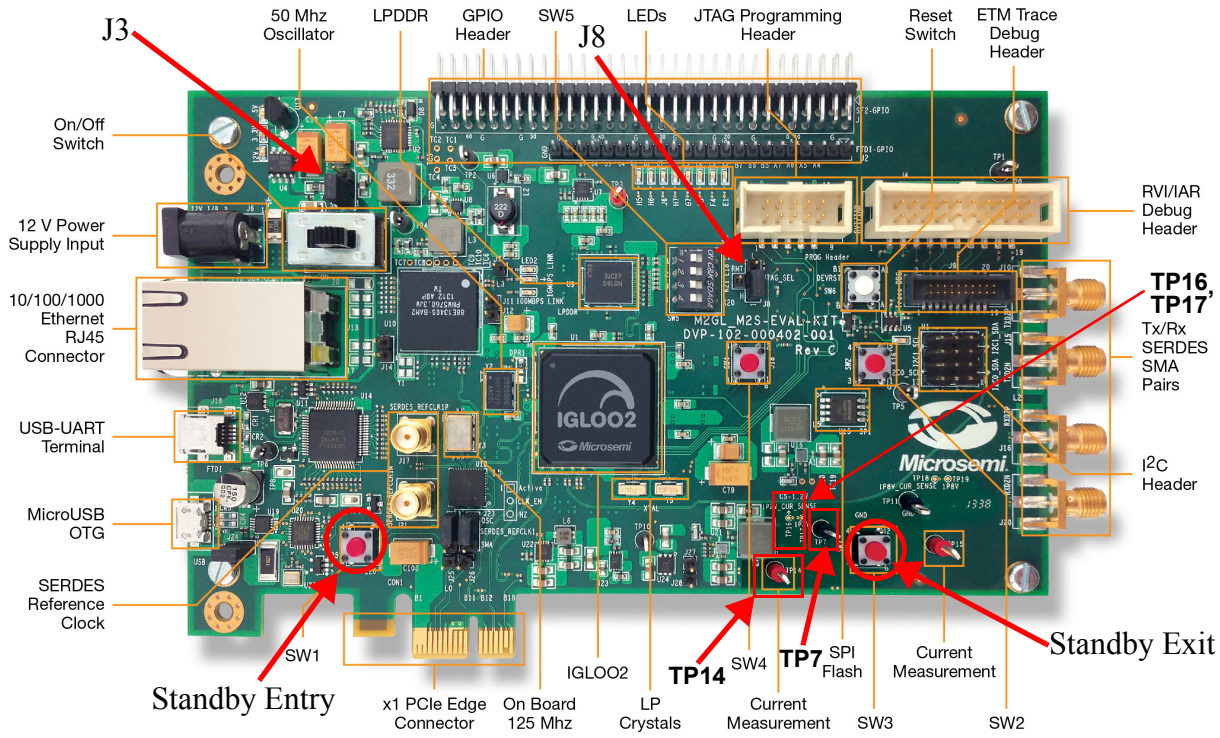


Figure 24 • **IGLOO2 Evaluation Kit**

2. Plug the FlashPro4 ribbon cable into connector J5 (JTAG Programming Header) on the IGLOO2 Evaluation Kit board.
3. Connect the mini USB cable between the FlashPro4 and the USB port of the PC.
4. Install the FlashPro4 drivers if prompted. The drivers are located in *<FlashPro Installation Directory>\Drivers* folder.
5. Power on the board by plugging in the power cable and switching on the power switch. Three Green LEDs on top left of the board are powered on.

6. Expand **Program Design** in the **Design Flow** tab. Right-click **Run PROGRAM Action** and select **Run** to begin programming.

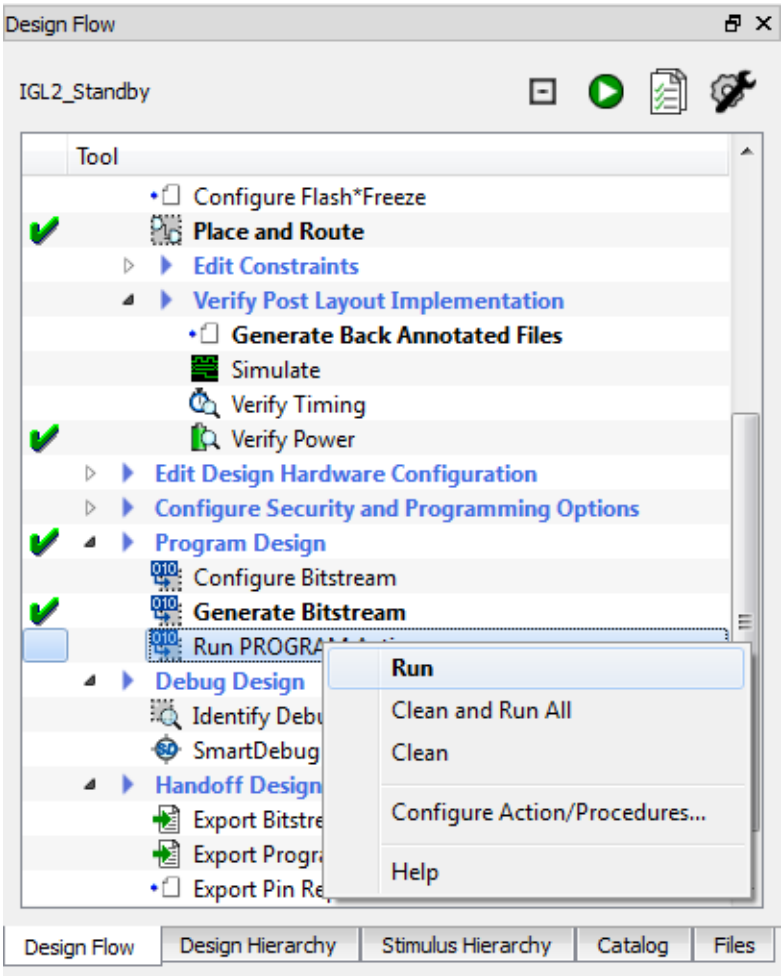


Figure 25 • **Launching Programming Software from Design Flow Tab**

7. FlashPro runs in batch mode and programs the device. Programming messages are visible in the Libero SoC log window. Programmer number differs.

Note: Do not interrupt the programming sequence. It may damage the device or programmer.

8. The following message is visible in the Reports view under Program Device when the device is programmed successfully (see Figure 25). Programmer number differs:

```
programmer '92327' : device 'M2GL010T' : Executing action PROGRAM PASSED.
```

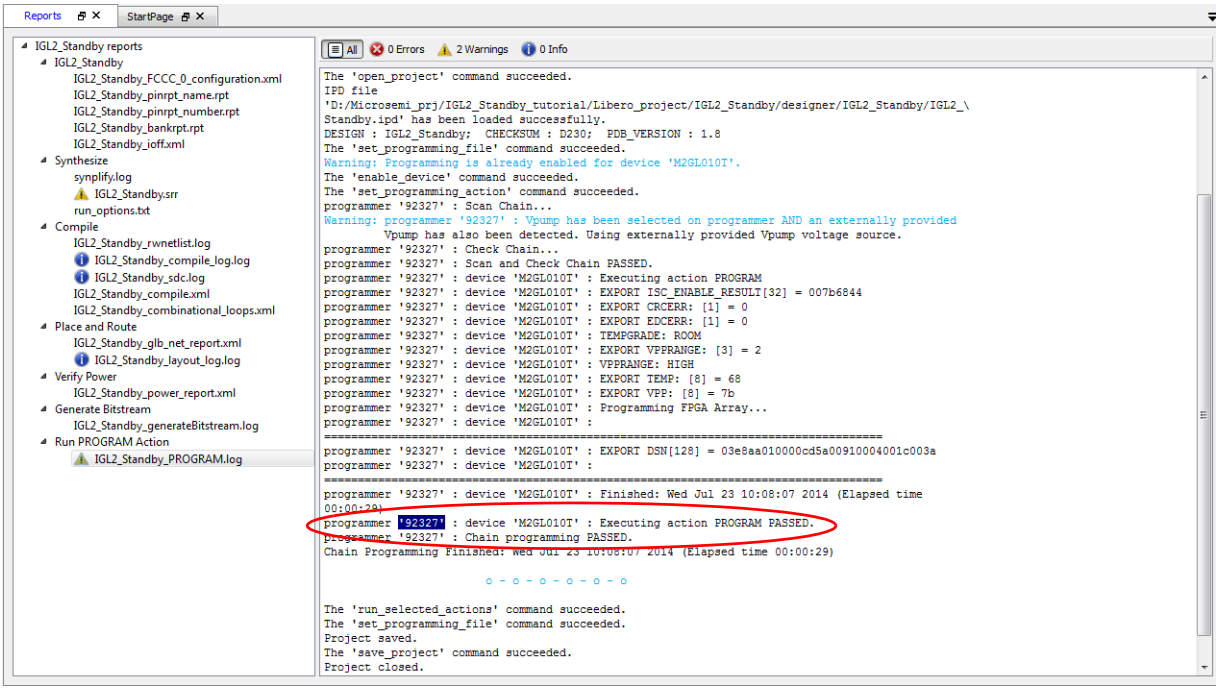


Figure 26 • **Programming Messages in Libero SoC Log Window**

9. A green check mark appears next to **Program Design and Program Device** in the **Design Flow** tab indicating that programming has been completed successfully.

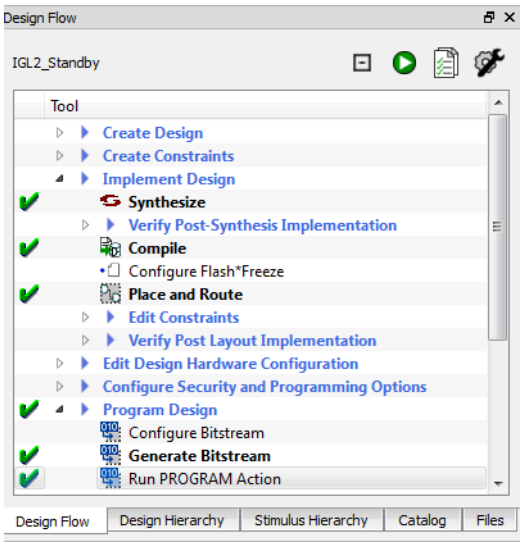


Figure 27 • **Design Flow Tab after Programming**

10. Close Libero SoC (**Project > Exit**). Select **Yes** if prompted about saving changes.

Running the Demo Design

Power Measurement (Normal Operation and Standby)

IGLOO2 Evaluation Kit board has a voltage measuring circuit which measures the voltage across the VDD (1.2 V) current sense resistor.

The core power can be calculated using following equations:

- Core Current (mA) = Measured Voltage (mV) ÷ 5 (Scaling Factor)
- Core Power (mW) = 1.2 × Core Current

Connect the positive terminal of a standard digital voltmeter (DVM)/Multimeter to TP14 and negative terminal to TP7.

Note the digital voltmeter/Multimeter reading and calculate the power using above equations.

Precise Standby Power Measurement

Precise and accurate power measurements can be obtained by measuring voltage across the 1.2 V, 0.05 Ω sense resistor. Test points TP16 and TP17 can be used to directly measure voltage across the 1.2 V sense resistor. Since the current drawn by the device in standby mode is expected to be around or less than 10 mA, the voltage measured across the 0.05 Ω sense resistor is expected to be less than 0.5 mV. A precise digital voltmeter such as Fluke-287 that can measure sub-millivolt readings should be used to read voltage measured across the sense resistor.

Convert the voltage measured across sense resistor to power using the following equation:

Power (mW) = (Voltage (mV)/0.05) × 1.2

Total Power (Dynamic and Static)

The following steps describe how to calculate total power:

1. Reset the board by pressing and releasing the Reset button (SW6 DEVRST).
2. Observe the pattern of the LEDs E1, F4, F3, and G7 after resetting the board.
3. Measure the power

Note: If LEDs are not toggling after reset, the device is in Standby mode. Press and release Standby Exit push button (SW3) and observe the LEDs pattern. The LEDs start toggling. Then, Measure the power.

Standby Power

The following steps describe how to calculate standby power:

1. Press and release Standby Entry push button (SW1) and observe the LEDs pattern. The LEDs stop toggling.
2. Measure the power
3. Press and release Standby Exit push button (SW3).
4. When finished, remove power from the board.

Appendix A - Power Estimator

Power Estimator

The following steps describe how to use Power Estimator and calculate the total power:

1. Download the Power Estimator, *SmartFusion2 and IGLOO2 Power Calculator*
2. Double-click and invoke the power estimator spreadsheet.
3. Click on the Summary worksheet. The Summary worksheet provides the device settings and the power summary.
4. Change the device settings. Enter the following information:
   – Family: Select **IGLOO2** from the pull-down menu
   – Device: Select **M2GL010T** from the pull-down menu
   – Package: Select **484 FBGA** from the pull-down menu

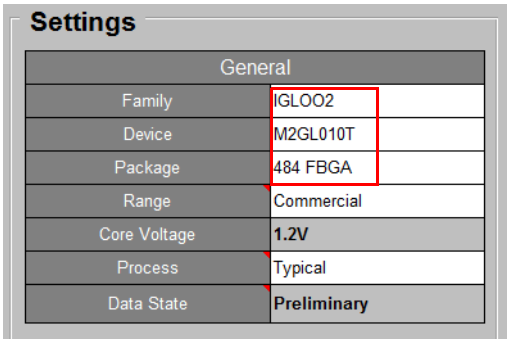


***Figure A-1* • Settings Section in the Device Settings and Summary Worksheet**

The Summary worksheet has an integrated initialize power estimator wizard. This wizard provides an option to select design specific information. Upon running the wizard, it populates the power calculator spreadsheet with information about the design and performs power estimation for the design.

5. Click **Initialize Power Estimator** (see Figure A-2) and invoke the Initialize power estimator wizard. **Initialize Power Estimator** dialog box opens (see Figure A-3).

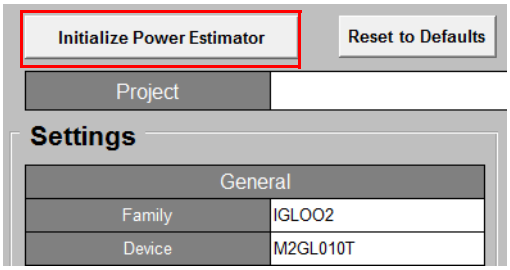


***Figure A-2* • Initialize Power Estimator**

6. Enter the following information in the **Initialize Power Estimator** dialog box:

- uSRAM: Move the slider to zero, 0/22 (0%)
- IO:
  – Technology: LVCMOS25

  - #Inputs: 21
  - #Outputs: 22
- Default RAM Enable Rate: 100%

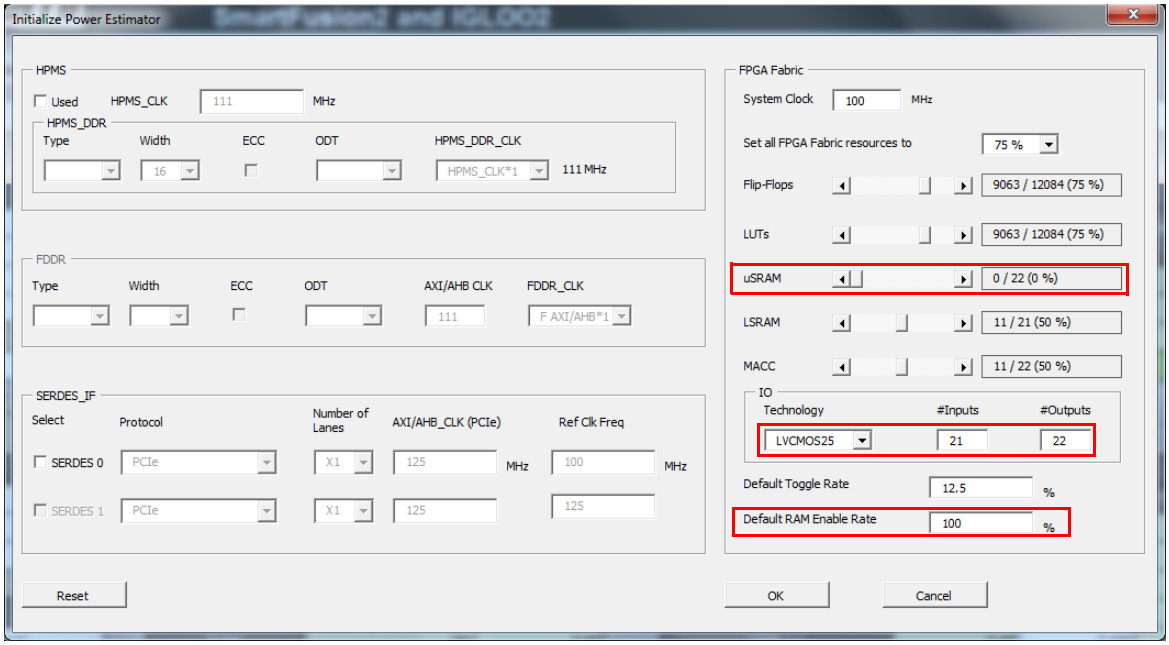


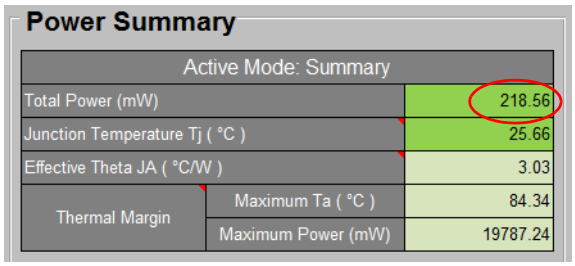
Figure A-3 • **Initialize Power Estimator Wizard**

7. Click **OK** and close the **Initialize Power Estimator** dialog box. Click **Yes** in the **Set to Defaults** dialog box.
8. Click on the **CCC & Oscillator** worksheet and scroll down to **FAB_CCC Power** section. Enter the following information in the **FAB_CCC Power** table:
   - Name: FCC_0
   - Reference clock frequency (MHz): 0.032
   - PLL output frequency (MHz): 500 MHz
   - Output1 frequency (MHz):100 MHz

FAB_CCC Power								
Name	Reference Clock Frequency (MHz)	PLL Output Clock Frequency (MHz)	Output1 Frequency (MHz)	Output2 Frequency (MHz)	Output3 Frequency (MHz)	Output4 Frequency (MHz)	VDD Power (mW)	PLL_VDDA Power (mW)
FCCC_0	0.032	500	100				2.59	5.00
							0.00	0.00
							0.00	0.00
							0.00	0.00
							0.00	0.00
							0.00	0.00
							0.00	0.00
							0.00	0.00

Figure A-4 • **FAB_CCC Section**

9. Click on the **Summary** worksheet to get the total power. The Power Summary section is populated with the Total Active mode power.

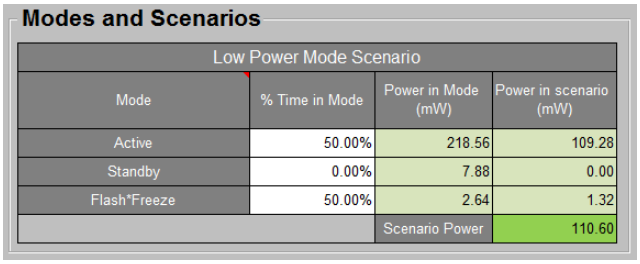


Power Summary

Active Mode: Summary		
Total Power (mW)		218.56
Junction Temperature Tj (°C)		25.66
Effective Theta JA (°C/W)		3.03
Thermal Margin	Maximum Ta (°C)	84.34
	Maximum Power (mW)	19787.24

Figure A-5 • **Power Summary**

10. The Modes and Scenarios section is populated with the total power in the Active, Standby and Flash*Freeze modes.



Modes and Scenarios

Low Power Mode Scenario			
Mode	% Time in Mode	Power in Mode (mW)	Power in scenario (mW)
Active	50.00%	218.56	109.28
Standby	0.00%	7.88	0.00
Flash*Freeze	50.00%	2.64	1.32
		Scenario Power	110.60

Figure A-6 • **Modes and Scenarios**

11. Close the Power Estimator.

A – List of Changes

The following table lists critical changes that were made in each revision of the chapter in the demo guide.

Date	Changes	Page
Revision 1 (August 2014)	Initial release	NA

B – Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call 800.262.1060
From the rest of the world, call 650.318.4460
Fax, from anywhere in the world, 408.643.6913

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Customer Support website (.microsemi.com/soc/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the website.

Website

You can browse a variety of technical and non-technical information on the SoC home page, at .microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at .microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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