Power Matters

Microsemi

Distribution Issues between Central Power and POL Architectures

Microsemi Space Forum Russia – November 2013

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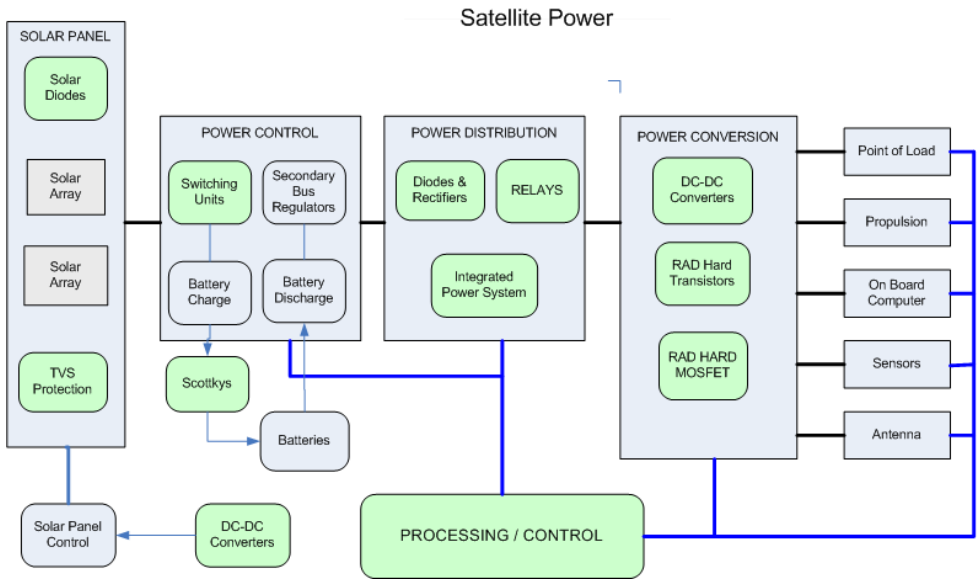
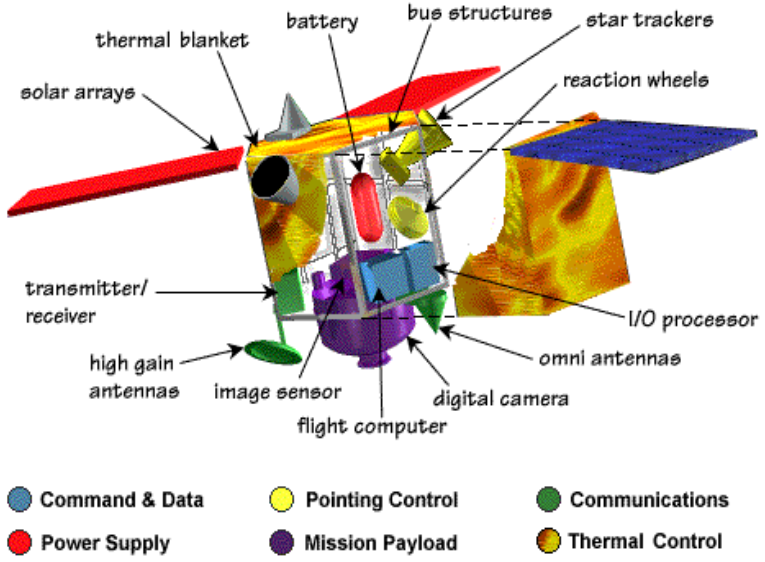
Overview

- Digital Power Requirement Trends
  - Voltage
  - Current
  - Transients
- A Typical System
- SB30 System Supply Concept
  - Direct / POL
  - Isolation
  - Sequencing
  - Regulation
- Additional Design Points
- Application Examples
- Summary

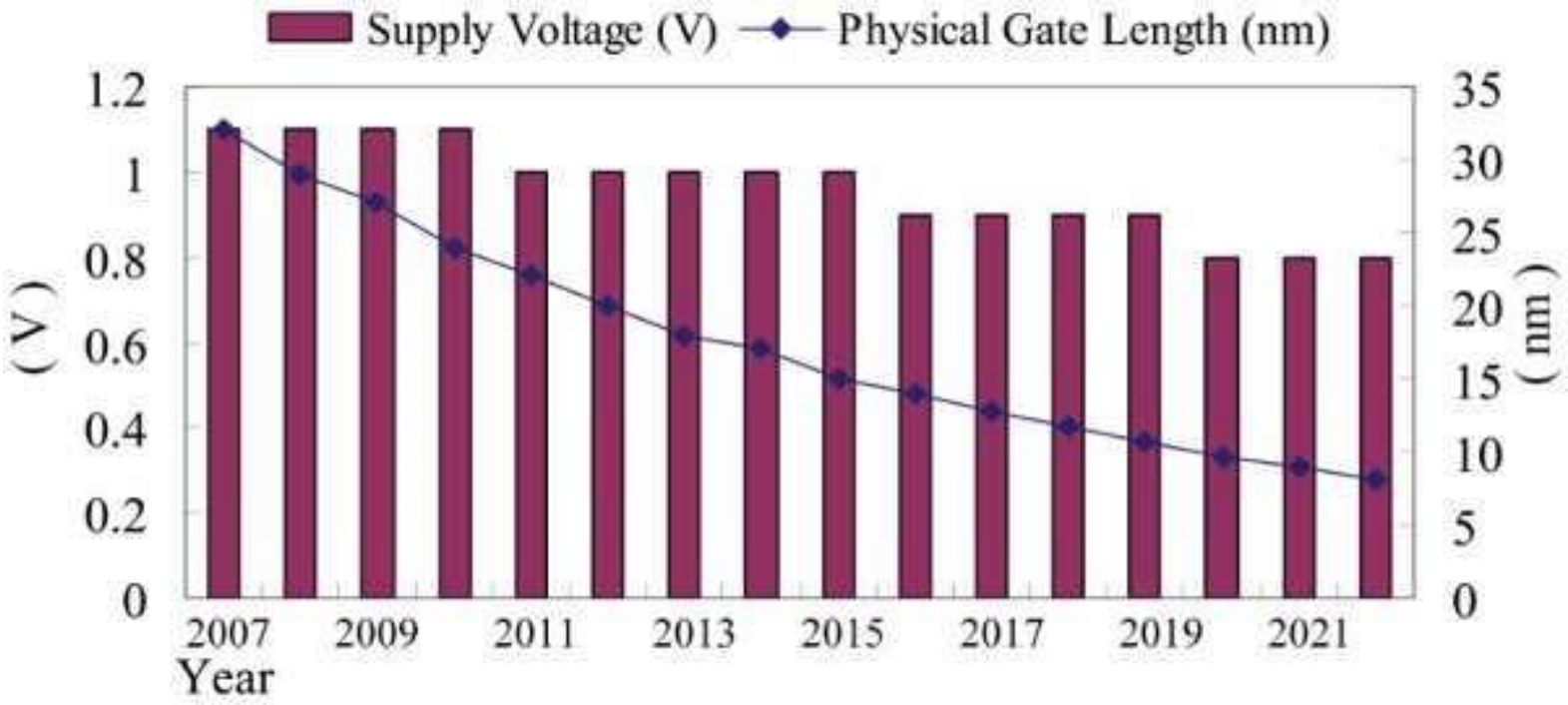




Digital/FPGA Power Trends

- Future requirements are for greater flexibility and much higher data capability while maintaining as low power as possible but retaining integrity and safety
- With reduced feature sizes comes lower core voltages, higher currents and greater transient requirements
- With advances in circuit topologies and design methodologies it is possible to partition the design in a number of ways
- The system designer needs to understand both analog and digital future requirements in order to effectively assess partitioning of the power system
- This is usually considered in conjunction with the entire power generation and distribution system in order to maximise the overall system efficiency and effectiveness
- Sufficient headroom to maintain system operation for the mission lifetime requirement MUST be built in

General FPGA Trend for Supply Voltage and Physical Gate Length



(ITRS 2008 update.)

Microsemi Space FPGAs

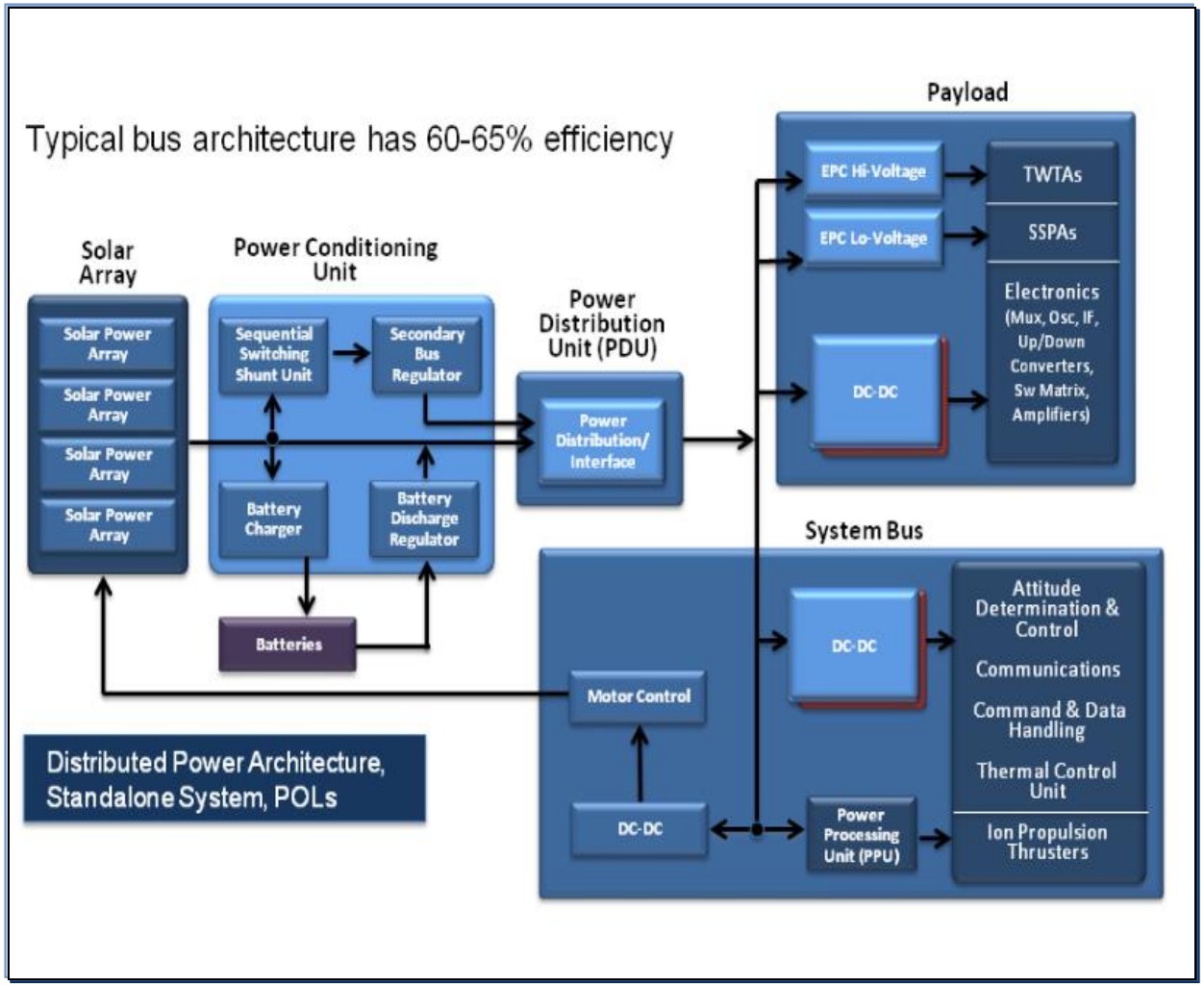
Actual power usage is determined by many factors including technology (e.g. generic static power consumption, dynamic power consumption) but also by the amount of utilization, switching frequency, I/O requirements and so on. Microsemi has a comprehensive tool set to determine power requirements pre and post net list.

	FPGA Core Voltage	I/O Voltage	Equivalent System system Gates	Max User I/O
RTSX-SU	1.5V Nom	1.5V to 3.3V	48K-108K	360
• A 0.22µm antifuse family.				
• Up to 100K gates				
RTAX-S	1.5V Nom	1.5V to 3.3V	250K-4000K	248-840
• Flagship family, 0.15µm antifuse, industry-standard space FPGA				
• Up to 4M gates				
RTAX-DSP	1.5V Nom	1.5V to 3.3V	2000K-4000K	684-840
• A new 0.15µ antifuse family based on the RTAX-S				
• Up to 4M gates and 120 18x18 Multiply Accumulate blocks				
• Targeting high performance payload applications				
RT-ProASIC3	1.2V to 1.5V	1.2V to 3.3V	600K-3000K	270-620
• 0.13um process				
• First Flash-based reprogrammable, non-volatile FPGA for space				
• Up to 3M gates				
RTG4 Serdes NEW! 65nm Rad Hard Flash process.	1.2V	1.2V to 3.3V	TBA	436-644 +

RTG4 Next-Generation Space-Flight FPGA Driving Performance

- Based on 65nm Flash low power process
  - Naturally resistant to configuration upsets
  - Non-volatile configuration so live at power-up
  - No external boot memory required
  - Low static power
- Designed for high-bandwidth data processing in payload applications
  - Abundant high-performance programmable logic fabric
  - Embedded high speed multiply-accumulate blocks
  - Ample on-board memory with fast access time, two block sizes
  - High performance I/Os – SERDES, LVDS, DDR2
- Radiation enhanced for space
  - Total ionizing dose
  - Single event effects
  - Latch-up immunity
- For the 1.2V Core we anticipate around 10A peak requirement depending on the FPGA size

Fully "Regulated" Electrical Bus Architecture

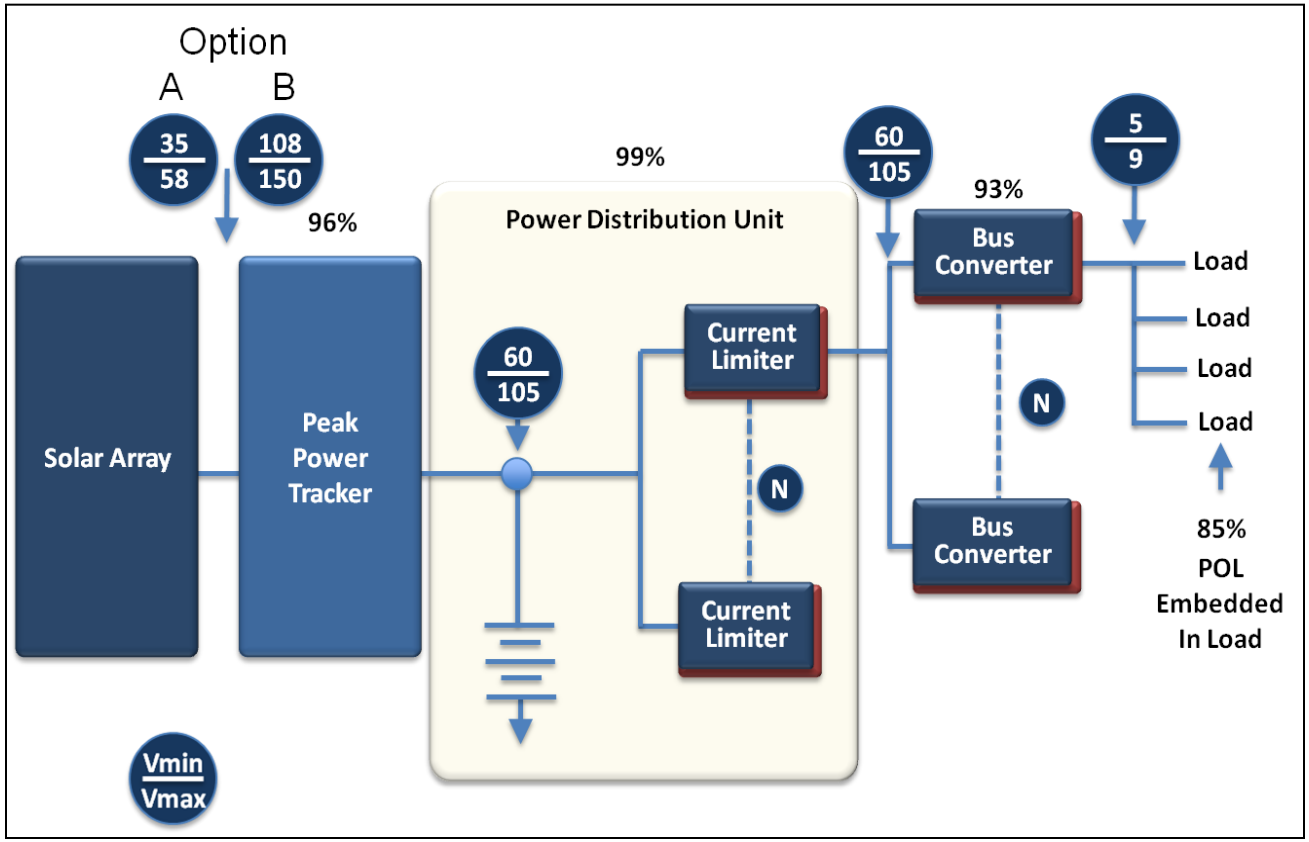


Trade-Offs Microsemi Value

- New solar array
- Higher voltages
- Battery regulation method
- Simplified Power conversion (SA50, SB30)
- SSPA Power Supplies
- Next gen POLs = +% efficiency
- Analog mixed signal – reduced component count/weight (SSM, High side drivers)
- Digital control – FPGAs
- Motor Control (Evolved from Aviation)

Typical Bus Voltages – 28V, 50V moving up to 70V, 100V and 120V

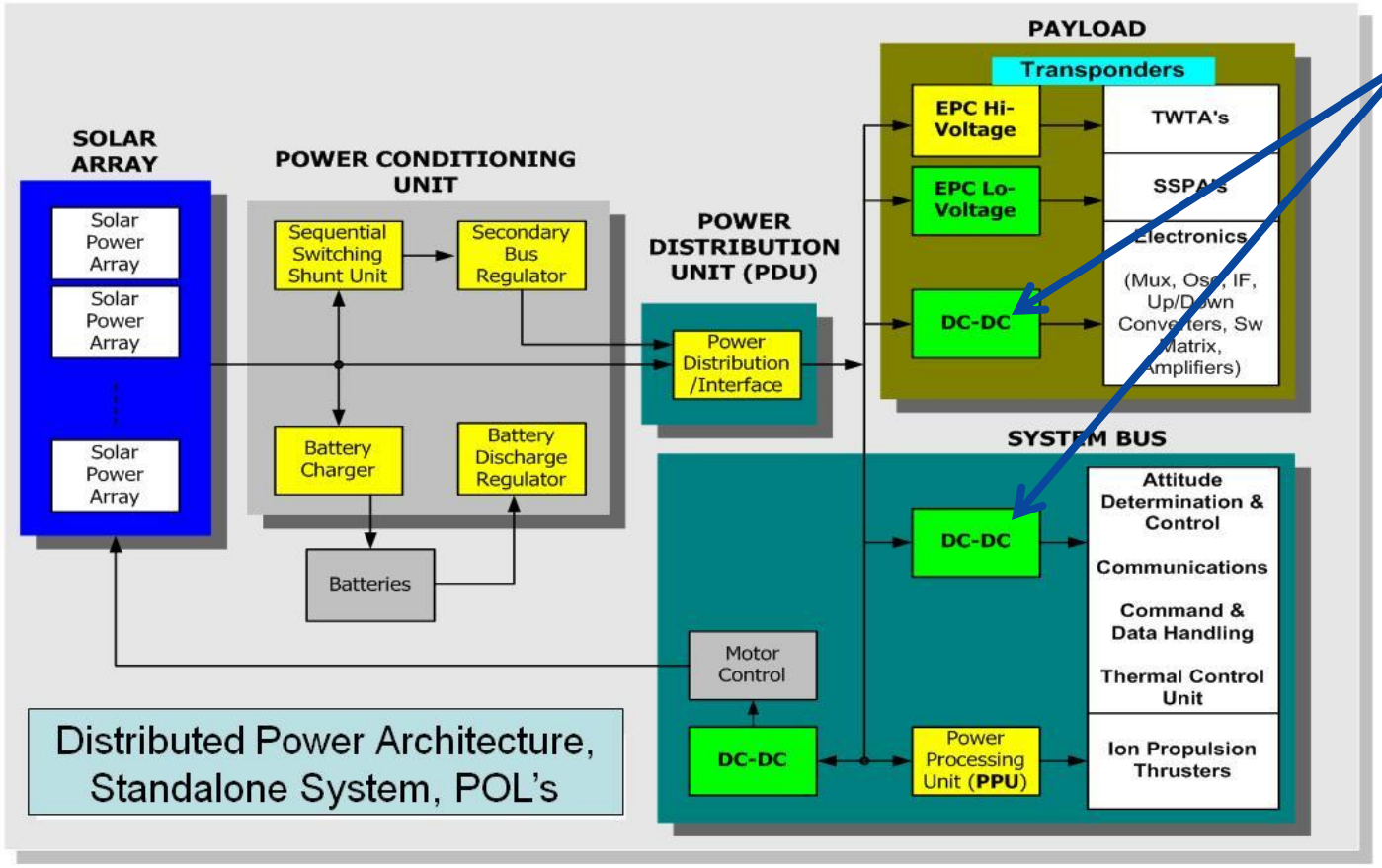
Unregulated Electrical Bus Architecture



- Trade-Offs
  - No battery charge / discharge system
  - Reduced weight & complexity
  - Fault tolerant architecture
  - Much improved efficiencies
  - Improved further with our next gen products (POLs, GaN)
  - Supports 5-10KW satellites
  - Reduced voltage range 60-105V
  - Optional Boost / Buck PPT

This architecture yielding 75% efficiency

SA50 Series Applications



Applications

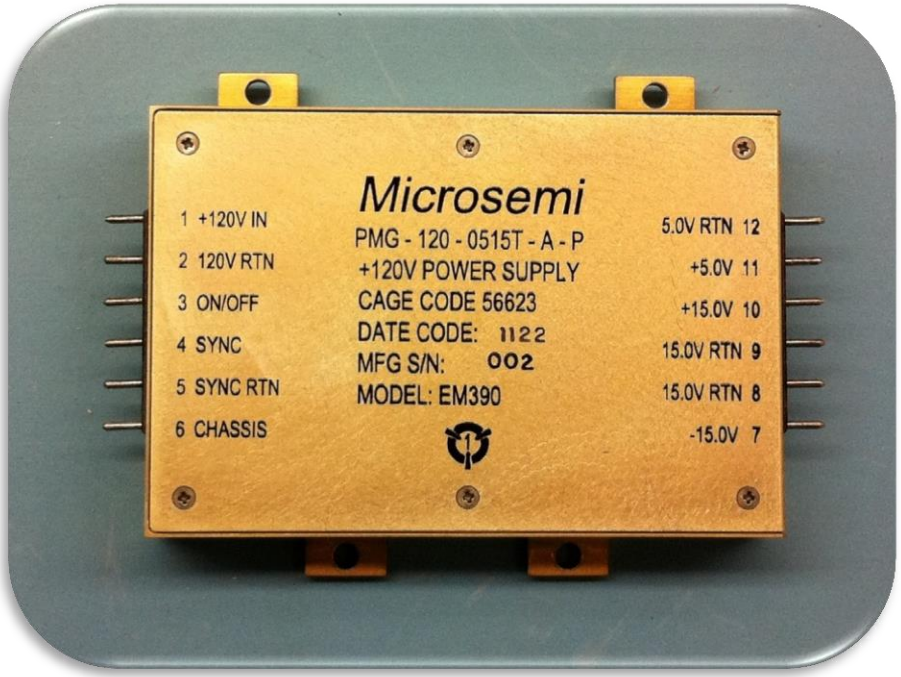
- Mux
- IF Oscillators
- Up / Down Converters
- Matrix Amplifiers
- Altitude / general Computers
- Communications
- Command
- Thermal Control

Converts Satellite Main Bus to Local Power Bus driving Analog and Digital Electronics loads

SA Version Customization Capabilities

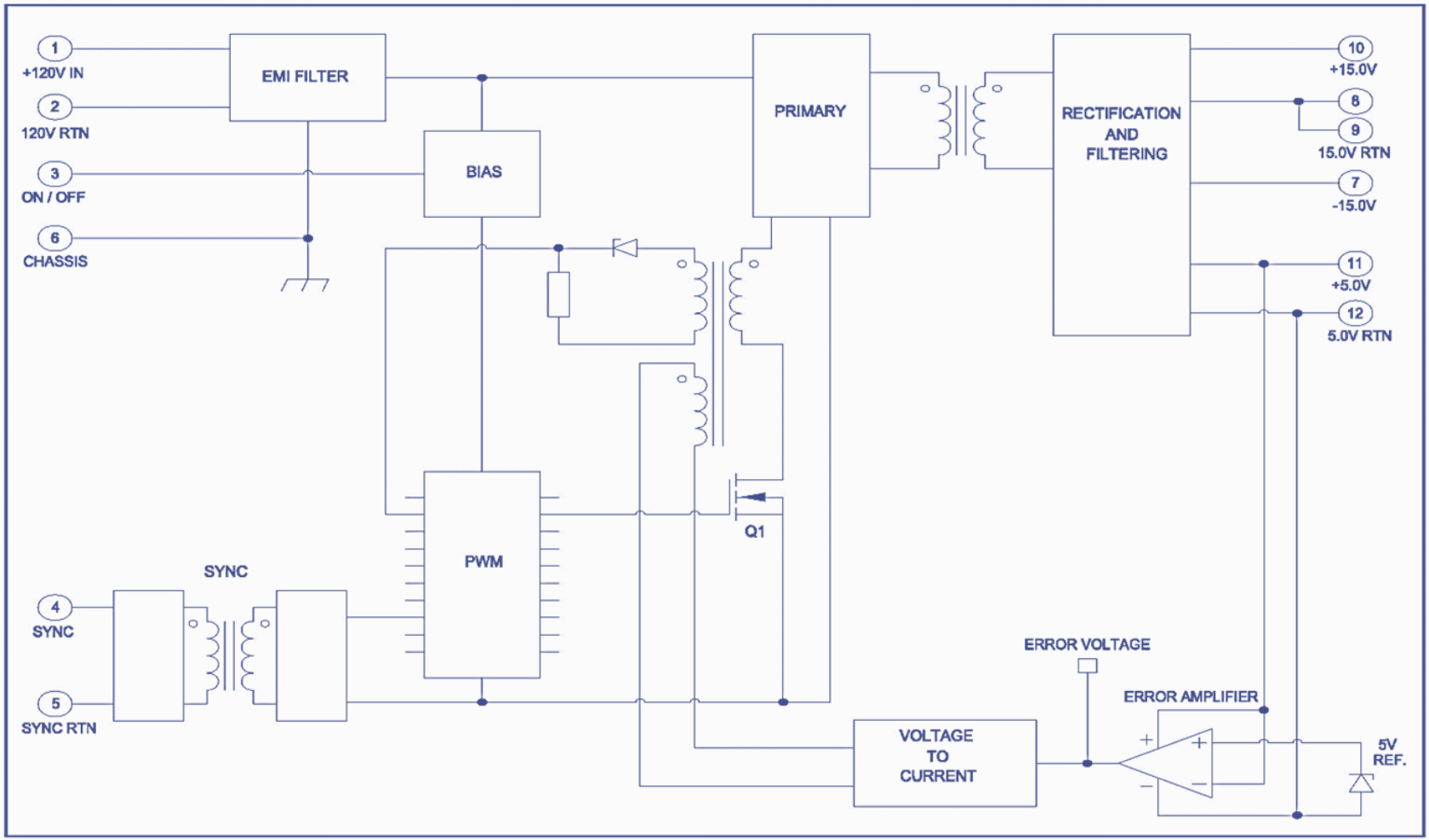
Customization enables opportunities to optimize power distribution design

- Typical Customizations
  - Input Voltage
  - Output voltage (combinations)
  - Package / Mounting
  - Customer Marking
  - Current / Power Limit settings
  - Power Up / Power Down profiles
  - Enhanced Tracibility
    - Custom material control
  - Special Process Control
    - Assembly
    - Screening



Standard Module First Prototype

SA50 Series Block Diagram Overview

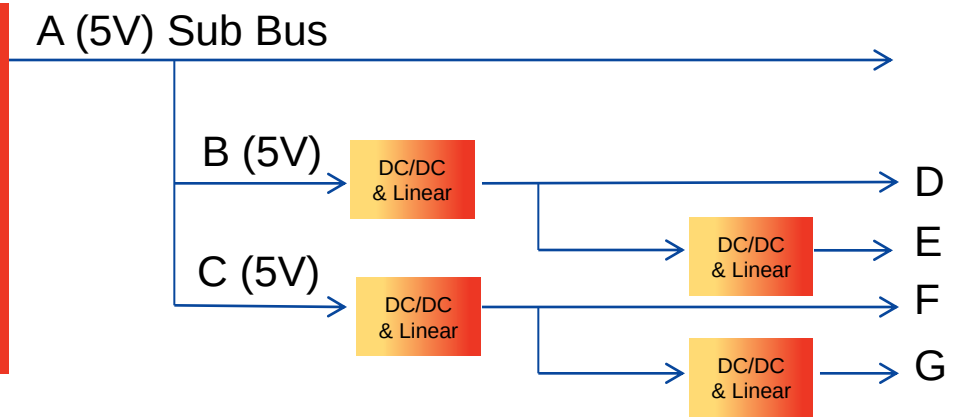


SA50 Series Block Diagram Overview

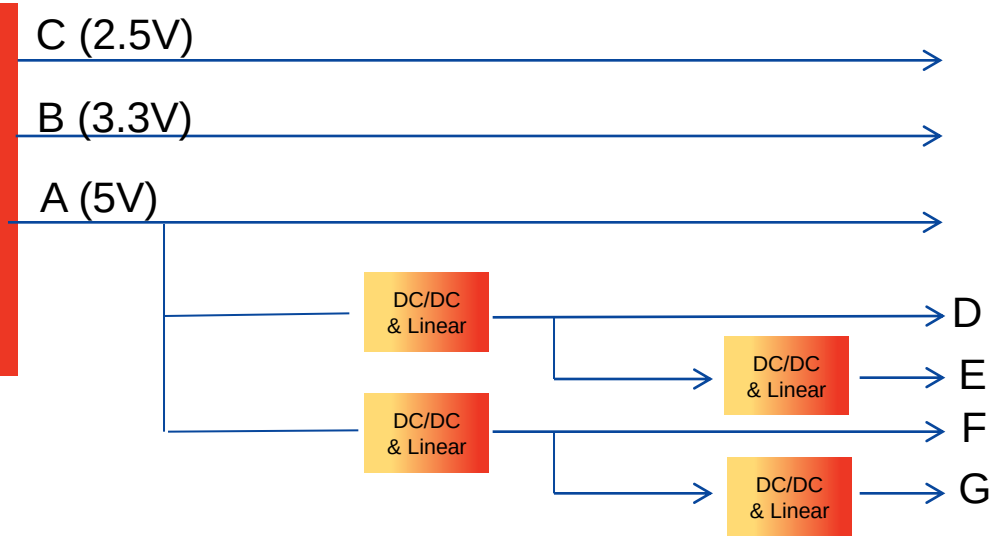
- Outputs ISOLATED from Inputs
- Outputs ISOLATED from each other
- No Opto-isolators used in feedback loop

Considerations to Partition the Traditional Solution

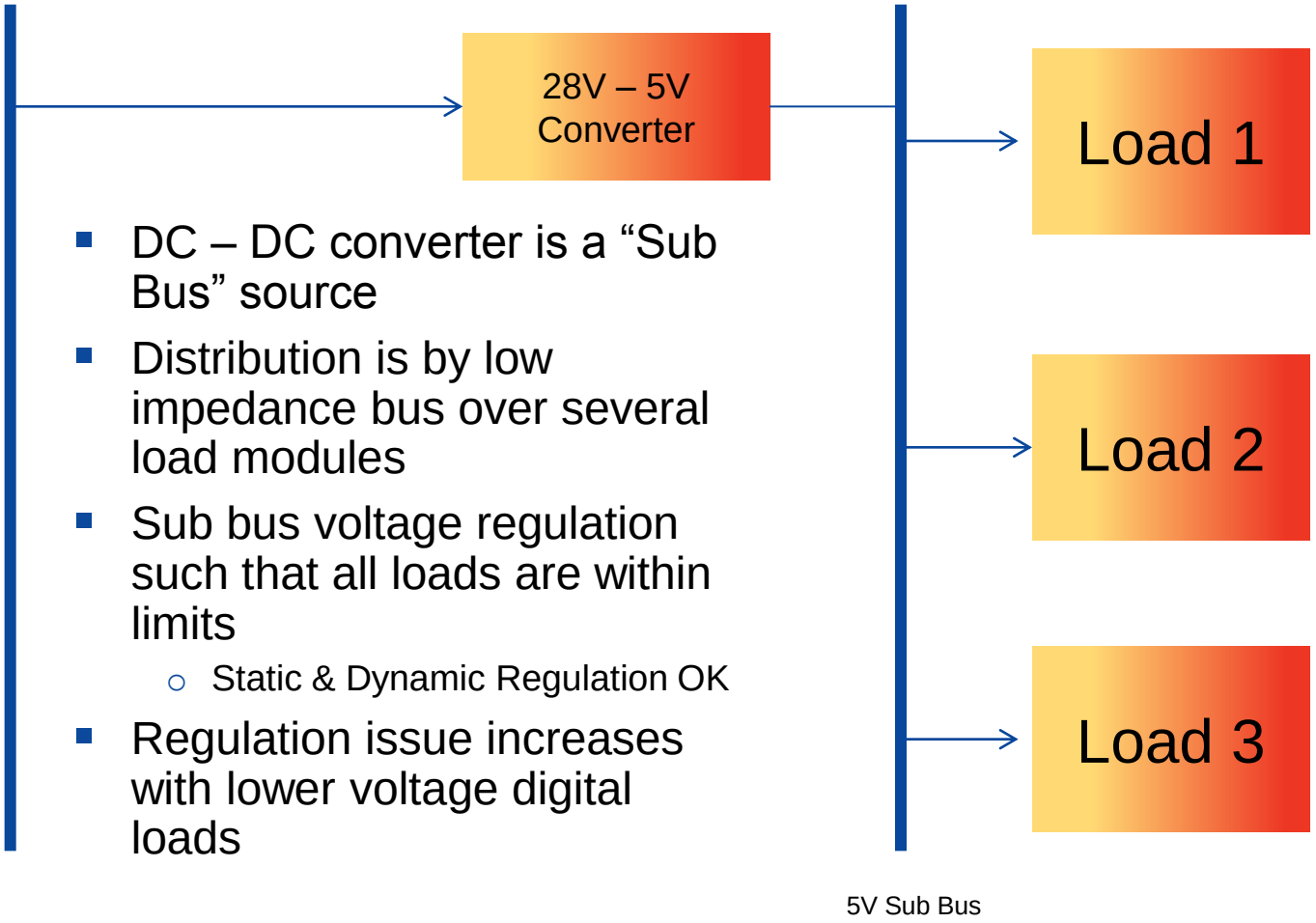
Isolated DC/DC 100V,50V or 28V Bus



Isolated DC/DC 100V,50V or 28V Bus



Traditional Power Distribution



- DC – DC converter is a “Sub Bus” source
- Distribution is by low impedance bus over several load modules
- Sub bus voltage regulation such that all loads are within limits
  - Static & Dynamic Regulation OK
- Regulation issue increases with lower voltage digital loads

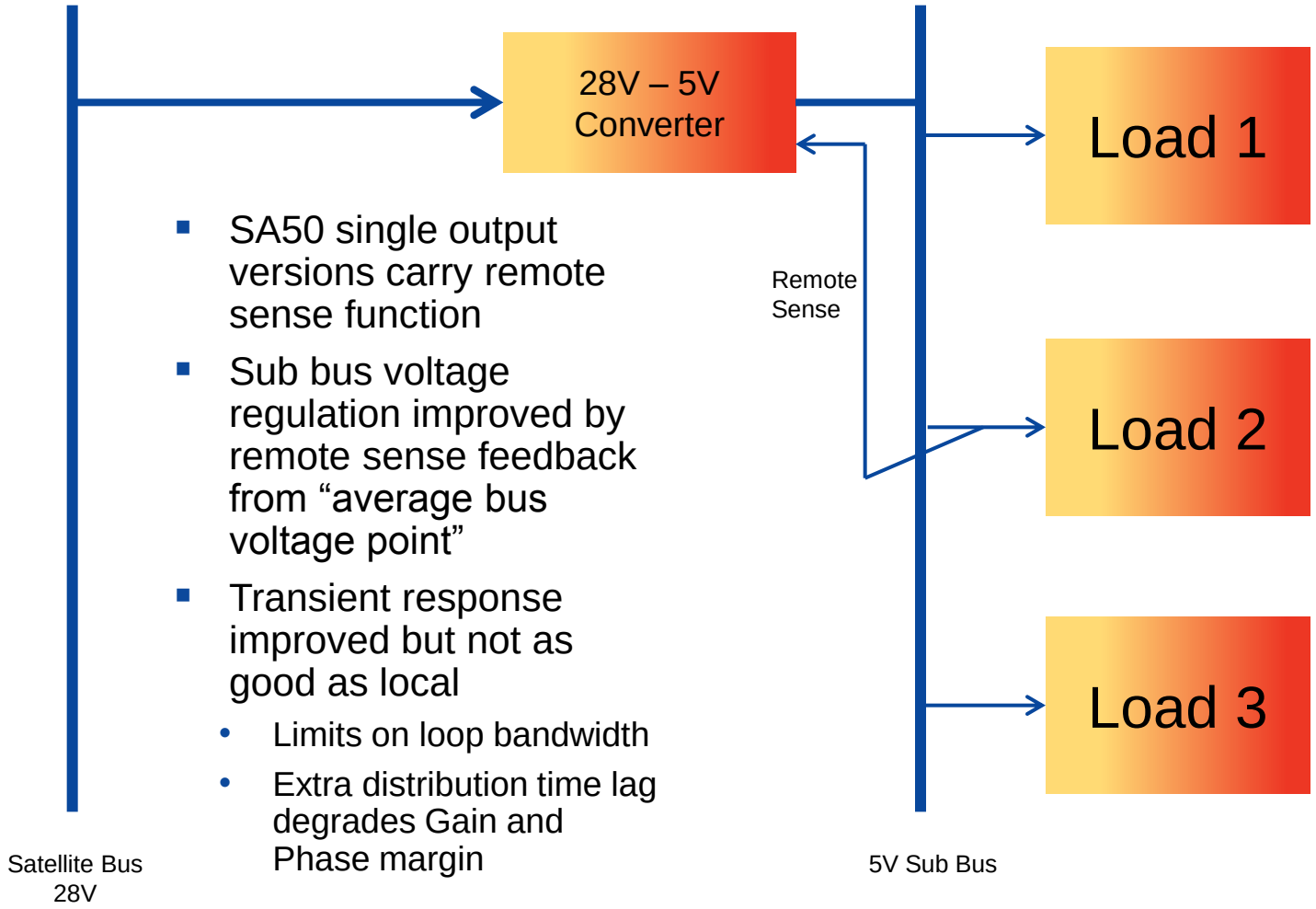
Considerations to Partition the Traditional Solution

Device	Output	Vin (V) +/-%	Vout (V) +/-%	Iout nom (A)	Iout peak (A)	Ripple Specs	Transient Specs	Efficiency at Full Load	Efficiency at x% Load	Sequence at Turn ON	Sequence at Turn Off	Sync Capability
Isolated DC/DC	A											
Isolated DC/DC	B											
Isolated DC/DC	C											
Pol/Linear 1	D											
Pol/Linear 2	E											
Pol/Linear 3	F											
Pol/Linear 4	G											

How to decide the Power Partitioning?

Single-event effects (SEE) during operation of some power regulators can cause the output to be as high as the regulator input for short durations, in the order of tenths of microseconds. Consequently, any device that is powered by the regulator could see this supply glitch during normal operation of the device.

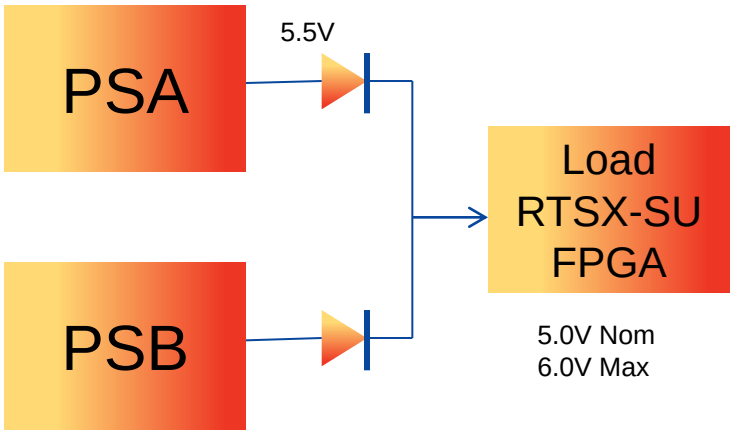
Load Regulation with Remote Sensing



- SA50 single output versions carry remote sense function
- Sub bus voltage regulation improved by remote sense feedback from “average bus voltage point”
- Transient response improved but not as good as local
  - Limits on loop bandwidth
  - Extra distribution time lag degrades Gain and Phase margin

Over-Voltage Protection Considerations

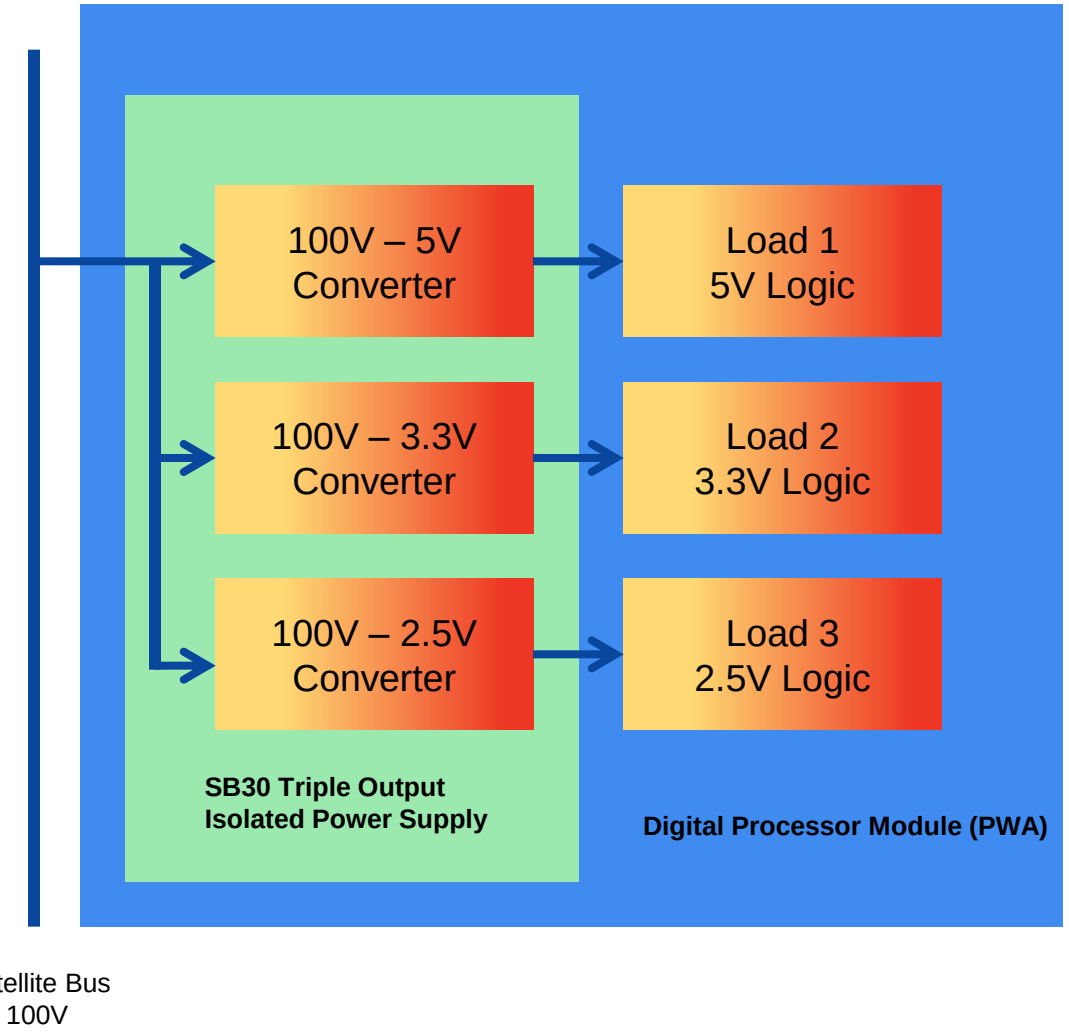
- Over-voltage most important on redundant power systems
  - An overvoltage fault would represent a single point failure
- Over-voltage protection by threshold detection and shutdown
  - Detection needs to be fast to limit voltage rise
  - Detection threshold has to be within Load rating
- Threat of false alarm shutdowns
  - Probability of false alarm increases with lower thresholds and faster response times



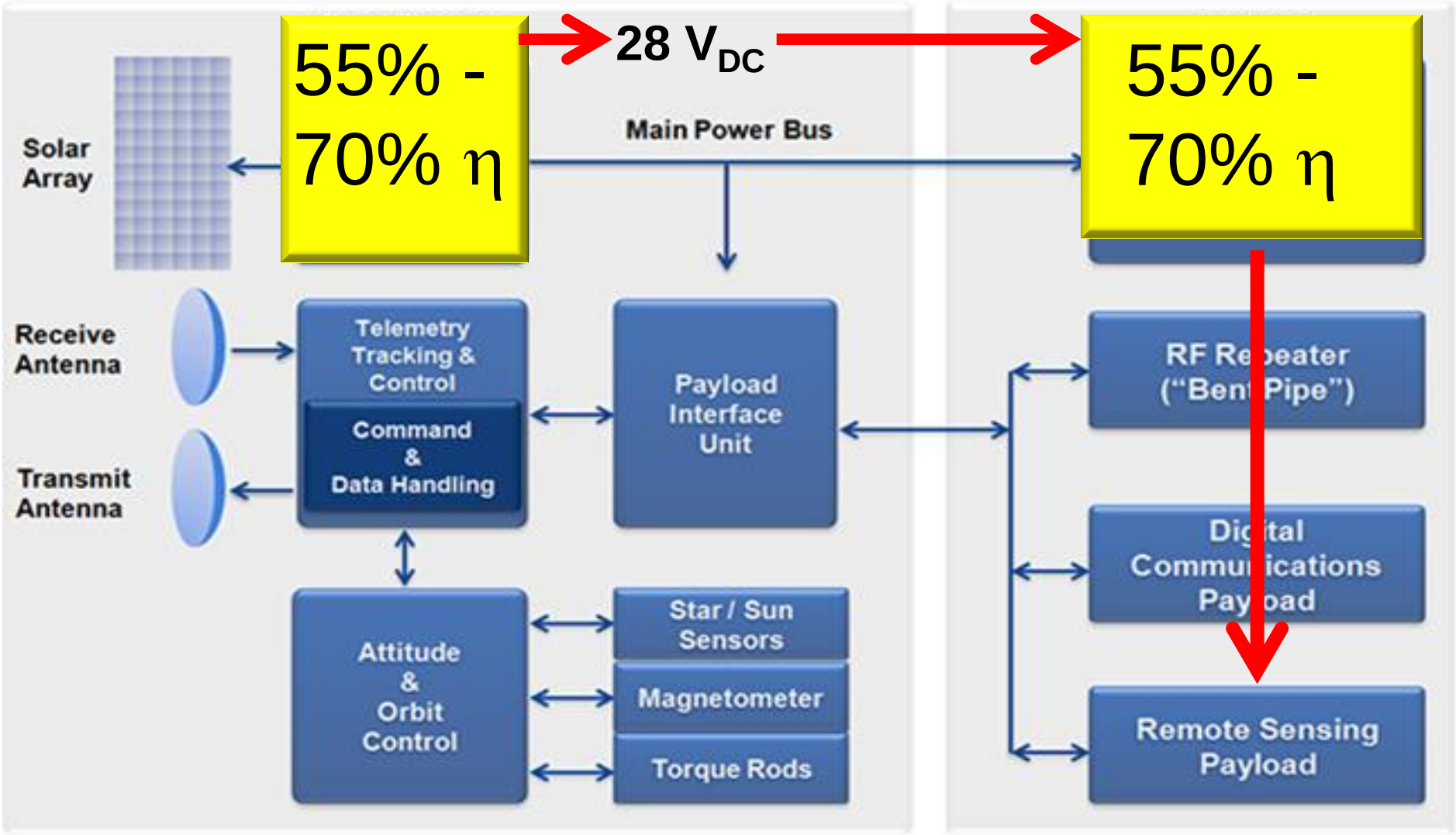
- Worst case analysis leads to OV threshold only 0.5V over highest operating voltage
- Significant risk of false alarm shutdowns from line / load transients
- Need to trade off risk of hard failure of FPGA during an OV event vs risk of False Alarm Shutdowns
- Microsemi has characterized survivability of devices under OV transient conditions. Ask for report
- Power Supply Transients on RTAX-S and RTSX-SU Devices

Point of Load Concept – SB30

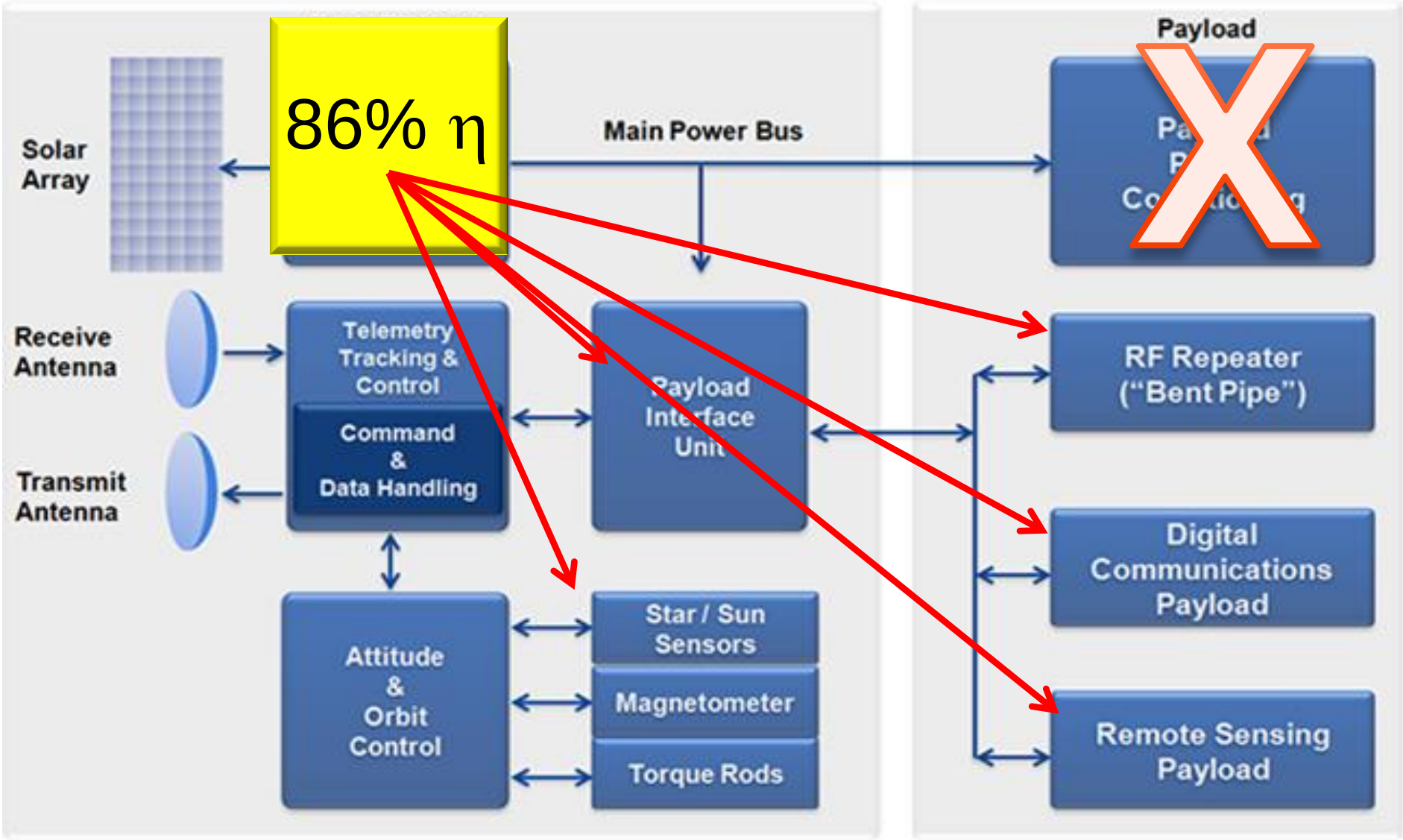
- Module level POL supply
- 3 independently regulated output rails
- Input – Output full galvanic isolation
- On PWA distribution to meet logic load regulation requirements



Legacy Architecture Efficiencies



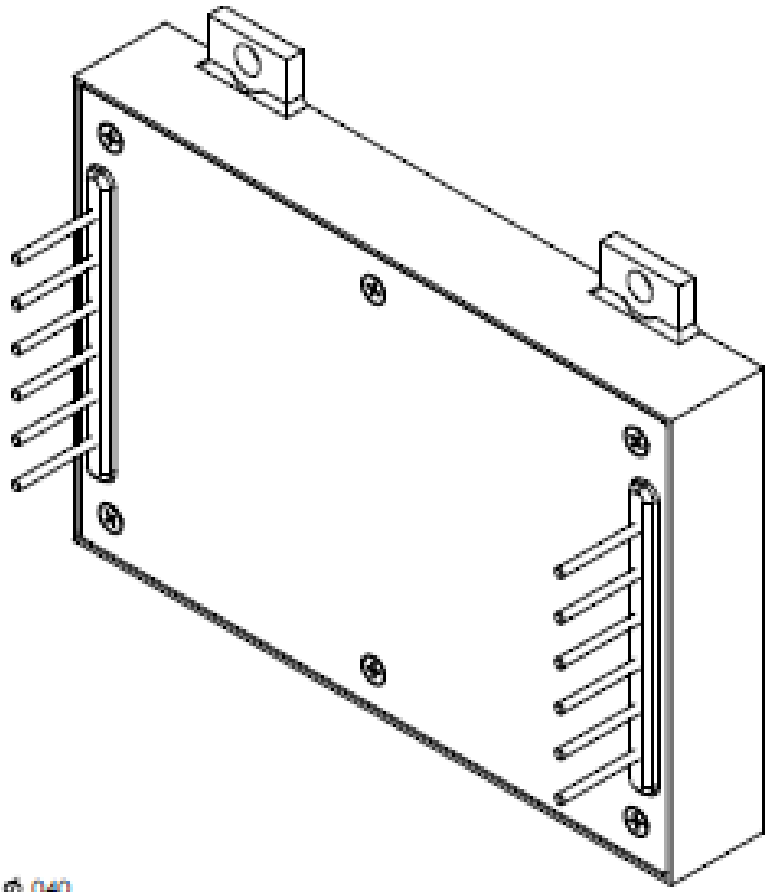
Future Architecture Efficiencies



SB30 Series Concept

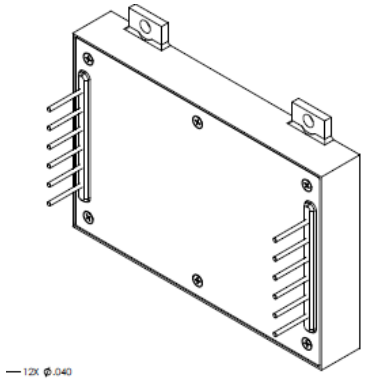
- SMT Construction in an industry standard package

- Samples available 2013
  - Triple Output for Digital Loads
    –5V @ 2A; 3.3V @ 3A; 2.5V @ 3A
  - +28V or 100V nominal Inputs
  - Internal EMI Filter
  - Outputs individually regulated
  - Power Good Status
  - 30W total combined power output
  - Inhibit Feature
  - Isolated Sync Input, 500kHz
  - 75% efficiency
  - Length Width Height
  - 3.055 x 2.055” x 0.60”
  - Total Dose Rating of 200KRads
  - Threshold (LET) with no latch-up
    >80MeV-cm2/mg



Single Event Concerns

- SA50 is SEE immune
  - Outputs remain within regulation limits
- SB30 is SEE immune also
  - All 3 channels remain within regulation
- Downstream POL regulators may have SEE issues
  - Linear regulators go “low impedance pass” at SEE event



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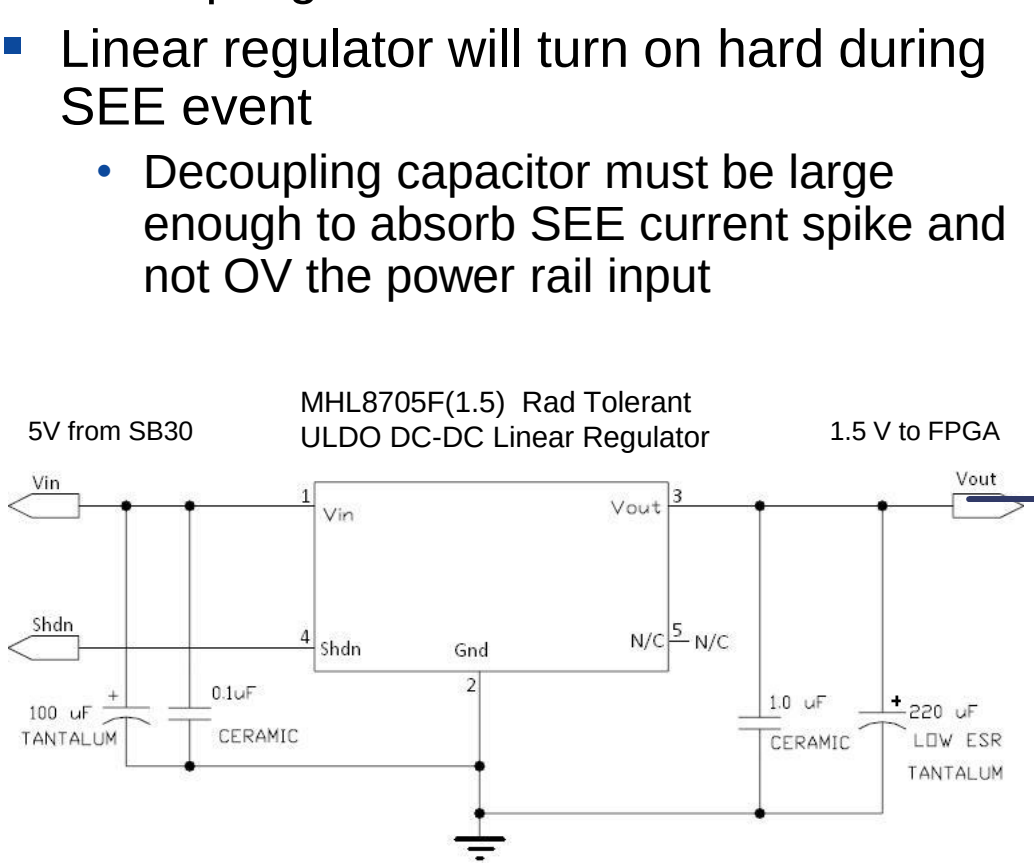
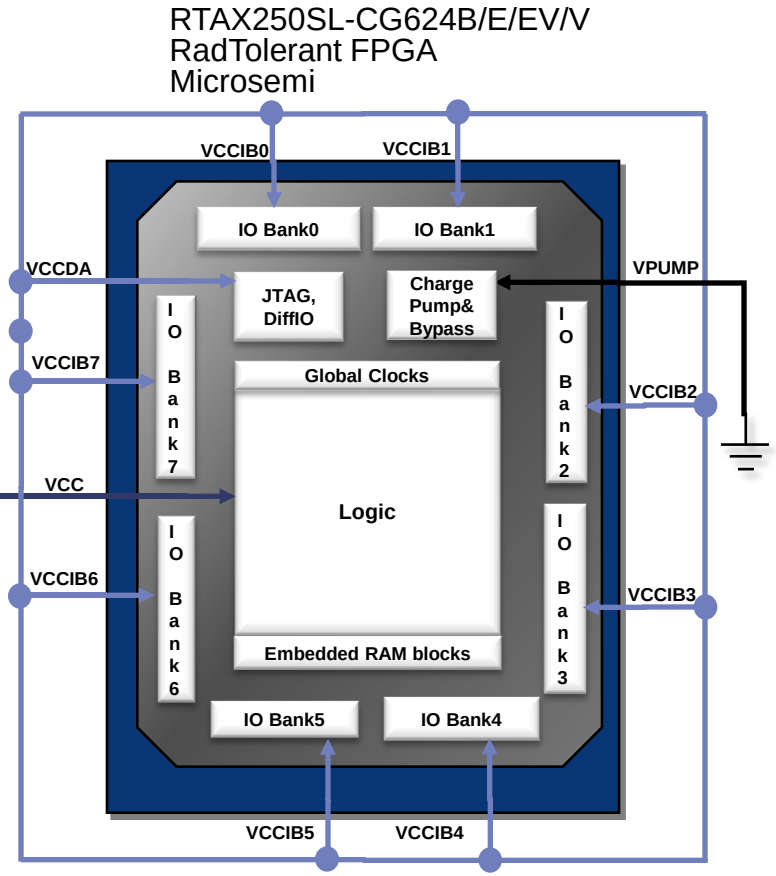
Local Transient Regulation Capacitance

- < 2.5V rails need POL at FPGA device
- 220uF tantalum provides local transient decoupling
- Linear regulator will turn on hard during SEE event
  - Decoupling capacitor must be large enough to absorb SEE current spike and not OV the power rail input





Additional Multi-Output Isolated DC/DC Design Points

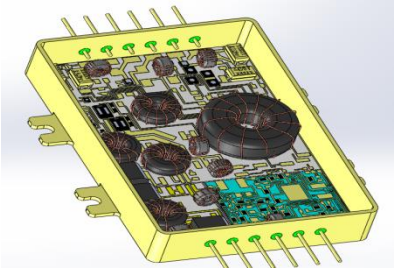
- Main Rail
  - Requires minimum of 5% Loading
- Sequencing
  - Global On/Off Pin
  - Main Rail comes up first, goes off last
  - The two additional rails are predefined in sequence BUT this is customisable
- Synchronization
  - Rails can be synchronized to an external clock with the external sync pin

Hybrid vs. SMT Technology

- Hybrid modules are constructed in certified MIL-PRF-38534 Class H/K facilities

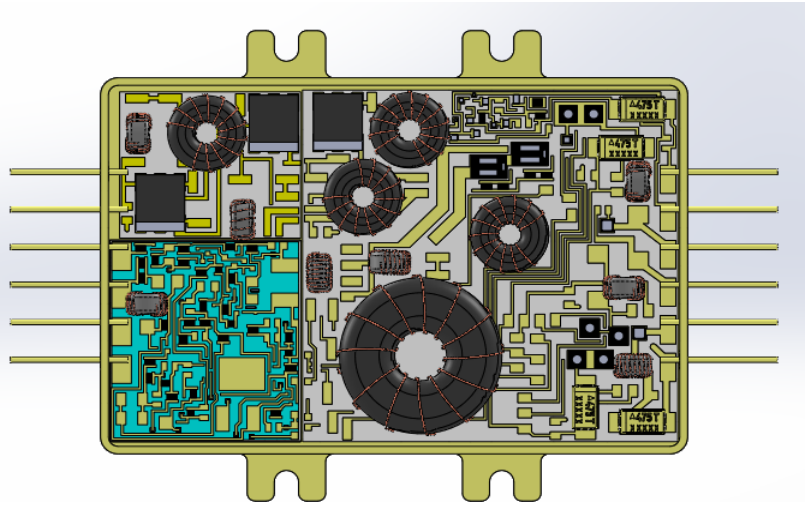
	SMT	HYBRID
Assembly Process	Automated	Manual/Automated
Device Attachment	Solder	Eutectic / Epoxy
Connections	Solder	Wire Bond
Components	Package pre-screened	Basic Die
Certification & Qualification	Internal Qualifications & To NASA Specifications	MIL-PRF-38534 Class K SMD

Hybrid process affords MIL-PRF-38534 Class K performance specification compliance with final submit to DLA for QML/SMD approvals



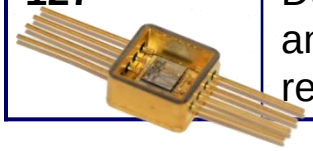
HIP50 Hardened Isolated Power Series (Preliminary)

- Hybrid construction in an industry-standard package
- Drop-in compatible to industry-leading rad-hard hybrids
- Features
  - +28v nominal input
  - Internal MIL-STD-461 compliant EMI filter
  - Triple, dual and single output versions
  - Isolated outputs
  - 50W total combined power output
  - Inhibit feature
  - Isolated sync input, 250kHz
  - Output trim on single & dual variants
  - >82% efficient full load @5 +-15V out
  - Length Width Height: 3.055 x 2.055” x 0.475”
  - Total Dose Rating of 200KRads
  - Threshold (LET) with no latch-up : >80MeV-cm2/mg



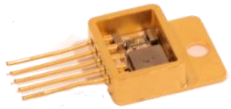
1st Gen POLs & Linear Regulators

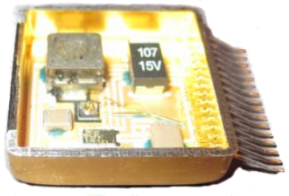
MHQL= Microsemi Qualified

Product	Description	Critical Parameters	Vin Range	Vout Range
8601 **MHQL**	Pos., Linear, 3A Fixed or Adjustable	VLDO = 0.300 V (3A), Rad-Hard to 300Krad+	+3V to +5.5V	+1.26V to +4.5V
8605 **MHQL**	Pos., Linear, 5A, Fixed or adjustable	VLDO = 0.300 V (2A), 0.400 V (5A) RadHard to 300 Krad+	+3V to +5.5V 	+1.26V to +4.5V
8701 **MHQL** **SMD: June**	Pos., Linear, 5A, Fixed or adjustable, SEE = 82 MeV	VLDO = 0.400 V (2A) RadHard to 300 Krad+	+3V to +5.5V	+1.26V to +5.5V
117 **MHQL** 	Pos. Linear, Adj., 1.25A, Vin = 40 V	RadHard to 300Krad	+5V to +37V	+1.21V to +4.5V
127 	Dual, ±1A, Pos. and Neg. Linear regulator	RadHard to 300 Krad	±5V to ±40V	±6.5V to ±37V

1st & 2nd Gen POLs & Linear Regulators

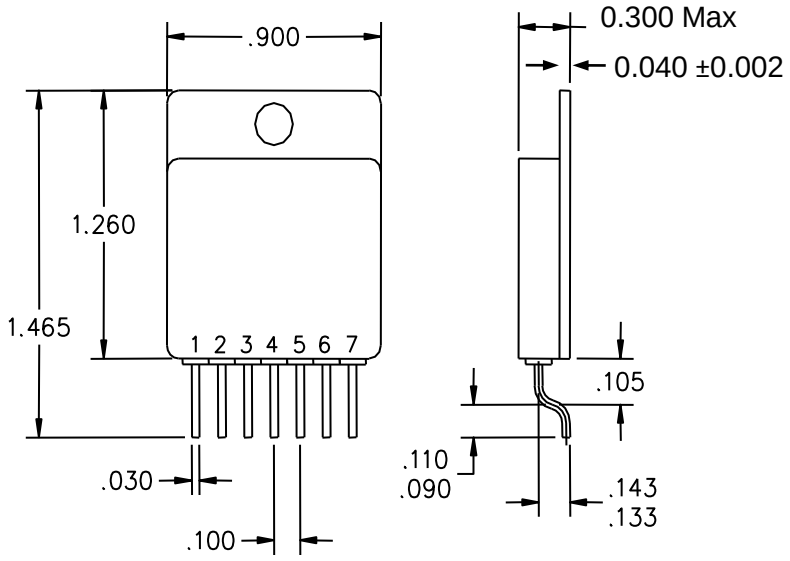
Product	Description	Critical Parameters	Vin Range (De-rated)	Vout Range
8564 **MHQL**	Sw. Reg., 4.5A, Adj./Fixed	300 Krad, Iout= 4.0A	+4.5V to +8V	+1.21V to +4.5V
8565 **MHQL** **SMD: Complete**	Sw. Reg., 3.0A, Adj	300 Krad, Iout = 3.0A	+4.5V to +8V	+1.21V to +4.5V
8566	Quad Sw. Reg., Adjustable Vout, 15A	100 Krad TID, 15A Efficiency, 15A	+4.5V to +8V	+1.0V to +4.5V
MHP9581 (Preliminary info) 2014	*Sw Reg, 12A, 1 MHz., synchronizable*	*300Krad, SEL Immune, Eff= 95% @ 3.3Vout/ Proto: 2014*	3V to +5.5V	O.8V to 3.3V





SET- Me Free 8701

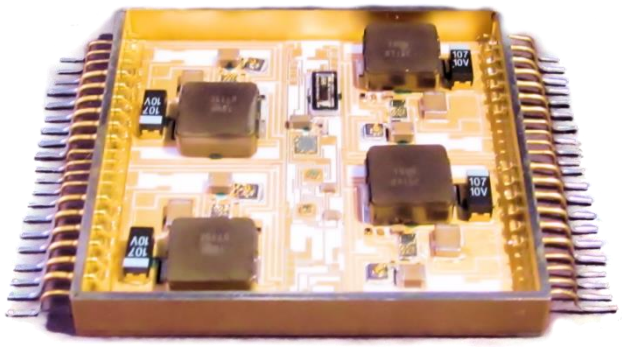
- Increased SEE performance
- SEL immune
- Additional filtering added to output
- TO- 267 package
- All performance features of 8601
- Internal Capacitors per MIL-PRF-123 or MIL-PRF-55365
- Rad-tolerant to 300 Krad TID



PRELIMINARY

Quad POL- MHP8566

- Rad-tolerant to 100 Krad [1]
- Quad adjustable output to +1.21 V.
- Up to 16A output current (total of all outputs)
- Vin Range: +4.5 V to +8 V
  (for +12 Vin consult factory)
  Surface-mount package
  2.0 in. X 2.0 in. X 0.290 in
- Complete assembly – just add voltage set resistors



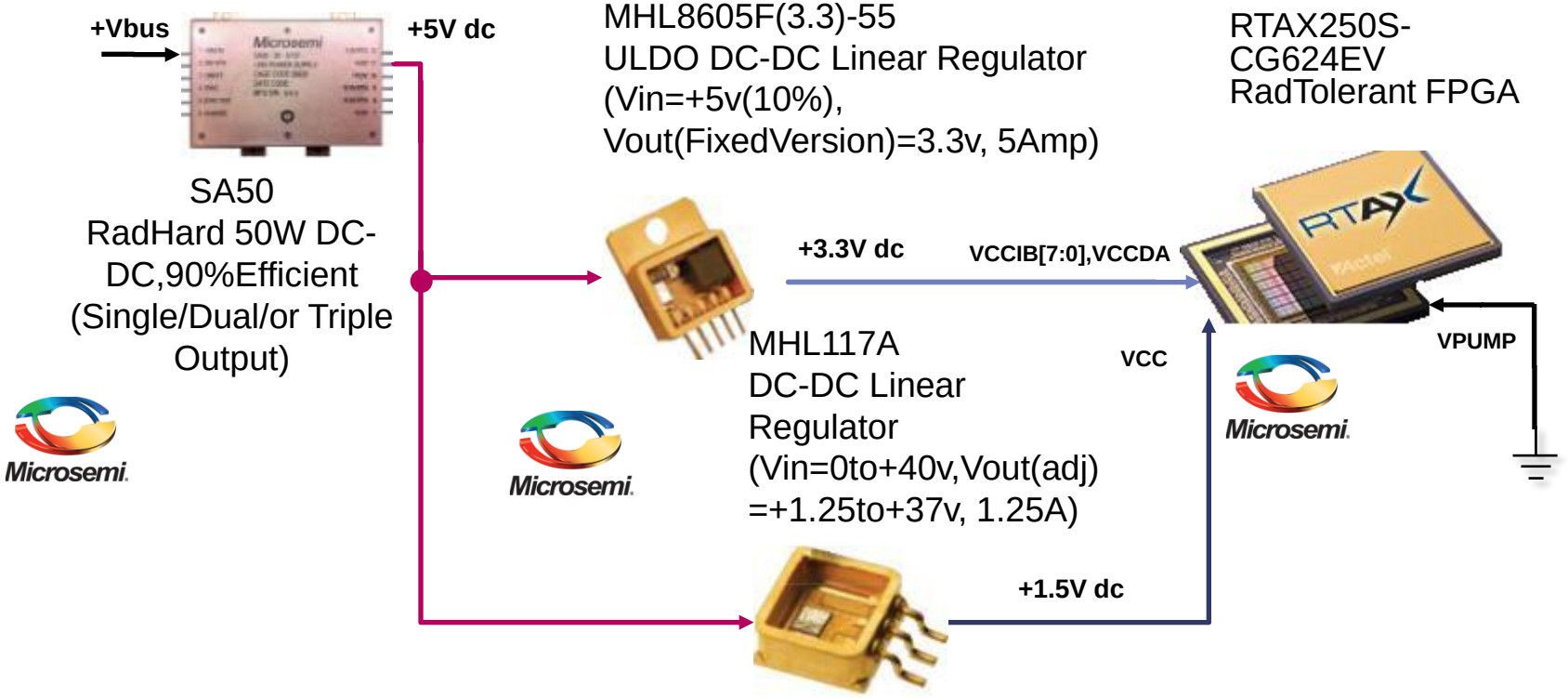
42 pin flat pack = L 82.5 X W 82.5 X H 11.2 mm

Configurable as four, 4A POLs or one 16A POL

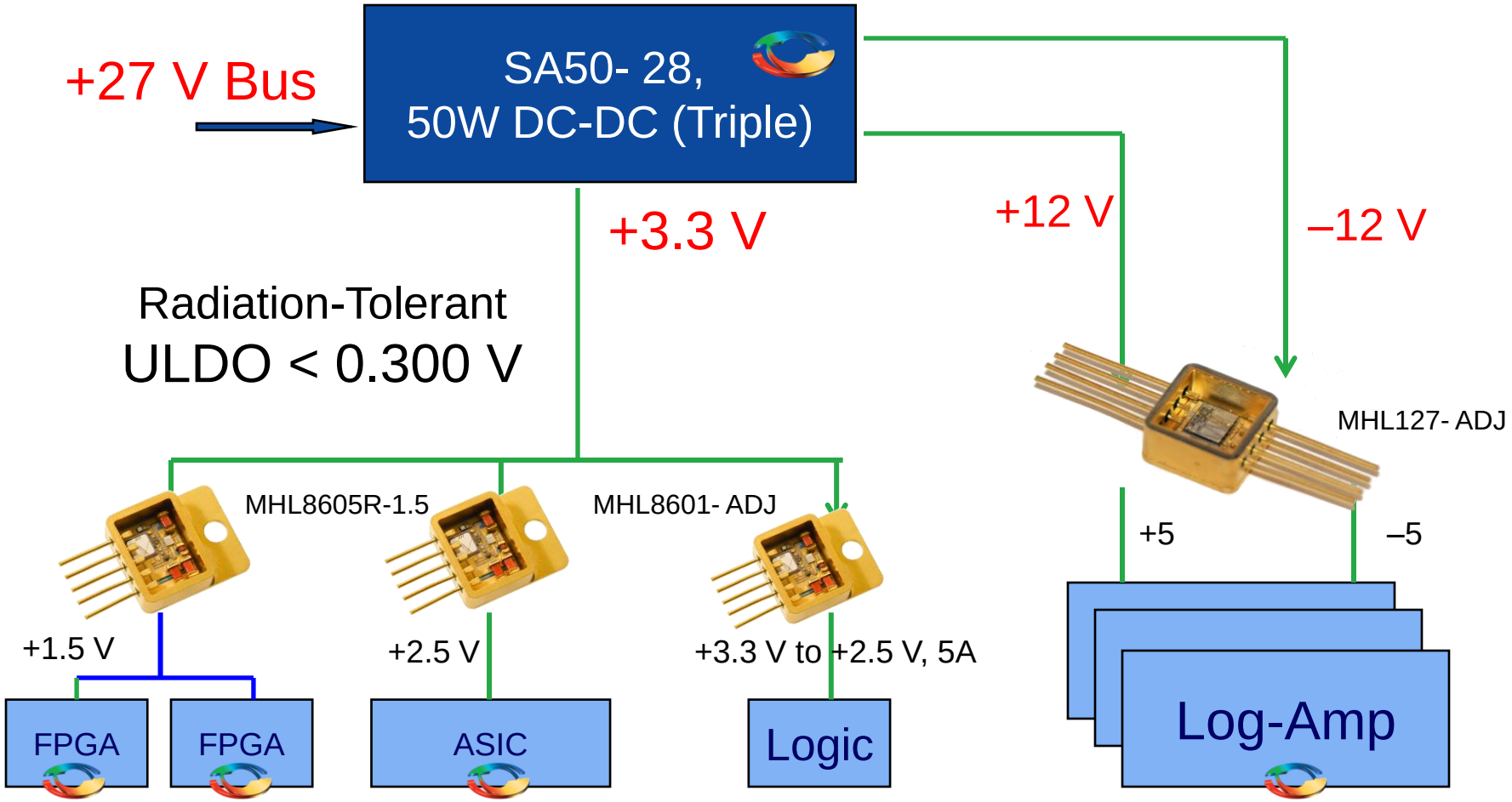
*****FPGA Power Supply*****

Space Products

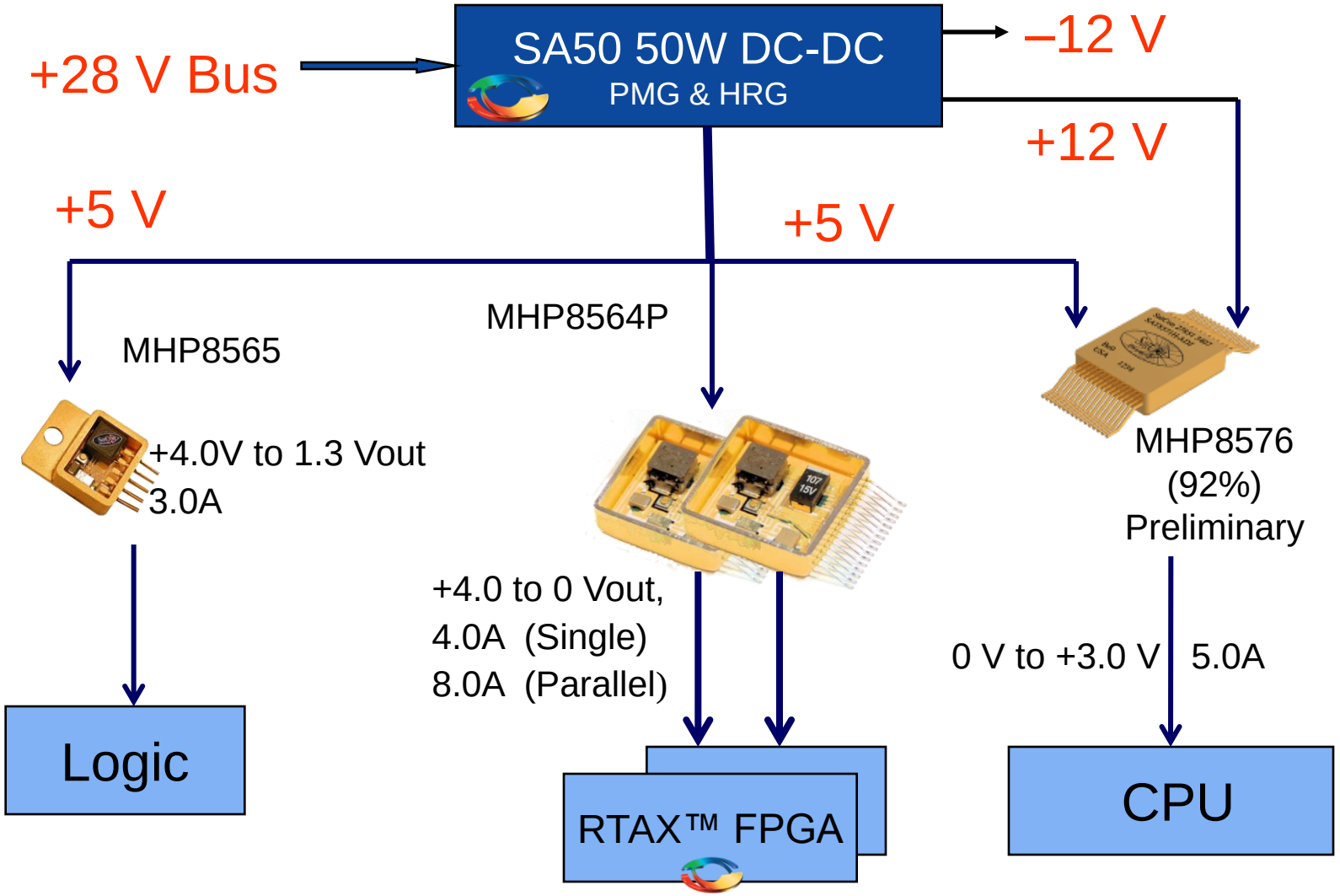
PRODUCT STRATEGY – COMPLETE SUPPLIER



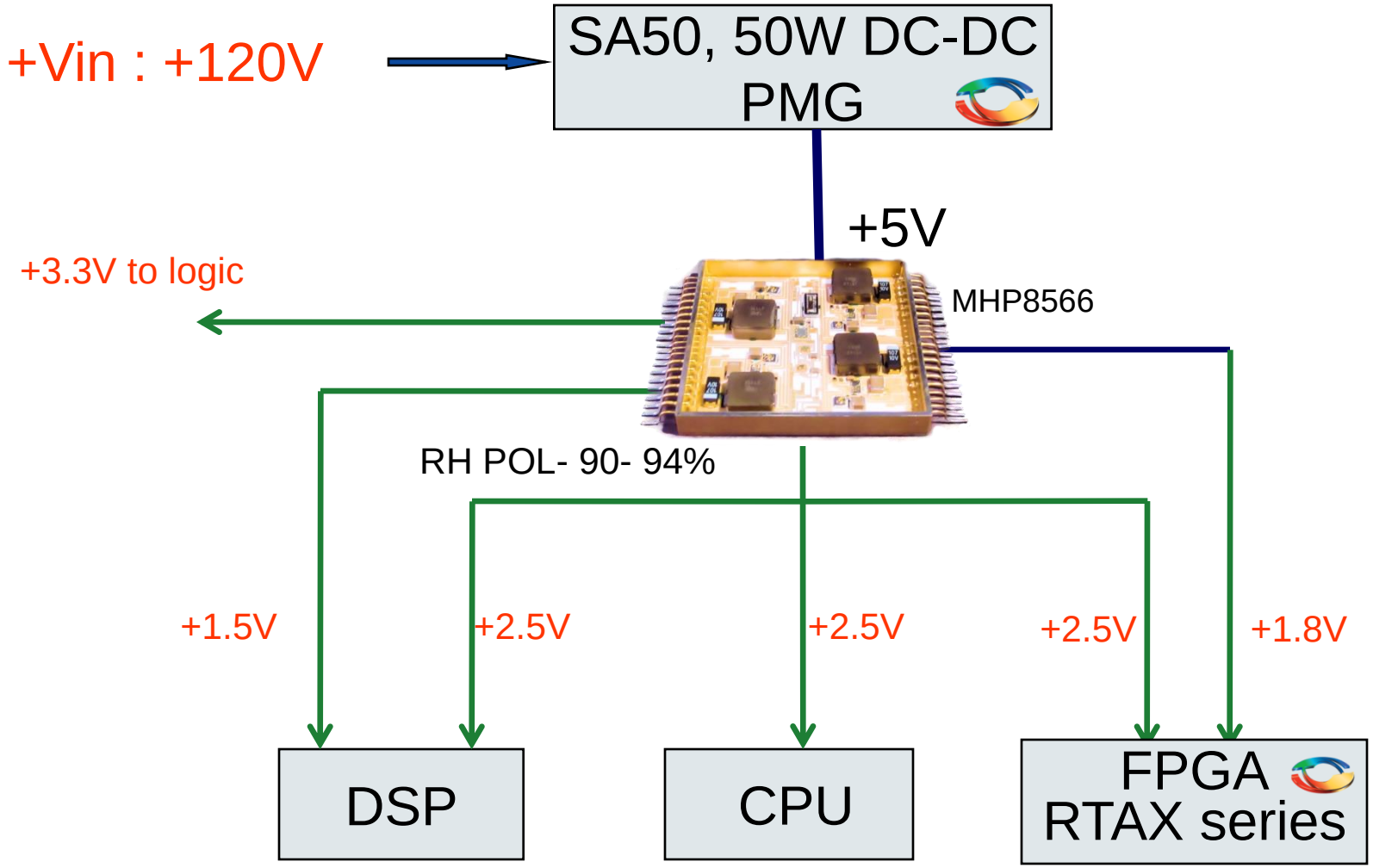
SA50 + Linear Application Example



SA50 + Switching Application Example



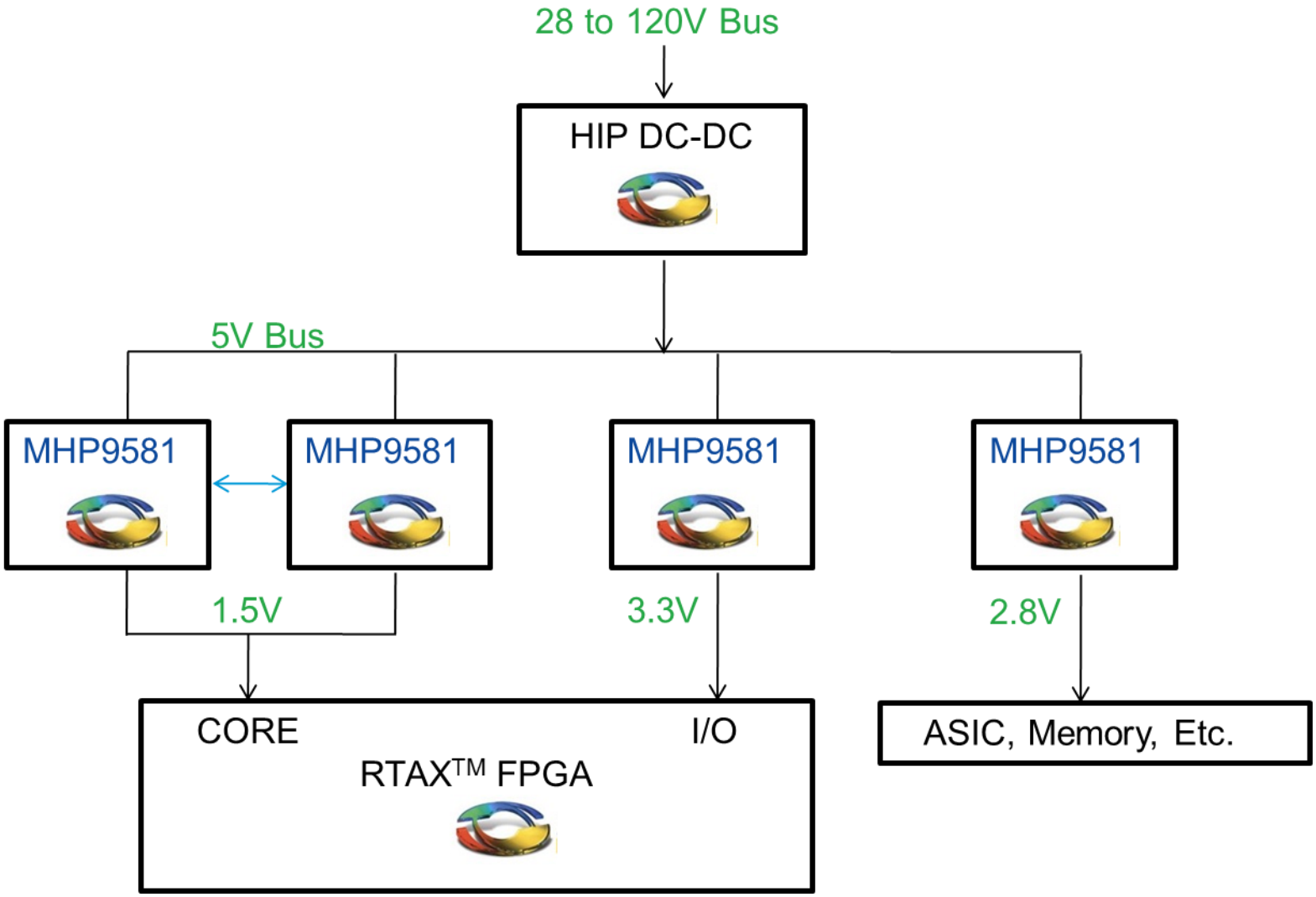
SA50 + Switching Multi-Rail Application Example



MHP9851 12A PoL in development

- Input voltage range: 3 to 5.5V
- Programmable output: 0.8V to 90% of the input voltage
- +/- 1% output voltage accuracy
- High efficiency; up to 94%
- 20 mohm high & low side MOSFETs
- 500 kHz switching frequency
- Up/down synchronization to external clock
- Active current sharing and phase delay implements up to 4 phase 48 Amp POL
- Average current mode control provides reliable PWM
- Soft start
- Enable input and Power Good output provides sequencing and fault detection
- Micropower sleep mode
- Pre-Bias start-up
- Fully protected against over-current and over temperature
- Radiation Hardened; 200Krads TID, 100Krad ELDRS, 85 MeV SEU
- No Latch-up under Single Event conditions

Typical MHP9851 Application



Microsemi

Thank You