Power Matters

Microsemi

Prototyping Solutions for Microsemi Radiation Tolerant FPGAs

MICROSEMI 55 YEARS in SPACE 1957-2012

Microsemi Space Forum Russia – November 2013

Alexander Bukhteev
Chief Technology Officer, StreamLine Design Solutions

ALDEC THE DESIGN VERIFICATION COMPANY

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Aldec Overview

- Founded 1984
- Privately Held, Profitable
- Employees 150+
- Aldec Solutions
  - FPGA DESIGN
  - ADVANCED VERIFICATION
  - DESIGN RULE CHECKING
  - HIGH-LEVEL SYNTHESIS
  - EMULATION/ACCELERATION
  - REQUIREMENTS MANAGEMENT
  - ASIC/SoC PROTOTYPING
  - MIL/AERO SOLUTIONS
  - IP CORES
- World-class Training and Resources
- Over 30,000 Licenses Worldwide
- Key Technology Patents

Office Locations:

- Aldec N. America (Corp. Headquarters)
- Aldec Europe
- Aldec Japan K.K.
- Aldec China
- Aldec India
- Aldec Taiwan
- Aldec Israel
- Global Support and Distribution

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Aldec Solutions

Riviera-PRO™

Advanced Verification Platform

Active-HDL™

FPGA Design and Simulation

ALINT™

Design Rule Checking

CyberWorkBench®

High-Level Synthesis and Verification

HES-DVM™

HW/SW Validation Platform

Spec-TRACER™

Requirements Lifecycle Management

DO-254/CTS™

FPGA Level In-Target Testing

HES-7™

SoC/ASIC Prototyping

RTAX/RTSX

Prototyping Microsemi™ Rad-Tolerant Devices

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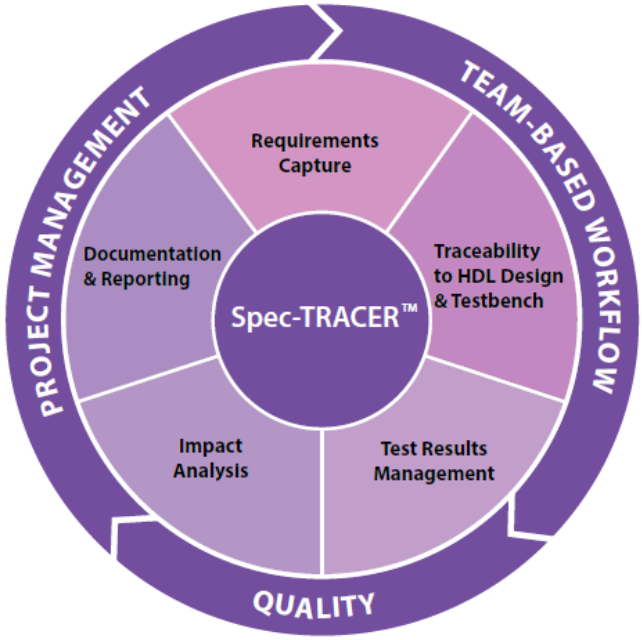
Spec-TRACER™

Requirements Lifecycle Management for FPGAs and ASICs

- Facilitates requirements capture, management, analysis and traceability
- Traceability to HDL design, testbench, log files and waveforms
- Compliance to safety-critical standards: DO-254 for avionics, ISO 26262 for automotive and IEC 61508/61511 for industrial



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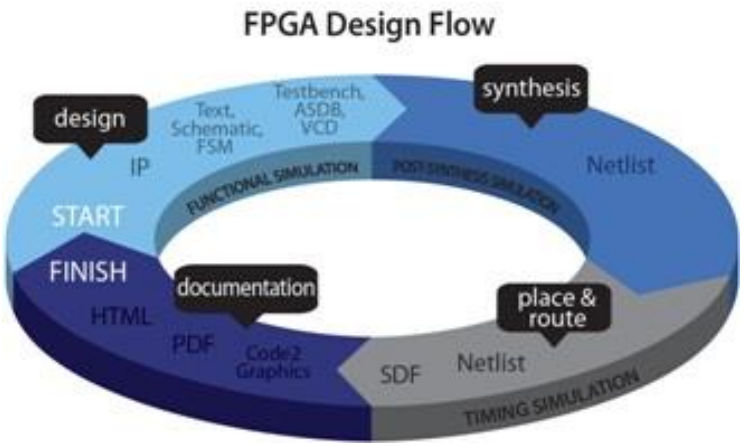
Active-HDL™

Windows® based, integrated FPGA Design Creation and Simulation solution for team-based environments

- IEEE VHDL, Verilog, SystemVerilog (Design)
- Multi-FPGA & EDA Tool Design Flow Manager
- HTML and PDF Design Documentation
- Graphical Design Entry & Editing
- Windows 7/XP/Vista/2003



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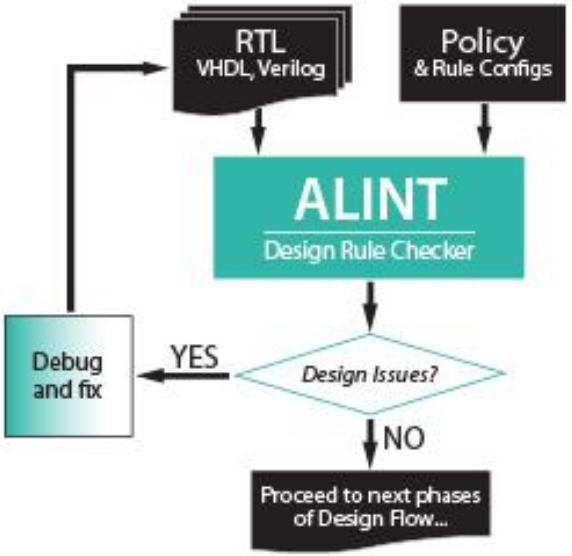
ALINT™

Design analysis tool that decreases verification time dramatically by identifying critical issues early in the design stage

- Industry-leading Rule Libraries: STARC, RMM, DO-254
- Early Bug Detection during RTL Design Phase
- IEEE VHDL, Verilog, Mixed-Language Designs
- IDE for In-Depth Design Troubleshooting
- Windows 7/XP/Vista/2003, Linux – 32/64-bit



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RTAX-S/RTSX Prototyping

- Prototyping is an important step in design verification
  - Assists in identifying problems with the design that were not detected during simulation
  - Increases design quality
  - Reduces costs

- Due to one time programmability and high cost of RTAX-S/RTSX devices, prototyping using the traditional approach (prototype uses the same device as final product) may be costly. Alternative methods are used instead

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Traditional Prototyping Solution

- Same family FPGA (AX)
- One time usable socket
- One time programmable device
  - Re-programmable only by replacing FPGA in the socket
- Moderately expensive
  - Socket ~$1000
  - Device ~$300
- Possibility for a bad mechanical connection between the device and the socket
  - Quick test must be run to verify good device insertion
  - Device may have to be reinstalled to correct problems

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Generic FPGA Prototyping Solution

- Numerous FPGA devices can be used
- Dual footprint board layout
- Generic FPGA vendor not the same as target device vendor
  - Different libraries/macros
  - Different device timing
  - Different tools
- May require additional components
  - EEPROM/PROM
- Re-programmable
- Lower cost

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Prototyping Adapter by Aldec, Inc.

- Pin to pin compatible adapter
  - Supports CQ208, CQ256, CQ352, CG624, CG1152, CG1272 packages
- Re-programmable
- Designed to prototype
  - RTAX1000S/SL
  - RTAX2000S/SL
  - RTAX4000S/SL
  - RTAX4000D
- Re-usable from project to project in most cases
- Netlist Converter for easy transition from RTAX-S/RTSX design to reprogrammable device on the adapter

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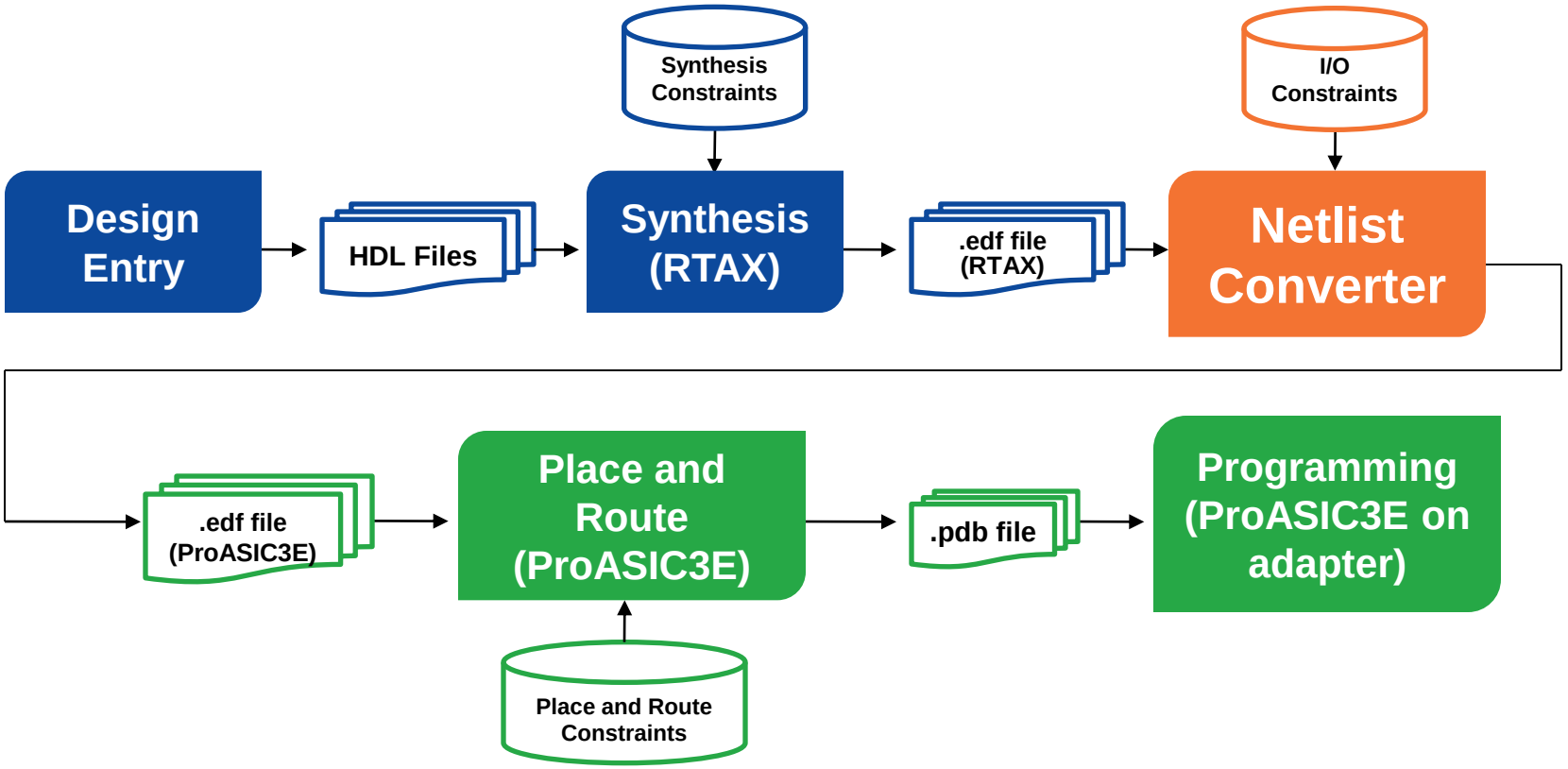
Netlist Converter

- Converts RTAX EDIF netlist to ProASIC3E EDIF netlist
- Converts RTAX I/O constraints (.pdc file) to ProASIC3E I/O constraints



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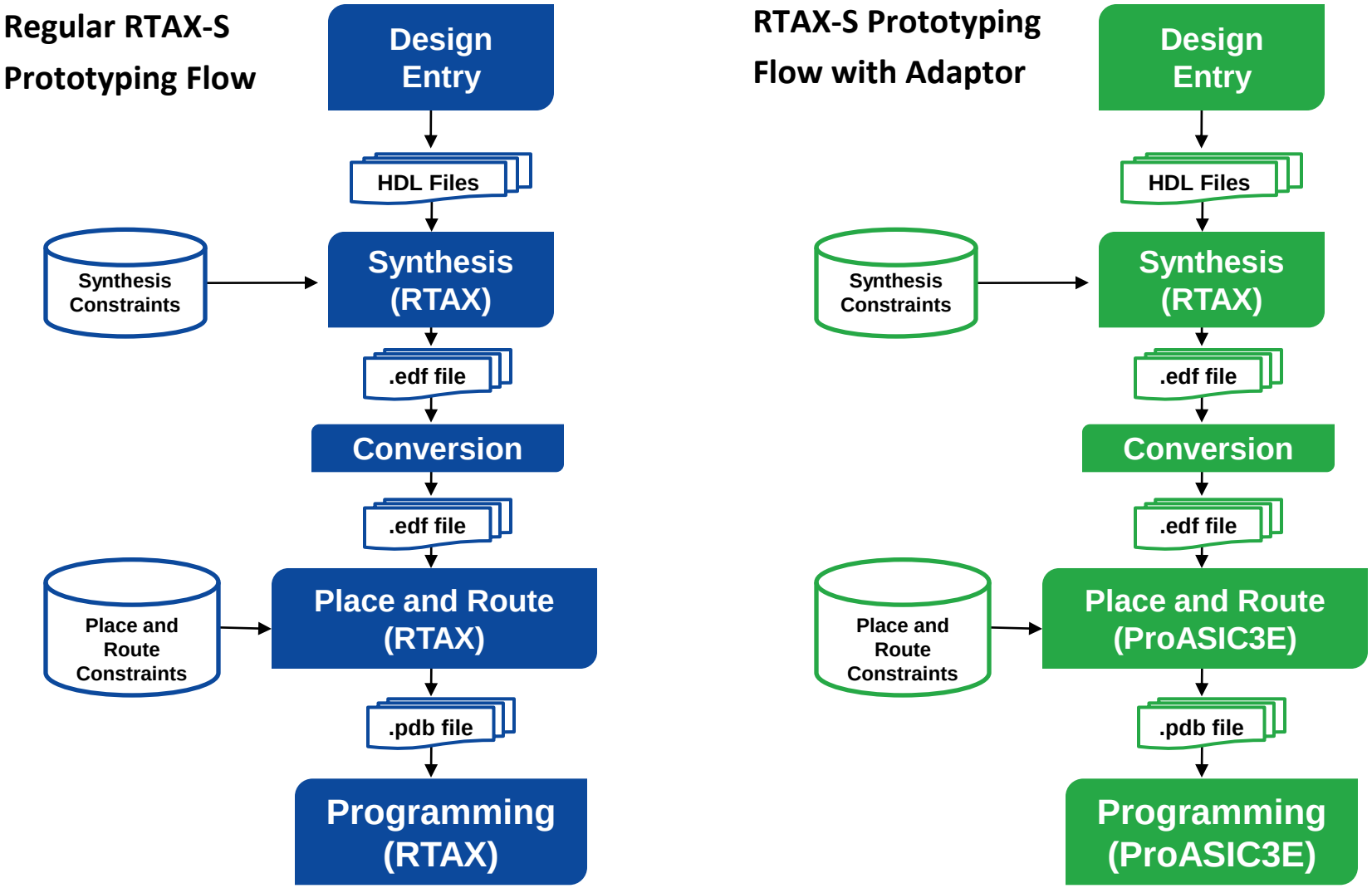
RTAX Prototyping Flow



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Samples of Adapter Options

ACT-H600-CQ208

ACT-H3K-CQ256

ACT-H3K-CQ352

ACT-H3K-CG624

ACT-H4K-CQ352

ACT-RTSX-CQ208

ACT-RTSX-CQ256

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Aldec Prototyping Customers

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Summary

Advantages

- In-system Programmable
  - Programmable via a JTAG port
- Re-programmability
- Faster design cycle
- Pin-to-pin compatibility
  - No dual footprint PCBs
- Tested by scores of companies using multiple units with some using in excess off one hundred units
- Manage OTP parts lead time and availability issues
- Saves time, man hours and money

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Thank you

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Solutions

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