Power Matters.

Microsemi

Radiation Characterization & Mitigation Techniques

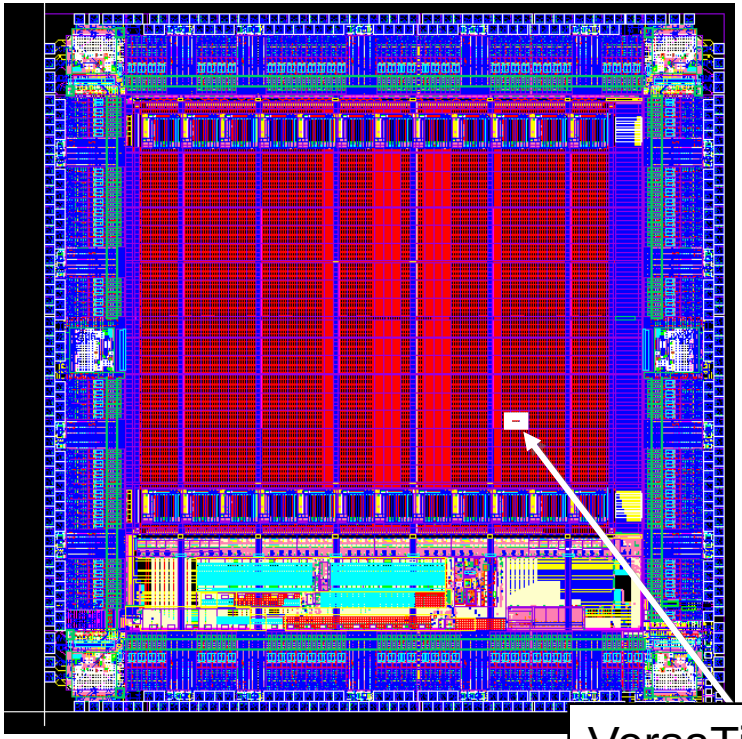
Microsemi Space Forum Russia – November 2013

Ken O'Neill
Director of Marketing, Space and Aviation, SoC Products Group

Agenda

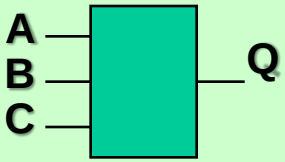
- RT ProASIC3 FPGAs Overview
- Total Ionizing Dose (TID) Effects in Flash FPGAs
- Temperature Effects in Flash FPGAs
- TID Experiments in High Temperature
- Summary

RT ProASIC3 FPGAs Overview

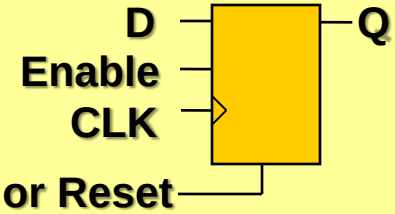


- 130-nm Flash Technology from UMC
- Reprogrammable
- Retain configuration in heavy ion radiation, unlike SRAM FPGAs
- Up to 75,264 VersaTiles
- Flexible core power supply 1.2 to 1.5 V
- Ultra low power in Flash*Freeze mode
- Qualified to MIL-STD-883B
- QML-Q qualification planned for 2014

Any 3-Input Combinatorial Function



D Flip-Flop With Enable and Set or Reset



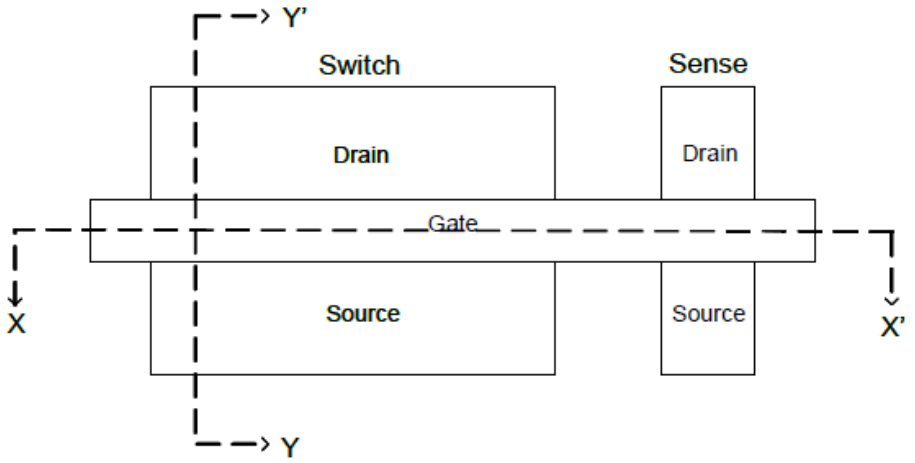
RT ProASIC3 Resources

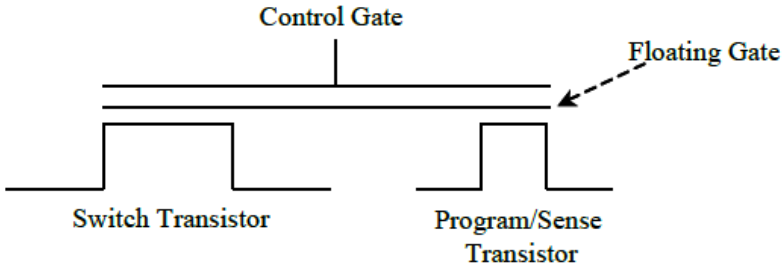
	RT3PE600L	RT3PE3000L
System Gates	600K	3M
Tiles	13,824	75,264
Total RAM bits	108K	504K
Flash (ROM) bits	1K	1K
PLLs	6	6
Globals	18	18
Maximum IO	270	620
Packages *(Availability)* CQFP CCGA/LGA	 256 *(NOW)* 484 *(NOW)*	 256 *(NOW)* 484 *(NOW)* , 896 *(NOW)*
STATUS	***Mil Std 883 Class B Qualification Complete***	

- Prototype with low-cost commercial ProASIC3 devices today
  - Identical silicon, identical timing
    - Plastic FG484 and FG896 match Ceramic CG484 and CG896 footprint
    - RT-PROTO versions are available NOW

Flash Transistor Overview

- Floating gate holds switch transistor in “on” or “off” state
- Switch transistor connects routing tracks and logic modules
- Charge on floating gate controls V_T of switch transistor
- Sense transistor allows programming and monitoring of charge on floating gate





Post-Irradiation V_T Shift in MOS

- Historical data shows that V_T shift recovers with room temp annealing
- Microsemi experiments are intended to show the effects of high temperature exposure during irradiation on V_T shift

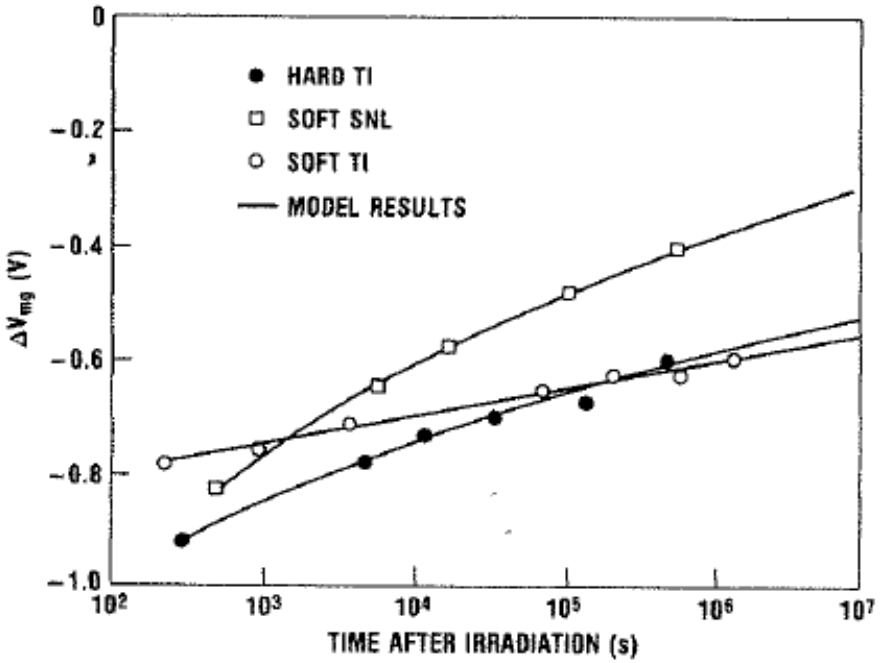
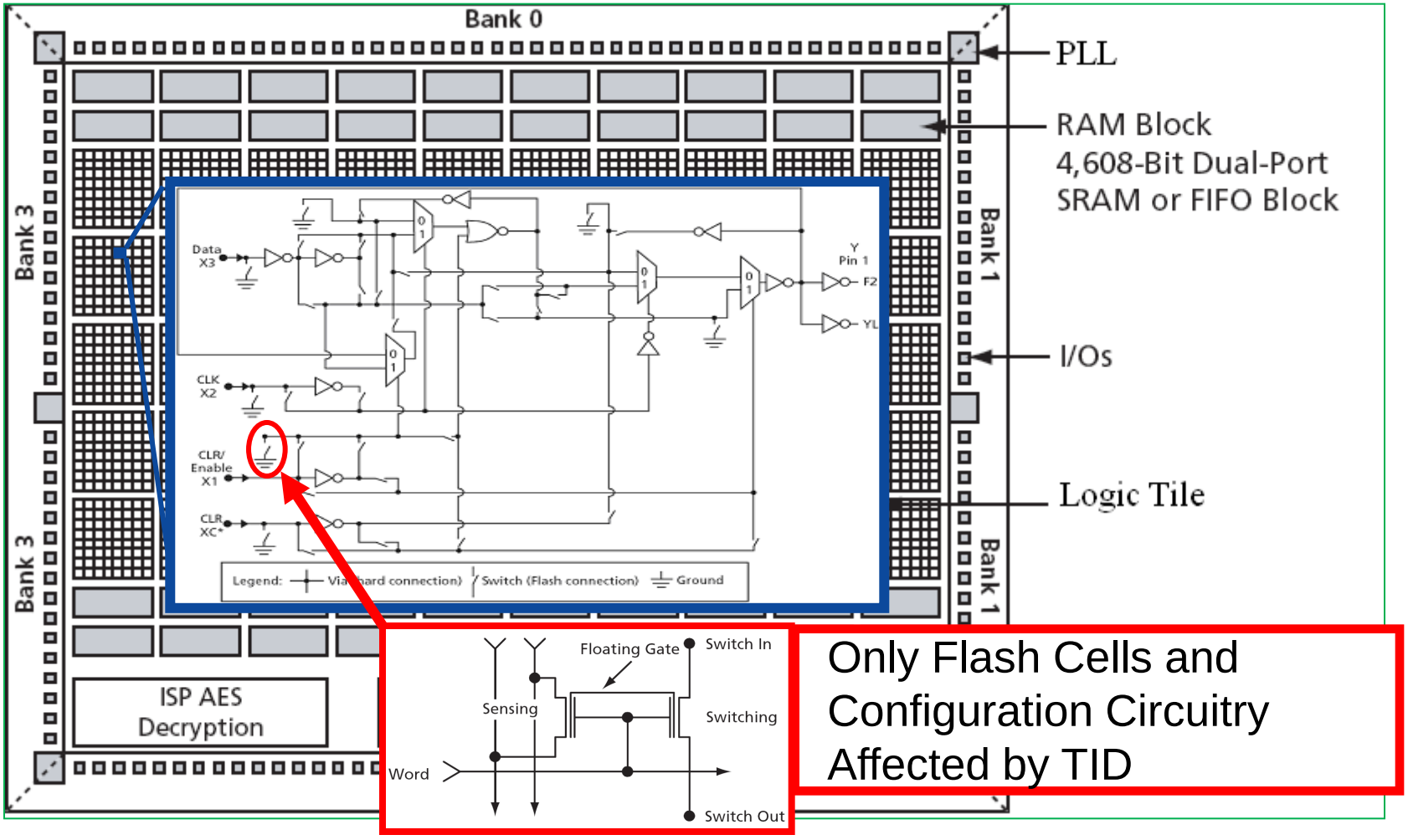


Fig. 3.33 Time dependence of the room temperature annealing of ΔV_{mg} in three oxide layers with different oxide processing. The solid curves are tunneling model fits to the data for "hard" and "soft" samples from Texas Instruments Corp. (TI) and a "soft" sample from Sandia National Laboratories (SNL). (From Oldham et al. [145], © 1986 IEEE. Reprinted with permission.)

TID Effects in Flash FPGAs



TID Effects in Flash FPGAs (cont.)

- TID only affects Flash cells and configuration circuitry
  - TID affects the amount of charge deposited on the floating gate of the Flash cells, resulting in transistor threshold voltage (V_T) shift
  - V_T shift of High Voltage (HV) pass transistors degrades propagation delay
    - HV pass transistors are used to implement connection between logic modules and routing tracks
    - These transistors have large V_T shift because of thick oxide to pass high voltages during programming

$\Rightarrow$TID degrades propagation delay through the pass transistors

- TID does not affect the embedded Flash ROM (FROM) as there is no passing of logic levels in the FROM
  - FROM only switches states between logic 0 and 1

- TID does not affect SRAM, PLL, I/O and I/O bank

Temperature Effects in Flash FPGAs

- Temperature affects Flash data retention
  - Data retention is limited by leakage current through the oxide
    - Higher temperature causes higher leakage
  - Leakage can flip a programmed cell to an erased cell causing verify errors
  - Leakage can also cause tail bits – cells which erase faster than normal cells causing verify errors

Tj (°C)	HTR Lifetime (yrs)
70	102.7
85	43.8
100	20.0
105	15.6
110	12.3
115	9.7
120	7.7
125	6.2
130	5.0
135	4.0
140	3.3
145	2.7
150	2.2

RT ProASIC3 High-Temperature Data Retention (HTR) Lifetime

TID Experiments in High Temperature

- **Experiment Goals**
  - Show reliability of Flash cells under TID and other stressful factors of space environments such as high temperature
  - Collecting more life test data on RT ProASIC3 FPGAs

- **Experiment Setup**
  - Used Gamma ray chamber with one step irradiation to 30 Krad, up to 60 Krad
  - Measured every Flash cell's V_T before and after irradiation
    - V_T is defined at 20 µA
  - Collected data until after 1000 device hours

Experiment Results

- **Test conditions**

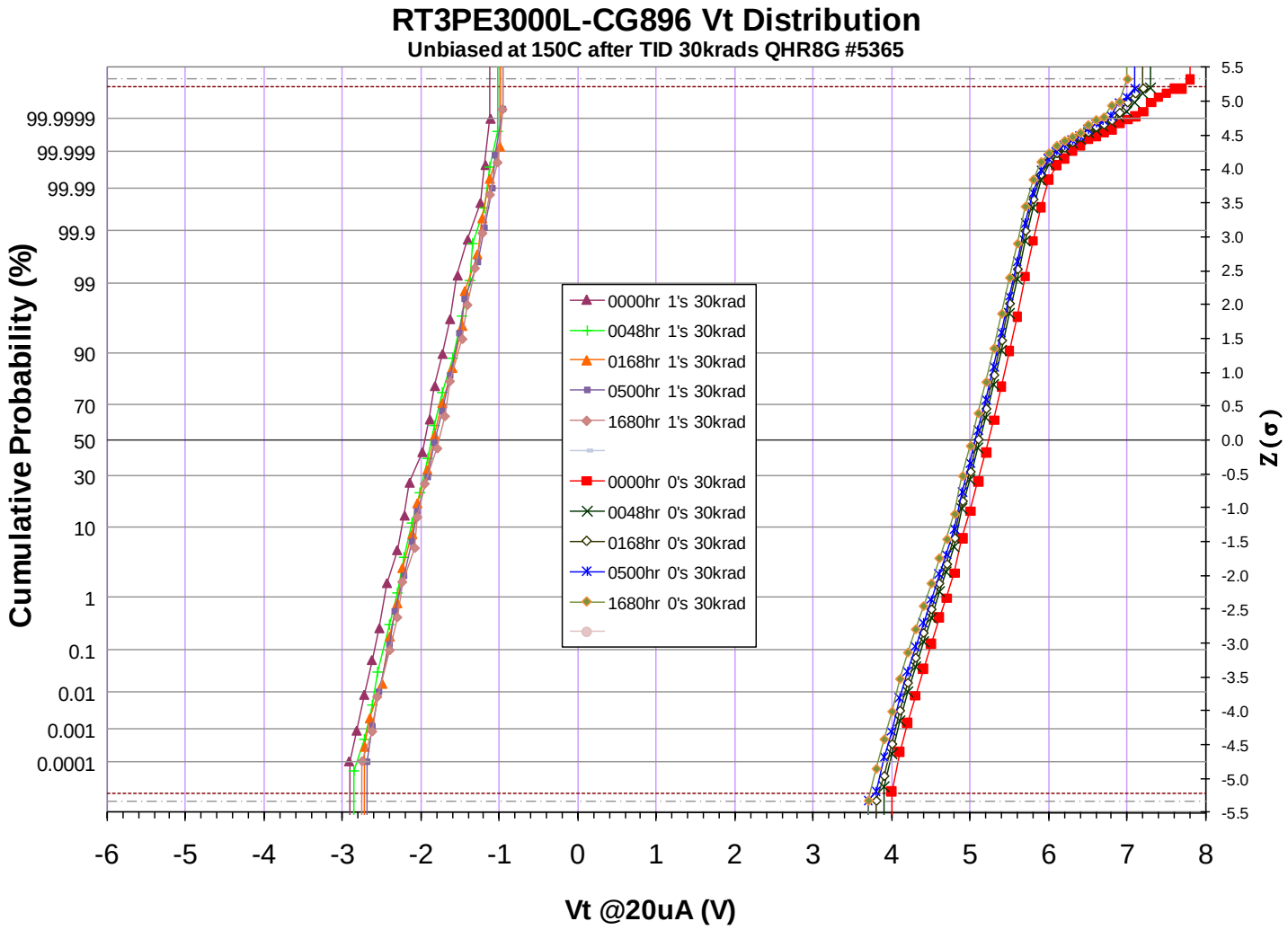
RT3PE3000L TID + High Temp Retention

Thermal	Electrical	Sample Size	Status	TID Dose	Reference	Fab lot#	Package	Note
150°C	Unbiased	6	1000h done	30 Krads	HTS data	QHR8G	CG896	2nd lot test
125°C	Unbiased	4	500h done	0~60 Krads	-	QJA2G	CG484	1st lot test dose varied
125°C	Biased	3	500h done	30~50 Krads	HTOL data	QJA2G	CG484	1st lot test dose varied

- **Results**
  - No tail bits observed in unbiased condition for 1000 hours
  - No tail bits observed in biased or un-biased condition for 500 hours
  - No tail bits on control samples which were exposed to high temperature but not irradiated

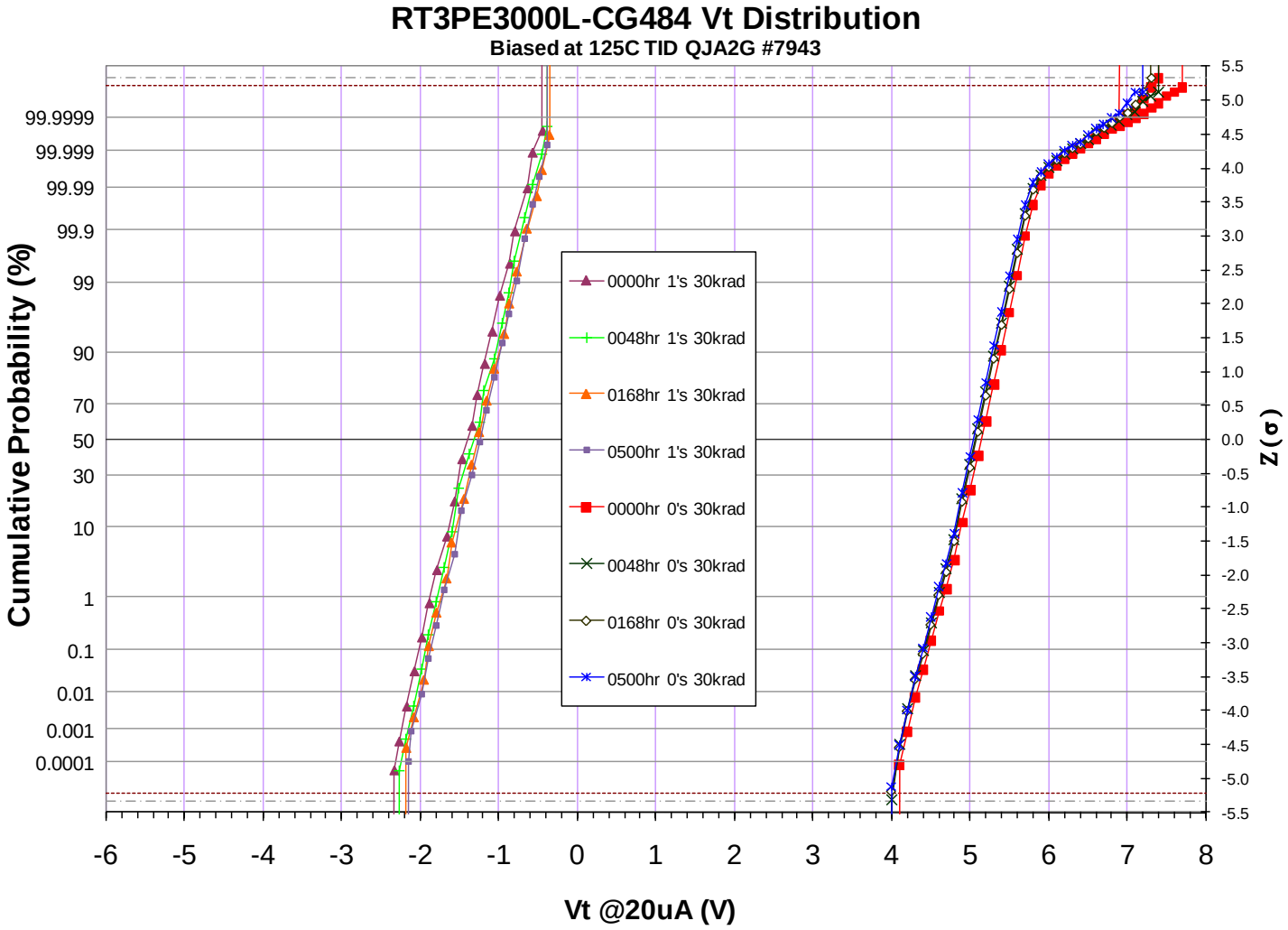
Results for Unbiased Condition at 150°C

- Devices exposed to 30Krad unbiased had very slight shift in V_T after 1680 hours at 150°C



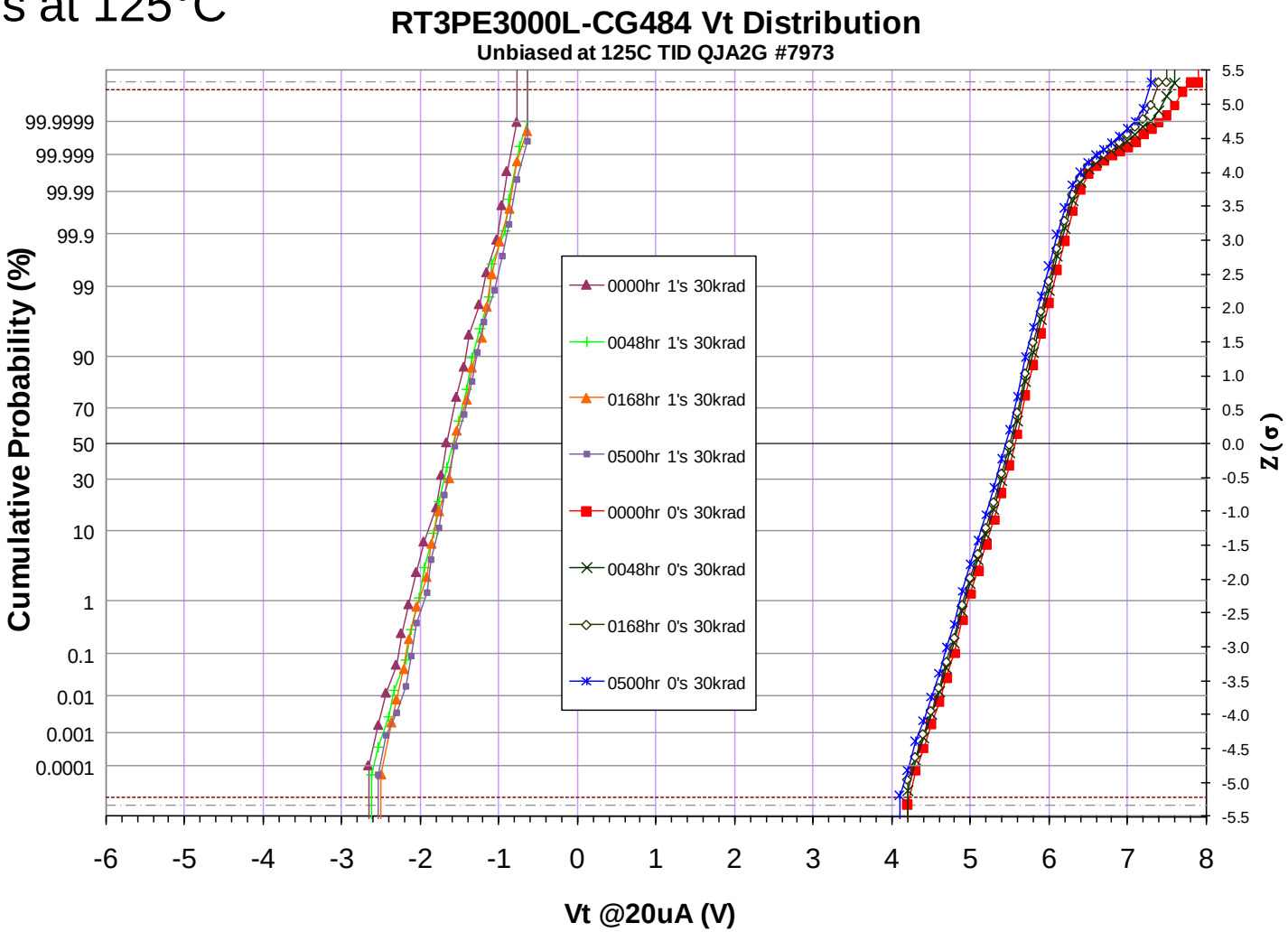
Results for Biased Condition at 125°C

- Devices exposed to 30Krad biased had very slight shift in V_T after 500 hours at 125°C



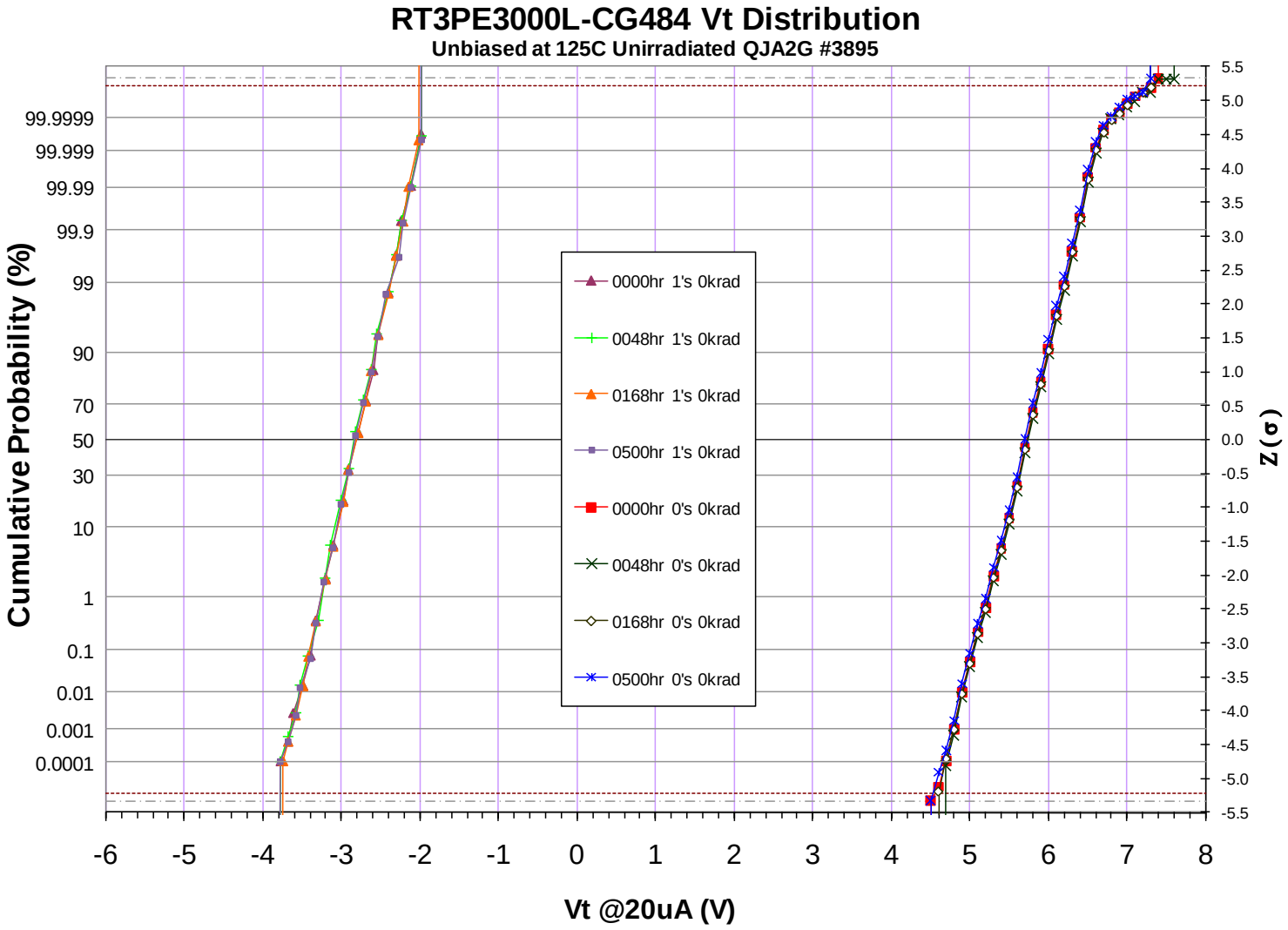
Results for Unbiased Condition at 125°C

- Devices exposed to 30Krad unbiased had very slight shift in V_T after 500 hours at 125°C



Results for Unbiased at 125°C (Not Irradiated)

- Devices with no TID had no V_T shift after 500 hours at 125°C



Summary

- RT ProASIC3 FPGAs have been tested extensively for TID and High Temperature Effects
  - The longest runners went through 1680 device hours at 150 C
- Irradiated devices had slow V_T shift and small impact on Flash cell data retention
- Devices, which were not irradiated, had no V_T shift and no impact on Flash cell data retention
- No tail bits, thus no defects, were observed
- Proven reliability of Microsemi Flash FPGAs under TID and high temperature
- Microsemi continues investing in the product family and collecting more life test data

Microsemi

Thank You