Power Matters.

Microsemi

Next-Generation Packaging Technology for Space FPGAs

Microsemi Space Forum Russia – November 2013

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Agenda

- CCGA (ceramic column grid array) package as the platform for Space
- Requirement from Hi-Rel community for flip-chip in Space
  - Class “Y”
- Microsemi flip-chip CCGA for Space
  - Packaging road map
  - CCGA package construction for hermetically seal with Space features
  - Package design to meet electrical performance
  - Test chip package qualification plan and status
  - Thermal management in Space
- Summary

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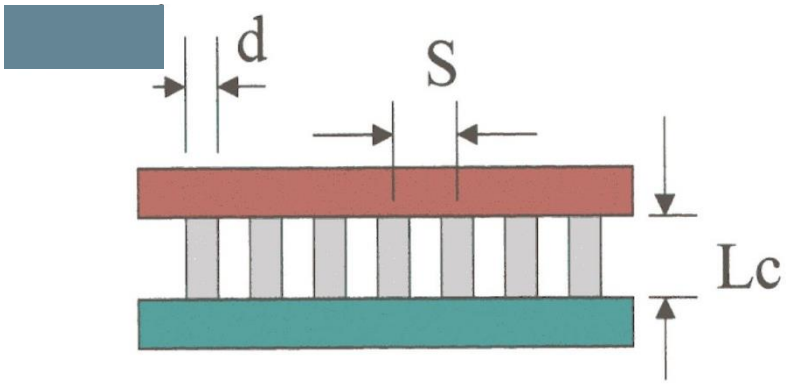
Packaging Platform for Space-Column Grid Array Solution



ΔT_1 = temperature change of board

ΔT_2 = temperature change of component

α_1 = CTE of the board

α_2 = CTE of the component

S = distance from neutral point (DNP)

E = modulus of elasticity of column

d = diameter of column

L = standoff height of column

$$\sigma_{max} \approx \frac{1.5 \cdot (\alpha_1 \cdot \Delta T_1 - \alpha_2 \cdot \Delta T_2)(S \cdot E \cdot d)}{L^2}$$

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Solder Columns Configurations

- Three basic types of solder columns
  - Wire column
    - High-lead wire with Sn63-Pb37 fillets
  - Solder column interposer
    - High-lead solder held in array with additional ceramic substrate
  - Reinforced solder column
    - High-lead wire core with spiral wrapped copper ribbon attached with Sn63-Pb37 fillets

Note: Reinforced columns show a significant performance advantage in comparison to other types of solder columns. See board level testing data result

High-lead solid wire core
---Sn20-Pb80 or Sn15-Pb85
Tin plated copper ribbon
Hot solder coating
---Sn63-Pb37

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Board Level Reliability Comparison

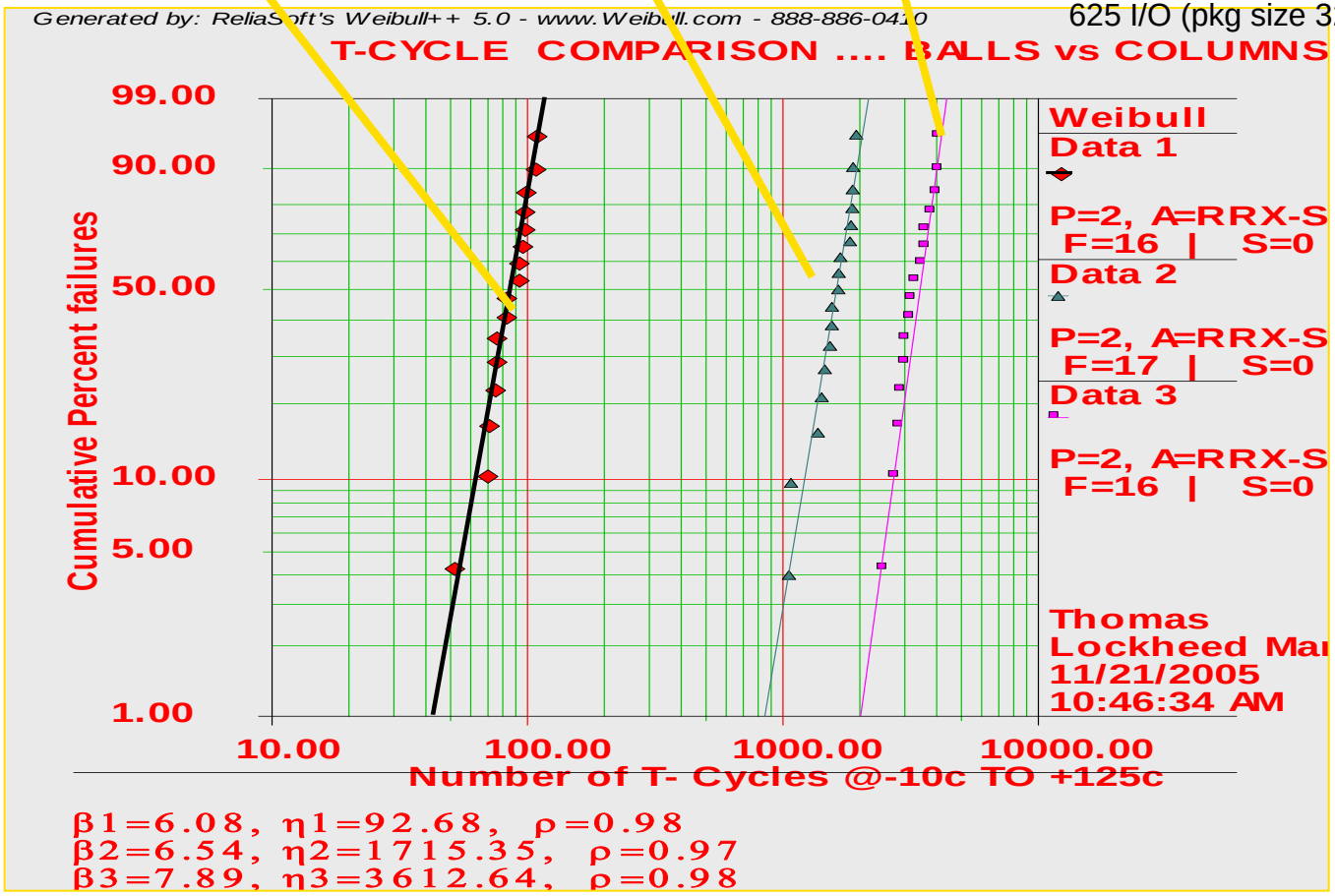
Reinforced Columns

BGA

Wire Columns

Results (from Six-Sigma)

All parts ceramic with 1.27mm pitch
625 I/O (pkg size 32mm)



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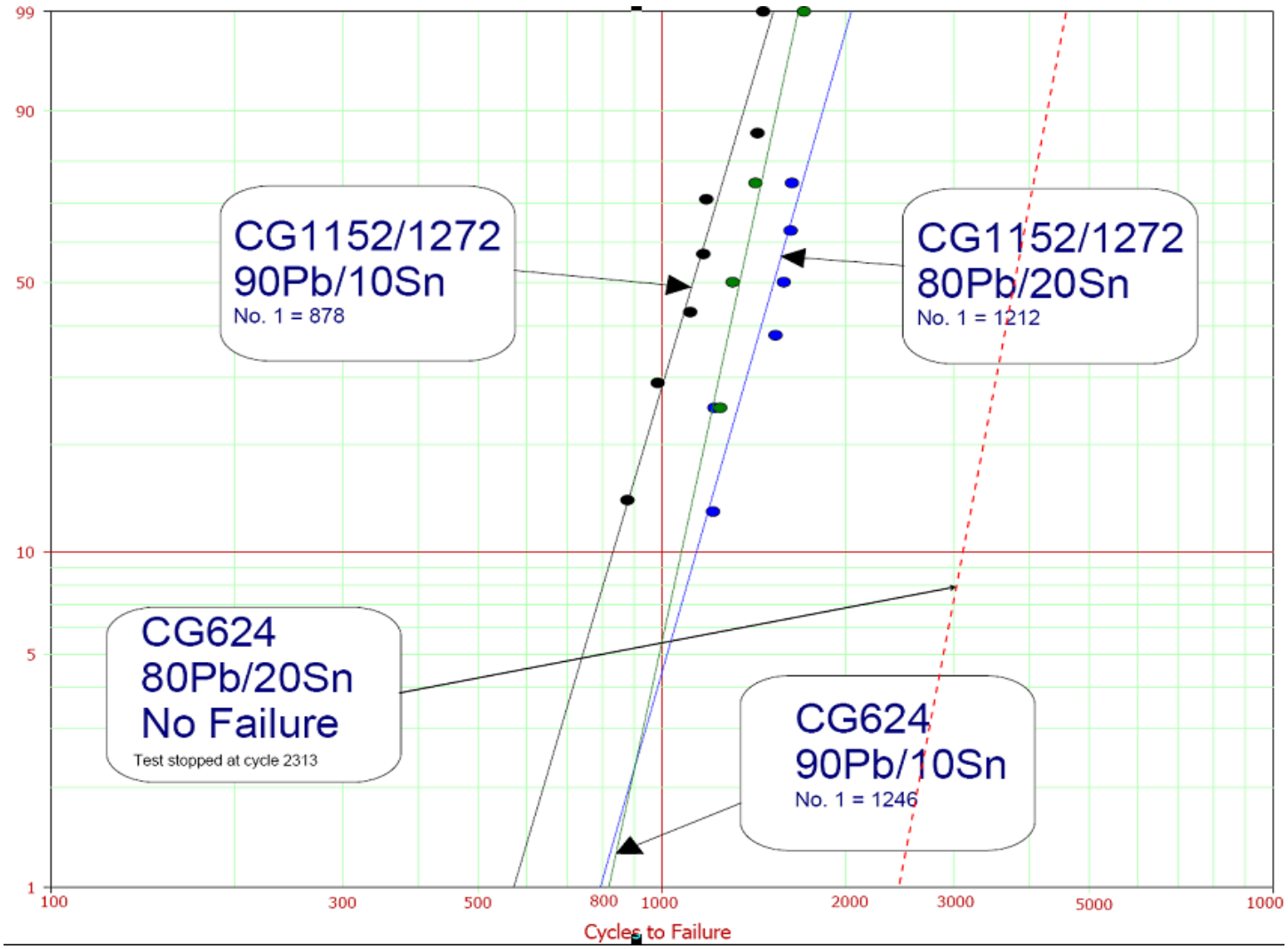
Board level Testing (-55C° to 105 C°) on Microsemi Current CCGAs

Lognormal Probability Distribution of Cumulative Fails vs. Temperature Cycles



Lognormal Probability of Cumulative Fails vs. thermal cycles----up to 2313 cycles

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Coffin Mason Relation

Lognormal Probability Distribution of Cumulative Fails vs. Temperature Cycles

$$\text{A. F.} = (\Delta T_t * DNP_t / \Delta T_f * DNP_f)^{1.9} \times (F_f/F_t)^{1/3} \exp\left[1414\,(1/T_{maxf} - 1/T_{maxt})\right]$$

Where :
N_f = Field Cycles
N_t = Test Cycles
ΔT_t Test Cycle Temperature Range
ΔT_f = Field Cycle Temperature Range
DNP_t = Test Distance to Neutral Point
DNP_f = Field Distance to Neutral Point
F_f = Field Cycle Frequency
F_t = Test Cycle Frequency
T_{maxf} = Maximum Field Temperature
T_{maxt} = Maximum Field Temperature

Test Conditions :

Temp. Range
-55 105

160 = ΔT_T, ΔTemp for Test

12 = F_T, cycles / day for Test

378 = T_{MaxT}, Max Temp for Test

*21.5mm = DNP for Test for CG624***
22.6mm =DNP for Test for CG1152
22.7mm =DNP for test for CG1272

** Note:

Distance of corner pin to the center point of the package (neutral point)

Used to related temperature cycle result to field condition

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CCGA Field Life Projection for Typical Satellite Applications

Based on Temperature cycling Data—for 80Pb/20Sn re-enforce column

	Field Cycles (CPD)	Field Temp Range	Field Delta Temp	DNP (mm)	Field Max Temp (C)	N.01 Test Cycles	Acceleration Factor	Projected Cycles	YEARS OF LIFE
CG624	18	20 to 45	25.00	21.5	45.0	2,313	78.88	182,445.8	27.8
CG1152	18	20 to 45	25.00	22.6	45.0	1,212	78.88	95,600.7	14.6
CG1272	18	20 to 45	25.00	22.7	45.0	1,534	78.88	120,999.5	18.4
CG624	12	70 to 85	15.00	21.5	85.0	2,313	110.67	255,970.0	58.4
CG1152	12	70 to 85	15.00	22.6	85.0	1,212	110.67	134,126.9	30.6
CG1272	12	70 to 85	15.00	22.7	85.0	1,534	110.67	169,761.3	38.8

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Summary of CCGA from Current RTAXS Family, Plan for Next-Generation Space Products

- Extended qualification data on wire bond version of CCGA (ceramic column grid array)
- Successful introduction of CCGA, and widely adapted by end customers for Space applications. Various flight programs have been used or in the planning stage to use CCGA packages
- Building on the current successful introduction of CCGA for Space, Microsemi is taking on to introduce flip-chip CCGA for Space
  - What are the requirement and expectation from Hi-Rel community?

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Requirement from JC-13 and Hi-Rel Community

Space Challenges for Complex Non-hermetic Packages

- **Vacuum:**
  - Outgassing, offgassing, property deterioration
- **Foreign Object Debris (FOD)**
  - From the package threat to the system, or a threat to the package
- **Shock and vibration**
  - During launch, deployments and operation
- **Thermal cycling**
  - Usually small range; high number of cycles in Low Earth Orbit (LEO)
- **Thermal management**
  - Only conduction and radiation transfer heat
- **Thousands of interconnects**
  - Opportunities for opens, intermittent - possibly latent
- **Low volume assembly**
  - Limited automation, lots of rework
- **Long life**
  - Costs for space are high, make the most of the investment
- **Novel hardware**
  - Lots of "one offs"
- **Rigorous test and inspection**
  - To try to find the latent threats to reliability

ONE STRIKE AND YOU'RE OUT!

Note: this slide is from July 2011 JC13 meeting on Non-hermetic for Space

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Requirement from JC-13 and Hi-Rel Community

Hermeticity

- NASA prefers hermetic packages for critical applications
- Hermeticity is measureable, assuring package integrity
- Only 3 tests provide assurance for hermetic package integrity:
  - Hermeticity – nothing bad can get in
  - Residual or Internal gas analysis – nothing bad is inside
  - Particle Impact Noise Detection – no FOD inside
- NON-HERMETIC PACKAGE INTEGRITY IS HARD TO ASSESS - NO 3 BASIC TESTS
- Non-hermetic packages expose materials' interfaces that are locked away in hermetic ones

Note: this slide is from July 2011 JC13 meeting on Non-hermetic for Space

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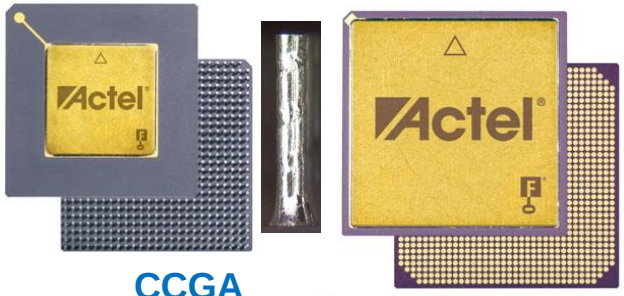
Hi-Rel Ceramic Packaging Roadmap

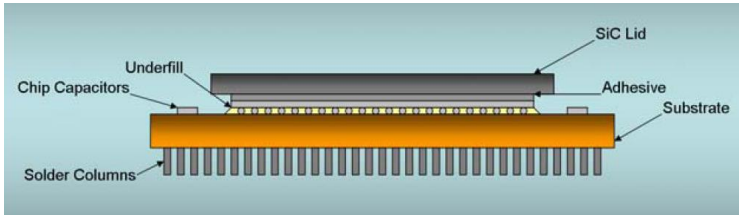
Mature Packages ***Future Packages***

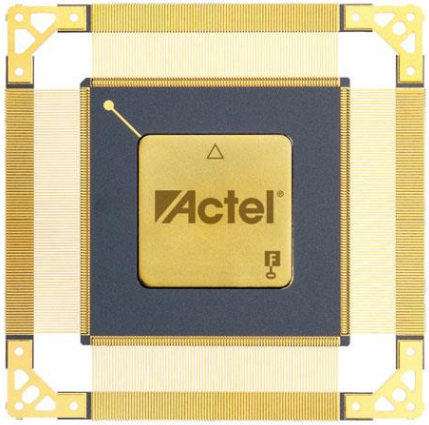
2008 to 2010 ***2011 to 2014***

PGA
132 – 391 Pins

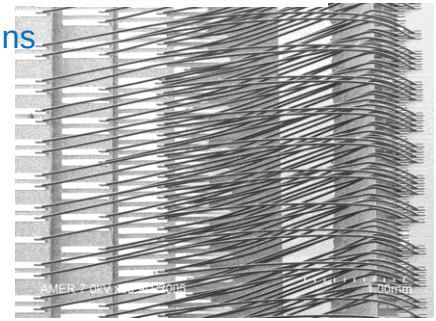


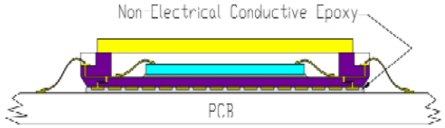
CCGA
624 – 1272 Columns



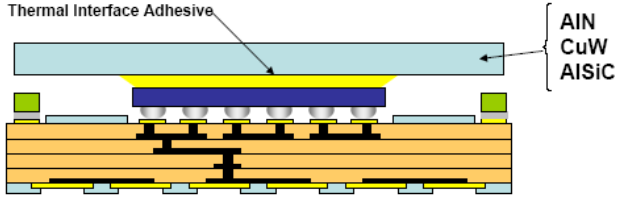


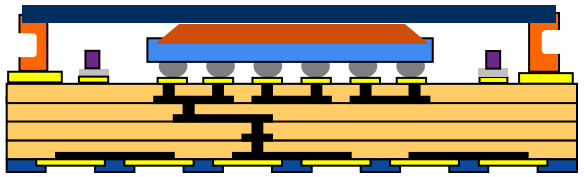
CQFP
84 – 352 Leads





CC256
Chip Carrier





Hermetically seal Flip-Chip CCGA
1432 to 2000+ Columns

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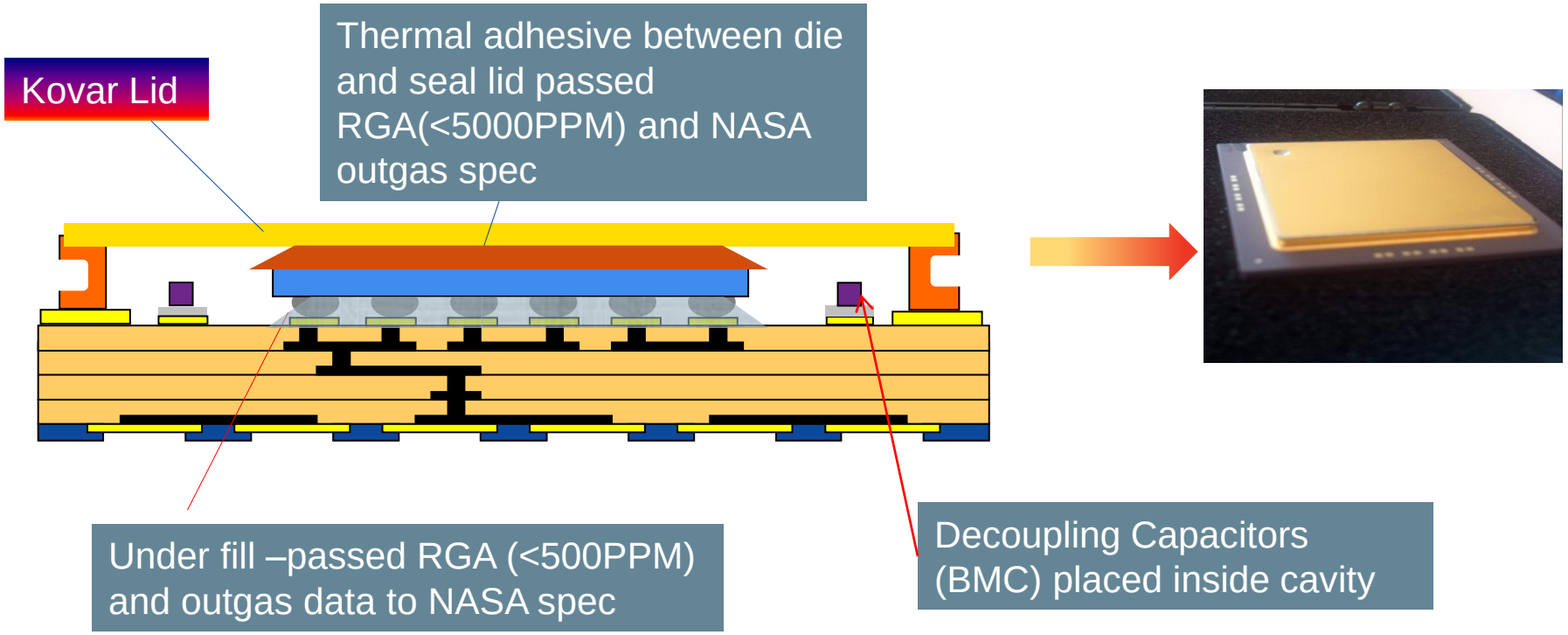
Microsemi Approach: Flip-Chip Package Hermetically Lid Seal and Target to V Flow

- Package size estimated: 42.5x42.5mm, 1657 balls. Target 11 to 13 layers of ceramic, with seam seal for hermetically seal. Note: dimension is not finalized
- Target to meet class V (hermetically seal), better than Class Y (non-hermetic)



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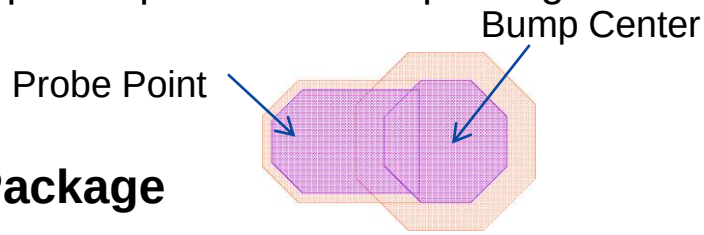
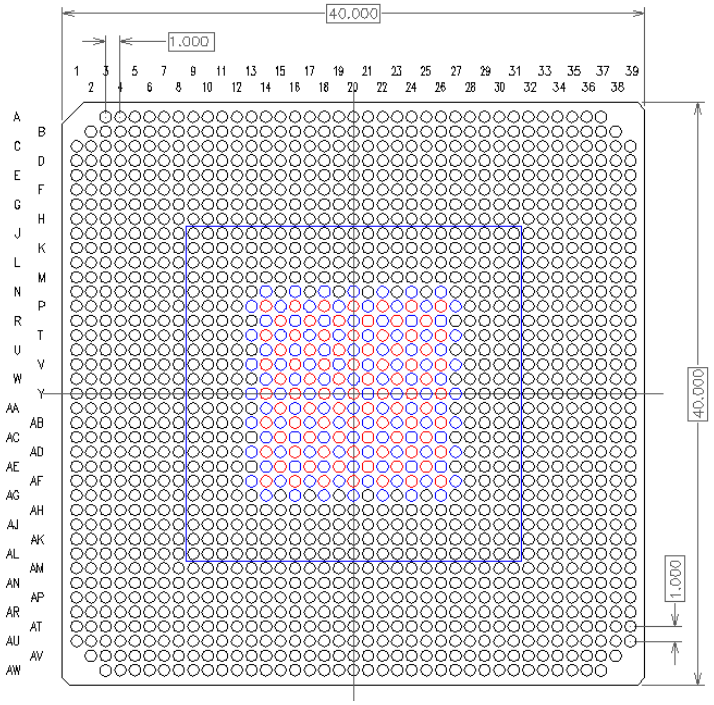
Test Chip: Flip-Chip Daisy Chain Test Chip

- **Silicon Die**
  - 23 mm X 23 mm
  - 200 um pitch
  - High lead bump: 5Sn/95Pb
  - 12992 Bumps (Daisy Chain)
  - 90 - 100 um bump height
  - With separate pads for wafer probing



- **Ceramic Package**
  - 40 mm X 40 mm
  - 100 um bump pad
  - 1.0 mm Column Pitch
  - 0.8 mm Solder Pad
  - 1509 Solder Columns, 0.51 mm Ø
  - ***Note: final package will be in 42.5mm SQ***
- **Capacitors**
  - BMC



- (Note: Test Chip package tooled up: 40x40mm, 1509 balls, with 1.0mm pitch, the final package for flight parts will be in **42.5x42.5mm 1657 columns pins**)

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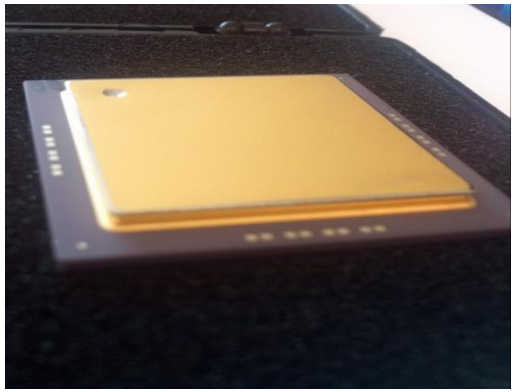
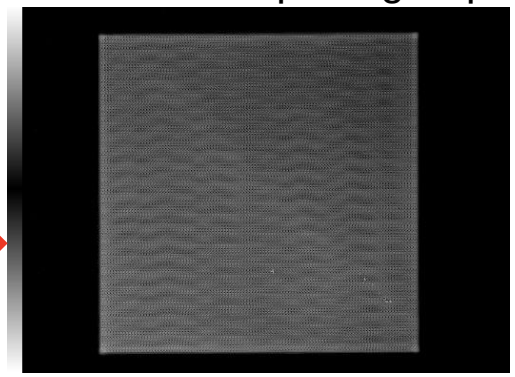
Test Chip: Flip-Chip Daisy Chain Status for V Flow

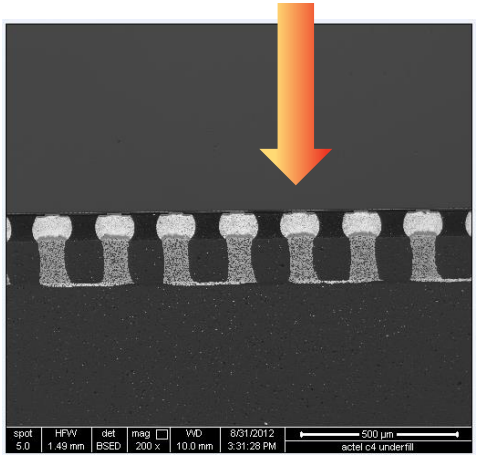
- **Current status for hermetically seal Flip-Chip**
  - Assembly process optimization has been finalized with under fill material and process parameters
  - Both underfill material and TIM material passed RGA(<5000PPM) and NASA outgas requirements
  - On track to build the daisy chain lots to complete group D testes under class V flow end of 2013



Assembled unit with seam seal process Kovar lid



CSAM checking flip-chip under-fill



Cross section of C4 flip-chip bumps

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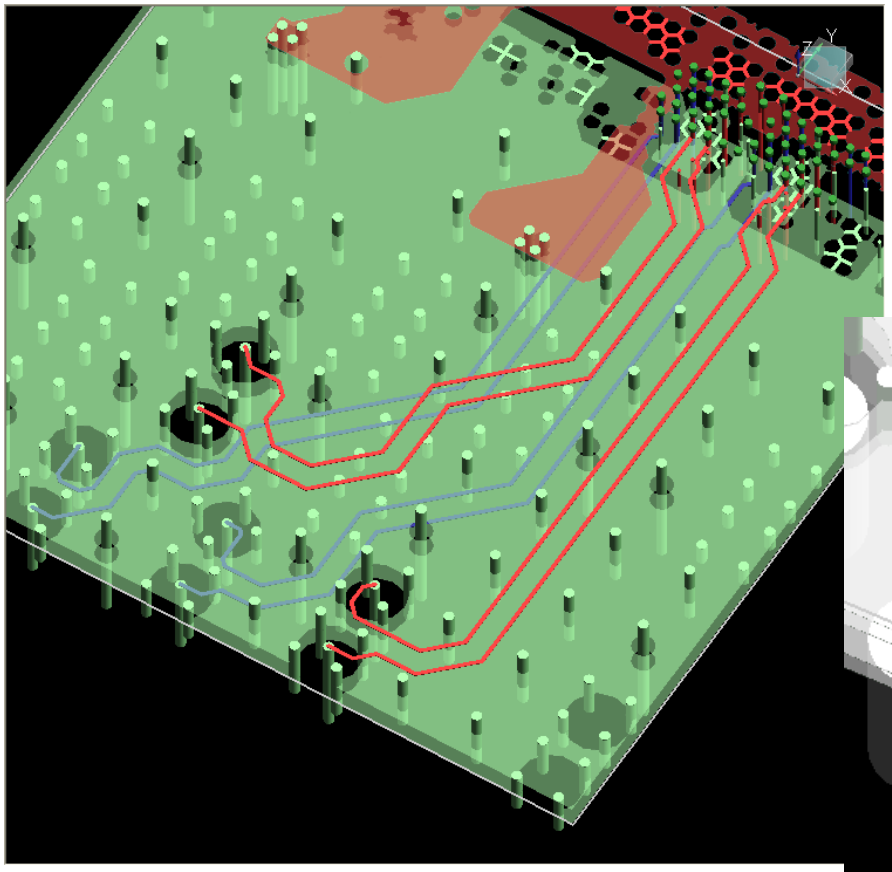
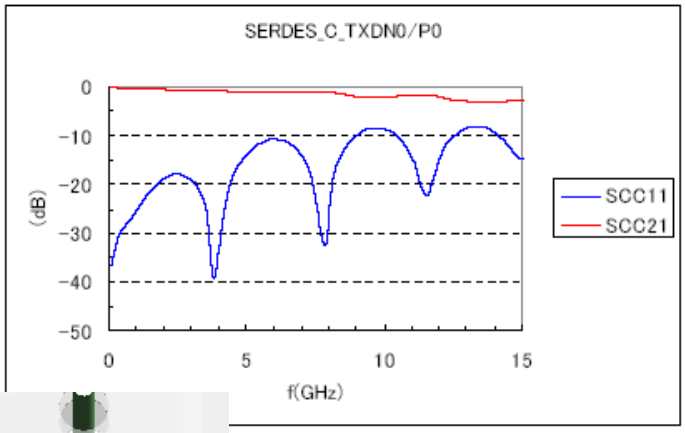
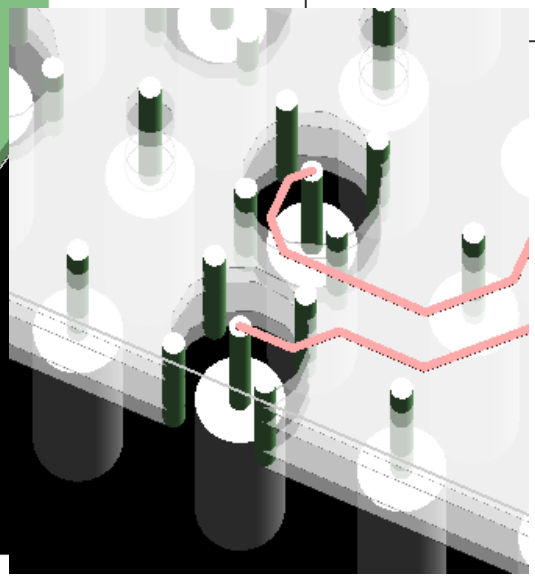
Package Design Aspect: SerDes RX & TX Design

- Co-axial ground via placement for all Rx and TX pairs
- Opening of the ground plane is optimized to reduce capacitance
- All Rx and Tx signals sandwiched between ground planes







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Thermal Management of Components in Space

- A cooling plate is normally attached between two boards within a system (box)
- Prefer no cooling plate attached to the top lid of the flip-chip CCGA (concerns on component reliability from vibration during launch stage)
- Since there is no air in space (vacuum condition), most of the heat from the junction can only be dissipated through the board
- The package's thermal resistance from junction-to-board (θ_{JB}) is the thermal parameter we can use to estimate the maximum power the product can handle

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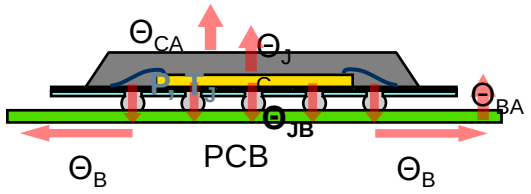
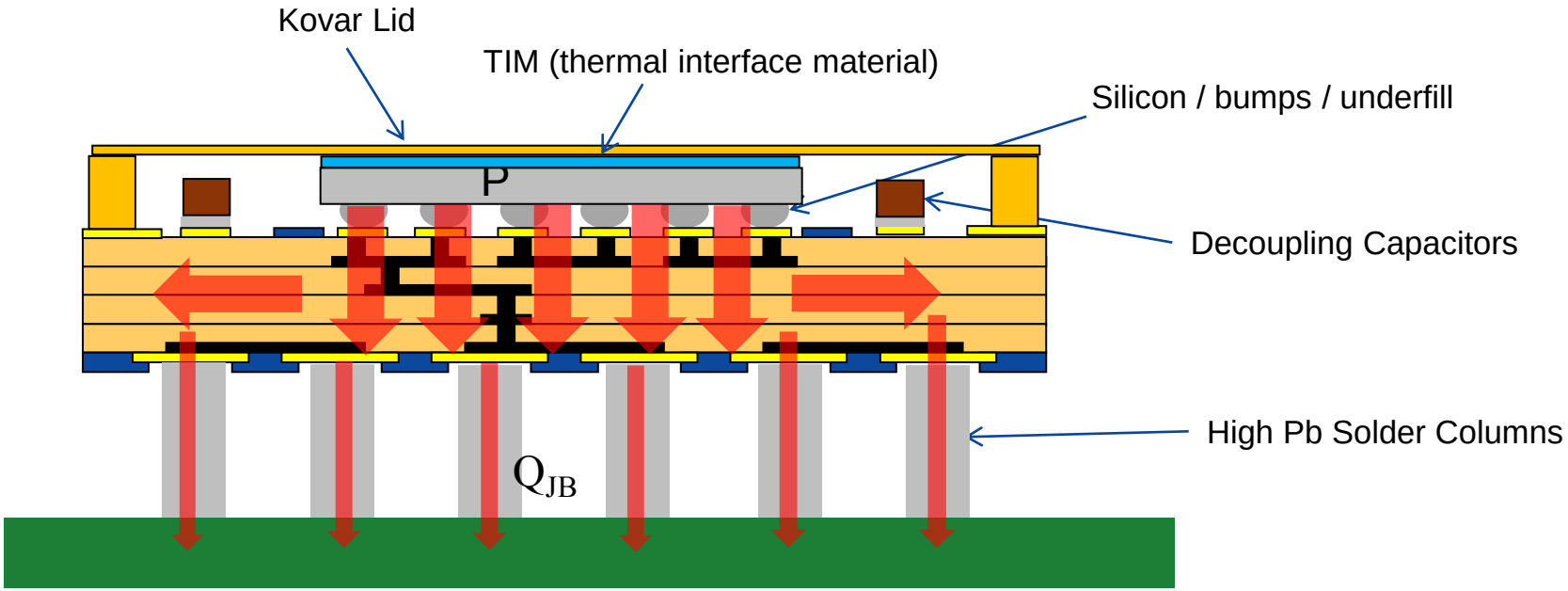
Heat Flow in Vacuum – Junction to Board

- Heat flow in a vacuum condition is through radiation and conduction which is from the die surface to the package, to the solder columns, to the PCB



Typical heat flow in air environment

$$\Theta_{JB} = (T_J - T_B) / Q_{JB} = 1.78\ ^{O}C/W \quad \ldots P = Q_{JB}$$



PCB Temperature @ 60 ^{O}C– 70 ^{O}C– 80 ^{O}C

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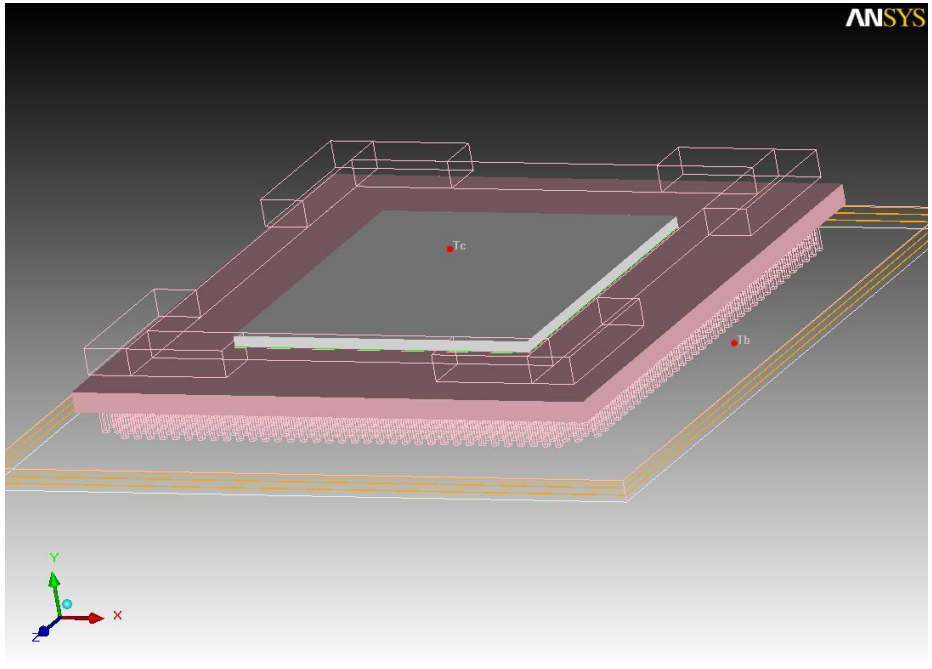
Test Chip Package Thermal Simulation Hermetic Version

- **Silicon Die**
  - 23 mm X 23 mm
  - 200 um pitch,
  - 12992 bumps
  - 100 um bump height
- **Ceramic Package**
  - 40 mm X 40 mm
  - 1.0 mm pitch,
  - 1509 solder columns
  - 0.51 mm Ø, 2.21 mm height
- **Kovar lid**



- (40x40mm, CG1509)

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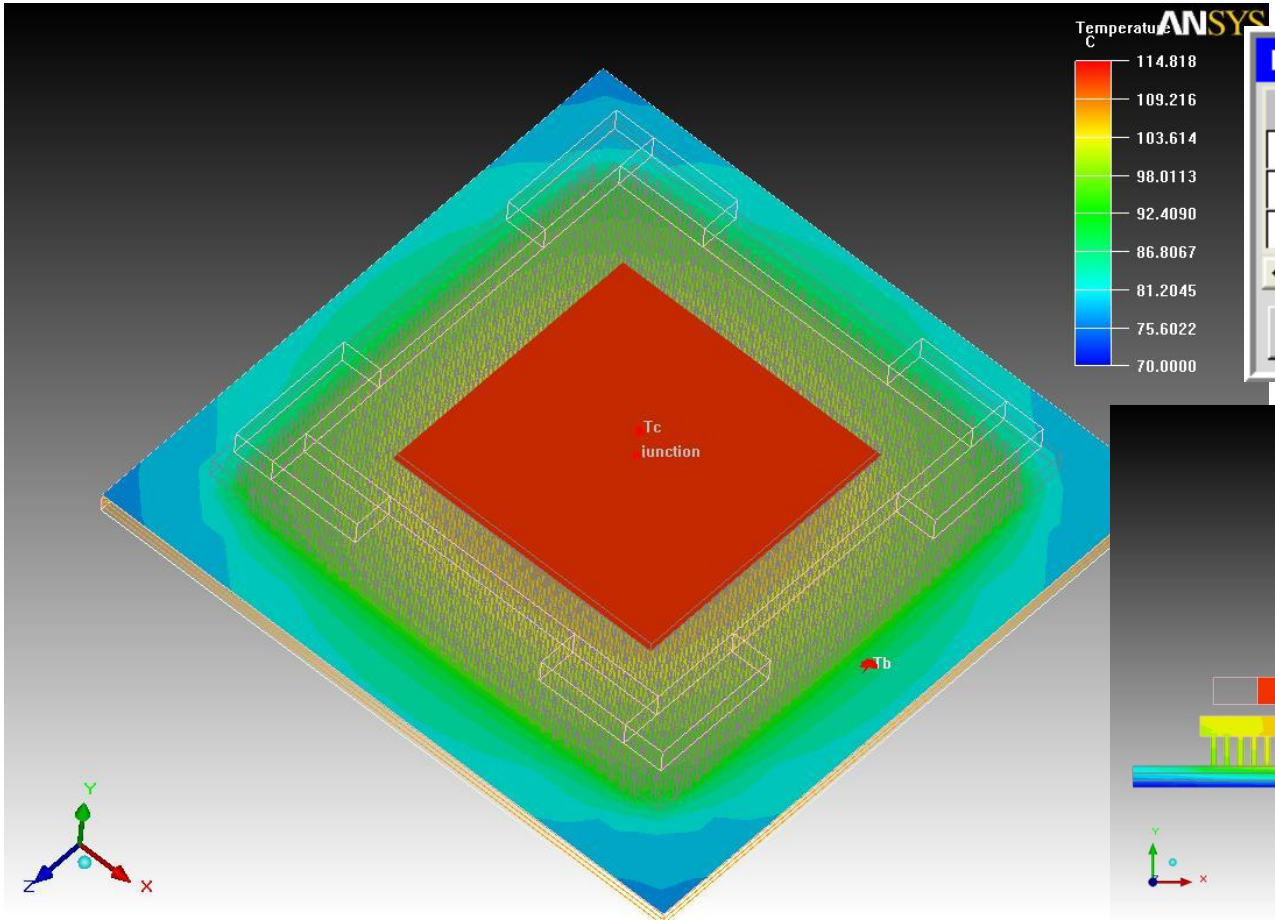
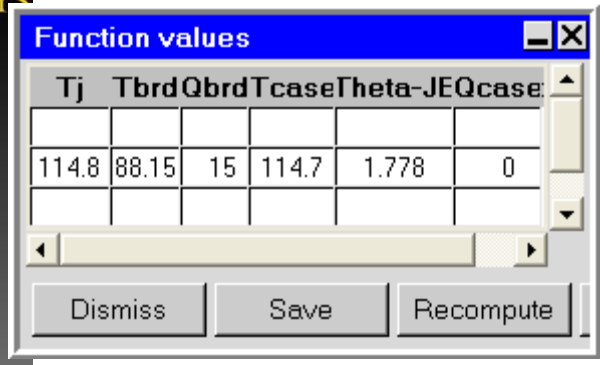
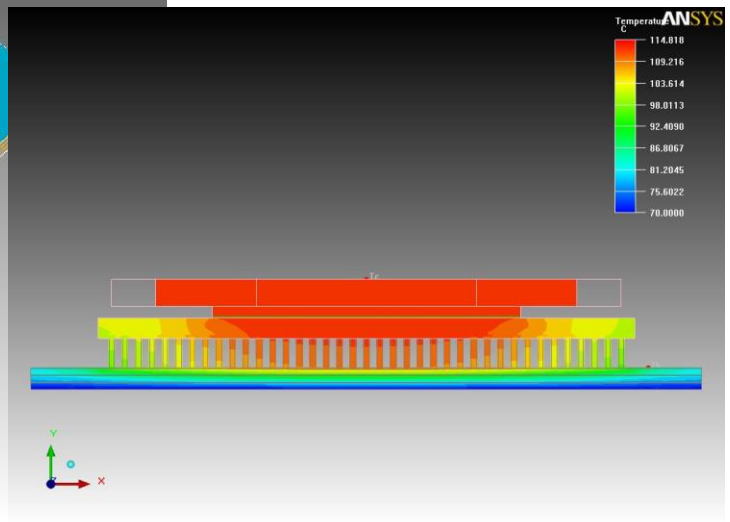
Simulation Result For Test Chip Package: Hermetic

- **Junction to Board Thermal Resistance**
  - θ_{JB} = 1.78 C/W

(40x40mm, CG1905)







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Power Estimated Calculation For Test Chip Package

(40x40mm-CG1509)

- Estimate Θ_{JB} = 1.78 ^{O}C/W for CG1509

Θ_{JB} (^{O}C/W)	T_J (^{O}C)	T_B (^{O}C)	P (W)
1.78	125	60	36.5
1.78	115	60	30.9
1.78	105	60	25.3
1.78	95	60	19.7

Θ_{JB} (^{O}C/W)	T_J (^{O}C)	T_B (^{O}C)	P (W)
1.78	125	70	30.1
1.78	115	70	25.3
1.78	105	70	19.7
1.78	95	70	14.0

Θ_{JB} (^{O}C/W)	T_J (^{O}C)	T_B (^{O}C)	P (W)
1.78	125	80	25.3
1.78	115	80	19.7
1.78	105	80	14.0
1.78	95	80	8.4

- T_B is the temperature measured by a thermocouple, placed 1.0 mm away from the package edge

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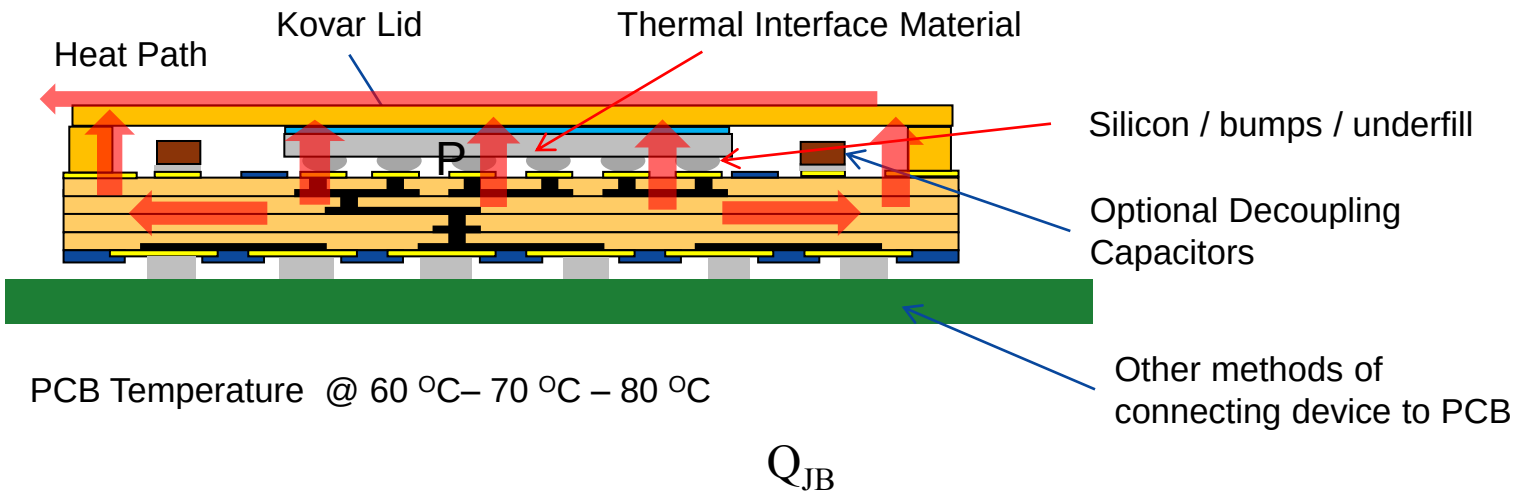
Potential Other Methods: Heat Flow in Vacuum – Junction to Case

- Heat flow in a vacuum condition is through radiation and conduction which is from the die surface to the silicon, to the heatsink or to the PCB

$$\Theta_{JC} = (T_J - T_C) / Q_{JC} = \text{estimated } 0.5\ ^{O}C/W \ \ldots P = Q_{JC}$$



- In this configuration, end users can attach some type of cooling plate on the top of the lid and connect it to a cooling system.
- For a conservative operating condition of (Tj=95^{O}C and Tb=70^{O}C), Delta T is: 25^{O}C, P=25 ^{O}C/ 0.5 (^{O}**C/W)=50W range**

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Summary

- CCGA (column grid array package) continues to be the platform for the new generation RT device for Space
- Flip-Chip (with eutectic solder bump) as interconnect technology
- Target hermetically seal packages with V flow
- Package design optimizing performance and minimize noise
- Heat dissipation in Space has been considered during design phase
- Test chip package has been tooled up to optimize flip-chip assembly processes, and to test to meet class V flow specifications. Final daisy chain package (which almost the same as to the final product) will be ready by Q4 2013

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Thank You

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