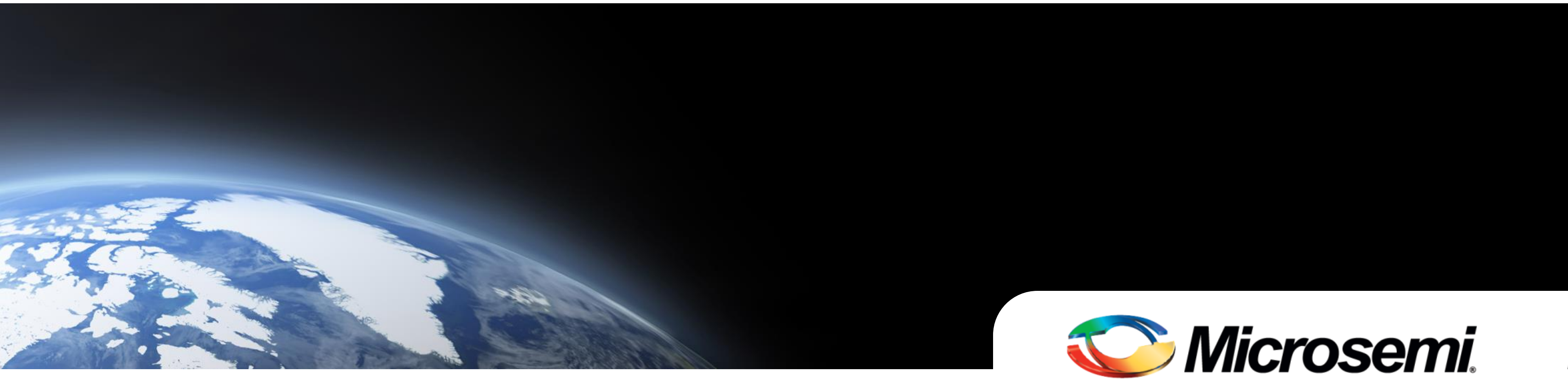
Power Matters



Integration of Common Spacecraft Interfaces & Support Functions

Microsemi Space Forum Russia – November 2013

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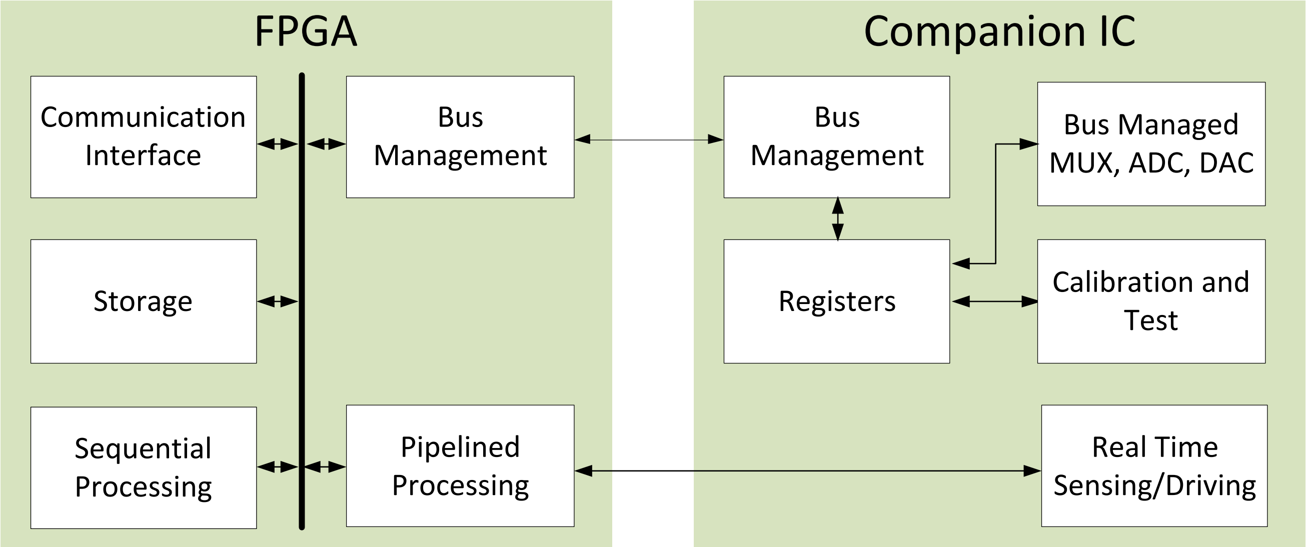
Space System Manager Concept

- Space System Manager (SSM) is a combination of an FPGA with a special purpose analog or power companion IC.
- The companion IC is intended to work with an FPGA
  - I/O levels and timing are compatible
  - The companion IC has a minimal amount of hard coded internal logic



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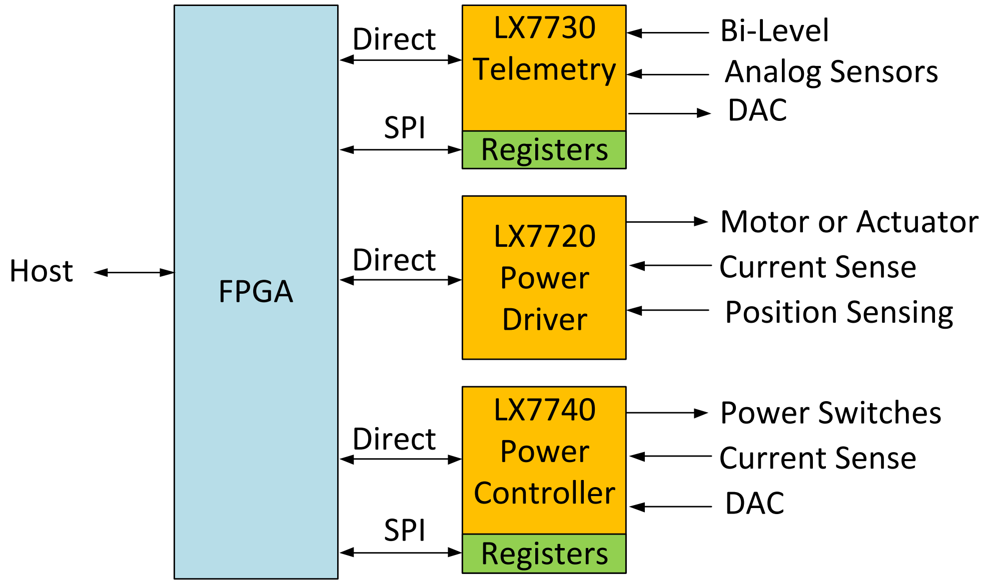
Space System Manager Characteristics

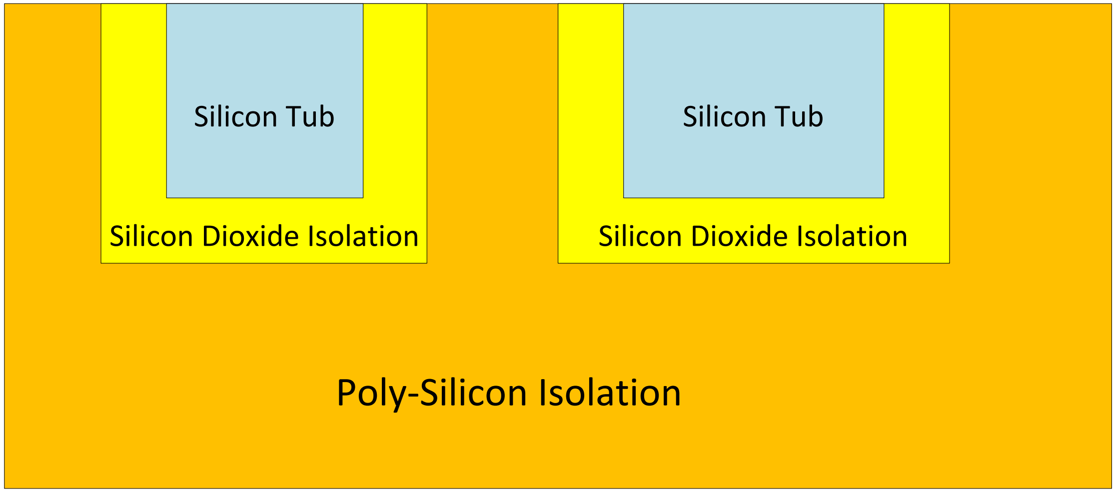
- Both the FPGA and the Companion IC are standard parts that are space qualified and DLA listed
- Companion IC standard attributes
  - Radiation Tolerant: 100krad TID; 50krad ELDRS, SE tolerant
  - Inputs are cold spared and dielectrically isolated
  - ESD and overvoltage clamping



IC Process for Fault Isolation

- The companion IC uses a special Dielectric Isolated (DI) process such that if any channel within the IC becomes compromised due to an external fault, the remaining IC continues to function normally
  - There is not a common substrate connection like is used with other IC processes
  - This process is similar in performance to the isolation achieved in Hybrid circuits
  - Isolation between tubs of at least 350V

Dielectric Isolation Cross Section



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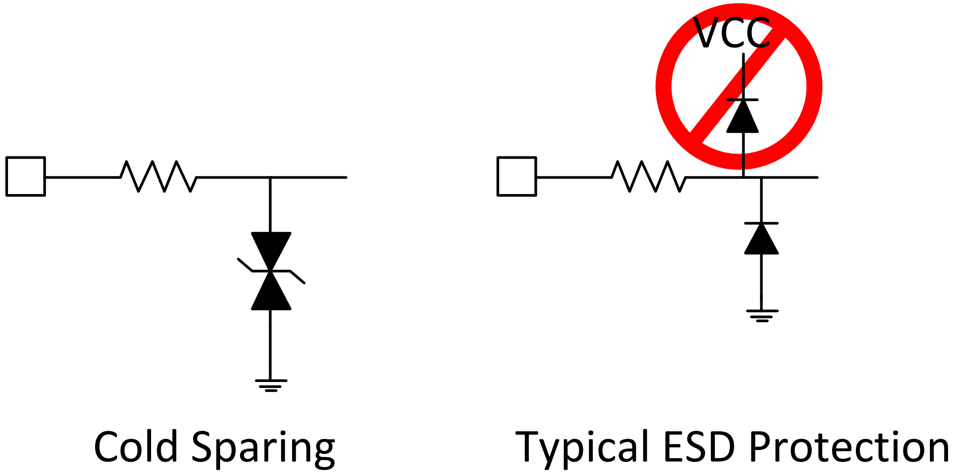
IC Process for Cold Sparing

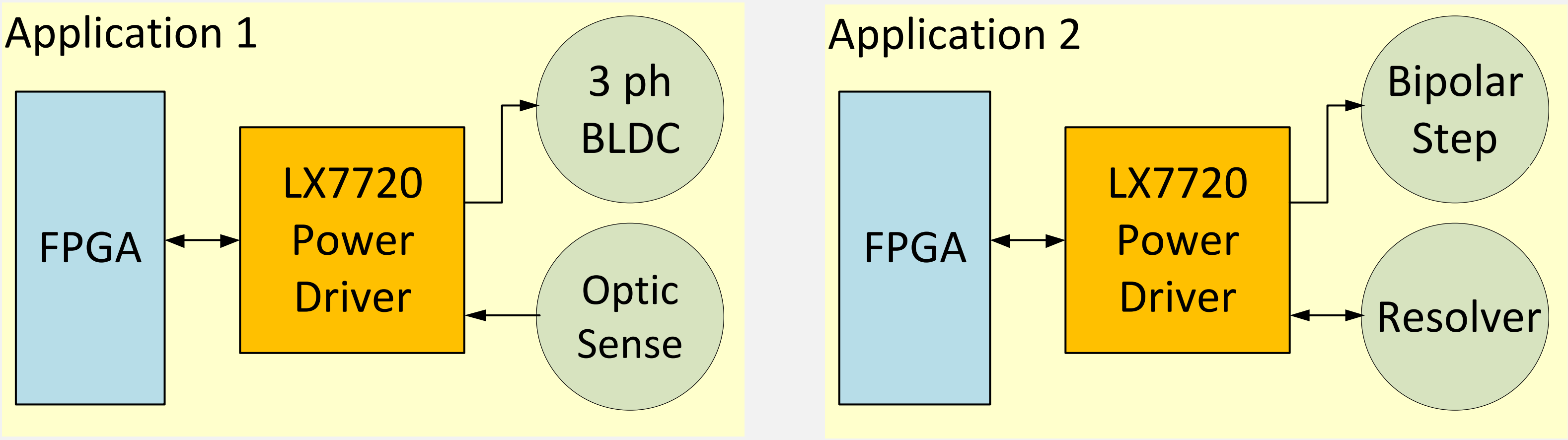
- An isolated ESD structure for each Companion IC pin along with design techniques considering low leakage with power removed allows the companion IC to be cold spared (becomes a high impedance with the power removed)



Companion IC Application Versatility

- Companion ICs exploit commonality between applications
  - Servo motor drivers require high power switches and position sensing
  - Telemetry monitoring requires an analog MUX, ADC and bi-level inputs

Different applications using the same IC part numbers.



System Manager System Integration

- FPGA HDL module examples are
  - Data sampling and logging
  - Motor micro-stepping
  - Brushless DC servo loop
  - Resolver to digital conversion
  - Sigma Delta filtering and dissemination
- Companion IC registers examples
  - Passive sensor drive current levels
  - ADC input range setting
  - MUX selection of inputs
- External Components adjust
  - External NMOS power sizing for motor drivers
  - Bi-level threshold levels

HDL Modules

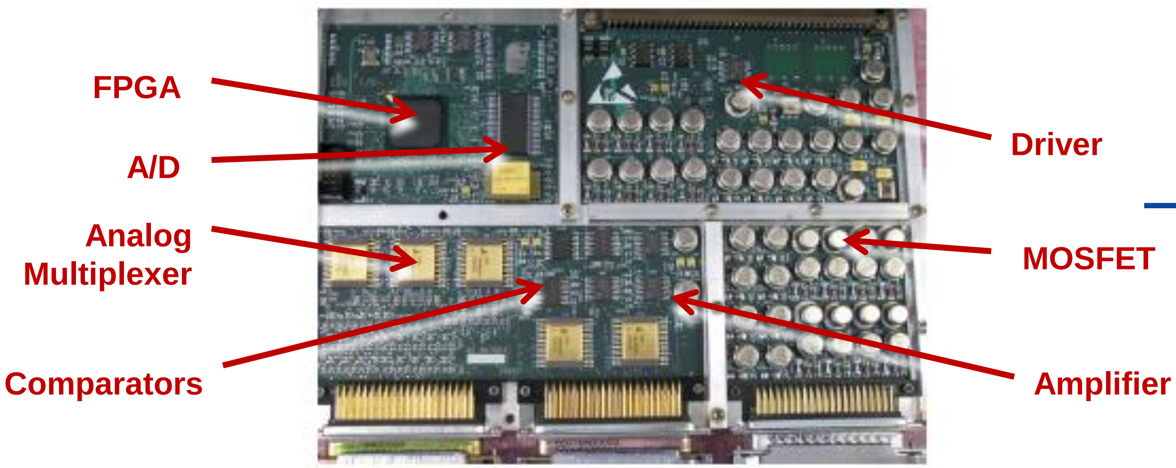
+

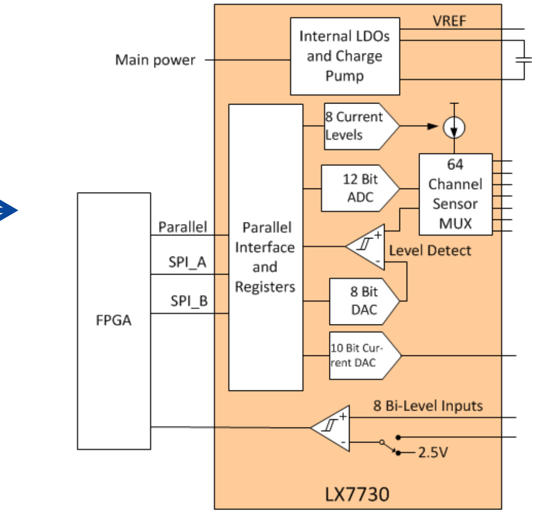
Register Map

+

Power Sizing & Programming Components

Approach Comparison - Discrete Components





- A typical circuit uses an FPGA with analog interface functions implemented with many single function ICs and discrete components
- Companion IC integrates commonly used functions into one package to reduce circuit board area and weight
- Although utilization may not be 100% for the space system manger, it is still likely to be a more compact solution

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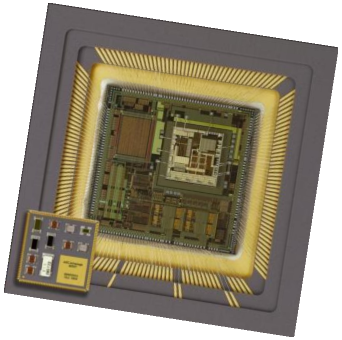
Approach Comparison - Custom ASIC

- The custom rad-hard mixed-signal solution provides an efficient solution but presents a number of challenges
  - Development Cost for a Mixed-Signal ASIC for Space applications is typically $2M-$4M
  - Development time typically of 2-4 man year.
  - Qualification is in excess of 1-2 year.
  - Time to production 4-5 years – very long R.O.I.



- Unlike the SSM, with a custom ASIC
  - Very few players are able to budget such development
  - Design to schedule and performance risk is usually high due to the high level of complexity associated with Rad Hard designs
  - The solution typically has minimal flexibility if requirements change

Reducing Risk While Maximizing Integration

	Discrete Solution	Space System Manager	Custom ASIC Solution
NRE	Low	Low	High
Development Time	Months	Months	Years
Qualification	Fast	Fast	Long
Risk	Small	Small	High
Flexibility	High	High	None
Power	Worst	Good	Best
Reliability	Average	Excellent	Excellent
Size and Weight	Poor	Good	Best

Value Proposition → High flexibility → High integration → Shorter development time → Minimum risk

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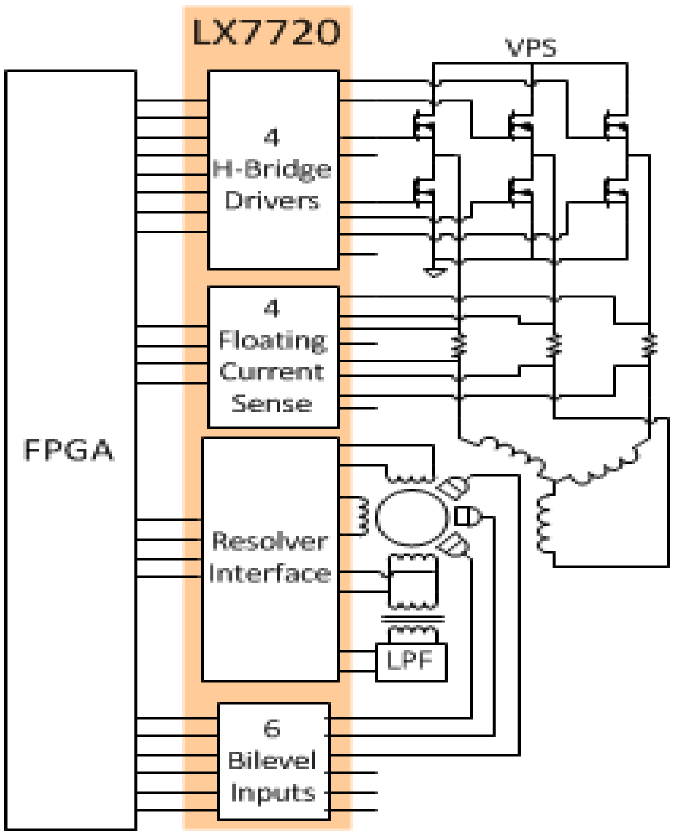
Companion ICs

- In Development
  - LX7720: Space Craft Power Driver with Rotation and Position Sensing
  - LX7730: 64 Analog Input Telemetry Controller

- In Definition Phase
  - LX7740: Power Sequencing and Management

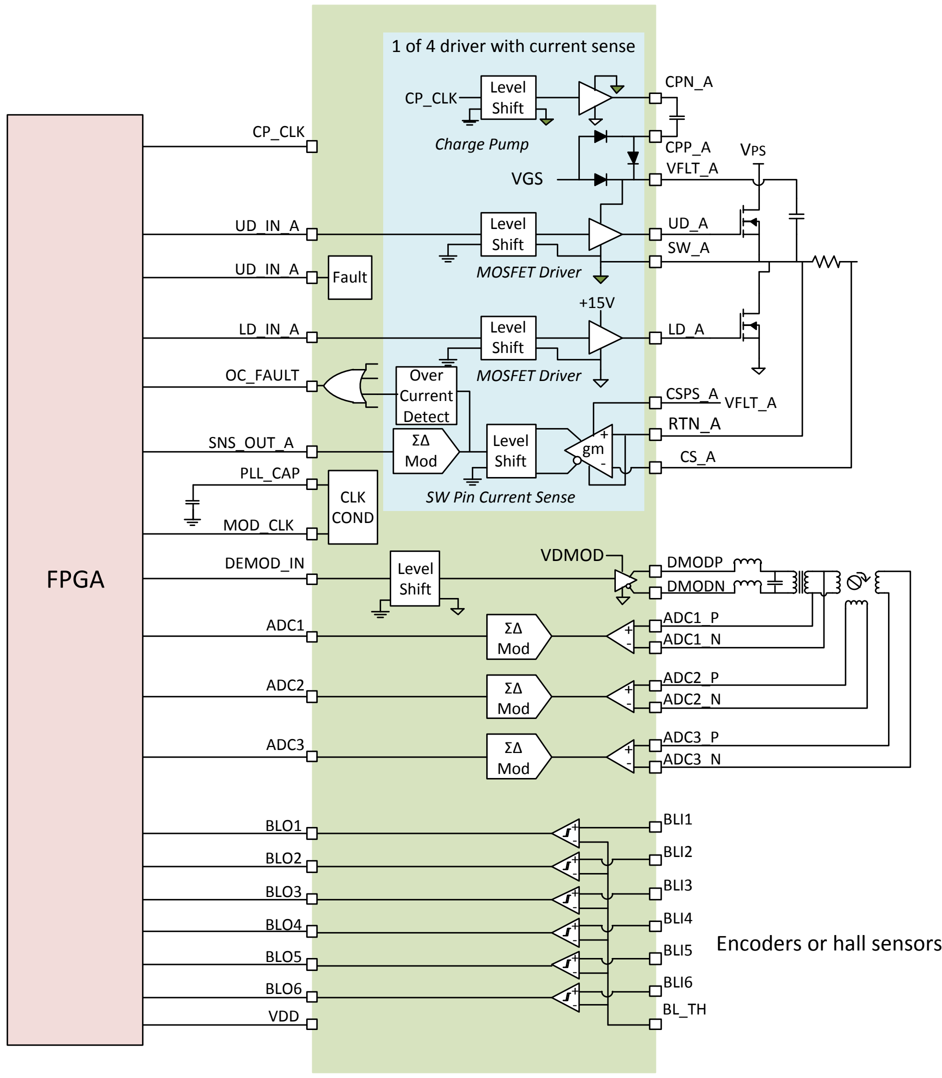
LX7720 Power Driver w Position Feedback

- Provides MOSFET motor drivers
  - 3 phase motors
  - Unipolar or bipolar steppers
- 4 high and low side relay drivers
- Up to 4 current sensors
  - In Line or to ground
  - Average current control loops
- Sensing for resolver or LVDT
- Detecting pulse sensors and limit switches



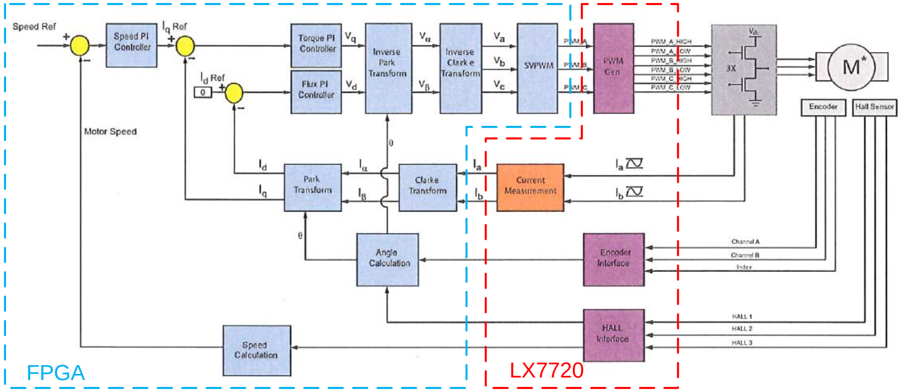
LX7720 Block Diagram

- LX7720 Features
  - Four H-Bridge Nch MOSFET drivers
  - Four floating differential current sensors with ΣΔmodulated processed outputs to FPGA
  - Pulse density modulated resolver exciter
  - Three differential resolver sensors with ΣΔmodulated processed outputs to FPGA
  - Six bi-level logic inputs
  - 100V isolation FPGA-to-Motor



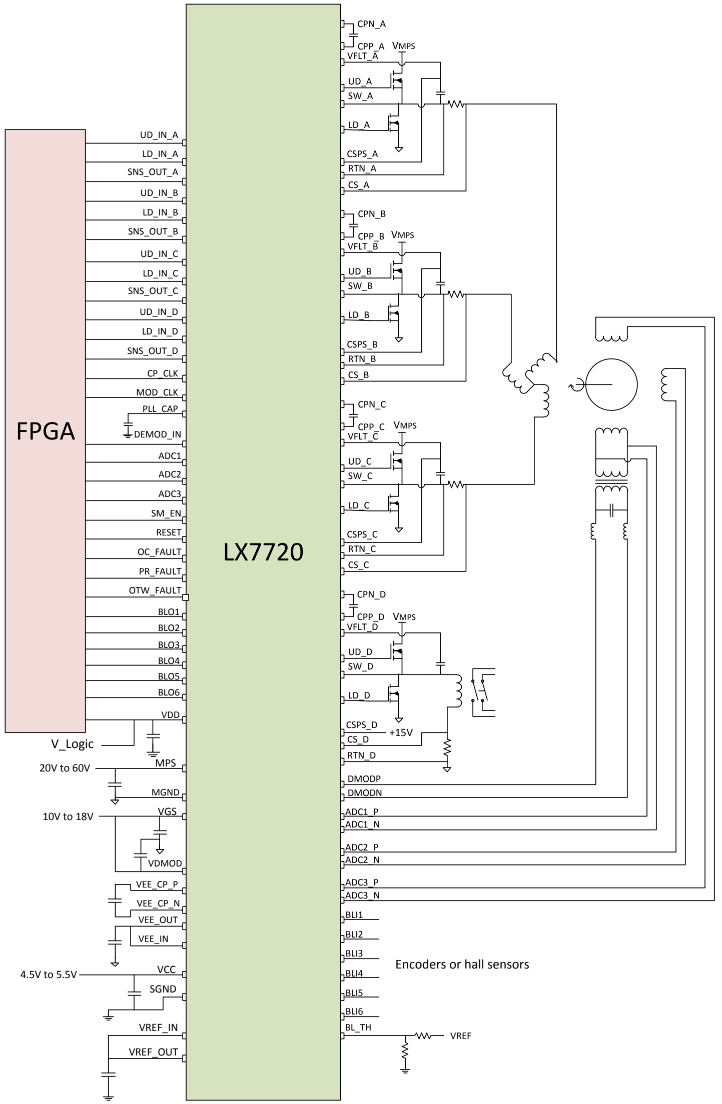
LX7720 HDL Module Tool Kit

- HDL Modules
  - 2 phase bipolar drive with modes for cardinal steps, max torque and microstepping using average current regulation
  - Sinc3 filter and disseminator with 7 to 14 bit ADC accuracy
  - Pulse density exciter drive /tracking resolver-to-digital converter
  - BLDC control with trapezoid drive
  - PMSM control with sinusoidal drive
  - Field oriented transformations
  - Space vector modulation
  - Fault management



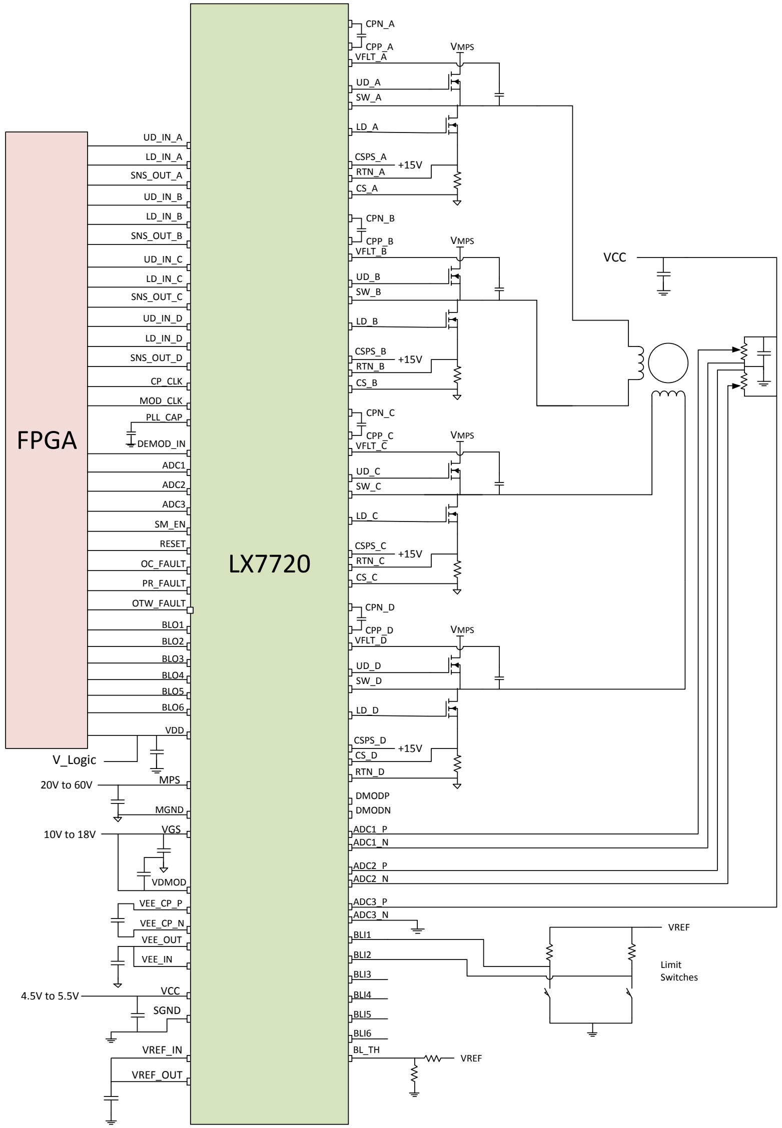
LX7720 PMSM Application

- Three phase PMSM motor
- Tracking resolver
- In line current sensing
- Phase D used for relay driver with current sense in return path



LX7720 Bipolar Microstepper

- Bipolar stepper motor
- Return path current sensing
- Potentiometer position sensing
- Limit switch sensing



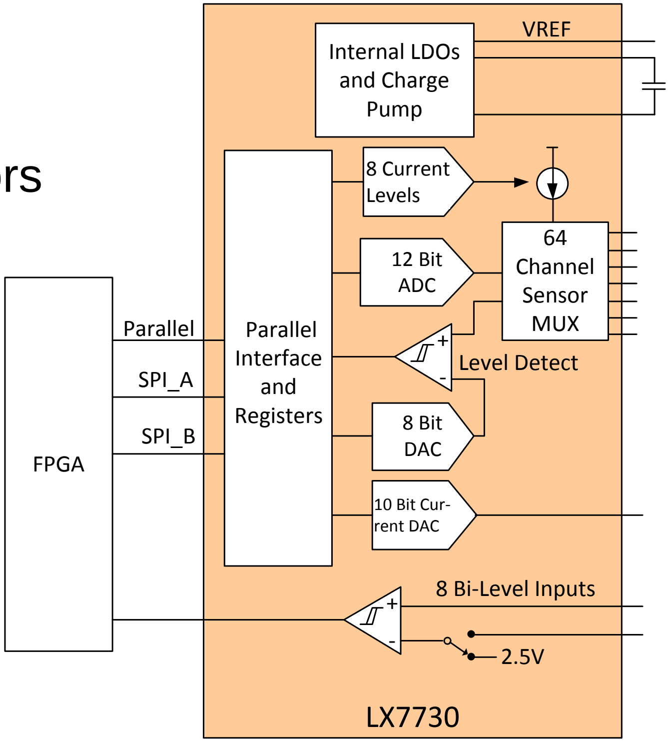
LX7720 Performance Highlights

- LX7720 Performance

Parameter	Comment	Min	Typ	Max	Units
Motor Power Supply	De-rated by 20%	20	48	80	V
MOSFET driver impedance	Source or sink		1		Ω
PWM frequency		DC		200	kHz
Current sense range		-250		250	mV
Current sense accuracy			7		bits
Current sense latency			4		uS
Resolver carrier frequency		0.36		20	kHz
Resolver accuracy			16		bits
Bi-level threshold range		0.5		4.6	V
Bi-level propagation delay			1		us

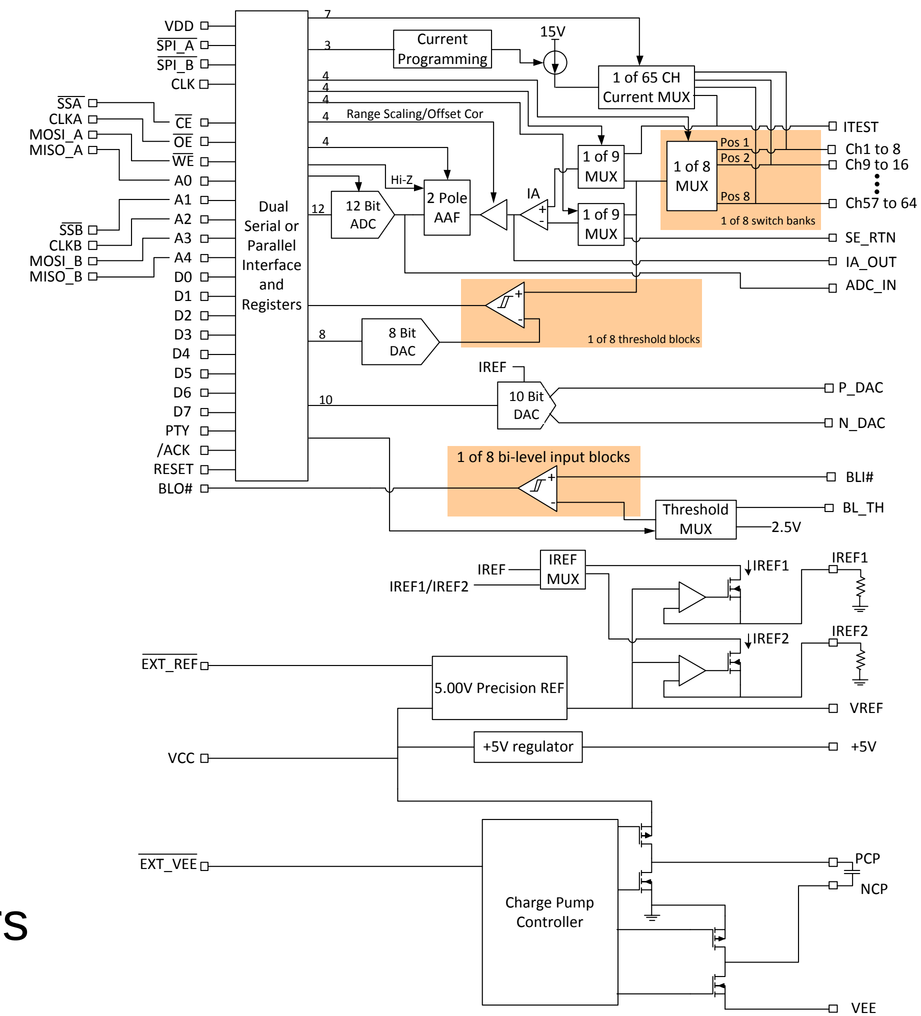
LX7730 64 Analog Input Telemetry Controller

- Single ended sensing for 64 sensors with simultaneous monitoring of 8 sensors
- Differential (Kelvin) sensing of 32 sensors
- Current demux to any input for driving passive sensors
- Voltage reference to bias bridge networks
- ADC ranging accurately measures low level voltage changes
- DAC out for level control
- 8 bi-level logic translators



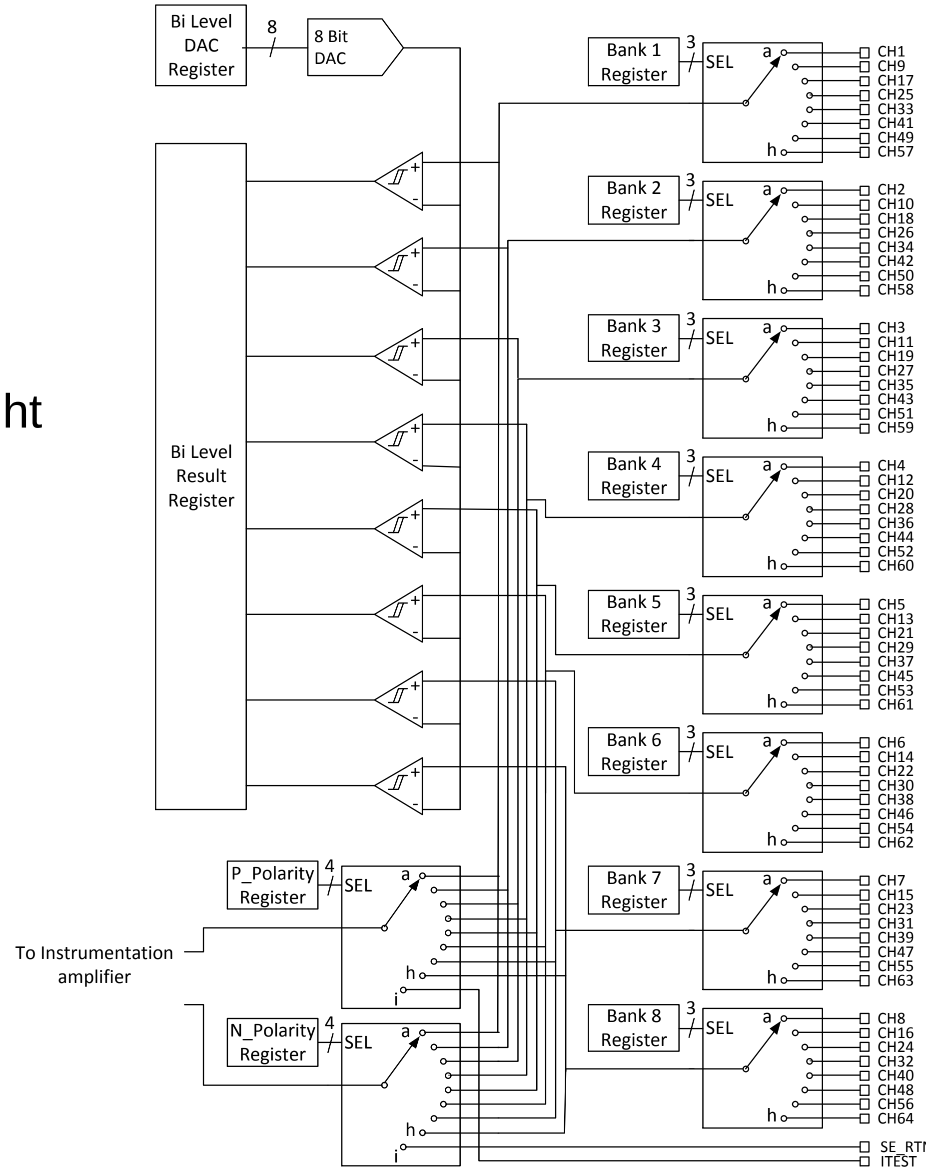
LX7730 Block Diagram

- 64 universal General Purpose Sensor Interfaces
  - 64 single ended or 32 differential
  - ADC range scaling
  - Level monitoring of 8 SE channels
  - Make before break switching
- 100ksps 12 bit ADC
- Optional 2 pole anti-aliasing filter
- 8 fixed bi-level logic interfaces
  - Internal or external threshold setting
- 10 bit current DAC
  - Complementary outputs
- 1% precision reference
- 2% current references
- Parallel or Dual SPI interface
- Built in test and calibration
- +15 VCC input to internal regulators



LX7730 Switch Matrix

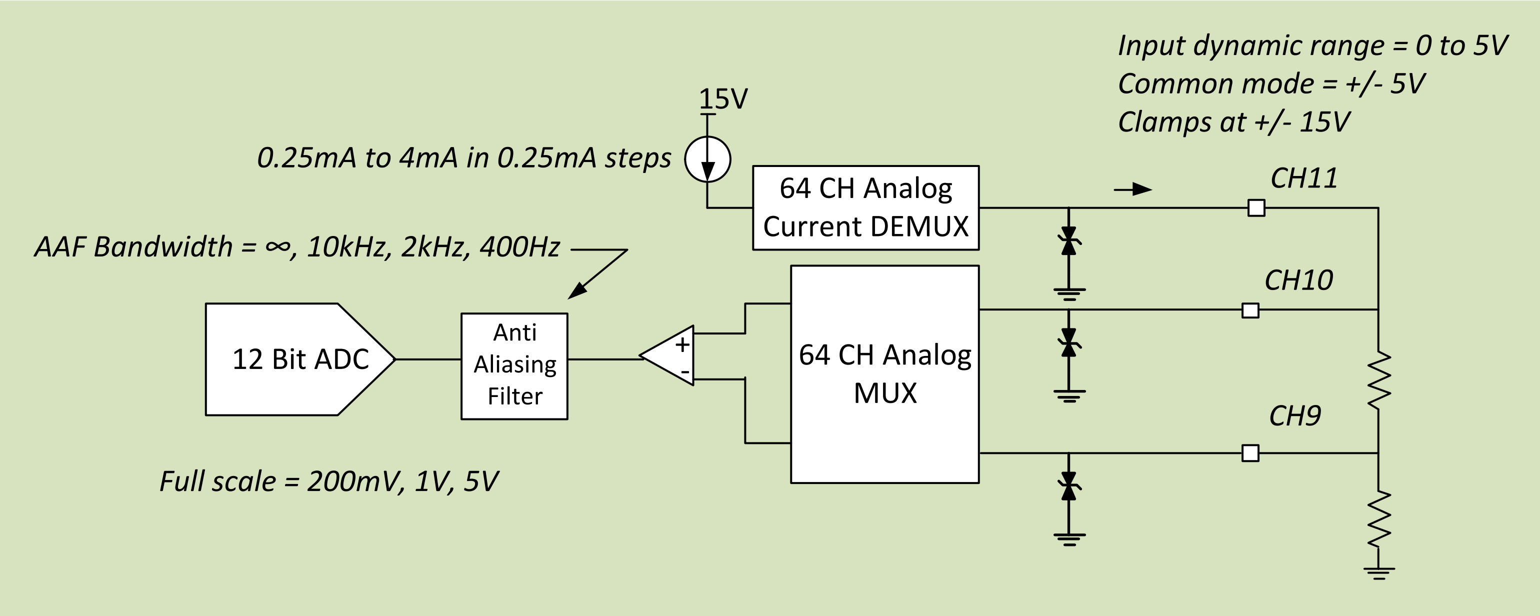
- Inputs are grouped in banks of 8.
- Differential measurements require inputs from 2 banks of 8
- SE_RTN input provides a common reference for up to 64 single ended measurements
- Simultaneous level monitoring for eight single ended inputs



	Pos 1	Pos 2	Pos 3	Pos 4	Pos5	Pos 6	Pos 7	Pos 8
Bank 1	CH1	CH9	CH17	CH25	CH33	CH41	CH49	CH57
Bank 2	CH2	CH10	CH18	CH26	CH34	CH42	CH50	CH58
Bank 3	CH3	CH11	CH19	CH27	CH35	CH43	CH51	CH59
Bank 4	CH4	CH12	CH20	CH28	CH36	CH44	CH52	CH60
Bank 5	CH5	CH13	CH21	CH29	CH37	CH45	CH53	CH61
Bank 6	CH6	CH14	CH22	CH30	CH38	CH46	CH54	CH62
Bank 7	CH7	CH15	CH23	CH31	CH39	CH47	CH55	CH63
Bank 8	CH8	CH16	CH24	CH32	CH40	CH48	CH56	CH64

LX7730 Current Source and Kelvin Sense

- Supports differential or single ended sensing
- Adjustable current source and DEMUX
- ADC range scaling
- Adjustable anti-aliasing filter



LX7730 HDL Module Tool Kit

- HDL Modules
  - Single register reads and writes
  - Data logging loop
  - Calibration
  - SPI interface
  - Parallel interface

LX7730 Direct Register Access

LX7730 Interface: SPIA ☐ SPIB ☑ Parallel ☐

Toggle Reset Pin

Parity Errors Detected: 0

Register Map	Contents	New Value	
ADDR 0: Master Reset	00000000	00000000	Write
ADDR 1: Function Enable	11111111	11111111	Write
ADDR 2: Power Status	00000000	00000000	Write
ADDR 3: Non-Inverting Chan Mux	00000000	00000000	Write
ADDR 4: Inverting Channel Mux	00000000	00000000	Write
ADDR 5: Current Source Level	00000000	00000000	Write
ADDR 6: Current Source DEMUX	00000000	00000000	Write
ADDR 7: Signal Conditioning Amp	00000000	00000000	Write
ADDR 8: ADC Control	00000000	00000000	Write
ADDR 9: ADC Upper Byte	00000000		
ADDR 10: ADC Lower Bits	00000000		
ADDR 11: Bi-Level Threshold DAC	00000000	00000000	Write
ADDR 12: Bi-Lvl Position and BLTH	00000000	00000000	Write
ADDR 13: Bi-Level Status	00000000		
ADDR 14: 10 Bit DAC Upper Byte	00000000	00000000	Write
ADDR 15: 10 Bit DAC Lower Bits	00000000	00000000	Write
ADDR 16: Calibration	00000000	00000000	Write
ADDR 17: Power and Ref Adjust	00000000	00000000	Write

Fixed Bi-Level Input Status (BLO7 to BLO0): 00000000

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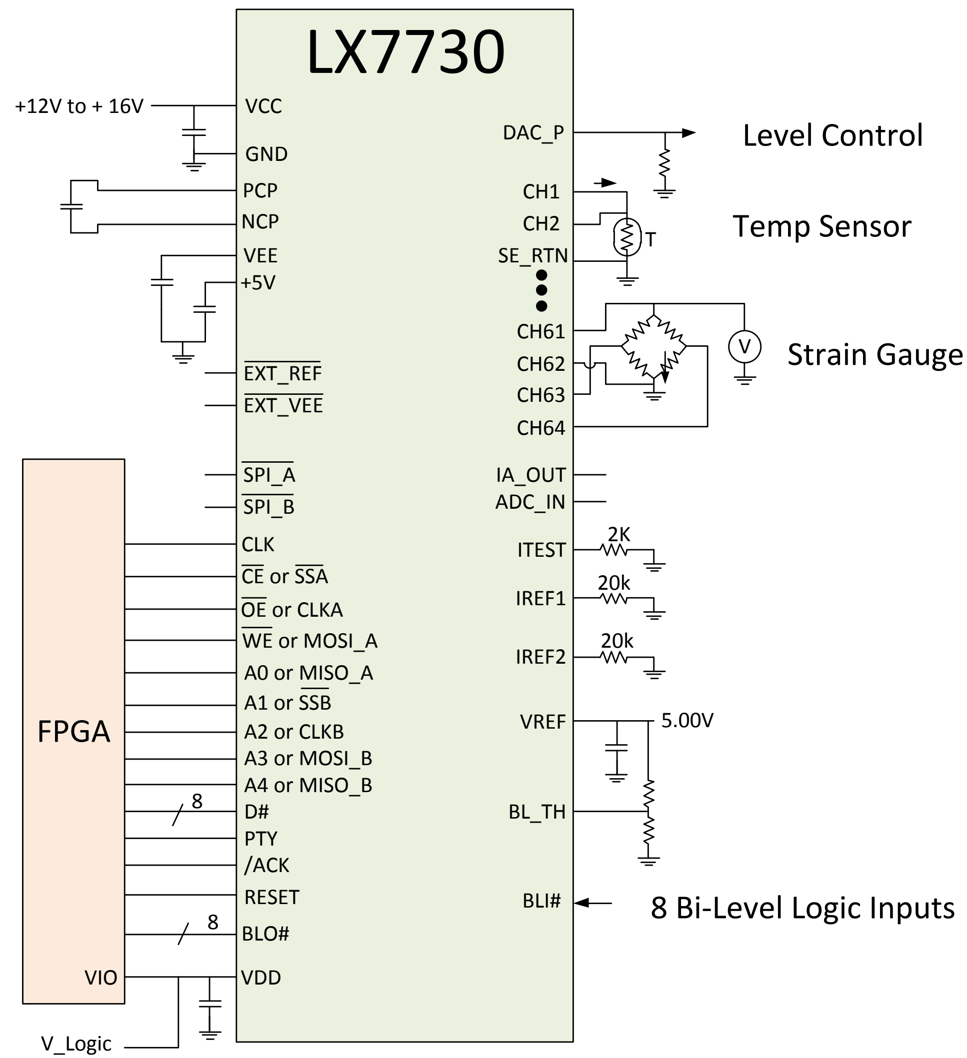
LX7730 Application Figure

- Level control
- Temp sensors monitor
- Strain gauges monitor
- Bi-level logic translation



LX7730 Performance Highlights

- LX7720 Performance

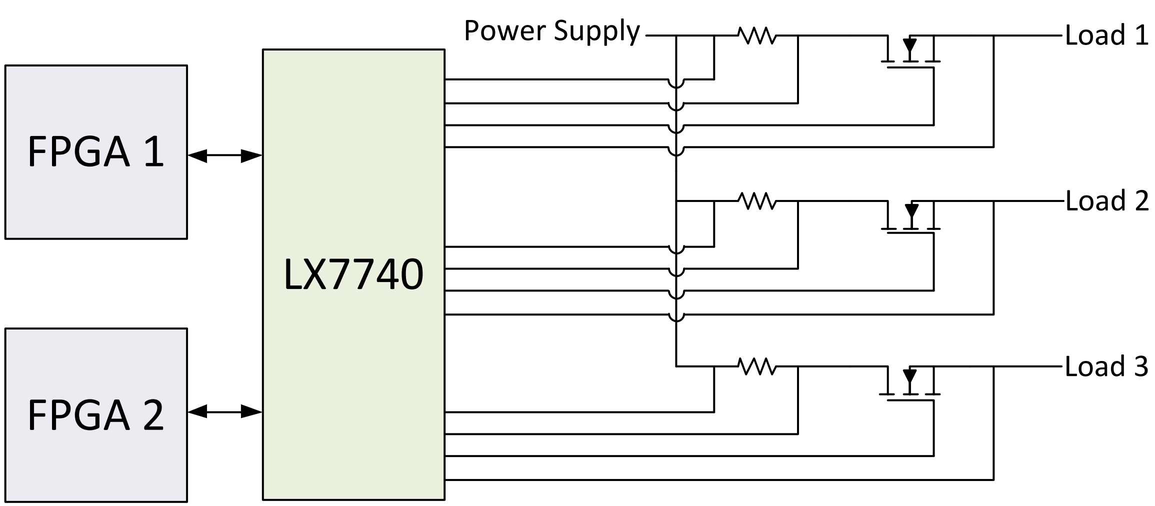
Parameter	Comment	Min	Typ	Max	Units
SE or Diff sensor input		0		5	V
Differential Sensor common mode		-5		5	V
ADC conversion rate			100		kHz
ADC acquisition time				500	ns
Reference voltage	Internal VREF	4.95	5.00	5.05	V
ADC non-linearity (integral or diff)		-1	0	1	LSB
MUX settling time			1.5		us
MUX leakage current	Power on or off	-100		100	nA
Bi-level threshold range		0.5		4.6	V
Bi-level propagation delay			1		us
DAC compliance range		0		3.0	V
DAC full scale current	Sourcing	1.94	2.00	2.06	mA

LX7740 Power Sequencing and Management

- Power Sequencing
  - Controls Ramp Rate and timing
  - Provides a clean power-up profile

- Power Management
  - Monitors analog voltage, current, temp

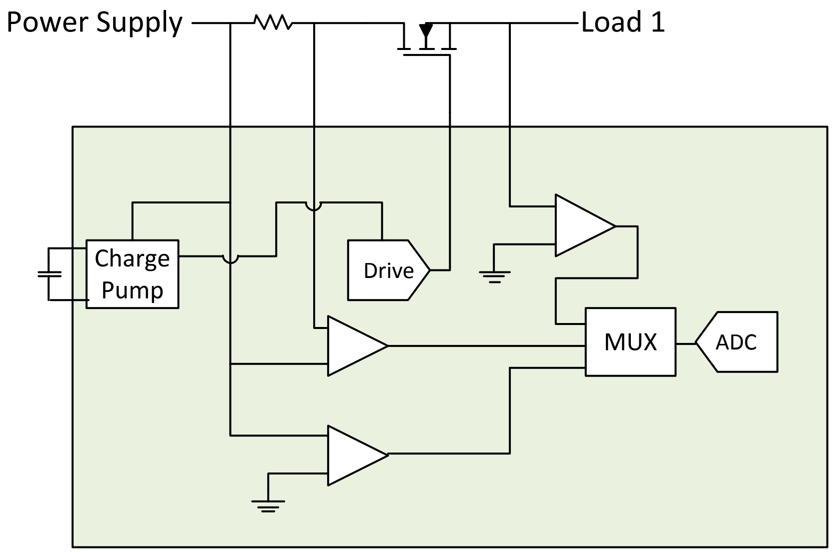
- Power Management
  - Fault detection and counter measures



3 of 8 channels shown

LX7740 Basic Element

- 8 Analog Quads
  - Monitor voltage, current temperature
  - Digital drive to ramp external switch
  - Charge pump provides Vgs for Nch switch full enhancement



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Companion Chip Advantages Summary

- Companion IC
  - Provides a high level of integration (smaller size and weight).
  - Is a standard part so there is minimal design risk or qualification risk.
  - No hardware development NRE.
  - Designed to work with the FPGA so flexibility designed in.
  - Designed for space applications so additional buffers and level shifting are not necessary.
  - Radiation tolerance, TID > 100kRad; ELDRS > 50KRad; SEL tolerant
  - Cold spared
  - Fault tolerant

Power Matters

Thank You