Content for the first 4 days will be split into 4 rooms with the content rotating through those sessions.
Everyone will attend each session and your track will be assigned on arrival.

	10/14/2013	10/15/2013	10/16/2013	10/17/2013	10/17/2013
	Monday SoC	**Tuesday SoC**	**Wednesday SoC**	**Thursday Verticals / MSCC Room A**	**Thursday Verticals / MSCC Room B**
8:00	Introduction SmartFusion2 and IGLOO2 Status (Si, 1V, Mil Temp, Package Rollout)	IGLOO2 System Builder Flow	Security – Programming – HSM Factory, Flash Pro 5	Vertical A / MSCC BU	Vertical E / MSCC BU
8:15				Vertical B / MSCC BU	Vertical D / MSCC BU
9:00	IP (TSE Soft Mac, EtherCAT, IP Protection Flow)	Constraints Tutorial (Lab)	Simple SPA/DPA primer	Vertical C / MSCC BU	Vertical B / MSCC BU
9:50	**Break**	**Break**	**Break**	Vertical D / MSCC BU	Vertical C / MSCC BU
10:10	Success Stories	Timing Analysis, MSS, FIC's (Lab)	Secure boot demo	**Break**	**Break**
11:00	Success Stories	AXI Tutorial	Applications using Data Security Features (Secure Boot)	Vertical E / MSCC BU	Vertical A / MSCC BU
12:00	**Lunch**	**Lunch**	**Lunch**	**Lunch**	**Lunch**
13:00	Low Cost PCIe Control Plane Demo (Lab)	DDR Configurator (Lab)	DSP Lab (Fir Filter Demo's)	MSCC Only Legal	
14:00	Basic PMA/SMA Demo (with char data) & Data Plane Demo	SMC_FIC how to use (Lab)	Third party DSP – Mathworks – Synphony	MSCC Only Legal	
14:50	**Break**	**Break**	**Break**	**Break**	**Break**
15:10	Low Power Demo (Lab)	Debug Identify and Live Probes (Lab) (debug broken Low power demo)	Core System Services (Lab)	MSCC Only Roadmap	
16:10	Design Security Settings (how to use, use models) (Lab)	SW Roadmap	IAP / ISP / Recovery Mode	MSCC Only FAE Feedback	
17:00	**Finish**	**Finish**	**Finish**	**Finish**	**Finish**
Theme	Seminar in a box day	SWE Day Libero 11.1 SP2 based (supports eval kit)	Processing + Security + Success Stories	Verticals / MSCC BU's	
Night	Happy Hour + Free	Free	Awards Night	Free	