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Power over Ethernet

PD690xx

Auto Mode Registers Map

Rev 1.3

Microsemi
Analog Mixed Signal Group
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Table of Contents

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1. Introduction

This Register Mapping Matrix comprises internal registers description for the **PD690xx (RTOEM) PoE** device.

1.1. General Note

PD690xx communication protocol is based on dual byte format (16 bit data), as illustrated in Section 2 below.

Each Read or Write transaction is framed in a dual byte packet. Registers of 8 bits or less are used as Read and Write pairs (two registers in a single packet). When calling a single 16 bit register, or two 8 bit registers, user (Host) should use a single "even" address, as specified in this document. There is no need to perform dual read/write transactions.

Note that writing/reading from an "odd" address will not be executed.

1.2. Example 1

To read Port 1 I_{cut} 8 bit register, user should access both Port 0 and Port 1 simultaneously through address “1000”. Note that register in address "1001" **CANNOT** be accessed directly, but only through address “1000”.

1.3. Example 2

To write into “System Power Budget 0” register, user should access “138C” address via 16 bit wide register. Register in address “138D” cannot be accessed directly.

If user attempts to read or write from “138D” address, data transfer will be corrupted and might damage IC configuration.

Addresses marked in brackets “(…)” cannot be accessed directly!

1.4. General Configuration Instructions

To protect PoE system from incorrect configuration sequencing, PD69012 has a dedicated software protection mechanism that ensures sensitive configuration registers are modified only when PoE ports are OFF.

This mechanism also ensures that PoE system is initialized properly after modifying those registers.

Important: Set PoE system configuration registers (such as AT/AF mode, Res/Legacy Detection mode, I_{CUT} currents levels etc.) only when system is initializing and ports are OFF.

The recommended sequence is:

1. Disable all ports (via Disable pin or via Disable Port Register)
2. Change mode to **config** mode (see instructions below)
3. Perform all necessary changes (Registers Set)
4. Return to normal operational Auto mode
5. Enable PoE ports power

To enter CONFIG mode, do the following:

1. DisPortsCmd register (address 0x1332) ➔ Write data = 0x03FF

   or disable each port in Portx_CR register (addresses 0x131A to 0x1330) bits [1:0] ➔ Data = 00
2. Change mode:
   a. SW_ConfigReg (address 0x139E) ➔ Write data = 0xDC03
   b. I2C_ExtSyncType (address 0x1318) ➔ Write data = 0x0020 (Mode Event Sync)
   c. EXT_EV_IRQ (address 0x1144) ➔ Write data = 0x0020 (Mode Event IRQ Sync)

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d. To ensure this command was properly performed, user may read SW_ConfigReg register (go to address 0x139E) ➔ Expected Read Data = 0x0003

Note: At this point, RAM space (address 0x1000 to the end) is open for Write operations. In this mode user can make changes to relevant registers.

3. After completing Write operation, return to operational Auto mode:
   a. SW_ConfigReg (address 0x139E) ➔ Write data = 0xDC00
   b. I2C_ExtSyncType (address 0x1318) ➔ Write data = 0x0020
   c. EXT_EV_IRQ (address 0x1144) ➔ Write data = 0x0020

To ensure that command was performed properly, user can read SW_ConfigReg register:

- (address 0x139E) ➔ Expected Data = 0x0000

4. Enable all PoE ports:
   - DisPortsCmd register (address 0x1332) ➔ Write data = 0x0000, or enable each port in the Portx_CR register (addresses 0x131A to 0x1330) bits [1:0] ➔ Write data = 01

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2. I²C Protocol Structure with Host

Figure 1 illustrates the sequence structure for Write cycles. Each packet ends with an Ack bit sent from the PoE system.

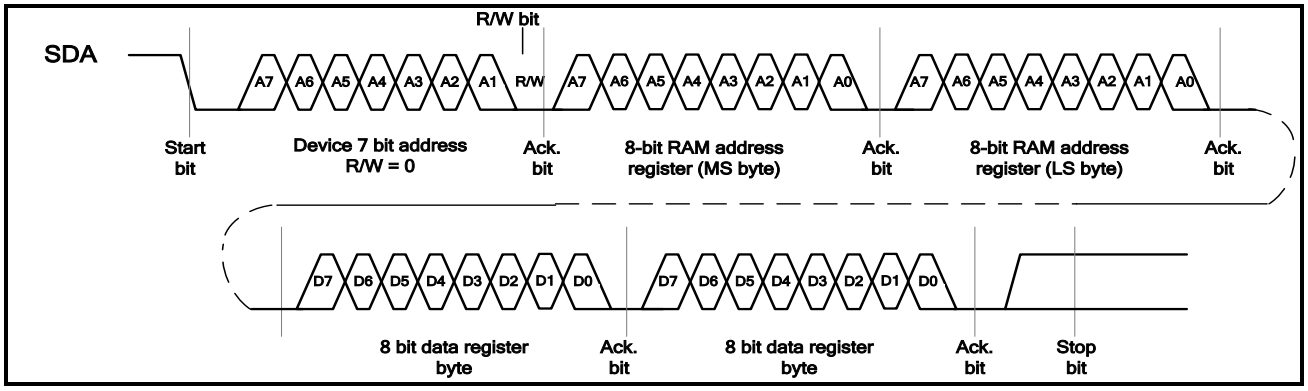

Figure 1: Sequence Structure for Write Cycles

Sequence structure for Read cycles (see Figure 2): Second start bit indicates a read cycle is following. The PoE system issues all Acknowledge bits, except for those issued by the Host as part of the reply from the PoE Device. The Host provides a stop bit.

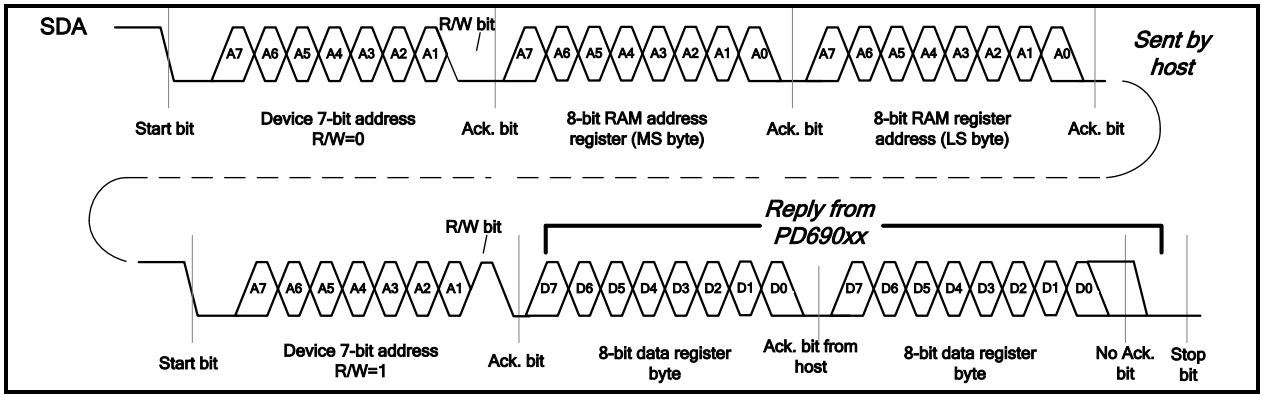

Figure 2: Sequence Structure for Read Cycles

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3. System Initialization Registers

Register Name	Register Description	Address (HEX)	Default Value	Register Width (BITS)	Read/ Write
Timer Value for Overload Conditions					
TovId_AF	Formula: • 1 LSB bit = 125µs • Range: 0 to 522ms *Example:* *For 10ms* *10 / .125 = 80 (decimal)*	100E	208H (65 ms)	16	R/W
TovId_AT		1010	208H (65 ms)	16	R/W
Maximum V_{main} Voltage Level Threshold (Before Powering Off All Ports)					
VmainHighTh	Formula: • 1 bit = 61mV, Range: 0 to 1023 = 0 to 59.392V *Example:* *For 50V max* *50V / 61mV = 820 (decimal)*	12FE	10'h3bc	10	R/W
Minimum V_{main} Voltage Level Threshold (Before Powering Off All Ports)					
VmainATLowTh	Formula: • 1 bit = 61mV, Range: 0 to 1023 = 0 to 59.392V *Example:* *For 45V min* *45V / 61mV = 738 (decimal)* *(Hysteresis of V_{main} Thresholds = 1V)*	1300	10'h313	10	R/W
VmainAFLowTh		1302	10'h2b0	10	R/W
Power Budget Guard Band Value for the Master PoE Device					
N/A – Irrelevant	PD69012 has a Dynamic Guard Band instead of a Static Guard Band See *PD690xx Technical Note TN-144* for Auto Mode Power Management's mechanism description.	N/A	N/A	N/A	N/A
Total Power Budget – Sets the Maximum Power Level, Available for All Ports (System)					
Master Configuration for SysPowerBudget0 …7	Master IC configuration for system power budget Supports up to eight power banks levels. Power budgets 000 to 111 (according to power good I/Os) 1 Bit LSB = 0.1W	138C 138E 1390 1392 1394 1396 1398 139A	8700 (3456W) 10E0 (432W) BB8 (300W) 898 (220W) 7D0 (200W) 5DC (150W) 4B0 (120W) 3E8 (100W)	16	R/W

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Register Name	Register Description	Address (HEX)	Default Value	Register Width (BITS)	Read/ Write
Power Management Mode					
PM mode – sys Flag	Set power management calculation method for IC: • "0": Static Mode; according to Class or Port Power Allocation Level (PPL) ➔ PPL is set through Address Registers 1334 to 134A • "1": Dynamic Mode; according to actual (real time) power consumption	1160 Bit [6]	0 = Static	1	R/W
General User Registers					
General User register	General User register for user's use	0318	16'h0000	16	R/W
Legacy CAP Detection	Legacy CAP Detection Enable register BIT[2] • "1" = Cap Detection disabled • "0" = Cap Detection enabled	1160 Bit[2]	1= Disabled	16	R/W
Software Configuration register	Software Configuration & Change Mode Protection register **Bits [2:0] = SW Configuration Key** • 000: Stand alone master \ slave • 001: Macro mode slave • 010: Manual mode • 011: Config. mode **Bits [7:3] = Spare = Not Used** **Bits [15:8] = Special Change Mode Key** Verification key for the mode change ➔ Only if 0xDC enable mode changes	139E	16'h0003	16	R/W
I2C Communication External Sync register	This register defines the type of external sync event expected by I2C communication • 0x01: Detection Sync • 0x02: Startup Sync • 0x04: Update PB Sync • 0x08: Read Indications Sync • 0x10: Macro Sync • 0x20: Mode Sync • 0x40: Interrupt Out Sync • 0x80: Read PM Indications Sync 0x100: Masters Sync (for Host use)	1318	16'h0000	16	R/W

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Register Name	Register Description	Address (HEX)	Default Value	Register Width (BITS)	Read/ Write
External Event: Interrupt register for SYNC	This register defines the type of external sync, Interrupt Request Signal event expected by I2C communication • 0x01: Detection Sync • 0x02: Startup Sync • 0x04: Update PB Sync • 0x08: Read Indications Sync • 0x10: Macro Sync • 0x20: Mode Sync • 0x40: Interrupt Out Sync • 0x80: Read PM Indications Sync • 0x100: Masters Sync (for host use)	1144	16'h0000	16	R/W

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4. Ports Initialization / Configuration Registers (Port Setting)

Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
Set / Updates Icut Value – According to Class Level					
ICUT mode – sys Flag	Set I_{cut} level according to CLASS Level: • "0": Set I_{cut} according to CLASS • "1": Set I_{cut} to maximum value according to power allocation limits (for more information see address registers 1334 to 134A)	1160 Bit[4]	1 = I_{cut} MAX	1	R/W
Per Port Configuration					
Per Port Configuration: (12 registers) Port0_CR… Port11_CR	BITS [0;1] = Port Enable • "00": Port Disable • "01": Port Enable • "10": Force Power • "11": Reserved (future use) BITS [2;3] = Port Pair Control • "00": Reserved (future use) • "01": ALT A • "10": ALT B (back off enable) • "11": Reserved (future use) BITS [4;5] = AF/AT Port type • "00": AF • "01": AT • "10": Reserved (future use) • "11": Reserved (future use) BITS [6;7] = Port Priority • "00": Critical = Highest priority level • "01": High • "10": Low • "11": Reserved (future Use)	131A 131C 131E 1320 1322 1324 1326 1328 132A 132C 132E 1330	DFLT= 01-EN 01-ALTA 01-AT 00-Critical	16	R/W

5. System Status / Monitoring

Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
V_{main} Voltage Measurement Register					
V_{main}	V_{main} voltage measurement register 1 LSB Bit =61 mV Range = 0 to 1023 = 0 to 62 V	105c	10'h0	10	Read
Hardware Configuration & Mode Register					

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
System INIT register	Internal Register: Latched from ASIC_INI and I2C_INI I/Os after Power Up Bits[0;3] = ASIC_INI Value Bits[4;7] = I2C_INI Value Bits[8;15] = Version Register Value	1164	16'h0	16	Read
Averaged Junction Temperature Level					
Averaged Junction Temperature	Averaged Junction Temperature, as constantly calculated and monitored by two temperature sensors, located on PD69012 Die. Typical accuracy is ±-5° C Temperature formula = Deg C = (reg_value: 684) / (-1.514)) - 40 (1 LSB = ~0.66C)	130A	10'h0	10	Read
Device Version Control Register					
CFGC_ICVER	IC HW & SW version; it is an internal / read only register. This register identifies chip type and internal analog, digital code, and ROM versions, based on the following coding: BITS [15-11]: Microsemi PoE Family Indication (5 MSB bits): • 5'b00010 = PD64004 • 5'b00110 = PD64012 • **5'b00111 = PD69012 (default)** • 5'b01000 = PD69004 BITS [10-8]: Analog version (3 bits) = 1 dec BITS [7-5]- Digital version (3 bits) = 1 dec BITS [4-0]: SW ROM version (5 LSB bits) = 2 dec	031A	16'b001 11,001, 001,00 010	16	Read
System Total Power Monitoring (Read from Master IC)					

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
SysTotalRealPowerCons	Total power consumption of the whole system (Master + 7 Slaves) 1 LSB = 0.1 Watt	**12E8**	16'h0	16	Read
TotalPowerConsSlave0 to Slave7	Power consumption monitoring – as read from Master IC. 16 bits register Per IC From Slave 0, address 12EC (Master), to Slave 7 – Add 12FA 1 LSB = 0.1W	12EC 12EE 12F0 12F2 12F4 12F6 12F8 12FA	16'h0	16	Read
Local Total Power Level (Read from Slave IC)					
LocalTotalRealPowerCons	Power consumption monitoring, as read from Slave IC. Real total power consumption ∑(PortXPowerCons) 1 LSB = 0.1W	12AA	16'h0000	16	Read
Additional IC Status Indications	Bit [0]: V_{main} is above upper threshold Bit[1]: Junction temperature is above threshold (150° C) Bit [2]: Disable ports I/O is active Bit [3]: V_{main} is below AT low threshold Bit [4]: V_{main} is below AF low threshold Bit [5]: The temperature is above alarm threshold	1314	16'h00	16	Read

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6. Port Status Monitoring

Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
Port Classification Results Status					
Port0_class… Port1_class	Port CLASS Status Monitoring: [3:0]: First finger result [7:4]: Second finger result [15:8]: Final detected class • 000: Class 0 • 001: Class 1 • 010: Class 2 • 011: Class 3 • 100: Class 4 • 101: Reserved • 110: Reserved • 111: Class not defined	11C2 11C4 11C6 11C8 11CA 11CC 11CE 11D0 11D2 11D4 11D6 11D8	7'h7	16	Read
Port Power Consumption Value					
Port0PowerCons…. Port11PowerCons	Real Time (actual) port power consumption. Calculated based on I_{port} * V_{port} 12 registers per IC: Port 0 to Port 11 LSB = 0.1W	12B4 12B6 12B8 12BA 12BC 12BE 12C0 12C2 12C4 12C6 12C8 12CA	16'h0	16	Read
AC Disconnect Status Register					
Port Disconnection Status	See port status registers address 11AA – 11C0				Read
Port Power Status Due to DC Disconnect					
	See port status registers Address 11AA – 11C0				
Port Overload Status					
Port Overload Status	See port status registers Address 11AA – 11C0				
Port Off Due to Disable_Ports pin or Vmain Out of Range					
Port Off due to Disable	See port status registers Address 11AA – 11C0				

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
OVL During Startup					
Over Load during Startup	See port status registers addresses 11AA – 11C0				
Port Start up Stage is Completed					
Start Up Completed	See port status registers addresses 11AA – 11C0				
Port Over Power Consumption Status					
Port Over Power	See port status registers addresses 11AA – 11C0				
Read Port Status Register					
Port Status [0-7] Port Status [8-10] Port Status [11]	Port status indication is based on real-time snapshot of port status. Status Indication Coding Bits are NOT latched and may be changed to reflect real-time (True) port status at Read Operation time slot. The indication is based on two fields: **Bits [7-0]**: Coded into 21 different status indications as listed below: Decimal Value = 0 (zero): Port is on; Port was turned on due to a valid signature (res or cap) Decimal Value = 1: Port is On; Port was turned on due to Force Power command Decimal Value 2: Port is in Starting Up stage Decimal Value 3: Port is powered up due to Force Power command Decimal Value 4: Searching; Port is waiting for detection, or during detection phase Decimal Value 5: Invalid Signature; Invalid signature (detection) has been detected Decimal Value 6: Class Error; Error in classification has been detected	11AA 11AC 11AE 11B0 11B2 11B4 11B6 11B8 11BA 11BC 11BE 11C0	16'h00	16	Read

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
	Decimal Value 7: Test Mode; Port is waiting to be turned on in Test Mode Force Power Decimal Value 8: Valid Signature; A valid signature has been detected (Detection Pass) Decimal Value 9: Disabled; Port is disabled Decimal Value 10: Startup OVL; Over-load during startup Decimal Value 11: Startup UDL; Under-load during startup Decimal Value 12: Startup Short; Short during startup Decimal Value 13: DvDtFail; Failure in the Dv/Dt algorithm Decimal Value 14: Test Error; Port was turned on as Test Mode (Force Power) and has error Decimal Value 15: OVL; Overload detected Decimal Value 16: UDL; Under-load detected Decimal Value 17: Short Circuit; Short circuit detected Decimal Value 18: PM; Port was turned off due to Power Management Mechanism Decimal Value 19: System Disabled; Chip level error Decimal Value 20: Unknown; General chip error **Bits [10-8]:** Additional 3 bits coding for 8 additional status indications BITS [8-10] Coding:				

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
	• 000: Disabled • 001: Searching • 010: Delivering Power • 011: Test Mode • 100: Test Error • 101: Implementation Specific* • 110: Reserved • 111: Reserved BIT[11]: • 0: Port in AF Mode after Class • 1: Port in AT Mode after Class				

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7. Port Commands

Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
Port Bypass Resistor (Res) Detection					
	No Bypass or Disable Res Detection function in Auto mode				
Port Bypass Classification					
	No Bypass or Disable Classification function in Auto mode				
Port Enable Control					
Port Disable/Enable – Fast Port Off in 1 register	One single register to disable ports (bit per port) 0: Port Enable 1: Port Disable	1332	16'h0	16	R/W
Turns off Main Switching FET (Port OFF)					
Port0_CR…. Port11_CR	Per Port Control register: Bits [0;1] 00: Port Disabled 01: Port Enabled 10: Force Power 11: Reserved	131A 131C 131E 1320 1322 1324 1326 1328 132A 132C 132E 1330	2'h01 Enable	2	R/W
Port Test Mode Force ON Command (event)					
Port0_CR…. Port11_CR	Per Port Control register – Bits [0 ;1] • 00: Port Disabled • 01: Port Enabled • 10: Force Power • 11: Reserved	131A 131C 131E 1320 1322 1324 1326 1328 132A 132C 132E 1330	2'h01 Enable	2	R/W

8. Interrupt Registers

Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
Interrupt Register					
Port Interrupt Out register	This 12 bits register has a bit per port indication corresponding to the port that had an interrupt out event. BIT [0 ..11] = Ports 0 to 11	13A6	12'd000	12	RO
Interrupt I/O Enable	This bit switches LSD I/O between LED stream data functionality output and interrupt (INT) functionality output (enabling the INTERRUPT OUT I/O at the LSD pin) BIT [5] "1" = LED Stream Data (LSD) Out "0" = INT Out	1160 BIT 5	1 = Disable	16	R/W
Interrupt Event Mask register	Each bit in this INT MASK register refers to a specific event MASKED or ENABLED to be latched in INT register. "1" = Event enabled (not masked) "0" = Masked The events are: • [0] Port Power Up • [1] Port Power Down • [2] Detection Fail • [3] OVL or Short • [4] UDL or Disconnect • [5] OVL During Start • [6] Port Off due to PM • [7] Port Off at Start Up • [8] Over Temperature • [9] Temperature Alarm • [10] V_{main} < AF limit • [11] V_{main} < AT limit • [12] V_{main} > Lim • [13] Reserved Event	13A4	16'd000	16	R/W
Power Up – Interrupt Event					

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
Port Power Up	Per Port Power Up event. Logic "1" indicates that the specific port was switched **on** (including force power command) • [0] Port #1 • [1] Port #2 • [2] Port #3 • [3] Port #4 Formula: • "1" = Event was detected • "0" = Event was not detected or was cleared	01AE	4'd0	4	RO
Interrupt – Clear On Read Command					
Port Power Up - Clear On Read register	Read Operation of this register clears up specific bit in associated interrupt register. Logic "1": clears specific bit. • [0] Port #1 • [1] Port #2 • [2] Port #3 • [3] Port #4 Formula: "1" = Clears event operation "0" = Does not clear operation	01AF	4'd0	4	RO

9. PD690xx Detailed Registers List and Description

REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
Port [0 to 11] Current Sense register (I_{sense})	Per Port Current Consumption (I_{sense}) Level Port 0 = Address 1044 Port 1 = Address 1046 … Port 11 = Address 105 A I_{sense} level is the port real time current monitoring (value) as measured on the external Sense Resistor (Sense pin). Register can range from 0 to 1.25A Register Resolution = 305µA per LSB I_{sense} value is automatically averaged and updated every ~1ms Reset value = 0 Typical accuracy of this Current Monitoring register is ±5%	1044 1046 1048 104A 104C 104E 1050 1052 1044 1056 1058 105A	0	[11:0]	RO
V_{main} Measurement register	Main Power Supply: Voltage Measurement register V_{main} voltage is measured on V_{main} pin Register can range from 0 to ~63V Register Resolution = 61mV per LSB V_{main} value is automatically averaged and updated every ~20 ms Reset value = 0 Typical accuracy is ±3%	105C	0	[9:0]	RO
I^2C External Sync Control register	IC Interrupt Signal (pin) is driven by an internal Interrupt register. This register is **doubled buffered.** This prevents skipping (missing) any internal event while busy with the Interrupt Handling Routine. For Host to update the Interrupt register, Microsemi recommends using the following routine: 1. Set **Register 1318** to the desired (expected)	1318	0	[15:0]	R/W

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
	Sync Type (see below). 2. Perform **Write Command** to Register 1144 (which updates the actual Double Register). This register defines the type of external sync Interrupt Request Signal event expected by I^2C communication • 0x01: Detection Sync • 0x02: Startup Sync • 0x04: Update PB Sync • 0x08: Read Indications Sync • 0x10: Macro Sync • 0x20: Mode Sync • 0x40: Interrupt Out Sync • 0x80: Read PM Indications Sync 0x100: Masters Sync (for Host use)				
Update Interrupt Event register	Write to this register. The access operation itself to this register (address 1144) creates an internal SYNC signal which activates (updates) External Sync Type – address 1318)	1144	0	[15:0]	WO
System Configuration and Control	Bit 0 = DC Disconnect Enable • 0: AC Disconnect mode (all ports) • 1: DC Disconnect mode (all ports) Bit 1 = Internal Use (should be set to 0) Bit 2 = Legacy PD Detection Mode (Capacitor Det) • 0: Legacy PD Detection Enable • 1: Legacy PD Detection Disable Bit 3 = Internal Use (should be set to 0) Bit 4 = Set I_{cut} Level • 0: Set I_{cut} Current Level according to Power Management and Power Budget algorithm • 1: Set I_{cut} Current Level to Maximum Level according to AF and AT modes Bit 5 = Internal Use (should be set to 0) Bit 6 = Power Management Calculation mode • 0: Static mode. Power is allocated and total power is calculated according to pre-defined fixed power level per port • 1: Dynamic mode. Power is allocated and	1160	0	[14:0]	R/W

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
	total power is calculated according to port power consumption (in real time) Bit 7 = Internal Use (should be set to 0) Bit 8 = Internal Use (should be set to 0) Bit 9 = V_{main} Under Voltage Protection in AT mode • 0: AT Ports are **not** disconnected when V_{main} is under 51V (not protected) • 1: AT Ports are disconnected when V_{main} drops below 51V Bit 10 = Detection of class 0 indicates AF operation mode. • 0: If Class 0 is detected, port is configured as AT • 1: If Class 0 is detected, port is configured as AF • Bit 11 = This bit interprets classes 1, 2 and 3 configuration: • 0: Classes 1, 2 or 3 are considered AT • 1: Classes 1, 2 or 3 are considered AF Bit 12 = Internal Use (should be set to 0) Bit 13 = Internal Use (should be set to 0) Bit 14 = Internal Use (should be set to 0)				
Software Boot State Monitoring	This register can be used to monitor and debug IC Internal CPU Core or internal RAM or EEPROM. When IC is powered-up, internal CPU Core is initialized through the following boot sequence. Boot sequence is based on 10 different phases (each phase duration is ~100µs) Bit 9 in used for Boot Sequence Completion indication. **Real Time Boot State Bits [7 to 0]**: Dec. value 1: Verified ASIC_INI read Dec. value 2: Verified I2C_INI read Dec. value 3: Master configured on enhanced chip Dec. value 4: Waiting for enhanced mode verification key Dec. value 5: ASIC_INI configured manual mode Dec. value 6: EEPROM Read Dec. value 7: Master held by disable ports	1168	0	[14:0]	RO

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
	line Dec. value 8: Slave in initial config. mode Dec. value 9: Boot done Internal CPU Core Register Monitoring, indicating last SW error Bits [13 to 8] 00000: No SW error since last reset 00001: Empty memory space 00010: Illegal bus access 00100: Write in ROM space 01000: Instruction fetch in register space Valid EEPROM Indication: Bit [14] "0" – No EEPROM found or Invalid data "1" – Valid EEPROM found and data updated successfully				
Startup Completed Voltage Threshold	Voltage threshold for early startup completion phase. If V_{port} reaches a specific threshold, then Startup phase is completed. Port proceeds to Ongoing state, releasing current limit from AF lim to AT lim while activating real time protections mechanisms (Overload, Disconnect, Power Management, etc) Threshold voltage is useful for High Power PD's that need to release Higher Current Limit as fast as possible, without waiting 70ms as defined in standard. Threshold is calculated by: [V_{main} + 1.2V - register value x 59.3mV] For example, if V_{main} = 48V and this register is set to dec. value 100, threshold level will be 48 + 1.2 - 5.9 = 43.3V Note that DFLT value is 0. Hence by default this Early Start Up Completion is **not** activated. Start Up phase will be completed only ~65ms after Port Power Up command. Register Range = 0 to 60V LSB = 59.3mV	11A8	0	[9:0]	R/W
Port [0 to 11] Status	Internal Status Bits [7 to 0]: Note that these 8 bits are **not** latched (non-sticky). Value of this 8 bit field is updated momentarily (real-time) by internal logic. Therefore it does not	11AA 11AC 11AE	9 [disable]	[11:0]	RO

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
Port 0 = 11AA . . . Port 11 = 11C0	necessarily reflect Port Status when actual read command is performed. For a better Port Status Visibility, it is recommended to use bits [10 to 8] which are more stable/practical. • 0 (dec) = Port On. Port was turned on due to a valid signature (res or cap) • 1 (dec) = Force On Port. Port was turned on due to Force Power • 2 (dec) = Startup. Port is starting up • 3 (dec) = Force Power StartupTM. Port is starting up by force power • 4 (dec) = Searching Phase. Port is waiting for detection or during detection phase • 5 (dec) = Invalid Signature. Invalid signature has been detected • 6 (dec) = Class Error. Error in classification has been detected (For example: Class Finger 1 is different than Finger 2) • 7 (dec) = Test mode. Port turned on in Test mode – Force Power • 8 (dec) = Valid Signature. A valid signature has been detected • 9 (dec) = Disabled. Port is disabled • 10 (dec) = StartupOVL. Overload during startup • 11 (dec) = StartupUDL. Under-load during startup • 12 (dec) = StartupShort: Short during startup • 13 (dec) = Port Start Up Fail. Failure in Start Up (dv/dt) algorithm • 14 (dec) = Test Error. Port was turned on in Test mode and has an error • 15 (dec) = OVL. Overload detected • 16 (dec) = UDL. Under-load detected • 17 (dec) = Short Circuit. Short circuit detected • 18 (dec) = Power Management Off – port was turned off due to Power Management • 19 (dec) = Sys. Disabled. Chip level error (over voltage or over temp.) • 20 (dec) = Unknown. General chip error Port Status: Bits [10 to 8] Value of this 3 bit field indicates Real Time Port	11B0 11B2 11B4 11B6 11B8 11BA 11BC 11BE 11C0			

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
	Status Change by internal logic. These 3 bits better reflect Port Status when actual read command is performed. • 000: Port Is Disabled (Port Off) • 001: Port is Searching for PD Detection • 010: Port is Delivering Power (Port On) • 011: Port is in Test mode • 100: Reserved • 101: Reserved • 110: Reserved • 111: Reserved AT mode [Bit 11]: After classification this bit indicates whether the port is an AF or an AT • 0: port is detected as AF • 1: port is detected as AT				
Port [0 to 11] Class Status Port 0 = 11C2 . . . Port 11 = 11D8	• First Finger Class Results: Bits [3 to 0] • Second Finger Class Results: Bits [7 to 4] • Final Class Results: Bits [15 to 8] • 000: Class 0 • 001: Class 1 • 010: Class 2 • 011: Class 3 • 100: Class 4 • 101: Class Error (>50mA) or Finger 1 different than Finger 2 • 110: Reserved • 111: Class is not Defined	11C2 11C4 11C6 11C8 11CA 11CC 11CE 11D0 11D2 11D4 11D6 11D8	7 (dec)	[15:0]	RO
Per Port Class Status register	Bit Per port: Overall result for classification Bit 0 = Port 0 Bit 1 = Port 1 . . Bit 11 = Port 11 0: class is completed okay 1: class fail	11DA	0	[11:0]	RO
Port Last Disconnection Event Port 0 = 11DC . . .	Reason for last port disconnection • 9 (dec) = Port was disabled • 10 (dec) = Port was overloaded during startup • 11 (dec) = Port was under-loaded during startup • 12 (dec) = Port was shorted during	11DC 11DE 11E0 11E2 11E4 11E6 11E8 11EA	0	[7:0]	RO

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
Port 11 = 11F2	startup • 13 (dec) = A port failure in startup algorithm • 14 (dec) = Port was turned on as Test, Mode and has an error • 15 (dec) = Overload detected • 16 (dec) = Under-load detected • 17 (dec) = Short circuit detected • 18 (dec) = Port was turned off due to Power Manager • 19 (dec) = Chip level error • 20 (dec) = General chip error	11EC 11EE 11F0 11F2			
Port Counter for Invalid Detection Events Port 0 = 11F4 . . . Port 11 = 120A	Per Port 8 Bit Counter: Counts the number of Invalid Detection Events (Wrong Signature) from IC's last power up This Counter is cyclic: When it is full (FF) it goes back to 0 and restarts counting.	11F4 11F6 11F8 11FA 11FC 11FE 1200 1202 1204 1206 1208 120A	0	[7:0]	RO
Port Counter for Power Denied Events Port 0 = 120C . . . Port 11 = 1222	Per Port 8 Bit Counter. Counts the number of Power Denied Events (Due To Power Management) from IC last power up. When counter is full (FF) it goes back to 0 and restarts counting.	120C 120E 1210 1212 1214 1216 1218 121A 121C 121E 1220 1222	0	[7:0]	RO
Port Counter for Over Load Events Port 0 = 1224 . . . Port 11 = 123A	Per Port 8 Bit Counter. Counts the number of Overload Events from IC last power up. When counter is full (FF) it goes back to 0 and restarts counting.	1224 1226 1228 122A 122C 122E 1230 1232 1234 1236 1238 123A	0	[7:0]	RO

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
Port Counter for Under Load Events Port 0 = 123C . . . Port 11 = 1252	Per Port 8 Bit Counter. Counts the number of Under-Load Events from IC last power up. When counter is full (FF) it goes back to 0 and restarts counting.	123C 123E 1240 1242 1244 1246 1248 124A 124C 124E 1250 1252	0	[7:0]	RO
Port Counter for Short Events Port 0 = 1254 . . . Port 11 = 126A	Per Port 8 Bit Counter. Counts the number of Short Events from IC last power up. When counter is full (FF) it goes back to 0 and restarts counting.	1254 1246 1258 125A 125C 125E 1260 1262 1264 1266 1268 126A	0	[7:0]	RO
Port Counter for Class Error Events Port 0 = 126C . . . Port 11 = 1282	Per Port 8 Bit Counter. Counts the number of Class Error Events from IC last Power Up. When counter is full (FF) it goes back to 0 and restarts counting.	126C 126E 1270 1272 1274 1276 1278 127A 127C 127E 1280 1282	0	[7:0]	RO
Per Port Status Indication Port 0 = 1284 . . . Port 11 = 129A	Per Port Status Indication Sticky Bits with Double Buffer Original bits are cleared on read To read this register → users need to perform Indication Sync: 1. Write to 1364 – Port Select 2. Perform Sync Read Indication (Type) 1318 3. Write to 1144 Bit 0 = Under Load (Disconnect) detected • 0: No under-load detected • 1: Under-load detected	1284 . . . 129A	0	[8:0]	RO

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
	Bit 1 = Overload detected • 0: No overload detected • 1: Overload detected Bit 2 = Short Detected • 0: No short detected • 1: Short detected Bit 3 = invalid PD Resistor Signature detected • 0: No Invalid signature detected • 1: Invalid signature detected Bit 4 = Valid PD Resistor Signature detected • 0: No Valid PD signature detected • 1: Valid PD signature detected Bit 5 = Power Was Denied • 0: Power has not been denied • 1: Power has been denied Bit 6 = Valid Capacitor signature detected • 0: No Valid Capacitor detected • 1: Valid capacitor detected Bit 7 = Back off state has occurred • 0: No Back off was made • 1: Back off was done Bit 8 = Class Error has occurred • 0: No class error detected • 1: Class error detected				
Ports Power Management Indication	Bit per port: Indicates a power management event Bit 0 = Port 0 . . Bit 11 = Port 11 • 0: Port is not marked to be a candidate for power management disconnection in case of missing budget • 1: Port is marked to be a candidate for power management disconnection in case of a missing budget	129C	0	[11:0]	RO

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
Port Real Time (Actual) Power Consumption Port 0 = 12B4 . . . Port 11 = 12CA	Port power consumption (Actual Real Time Power Consumption) Port Power is calculated based on: I_{port} x V_{port} LSB = 0.1W Range = 0 to FF For example: Register Decimal Value = 100 = 10W	12B4 . . 12CA	0	[15:0]	RO
ChipTotalCurrentCons	IC total port current (summary of all 12 ports); based on port actual current (load) LSB = 4.88mA For example: Register Value = AA (hex) = 170 (dec) = 0.8 amp	12D2	0	[15:0]	RO
Total System Calculated Power Consumption	Sum of the whole system calculated power consumption (including all IC's, masters and slaves, that are currently connected to this master IC) This calculated power consumption is based on Port Requested Power by Class and AF/AT mode Note that this register should be read from master only. Before reading this register it is recommended to update its content by writing "1" to register address 139C LSB = 0.1W Range = 0 to FF For example: Register Decimal Value = 500 = 50W	12E2	0	[15:0]	RO
Total System Real Time / Actual Power Consumption	Sum of whole system real time power consumption Power consumption is based on All Active Ports Power Consumption Note that this register should be read from master only. Before reading this register it is recommended to update its content by writing "1" to register address 139C LSB = 0.1W Range = 0 to FF For example: Register Decimal Value = 500 = 50W	12E8	0	[15:0]	RO

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
Active Slave List Register	First 8 LSBits [7 to 0] represent a bit per Active Slave IC Bit 0 = Slave 0 … Bit 7 = Slave 7 1 = Slave IC is active 0 = Slave IC is not active Note that this register should be read from master IC only. Before reading this register it is recommended to update its content by writing “1” to register address 139C Other 8 MSBits [15 to 8] represent a bit per detected slave IC on power up Bit 8 = slave 0 … Bit 15 = Slave 7 • 1 = Slave IC was detected on Power Up • 0 = Slave IC was not detected	12EA	0	[15:0]	RO
Total (Actual) Power Consumption Per Slave IC Slave 0 = 12EC . . . Slave 7 = 12FA	Total real time / actual power consumption of slave 0 (master) Note that this register should be read from master only. Before reading this register it is recommended to update its content by writing “1” to register address 139C LSB = 0.1W Range = 0 to FF For example: Register Decimal Value = 100 = 10W	12EC . . 12FA	0	[15:0]	RO

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
V_{main} High (MAX) Threshold	Maximum V_{main} Threshold Above this level all ports are disconnected to protect PD from overvoltage This policy is always activated. LSB = 61mV Range = 0 to 62V For example: Register DFLT Value = 3BC (hex) = 956 (dec) = 58V	12FE	3BC	[9:0]	R/W
AT mode V_{main} Low (MIN) Threshold	Minimum V_{main} threshold for AT mode. Below this level “AT” ports are disconnected to comply with AT standard. This policy can be activated or deactivated according to register address 1160 Bit 9. LSB = 61mV Range = 0 to 62V For example: Register DFLT Value = 313 (hex) = 787 (dec) = 48V	1300	313	[9:0]	R/W
AF mode V_{main} High (MAX) Threshold	Minimum V_{main} Threshold for AF Mode. Below this level “AF” ports are disconnected to comply with AF standard. This policy is always activated. Range = 0 to 62V For example: Register DFLT Value = 2B0 (hex) = 688 (dec) = 42V	1302	2B0	[9:0]	R/W
Junction Averaged Temperature	Junction average temperature, based on two temperature sensors located on Die. Temperature (deg C) = ((reg_value: 684) / (-1.514)): 40 Range = ~-200°C to ~400°C For example: Register value = 500 (dec) = 82°C	130A	0	[9:0]	RO

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
Junction Max. Temperature Threshold for Ports Disconnect	Junction maximum temperature for ports operation. Above this value ports are disconnected to protect IC from temperature damage. For example: Register DFLT Value = 184 (hex) = 155°C	130C	184	[9:0]	R/W
Junction Max. Temperature Threshold for Alarm	Junction maximum temperature for activating temperature alarm. Above this value temperature alarm is activated to protect IC (see address 1314 bit 5). For example: Register DFLT Value = 184 (hex) = 155°C	130E	184	[9:0]	R/W
Junction Max. Temperature Capture	Junction maximum temperature captured and latched. This register is reset on power up or reset	1312	3FF	[9:0]	RO
General System Errors Flags register	Bit 0 = V_{main} is over the upper threshold Bit 1 = Temperature is over threshold Bit 2 = Disable ports pin is active Bit 3 = V_{main} is under AF low threshold Bit 4 = V_{main} is under AT low threshold Bit 5 = Temperature is over alarm threshold	1314	0	[5:0]	RO

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
Port Configuration register Port 0 = 131A . . . Port 11 = 1330	Bits [1:0] = Port Enable Status • 00: Port Disabled • 01: Port Enabled (DFLT) • 10: Force Power • 11: Reserved Bits [3:2] = Port Pair Control 00: Reserved • 01: Alternative A (DFLT) • 10: Alternative B (Back-off Enable) • 11: Reserved Bits [5:4] = Port Type Definition • 00: AF mode enable • 01: AT mode enable (DFLT) • 10: Reserved • 11: Reserved Bits [7:6] = Port Priority Level • 00: Critical – Highest Priority (DFLT) • 01: High • 10: Low • 11: Reserved	131A .. 1330	21 (dec)	[7:0]	R/W
Port Enable / Disable register	Bit Per Port: External disable port command Bit 0 = Port 0 … Bit 11 = Port 11 • 0: Port enabled • 1: Port disabled	1332	0	[11:0]	R/W

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
Port Power Allocation Limit register Port 0 = 1334 . . . Port 11 = 134A	Port Power Allocation Limit (PPL) for Power Management Mechanism. These registers' values are set automatically (write) by the Power Management Mechanism, according to a predefined algorithm. This algorithm monitors and distributes power for each port based on system power budget, port priority, port status, and port class. When power budget is limited, a port that exceeds this power level is disconnected due to power management. In Auto mode, content of these registers is set periodically by master (every ~20ms). Therefore it is not practical to set (write) a different value by an external CPU. LSB = 0.1W Default Value = 140 (hex) = 320 (dec) = 32W	1334 .. 134A	140	[15:0]	R/W
Port Power Allocation Limit register For Layer 2 Support Port 0 = 134C . . . Port 11 = 1362	Port Power Allocation Limit Register for Layer 2 Classification Support (TPPL). These registers can be used for setting (writing) by an external CPU (Host), to set port power allocation for Power Management Mechanism. When these registers are manually set by an external CPU/Host (usually after port is powered up), Power Management will use its value for Port Power control. When power budget is limited, a port that exceeds this power level might be disconnected due to power management LSB = 0.1W Default Value = 0W	134C .. 1362	0	[15:0]	R/W
Port Indication Clear	Port number to be cleared using an indications clear sync event 0000 = Port 0 is selected to clear 0001 = Port 1 is selected … 1011 = Port 11 is selected	1364	0	[3:0]	R/W

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
Total System Power Budget for Emergency Bank 0	System power budget for state 000 of Power Good lines LSB = 0.1W Default = 36W x 96 = 3456W	138C	8700	[15:0]	R/W
Total System Power Budget for Emergency Bank 1	System power budget for state 001 of Power Good lines LSB = 0.1W Default: 36W x 12 = 432W	138E	10E0	[15:0]	R/W
Total System Power Budget for Emergency Bank 2	System power budget for state 010 of Power Good lines LSB = 0.1W Default: 36W x 8 = 300W	1390	BB8	[15:0]	R/W
Total System Power Budget for Emergency Bank 3	System power budget for state 011 of Power Good lines LSB = 0.1W Default: 36W x 6 = 220W	1392	898	[15:0]	R/W
Total System Power Budget for Emergency Bank 4	System power budget for state 100 of Power Good lines LSB = 0.1W Default: 200W	1394	7D0	[15:0]	R/W
Total System Power Budget for Emergency Bank 5	System power budget for state 101 of Power Good lines LSB = 0.1W Default: 150W	1396	5DC	[15:0]	R/W
Total System Power Budget for Emergency Bank 6	System power budget for state 110 of Power Good lines LSB = 0.1W Default: 15.4W x 8 = 120W	1398	4B0	[15:0]	R/W
Total System Power Budget for Emergency Bank 7	System power budget for state 111 of Power Good lines LSB = 0.1W Default: 15.4W x 6 = 100W	139A	3E8	[15:0]	R/W

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
Monitoring Power Good Input Pins (0:2)	Read Power Good Input Pins Logic State (PG0 to PG2) This register monitors IC Active Power Budget (Real-Time State), from Budget 0 to 7 (see Master Configuration for SysPowerBudget0…7 Register) Bit 0 = PG0 Bit 1 = PG1 Bit 2 = PG2 "1" = Power Good Active "0" = Power Good Not Active	300	0	[2:0]	RO
Updated Power Management Parameters	Parameters update request and indication • 0: Parameters were updated • 1: Waiting for parameters update	139C	0	[0]	R/W
General User register	General user define byte: This register is used for detecting reset events by Host or by local CPU. User can program (write) into this register any value (different than 0). Upon Reset Event: This register returns to its DFLT value (0)	13A0	0	[7:0]	R/W
Interrupt Mask register	Interrupt Mask register. Bit Per Event, Indicating an event was captured at one (or more) ports. 0 = Event is masked (disabled) 1 = Event is enabled To trace the specific port location in which the event was traced, go to address 13A6 Bit 0 = port turned on Bit 1 = port turned off Bit 2 = detection failed Bit 3 = OVL or SC Bit 4 = Under-load Detected Bit 5 = OVL or SC during startup or dv/dt fail Bit 6 = port turned off due to PM Bit 7 = port power denied at startup Bit 8 = over temp. Bit 9 = temp. alarm Bit 10 = V_{main} low AF Bit 11 = V_{main} low AT Bit 12 = V_{main} high Bit 13 = Reserved	13A4	0	[13:0]	R/W

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
Interrupt Port Location register	Bit per port indication of the port that had an Interrupt Out event 0 = Event was **not** captured 1 = Event was captured in this port Bit 0 = Port 0 … Bit 11 = Port 11	13A6	0	[11:0]	RO

10. Opening a Configuration Register for Write Operation

To protect the PoE system from incorrect configuration sequencing, some of PD69012 Configuration Registers (from address 0x1000 to 0x1314) are locked.

If you want to unlock these locked mechanisms, use the following sequence.

Note: Set PoE system configuration registers such as AT/AF Mode, Res. Detection / Legacy Detection Mode, I CUT Currents Levels, and others, only when system is initializing and ports are **OFF**.

To Unlock Mechanisms:

1. Disable all ports (via Disable pin or via Disable Port register).
2. Change mode to CONFIG mode (see instructions below).
3. Perform all necessary changes (Registers Set).
4. Return to normal operational Auto mode.
5. Enable PoE ports power.

To Enter CONFIG Mode:

1. DisPortsCmd reg (address 0x1332) ➔ Write Data = 0x03FF

or disable each port in Portx_CR register (address 0x131A to 0x1330) bits [1:0] ➔ Write Data = 00

2. Change mode:

   a. SW_ConfigReg (address 0x139E) ➔ Write Data = 0xDC03

   a. I2C_ExtSyncType (address 0x1318) ➔ Write Data = 0x0020 (Mode Event Sync)

   b. EXT_EV_IRQ (address 0x1144) ➔ Write Data = 0x0020 (Mode Event IRQ Sync)

   c. To ensure that this command was properly performed, users may read SW_ConfigReg register (go to address 0x139E) ➔ Expected Read Data = 0x0003

3. Note that at this point RAM space (from address 0x1000 to the end) is open for Write operations. In this mode users can make changes to relevant registers

4. Upon write operation completion it is recommended to return to operational Auto mode:

   a. SW_ConfigReg (address 0x139E) ➔ Write Data = 0xDC00

   b. I2C_ExtSyncType (address 0x1318) ➔ Write Data = 0x0020

   c. EXT_EV_IRQ (address 0x1144) ➔ Write Data = 0x0020

   d. To ensure this command was performed properly, read SW_ConfigReg register (address 0x139E) ➔ Expected Data = 0x0000

5. Re-enable all PoE ports:

   DisPortsCmd reg (address 0x1332) ➔ Write Data = 0x0000, or enable each port in Portx_CR register (address 0x131A to 0x1330) bits [1:0] ➔ Write Data = 01

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Appendix A:

This appendix describes the flowchart implemented in Host to remove power from low priority port. This way high priority ports that were connected will be powered when power budget exceeds its max level.

The principal of the flowchart is as follows:

As a routine, the host checks if new ports with higher priority have been connected. If so, and existing power budget cannot support the new connected ports; the host increases the budget in 32 Watts.

Following, the new higher priority single port is powered. Then the host decreases the budget back to its original value, causing the lowest priority port to turn off.

For each high priority port that needs to be powered, the complete flowchart should be implemented once.

Important!

Power-supply must be able to provide extra 32 Watts above its maximum noted spec for time duration of 2 sec.

Register Name	Register Description	Address (HEX)	Default Value	Register Width (BITS)	Read/ Write
Updated Power Management Parameters	Parameters update request and indication • 0: Parameters were updated • 1: Waiting for parameters update	139C	0	[0]	R/W
SysTotalDeltaPower	The power held by the system (Available power). LSB = 0.1W	12E6	0	[15:0]	
SysTotalHighCons	Calculated system power consumption of high priority ports. LSB = 0.1W	12D8	0	[15:0]	
SysTotalLowCons	Calculated system power consumption of low priority ports. LSB = 0.1W	12DA	0	[15:0]	
SysTotalCriticalReq	Total system power request for critical priority ports. LSB = 0.1W	12DC	0	[15:0]	
SysTotalHighReq	Total system power request for high priority ports. LSB = 0.1W	12DE	0	[15:0]	

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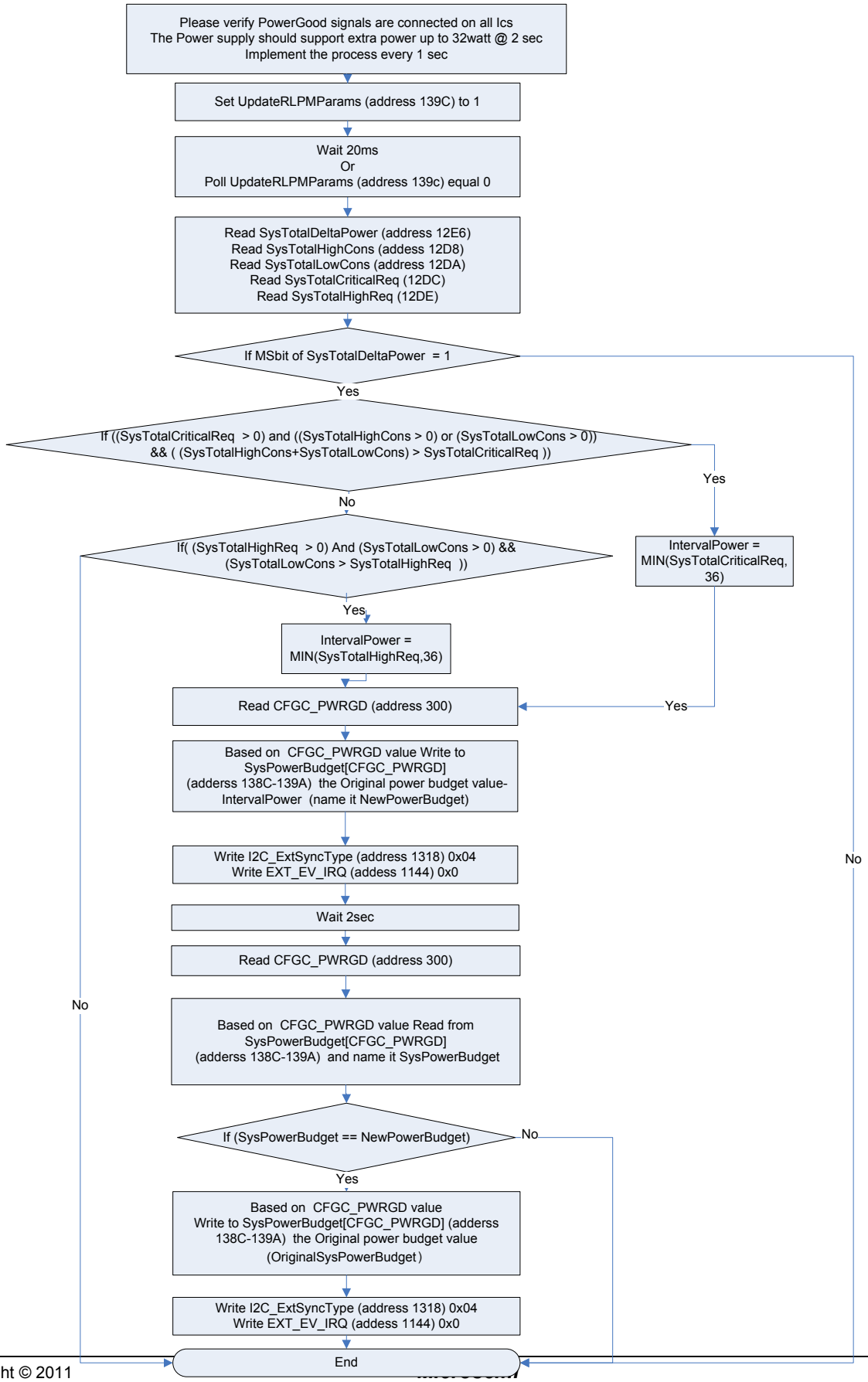

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References code how to implement the flowchart:

```
protected System.Threading.Timer timerIgnoreHighPriority; // Tick every 1 second (call
IgnoreHighPriority function)
int byIgnorePriorityStep = 0;
ushort wOriginalSysPowerBudget_dW = 0;
ushort MAX_POWER_PER_PORT_dW = 360;

private void IgnoreHighPriority(object[] objArgsArr)
{

   byte[] byaRxData = new byte[16];
   byte byActivePowerBank;
   short wSysTotalHighCons_dW;
   ushort wSysTotalLowCons_dW;
   ushort wSysTotalCriticalReq_dW;
   ushort wSysTotalHighReq_dW;
   ushort wSysTotalDeltaPower_Reg;
   bool bSysTotalDeltaPower_PositiveSign;
   ushort wHighestPriorityRequest_dW = 0;
   ushort wSysTotalCalcPowerCons_dW;
   ushort wPowerAvilableForStartup_dW = 0;
   short wRequestPowerForStartup_dW = 0;
   ushort wMinimumPowerToReduce_dW;
   ushort wPowerToReduce_dW;
   ushort wNewPowerBudget_dW = 0;

   switch (byIgnorePriorityStep)
   {
     case -1:
     {
        byIgnorePriorityStep = 0;
        break;
     }
     case 0:
     {
        /* sync command */
        SendWriteRegisterCommand("UpdateRLPMParams", chipData[0].Address,
                                 (int)PD690xxRegistersAddress.PM_MASTER_CFG.UpdateRLPMParams, 1,
                                 false);

        Thread.Sleep(20);

        //read registers
        int NumberOFBytesToRead = 16;
        poEPD690xxAutoModeEndPoint.SendReadCommand(ref tMsg, "GetPM_parameters",
                                chipData[0].Address, (int)
                                PD690xxRegistersAddress.PM_MASTER.SysTotalHighCons,
                                NumberOFBytesToRead, false);

        //extract registers data
        wSysTotalHighCons_dW = (ushort)AccessoriesPD690xx.extractData(tMsg.RxDataArr[0],
                                tMsg.RxDataArr[1]);
        wSysTotalLowCons_dW = (ushort)AccessoriesPD690xx.extractData(tMsg.RxDataArr[2],
                                tMsg.RxDataArr[3]);
        wSysTotalCriticalReq_dW = (ushort)AccessoriesPD690xx.extractData(tMsg.RxDataArr[4],
                                  tMsg.RxDataArr[5]);
         wSysTotalHighReq_dW = (ushort)AccessoriesPD690xx.extractData(tMsg.RxDataArr[6],
                                tMsg.RxDataArr[7]);
```

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```
wSysTotalCalcPowerCons_dW = (ushort)AccessoriesPD690xx.extractData(tMsg.RxDataArr[10],
                            tMsg.RxDataArr[11]);
wSysTotalDeltaPower_Reg = (ushort)AccessoriesPD690xx.extractData(tMsg.RxDataArr[14],
                            tMsg.RxDataArr[15]);


/*check whether register SysTotalDeltaPower is negative or positive(the MSb is a sign bit)*/
bSysTotalDeltaPower_PositiveSign = ((wSysTotalDeltaPower_Reg & 0x8000) == 0) ? true : false;

if (bSysTotalDeltaPower_PositiveSign)
     return;

if ((wSysTotalCriticalReq_dW > 0)&&((wSysTotalHighCons_dW > 0)||(wSysTotalLowCons_dW > 0)))
    wHighestPriorityRequest_dW = (ushort)Math.Min(wSysTotalCriticalReq_dW,
                                    wSysTotalHighCons_dW + wSysTotalLowCons_dW);
else if ((wSysTotalHighReq_dW > 0) && (wSysTotalLowCons_dW > 0))
    wHighestPriorityRequest_dW = Math.Min(wSysTotalHighReq_dW, wSysTotalLowCons_dW);
else
    return;

 // get selected active budget
 GetSelectedBank(0);
 byActivePowerBank = (byte)chipData[0].IcRegisters.CFGC.CFGC_PWRGD;


 /* Get selected active bank power budget and save it in usOriginalSysPowerBudget varible */
 wOriginalSysPowerBudget_dW = SendReadRegisterCommand("GetSysTotalActivePowerBudget",
                              chipData[0].Address, (int)
                              PD690xxRegistersAddress.PM_MASTER_CFG.SysPowerBudget0 + (2 *
                              byActivePowerBank), false);

 wPowerAvilableForStartup_dW = (ushort)(wOriginalSysPowerBudget_dW -
                              wSysTotalCalcPowerCons_dW);

 if (wPowerAvilableForStartup_dW >= MAX_POWER_PER_PORT_dW)
     return;

 wRequestPowerForStartup_dW = Math.Min(wHighestPriorityRequest_dW, MAX_POWER_PER_PORT_dW);

 if (wRequestPowerForStartup_dW < wPowerAvilableForStartup_dW)
     return;

 wMinimumPowerToReduce_dW = (ushort)(wSysTotalCalcPowerCons_dW * 0.125);

 wPowerToReduce_dW = Math.Max(wRequestPowerForStartup_dW, wMinimumPowerToReduce_dW);

 /* decrement wIntervalPower_dW from the selected active bank power budget and save it in
     usNewPowerBudget varible */
 wNewPowerBudget_dW = (ushort)(wSysTotalCalcPowerCons_dW - wPowerToReduce_dW);

 /* write the usNewPowerBudget to the selected active bank power */
 SendWriteRegisterCommand("SetSingleBankPowerBudget",
                          Globals_PD690xx_AutoMode.BROADCAST_I2C_ADDRESS, (int)
                          PD690xxRegistersAddress.PM_MASTER_CFG.SysPowerBudget0 + (2 *
                          byActivePowerBank), wNewPowerBudget_dW, false);

 // sync commands
 SendWriteRegisterCommand("I2C_ExtSyncType", Globals_PD690xx_AutoMode.BROADCAST_I2C_ADDRESS,
                          (int) PD690xxRegistersAddress.I2C_EXT_SYNC.I2C_ExtSyncType, 4,
                          false);
```

```
            SendWriteRegisterCommand("EXT_EV_IRQ", Globals_PD690xx_AutoMode.BROADCAST_I2C_ADDRESS,
                                     (int) PD690xxRegistersAddress.GNRL_RAM.EXT_EV_IRQ, 4, false);

            byIgnorePriorityStep = 1;
            /* remain power low for one second */

            break;
        }
        case 1:
        {
           // get selected active budget
           GetSelectedBank(0);
           byActivePowerBank =(byte) chipData[0].IcRegisters.CFGC.CFGC_PWRGD;


           // write the Original power budget to the selected active bank power
           SendWriteRegisterCommand("SetSingleBankPowerBudget",
                                    Globals_PD690xx_AutoMode.BROADCAST_I2C_ADDRESS,
                                    (int)PD690xxRegistersAddress.PM_MASTER_CFG.SysPowerBudget0 + (2 *
                                    byActivePowerBank), wOriginalSysPowerBudget_dW, false);

            // sync commands
            SendWriteRegisterCommand("I2C_ExtSyncType", Globals_PD690xx_AutoMode.BROADCAST_I2C_ADDRESS,
                                    (int)PD690xxRegistersAddress.I2C_EXT_SYNC.I2C_ExtSyncType, 4,
                                    false);
            SendWriteRegisterCommand("EXT_EV_IRQ", Globals_PD690xx_AutoMode.BROADCAST_I2C_ADDRESS,
                                    (int)PD690xxRegistersAddress.GNRL_RAM.EXT_EV_IRQ, 4, false);

            byIgnorePriorityStep = -1;
            break;
         }
      }
   }
```

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Revision History

Revision Level / Date	Para. Affected	Description
1.0 / 30-Aug-10	-	Initial Release – First Release for PD69xx
1.2 / 21-Apr-11		Wording and Proofing
1.3 / 9-Aug-11		Wording and Proofing

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