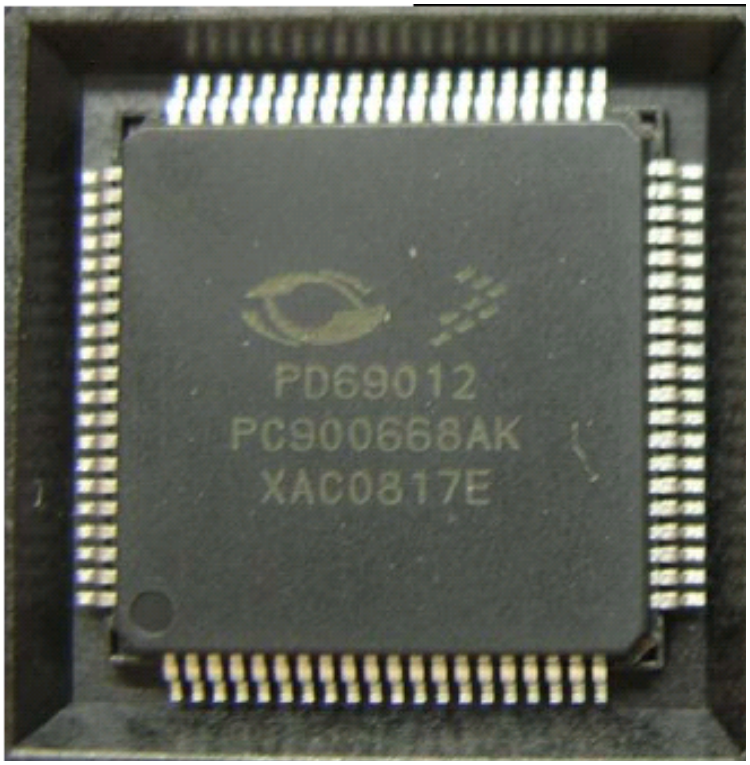
Preliminary

PD69012

12 Ports AF/AT PoE Device Qualification Report



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1. Introduction

This document provides a detailed technical report of the PD69012 qualification results. The qualification tests were performed by the chip manufacturer (FreeScale), based on the JEDEC Standard 47B for Stress-Test-Driven qualification of Integrated circuits.

1.1 Reference Documents

1. JESD22, Reliability Test Methods for Packaged Devices (main qualification reference)
2. MIL-STD-883, Test Methods and Procedures for Microelectronics
3. UL94, Tests for Flammability of Plastic Materials for Parts in Devices and Appliances
4. ASTM D2863, Flammability of Plastic Using the Oxygen Index Method
5. IEC Publication 695, Fire Hazard Testing
6. JESD34, Failure-Mechanism-Driven Reliability Qualification of Silicon Devices
7. JESD46, Guidelines for User Notification of Product/process Changes by Semiconductor Suppliers

2. Product Information

Product Information	
Microsemi Part Number	PD69012
Supplier Name	Freescale Semiconductor, Tx. USA
Package & Assembly Code	TQFP_EP
Final Quality Control Facility	ASECL & A6 (BAT3)
Package Type	TQFP_EP
Lead Count	80
Flammability Ratings	UL94V0
MSL level	MSL3, 260^{0}C peak

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3. IC Design and Manufacturing Flow Chart

IC High Level Flowchart		
Process	**Location**	**City, State or Country**
Architecture & Specifications	Microsemi	Israel
Digital Design	Microsemi	Israel
Analog Cells Design	APD Design Center	Toulouse France
Integrations & Verifications	APD Design Center	Toulouse France
Wafer Fab	MOS12	Chandler Arizona USA
Probe Test	MOS12	Chandler Arizona USA
Assembly	BAT3	Tianjin China
Final Test	BAT3	Tianjin China
Tape & Reel	N/A	Tianjin China
Final Inspection	BAT3	Tianjin China
Any Subcontractor Process	None	--
Product Distribution Center	Tianjin	Tianjin China
Customer Ship-to Locations	Microsemi	Israel

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4. Qualification Tests Results

Qualification Procedure & Tests Results					
Item	**Stress Name**	**Abbreviation**	**Description / Conditions**	**Tests Results Fail / Sample**	**Pass / Fail Remarks**
1.	Pre stress & Post stress electrical	TST	Full functional test as per Microsemi's PoE specification. before and after each stress tests. Room temperature	All tested parts - 150 parts from 2 x LOTS	PASS
2.	High temperature Operating Life	HTOL	+150 ^{0}C, Junction/ 600 hrs Vmain = max. Repeat TST @ room temperature	1 / 154 (77 parts of 2 lots)	PASS 1 Part Failure "8D" Analysis - done (report is available)
3.	Early Life Fail Rate	ELFR	+ 150 ^{0}C, Junction /26 hrs	0 / 154 (77 parts of 2 lots)	PASS
4.	Electrical characterization	ED	Functional tests @ room temperature	0 / 60 (30 parts of 2 lots)	PASS
5.	Electrostatic Discharge ESD – HBM	ESD	HBM – 500v, 1000v, 1500v and 2000v (Class 2) MM – not specified CDM – not specified	0 / 45 (15 parts of 2 lots)	PASS
6.	Latch-Up	LU	Test at room temperature and at +85 ^{0}C All pins stressed @ 200mA	0 / 6 (6 parts of 1 lot)	
7.	Temperature Humidity Bias (Highly Accelerated Temperature & Humidity Stress)	HAST	+130 ^{0}C / 85 % RH / 96 hrs Vmain = min. / I load = min. Repeat TST @ room temperature	0 / 154 (77 parts of 2 lots)	PASS
8.	Temperature Cycling / Thermal Shocks	TC	-65 to +150 ^{0}C / air-to air 10 cycles + 100 cycles Repeat TST @ room temperature	0 / 16 (16 parts of 1 lot)	PASS (system tests)
9.	Autoclave (pressure)	AC	121 ^{0}C / 15 PSIG / 96 hrs Repeat TST @ room temperature	0 / 154 (77 parts of 2 lots)	PASS
10.	High Temperature Hours Bake	HTB	+150 ^{0}C / 504 hrs Vmain = max. Repeat TST @ room temperature	0 / 154 (77 parts of 2 lots)	PASS
11.	Physical Dimension	PD	See attached report	- / 30 (30 parts of 1 lot)	PASS
12.	Bond Pull Strength	BPS	As per MIL-STD-883-2011	- / 5 (5 parts of 1 lot)	PASS
13.	Bond Shear	BS	As per JESD47-JB116	- / 5 (5 parts of 1 lot)	PASS
14.	Solderability	SD	As per JESD47-JB102	- / 15	PASS

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Qualification Procedure & Tests Results					
Item	**Stress Name**	**Abbreviation**	**Description / Conditions**	**Tests Results Fail / Sample**	**Pass / Fail Remarks**
				(5 parts of 3 lots)	(system tests)
15.	Package Temperature Humidity Bias (85/85)	THB	+150 ^{0}C / 85 % / 504 hrs Vmain = min. / I load = min. Repeat TST @ room temperature	0 / 154 (77 parts of 2 lots)	PASS (system tests)
16.	Preconditioning	PC	Before THB, HALT, TC & AC @ 245 ^{0}C Repeat TST @ room temperature	All parts for HALT, TC & AC tests	PASS (system tests)
17.	Power Temperature Cycling	PTC	-40 to +125 ^{0}C / 1000 cycles + Repeat TST @ room temperature	0 / 16 (16 parts of 1 lot)	PASS (system tests)
18.	Package & Mechanical Shocks	MS	5 pulses @ Y plane @ 0.5mS 1500 G peak Repeat TST @ room temperature	0 / 16 (16 parts of 1 lot)	PASS (system tests)
19.	Package & Vibration Variation Freq.	VVF	20Hz to 2 KHz, in > 4 min. x4 times in each orientation 50 G peak Repeat TST @ room temperature	0 / 16 (16 parts of 1 lot)	PASS (system tests)
20.	Constant Acceleration	CA	4 times @ Y plane @ 20 kg Repeat TST @ room temperature	0 / 16 (16 parts of 1 lot)	TBD (system tests)
21.	Visual Inspections	EV	Visual test before and after any mechanical shock test	0 / 16 (16 parts of 1 lot)	PASS (system tests)
22.	Gross / Fine Leak	FL	Electrical test before and after any mechanical shock test	0 / 16 (16 parts of 1 lot)	PASS (system tests)
23.	Low Temperature Operating Life	LTOL	30 ^{0}C / 240 hrs Vmain = max. Repeat TST @ room temperature	0 / 77 (77 parts of 1 lot)	PASS (system tests)
24.	Design Marginality Tests	N/A	Application level (system) tests done over Spec. level to confirm design margins	0 / 16 (16 parts of 1 lot)	PASS (system tests)
25.	Destructive Tests	N/A	Application level (system) tests – Over Spec. Parameters levels until system is damaged to confirm design margins	16 parts of 1 lot	PASS (see system tests detailed report)

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5. Package Mechanical & Physical Dimensions

Vital package dimensions compared to the manufacturer drawings and or to case outline.

Criteria: Refer to specific case outline drawing
Sample size: 30 units/lot.

Select units randomly between at least three strips within each lot.

Requirement: Record actual measurement and NOT Pass/Fail results.
Specify unit being tested.
Calculate average, standard deviation and Cpk.

TBD here by Feb 10

For detailed view – refer to the detailed mechanical drawing specified in the PD69012 Data Sheet, Cat. No. 06-0072-058.

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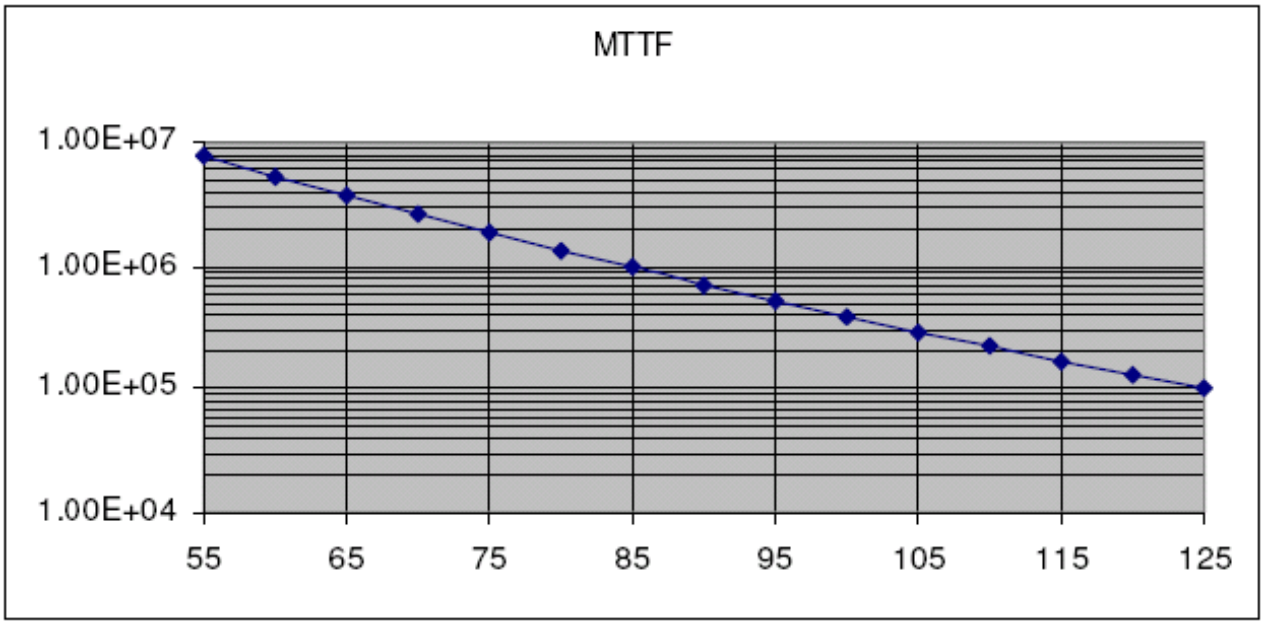
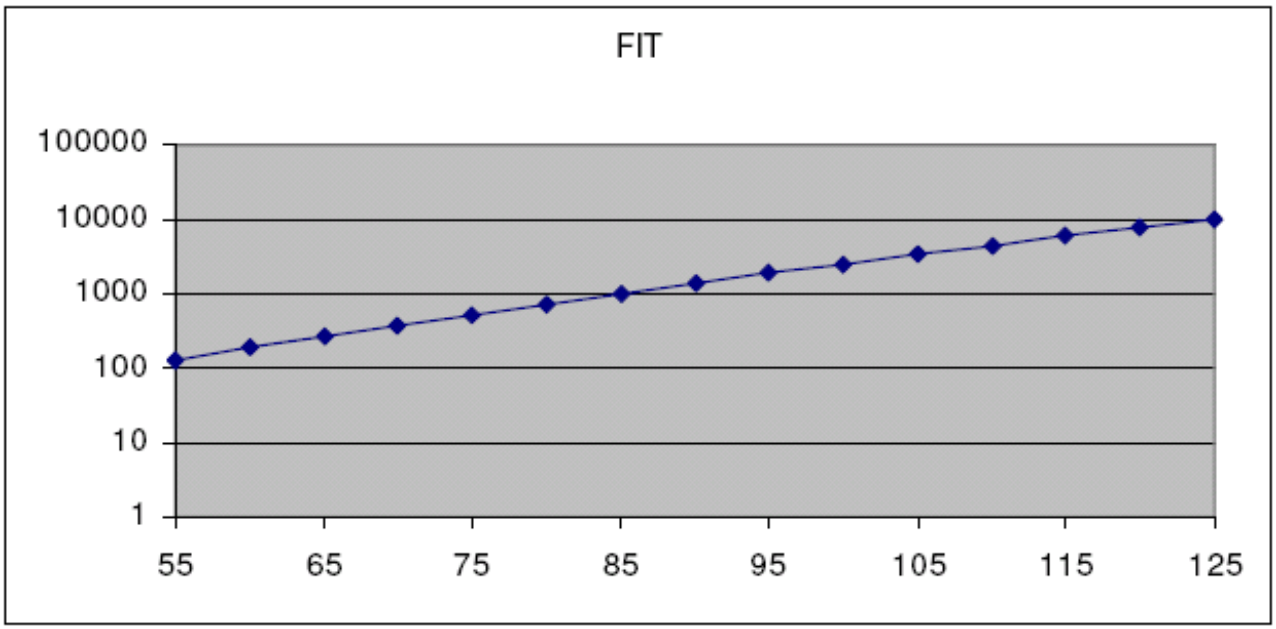
6. MTTF vs. Junction Temperature @ 60% C.L. , Vmain = 57v



7. FIT Rate vs. Junction Temperature @ 60% C.L. , Vmain = 57v (after 1000 hours)



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8. DECLARATION

I hereby affirm that the samples represented by this qualification report are representative of Microsemi parts and have been made to the applicable specifications.

This is to declare that part number "PD69012" (also referenced as "ROTEM" V2R1) is fully qualified as per Microsemi qualification procedure, listed in this report.

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Signature

Date December 20, 2008

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Revision History

Revision Level / Date	Para. Affected/page	Description
Ver 1.0, 07 January, 2009		Initial release
Ver 1.1, 25 May, 2009		Mechanical qual results added.

For support contact: sales_AMSG@microsemi.com

Visit our web site at: www.microsemi.com **Cat. No. 06-0108-085**