Power over Ethernet

PD640xx & PD690xx

Auto Mode Registers Map

PRELIMINARY RELEASE

Rev 1.4

Black Text – PD640xx

Blue Text – PD690xx

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Introduction

This Register Mapping Matrix comprises the internal Registers description for both PD640xx and **PD690xx** PoE devices.

The document is presented as a comparison table between the PD640xx and the new PD690xx, easing the migration between those PoE products and facilitate the communication development with the devices.

Registers related to the New PoE Generation PD690xx are marked in BLUE.

For a detailed list of the PD690xx Registers, refer to Appendix A.

General Note:

The PD690xx communication protocol is based on dual byte format (16 bit data), as illustrated in Section 2 below.

Each Read or Write transaction is framed in a Dual Byte Packet. 8 bits registers or less are read and write pairs (two registers in a single packet). When calling a single 16 bit register, or dual 8 bit registers, the user (Host) should use a single "even" address, as specified in this document. There is no need to perform dual read/write transactions.

Note that writing/reading from "odd" address will not be executed.

Example 1:

To read the Port 1 Icut 8 bit register, the user should access both Port 0 and Port 1 simultaneously, through address “1000”. Note that the register in address "1001" is **NOT** accessible directly, but only through Address “1000”.

Example 2:

To write into the “System Power Budget 0” register, the user should access “138C” address via the 16 bit wide register. The register in address “138D” is not accessible directly.

If the user attempts to read or write from the “138D” address, data transfer will be corrupted and might damage the IC configuration.

Addresses marked in brackets “(…)” are not accessible directly!

General Configuration Instructions Note:

To protect the PoE system from incorrect configuration sequencing, the PD69012 has a dedicated software protection mechanism ensuring that sensitive configuration registers are modified only when PoE ports are OFF.

This mechanism also ensures that the PoE system is initialized properly after modifying those registers.

It is highly recommended that PoE system configuration registers, such as AT / AF mode, Res Detection / Legacy Detection Mode, I CUT currents levels etc. are set only when the system is initializing and ports are OFF. The recommended sequence is as follow:

1. Disable all ports (via the Disable pin or via the Disable Port Register)
2. Change mode to config mode (see instructions below)
3. Perform all the necessary changes (Registers Set)
4. Return to normal operational Auto mode
5. Enable PoE ports power

To enter the CONFIG mode, do the following:

1. DisPortsCmd reg (addr 0x1332) ➔ Data = 0x03FF

   or disable each port in the Portx_CR register (addr 0x131A to 0x1330) bits [1:0] ➔ Data = 00

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2. Change mode:
   - SW_ConfigReg (addr 0x139E) ➔ Data = 0xDC03
   - I2C_ExtSyncType (addr 0x1318) ➔ Data = 0x0020 (Mode Event Sync)
   - EXT_EV_IRQ (addr 0x1144) ➔ Data = 0x0020 (Mode Event IRQ Sync)
   - To ensure that this command was properly performed, the user may read the SW_ConfigReg register (go to addr 0x139E) ➔ Expected Read Data = 0x0003

3. Please note that at this point, the RAM space (from addr 0x1000 to the end) is open for Write operations. In this mode the user can make changes to relevant registers.

4. After completing the write operation, return to the operational Auto mode:
   - SW_ConfigReg (addr 0x139E) ➔ Data = 0xDC00
   - I2C_ExtSyncType (addr 0x1318) ➔ Data = 0x0020
   - EXT_EV_IRQ (addr 0x1144) ➔ Data = 0x0020

To ensure that this command was performed properly, the user can read the SW_ConfigReg register:

(addr 0x139E) ➔ Expected Data = 0x0000

5. Enable all PoE ports:
   - DisPortsCmd reg (addr 0x1332) ➔ Data = 0x0000, or enable each port in the Portx_CR register (addr 0x131A to 0x1330) bits [1:0] ➔ Data = 01

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I²C Protocol Structure with Host

Figure 1 illustrates the sequence structure for write cycles. Each packet ends with an Ack bit, sent from the PoE system.

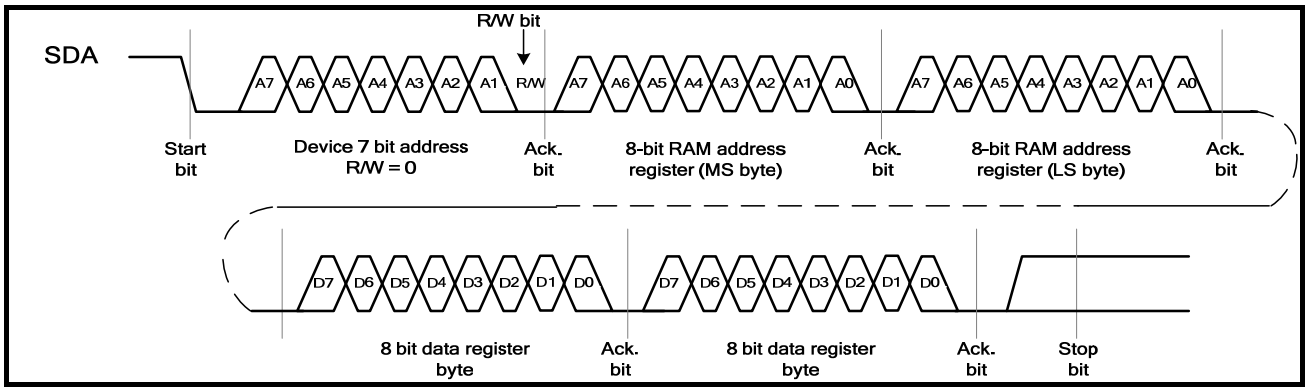

Figure 1: Sequence Structure for Write Cycles

Sequence structure for read cycles (see Figure 2**)**: The second start bit indicates that a read cycle follows. The Acknowledge bits are all issued by the PoE system, except for those issued by the Host as part of the reply from the PoE Device. The Host provides a stop bit.

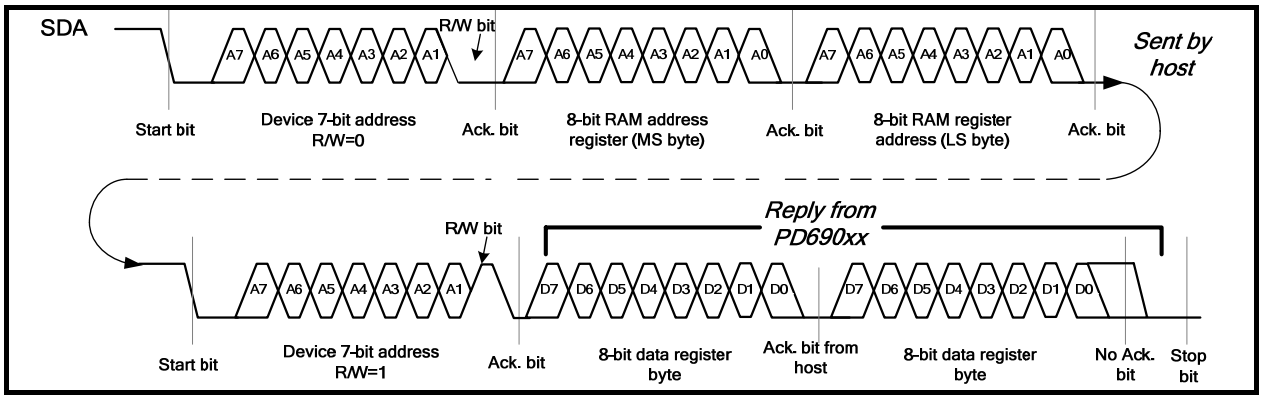

Figure 2: Sequence Structure for Read Cycles

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System Initialization Registers

Register Name	Register Description	Address (HEX)	Default Value	Register Width (BITS)	Read/ Write
Timer Value for Overload Conditions					
tovld_reg	Formula: • 1 bit = 2.048 mSec, Range: 0 to 64 = 0 to 131.072 mSec *Example:* *For 100 mS* *100 / 2.048 = 49 (decimal)*	008C	6'd32 (65mS)	6	R/W
Tovld_AF	Formula: • 1 LSB bit = 125 uSec. • Range: 0 to 522 mSec *Example:* *For 10mS* *10 / .125 = 80 (decimal)*	100E	208H (65 ms)	16	R/W
Tovld_AT		1010	208H (65 ms)	16	R/W
Maximum Vmain Voltage Level Threshold (Before Powering Off All Ports)					
vmain_high_th_reg	Formula: • 1 bit = 58 mV, Range: 0 to 1023 = 0 to 59.392 V *Example:* *For 56v max* *56V / 58 mV = 966 (decimal)*	00BB	10'd999 (58v)	10	R/W
VmainHighTh	Formula: • 1 bit = 61 mV, Range: 0 to 1023 = 0 to 59.392V *Example:* *For 50v max* *50V / 61 mV = 820 (decimal)*	12FE	10'h3bc	10	R/W
Minimum Vmain Voltage Level Threshold (Before Powering Off All Ports)					
vmain_low_th_reg	Formula: • 1 bit = 58mV, Range: 0 to 1023 = 0 to 59.392 V *Example:* *For 45v min* *45V / 58mV = 776 (decimal)*	00BC	10'd741 (43v)	10	R/W

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Register Name	Register Description	Address (HEX)	Default Value	Register Width (BITS)	Read/ Write
VmainATLowTh	Formula: • 1 bit = 61 mV, Range: 0 to 1023 = 0 to 59.392 V *Example:* *For 45v min* *45V / 61 mV = 738 (decimal)* *(Hysteresis of Vmain Thresholds = 1v)*	1300	10'h313	10	R/W
VmainAFLowTh		1302	10'h2b0	10	R/W
Power Budget Guard Band Value for the Master PoE Device					
pmng_guard_band_reg	If System Total Power Consumption is higher than (*sys_avlb_pwr_bdgt_reg-pmng_guard_band_reg*), it means that the power consumption is WITHIN the guard band zone. In this zone, no additional ports will be connected. This guard band zone protects the main power supply from Over-Power consumption Formula: • 1LSB = 36.34 mW *Example:* *For 20 watt = 550 (decimal)*	0106	16'd550 (20 watt)	16	R/W
N/A – Irrelevant	PD69012 has a Dynamic Guard Band instead of a Static Guard Band See PD690xx Technical Note TN-144 for Auto Mode Power Management's mechanism description.	N/A	N/A	N/A	N/A
Total Power Budget - Sets the Maximum Power Level , Available for All Ports (System)					
sys_avlb_pwr_bdgt_reg	**This value is relevant for the Master PoE Device only!** Formula: • 1 bit = 36.34 mW, Range: 0 to 65536 = 0 to 2380 W *Example:* *For 750 watt* *750 / 36.34 = 20638 decimal*	0107	16'd22026 800 watt	16	R/W

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Register Name	Register Description	Address (HEX)	Default Value	Register Width (BITS)	Read/ Write
Master Configuration for SysPowerBudget0 …7	Master IC Configuration for System power budget Supports up to eight power banks levels. Power budgets 000 to 111 (according to power good I/Os) 1 Bit LSB = 0.1 W	138C 138E 1390 1392 1394 1396 1398 139A	8700 (3456w) 10E0 (432w) BB8 (300w) 898 (220w) 7D0 (200w) 5DC (150w) 4B0 (120w) 3E8 (100w)	16	R/W
Power Management Mode					
ltp_alloc_mode_reg	Formula: • FFF = Enabled; power management in accordance with power allocation level (Dynamic Mode; see registers 0X11F to 0X12A) • 000 = Disabled; port power allocation is ignored	0110	12'h000	12	R/W
ltp_class_mode_reg	**Bit per port - LSB is port #0.** Formula: • "1" = power calculation is based on class level • "0" = port power and port class are ignored. Local power calculation is based on power allocation register (manual write command)	0111	12'h000	12	R/W
ltp_auto_mode_reg	**- Bit per port - LSB is port #0.** Formula: • "1" = Auto mode enabled; port total power calculation is based on Auto mode (class & consumption) • "0" = Manual mode; port total power calculation is based on power allocation register (pre-defined)	0112	12'hFFF	12	R/W

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Register Name	Register Description	Address (HEX)	Default Value	Register Width (BITS)	Read/ Write
PM mode – sys Flag	Set Power Management calculation method for the IC: • "0": Static Mode; according to Class or Port Power Allocation Level (PPL) ➔ PPL is set through Address Registers 1334 to 134A • "1": Dynamic Mode; according to actual (real time) power consumption	1160 Bit [6]	0 = Static	1	R/W
General User Registers					
General User Register	General User Register for user Use	0318	16'h0000	16	R/W
Legacy CAP Detection	Legacy CAP Detection Enable Register BIT[2] • "1" = Cap Detection disabled • "0" = Cap detection enabled	1160 Bit[2]	1= Disabled	16	R/W
Software Configuration Register	Software Configuration & Change Mode Protection Register **Bits [2:0] = SW Configuration Key** • 000: stand alone master \ slave • 001: macro mode slave • 010: manual mode • 011: config mode **Bits [7:3] = Spare = Not Used** **Bits [15:8] = Special Change Mode Key** Verification key for the mode change ➔ Only if 0xDC enable mode change	139E	16'h0003	16	R/W
I2C Communication External Sync Register	This register defines the type of the external sync event expected by the I2C communication • 0x01: Detection Sync • 0x02: Startup Sync • 0x04: Update PB Sync • 0x08: Read Indications Sync • 0x10: Macro Sync • 0x20: Mode Sync • 0x40: Interrupt Out Sync • 0x80: Read PM Indications Sync	1318	16'h0000	16	R/W

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Register Name	Register Description	Address (HEX)	Default Value	Register Width (BITS)	Read/ Write
	0x100: Masters Sync (for host use)				
External Event: Interrupt Register for SYNC	This register defines the type of the external sync Interrupt Request Signal event expected by the I2C communication • 0x01: Detection Sync • 0x02: Startup Sync • 0x04: Update PB Sync • 0x08: Read Indications Sync • 0x10: Macro Sync • 0x20: Mode Sync • 0x40: Interrupt Out Sync • 0x80: Read PM Indications Sync • 0x100: Masters Sync (for host use)	1144	16'h0000	16	R/W

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Ports Initialization / Configuration Registers (Port Setting)

Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
I CUT - Sets Threshold Level for Maximum Port Current					
icut_reg	Register per port: Address 0x0080 for port #0, Address 0x008B for port #11 Formula: • 1 bit = 2.44 mA, Range: 0 to 256 = 0 to 625 mA Example: For 150 mA 150 / 2.44 = 62 decimal	0080 to 008B	8'd153 373mA	8	R/W
OVL_P0_ICUT… OVL_P11_ICUT	12 Registers (Register Per Port) Formula: • 1 LSB bit = 4.88 mA • Range: 0 to 255 = 0 to 1.2A Example: For 150 mA 150 / 4.88 = 61 decimal	1000 (1001) 1002 (1003) 1004 (1005) 1006 (1007) 1008 (1009) 100A (100B)	4D'h for 802.3af = 375mA 9D'h for 802.3at = 770mA	8	R/W
Set / Updates Icut Value – According to Class Level					
dis_iclass_update_reg	Formula: • "1" = Auto update is disabled. Icut will not be changed in accordance with class level. • "0" = Auto update is enabled. Icut will be changed in accordance with class level	0092	1'b1	1	R/W
ICUT mode – sys Flag	Set Icut level according to CLASS Level: • "0": Set Icut according to CLASS • "1": Set Icut to maximum value according to power allocation limits ➔ see Address Registers 1334 to 134A	1160 Bit[4]	1 = Icut MAX	1	R/W

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
AC or DC Disconnect Control Function					
ac_disco_disable_reg	**Bit per port - LSB is port #0** Formula: • "0" = AC disconnect mode Enabled • "1" = AC disconnect mode Disabled	0095	12'h000	12	R/W
dc_disco_disable_reg	**Bit per port - LSB is port #0** Formula: • "1" = DC disco. disabled • "0" = DC disco. enabled	00CA	12'hFFF	12	R/W
ACD_DCD_SEL	AC Disconnect/DC Disconnect select, 1 bit per IC • “0”: AC Disconnect select; • “1”: DC Disconnect select IC control **– not per port**	1160 BIT [0]	1 = DC disco.	16	R/W
Per Port Configuration					
priority_port0_reg	**Register per port:** Address 0x00FA for port #0 Address 0x0105 for port #11 Formula: • Range = 0 to 47 • 0 = Highest priority • 47 = Lowest priority Assigning the same priority to different channels will set the ports in accordance with their physical order, with port #1 having the highest priority. Initial value: 0d (highest priority)	00FA to 0105	6'd0	6	R/W

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
Per Port Configuration: (12 Registers) Port0_CR… Port11_CR	BITS [0;1] = Port Enable • "00": Port Disable • "01": Port Enable • "10": Force Power • "11": Reserved (future use) BITS [2;3] = Port Pair Control • "00": Reserved (future use) • "01": ALT A • "10": ALT B (back off enable) • "11": Reserved (future use) BITS [4;5] = AF/AT Port type • "00": AF • "01": AT • "10": Reserved (future use) • "11": Reserved (future use) BITS [6;7] = Port Priority • "00": Critical = Highest priority level • "01": High • "10": Low • "11": Reserved (future Use)	131A 131C 131E 1320 1322 1324 1326 1328 132A 132C 132E 1330	DFLT= 01-EN 01-ALTA 01-AT 00-Critical	16	R/W

System Status / Monitoring

Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
Vmain Voltage Measurement Register					
vmain_reg	Formula: • 1 bit = 58 mV, Range: 0 to 1024 = 0 to 59.392V Example: 896 decimal = 896 x 0.058 = 52v	0146	10'h0	10	Read
Vmain	Vmain voltage measurement register 1 LSB Bit =61 mV Range = 0 to 1023 = 0 to 62v	105c	10'h0	10	Read
Hardware Configuration & Mode Register					
HW_STATUS_REG	[1:0] = ASIC internal address (2 LSB); • 00: unit 0 • 01: unit 1 • 10: unit 2 • 11: unit 3 [6:2] = i2c_ini (5 MSB – I2C address); 0x0 – address 0 … 0x7 – address 15 {do not use 0x0 to 0x3 – general call address} • [7] = Master bit 1 = Master; 0 = Slave • [8] = i2c_mode; 1 = I2C, 0 = SPI • [9] = asic_ini_is_good; 1 = configure good • [10] = i2c_ini_is_good; 1 = configure good • [11] = config_is_good; 1 = both asic and I2C are completed	0147	12'h0	12	Read
System INIT Register	Internal Register: Latched from ASIC_INI and I2C_INI I/Os after Power Up	1164	16'h0	16	Read

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
	Bits[0;3] = ASIC_INI Value Bits[4;7] = I2C_INI Value Bits[8;15] = Version Register Value				
Averaged Junction Temperature Level					
temp_reg	Formula: • Temperature = [(684-temp_reg)/1.514]-40, Range: 0 to 684 = -40 to 441.78° C Example: 220 decimal = [(684-220)/1.514 – 40] = 266° C	0148	10'h0	10	Read
Averaged Junction Temperature	Averaged Junction Temperature, as constantly calculated and monitored by two temperature sensors, located on the PD69012 Die. Typical accuracy is ±5° C Temperature formula = Deg C = (reg_value: 684) / (-1.514)) - 40 (1 LSB = ~0.66C)	130A	10'h0	10	Read
Device Version Control Register					
ver_dev_reg	Formula: • [15-10]: POL Family, for example 001100 - 12 port family • [9-0]: Code Ver., for example: 0000000010 - version 2	015A	16'h3002	16	Read

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
CFGC_ICVER	IC HW & SW version;an internal / read only register. This register is typically used to identify chip type and the internal analog, digital code and ROM versions, based on the following coding: BITS [15-11]: Microsemi PoE Family Indication (5 MSB bits): • 5'b00010 = PD64004 • 5'b00110 = PD64012 • **5'b00111 = PD69012 (default)** • 5'b01000 = PD69004 BITS [10-8]: Analog version (3 bits) = 1 dec BITS [7-5]- Digital version (3 bits) = 1 dec BITS [4-0]: SW ROM version (5 LSB bits) = 2 dec	031A	16'b001 11,001, 001,00 010	16	Read
System Total Power Monitoring (Read from Master IC)					
sys_total_pwr_reg	**System Total Power should be read from the Master PoE Device only** Formula: • 1 bit = 36.32 mW, Range: 0 to 65536 = 0 to 2380 W *Example:* *6900 decimal = 6900 x 0.03632 = 250 watt*	019B	16'h0	16	Read
SysTotalRealPowerCons	Total power consumption of the whole system (Master + 7 x Slaves) 1 LSB = 0.1 watt	**12E8**	16'h0	16	Read

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
TotalPowerConsSlave0 to Slave7	Power consumption monitoring – as read from Master IC. 16 bits register Per IC From Slave0, add 12EC (Master) to Slave 7 – Add 12FA 1 LSB = 0.1 watt	12EC 12EE 12F0 12F2 12F4 12F6 12F8 12FA	16'h0	16	Read
Local Total Power Level (Read from Slave IC)					
ltp_slv_mng_reg	**Per each of the operating PoE Devices** Formula: • 1 bit = 9.08 mW Range: 0 to 65536 = 0 to 595 W *Example:* *8810 decimal = 8810 x 0.00908 = 80 watt*	010D	16'h0	16	Read
LocalTotalRealPowerCons	Power consumption monitoring – as read from Slave IC. Real total power consumption ∑(PortXPowerCons) 1 LSB = 0.1 watt	12AA	16'h0000	16	Read
Additional IC Status Indications	Bit [0]: Vmain is over the upper threshold Bit[1]: Junction temperature is over the threshold (150 deg C) Bit [2]: Disable ports I/O is active Bit [3]: Vmain is under AT low threshold Bit [4]: Vmain is under AF low threshold Bit [5]: The temperature is over the alarm threshold	1314	16'h00	16	Read

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Port Status Monitoring

Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
Port Classification Results Status					
class_rslt_reg	**Register per port:** Address 0x00DB for port #0, Address 0x00E6 for port #11 Formula: • 000 = Class 0 • 001 = Class 1 …. • 101 = Class 5 (future) 50 mA < I < 70 mA • 110 = Stop Class Due to OVL during Class • 111 = Un-known result	00DB to 00E6	3'h0	3	Read
Port0_class… Port1_class	Port CLASS Status Monitoring: [3:0]: First finger result [7:4]: Second finger result [15:8]: Final detected class • 000: Class 0 • 001: Class 1 • 010: Class 2 • 011: Class 3 • 100: Class 4 • 101: Reserved • 110: Reserved • 111: Class not defined	11C2 11C4 11C6 11C8 11CA 11CC 11CE 11D0 11D2 11D4 11D6 11D8	7'h7	16	Read
Port Power Consumption Value					
pwr_cons0_reg	**Register per port:** Address 0x0113 for port #0, Address 0x011E for port #11 Formula: • 1 bit = 9.08 mW, Range: 0 to 4096 = 0 to 37.2 W	0113 to 011E	12'h0	12	Read

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
Port0PowerCons…. Port11PowerCons	Real Time (Actual) port power consumption. Calculated based on Iport * Vport 12 Registers per IC: Port 0 to Port 11 LSB = 0.1 W	12B4 12B6 12B8 12BA 12BC 12BE 12C0 12C2 12C4 12C6 12C8 12CA	16'h0	16	Read
AC Disconnect Status Register					
ac_disco_port_off_reg	**Bit per port – LSB is port #0** Formula: • ”1” = Port is **off** due to AC disconnect detection. • ”0” = Port is disconnected for reasons other than AC disconnect detection.	0137	12’h000	12	Read
Port Disconnection Status	See Port status registers address 11AA – 11C0				Read
Port Power Status due to DC Disconnect					
dc_disco_port_off_reg	**Bit per port – LSB is port #0** Formula: • ”1” = Port is off due to DC disconnect. • ”0” = Port is not successful.	0138	12’h000	12	Read
	See Port status registers Address 11AA – 11C0				
Port Overload Status					
over_load_port_of_reg	**Bit per port – LSB is port #0** Formula: • ”1” = Port power off due to OVL. • ”0” = Non OVL conditions.	0139	12’h000	12	Read
Port Overload Status	See Port status registers Address 11AA – 11C0				

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
Port Off due to Disable_Ports pin or Vmain Out of Range					
dis_pdu_port_off_reg	**Bit per port – LSB is port #0** Formula: • ”1” = Port off. • ”0” = Port on.	013B	12’h000	12	Read
Port Off due to Disable	See Port status registers Address 11AA – 11C0				
OVL during Startup					
ovld_during_startup	**Indicates that the port is off due to over load during start up** **Bit per port – LSB is port #0.** Formula: • ”1” = Off due to OVL during startup. • ”0” = No OVL during startup.	0142	12’h000	12	Read
Over Load during Startup	See Port status registers Address 11AA – 11C0				
Port Present Current Consumption Level					
ichannel0_reg	**Register per port:** Address 0x014E for port #0, Address 0x0159 for port #11 Formula: • 1 bit = 1.22 mA, Range: 0 to 512 = 0 to 625 mA	014E to 0159	9’h000	9	Read
Port Start up Stage is Completed					
port_is_started_up_reg	**Bit per port – LSB is port #0** Formula: • ”1” = Port has started up. • ”0” = Port has not started up.	015B	12’h000	12	Read
Start Up Completed	See Port status registers Address 11AA – 11C0				

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
Port Over Power Consumption Status					
port_over_pwr_cons_reg	**Bit per port – LSB is port #0** Formula: • ”1” = Port power consumption is higher than maximum allowable level (this level may be based on pre-programmed fixed power consumption or class level).	0160	12’h000	12	Read
Port Over Power	See Port status registers Address 11AA – 11C0				
Read Port Status Register					
port_status0_reg	**Register per port:** Address 0x0162 for port #0, Address 0x016D for port #11 **Formula**: • [0] = port_on_reg[i]; (1= Fet is ON) • [1] = port_is_started_up_reg[i] (1= startup was completed successfully) • [2] = ovld_during_startup_reg[i] (1 = dvdt closed the port during startup) • [3] = ac_disco_port_off_reg[i] • [4] = dc_disco_port_off_reg[i] • [5] = over_load_port_off_reg[i] • [6] = short_circuit_port_off_reg[i] • [7] = dis_pdu_port_off_reg[i]; (disable ports was asserted or vmain is out of range) • [8] = overtemp_high_prot_reg[i] • [9] = overtemp_low_prot_reg[i] • [10] = port_off_due2_pwr_mng_reg[i] • [11] = ovl_rcv_reg[i]; (counter of 5 sec) • [12] = disco_rcv_reg[i] • [13] = available_ports_reg[i]	0162 to 016D	3'h0	16	Read

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
	• [14] = res_det_final_rslt_reg[i] • [15] = Back Off State [i]				
Port Status [0-7] Port Status [8-10] Port Status [11]	Port status indication is based on real time snapshot of port status. Status Indication Coding Bits are NOT latched and may be changed to reflect the real time (True) port status at the Read Operation time slot. The Indication is based on two fields: **Bits [7-0]**: Coded into 21 different status Indications as listed below: Decimal Value = 0 (zero): Port is **on**. Port was turned on due to a valid signature (res or cap) Decimal Value = 1: Port is On; Port was turned on due to Force Power command Decimal 2: Port is in starting up stage Decimal 3: Port is powered up due to Force Power command Decimal 4: Searching; Port is waiting for detection, or port during detection phase Decimal 5: Invalid Signature; Invalid signature (detection) has been detected Decimal 6: Class Error; Error in classification has been detected Decimal 7: Test Mode; Port is waiting to be turned on in Test Mode Force Power Decimal 8: Valid Signature; A valid signature has been detected (Detection Pass)	11AA 11AC 11AE 11B0 11B2 11B4 11B6 11B8 11BA 11BC 11BE 11C0	16'h00	16	Read

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
	Decimal 9: Disabled; Port is disabled Decimal 10: Startup OVL; Over-load during startup Decimal 11: Startup UDL; Under-load during startup Decimal 12: Startup Short; Short during startup Decimal 13: DvDtFail; Failure in the Dv/Dt algorithm Decimal 14: Test Error; Port was turned on as Test Mode (Force Power) and has error Decimal 15: OVL; Overload detected Decimal 16: UDL; Under-load detected Decimal 17: Short Circuit; Short circuit detected Decimal 18: PM; Port was turned off due to Power Management Mechanism Decimal 19: System Disabled; Chip level error Decimal 20: Unknown; General chip error **Bits [10-8]: Additional 3 bits Coding for 8 Additional Status Indications** **BITS [8-10] Coding:** • 000: Disabled • 001: Searching • 010: Delivering Power • 011: Test Mode • 100: Test Error • 101: Implementation Specific*				

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
	• 110: Reserved • 111: Reserved **BIT[11]:** • 0: Port in AF Mode after Class • 1: Port in AT Mode after Class				

Port Commands

Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
Port Bypass Resistor (Res) Detection					
bypass_res_det_reg	**Bit per port - LSB is port #0** Formula: • "1" = Ignore res. line detection • "0" = Include res. line detection	0134	12'd000	12	R/W
	No Bypass or Disable Res detection function in Auto Mode				
Port Bypass Classification					
dis_class_port_reg	**Bit per port - LSB is port #0.** Formula: • "1" = Disables classification function • "0" = Enables classification function If class is disabled, class is always 0	0136	12'd000	12	R/W
	No Bypass or Disable Classification function in Auto Mode				
Port Power Allocation Value (Static Max. Power Limit)					
pwr_alloc0_reg	**Register per port:** Address 0x011F for port #0, Address 0x012A for port #11 Formula: • 1 bit = 145.3 mw, Range: 0 to 256 = 0 to 37.2 W	011F to 012A	8'd0	8	R/W
Port0_PPL…. Port11_PPL	Per Port Power Allocation Limit (Static Allocation) When Port power exceeds this Power level – Port will be disconnected by the PM mechanism (when Static Power Management algorithm is selected) • LSB = 0.1W • Range = 0 to 3200 watt • DFLT value = 32 watt	1334 1336 1338 133A 133C 133E 1340 1342 1344 1346 1348 134A	16'h140 32 watt	16	R/W

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
Port Enable Control					
enable_port_reg	**Bit per port - LSB is port #0** Formula: • "1" = Enables port line detection and Port Power • "0" = Disables port line detection and Port Power	0130	12'hFFF	12	R/W
Port0_CR…. Port11_CR	Per Port Control Register – BITs [0 ;1] • 00: Port Disabled • **01: Port Enabled** • 10: Force Power • 11: Reserved	131A 131C 131E 1320 1322 1324 1326 1328 132A 132C 132E 1330	2'h01 Enable	2	R/W
Port Disable / Enable – Fast Port Off in 1 Register	One Single register to disable Ports (bit per port) 0: Port Enable 1: Port Disable	1332	16'h0	16	R/W
Turns off Main Switching FET (Port OFF)					
force_off_reg	**Bit per port - LSB is port #0.** Formula: • "1" = FET is forced off • "0" = FET is in normal mode	0132	12'd000	12	W
Port0_CR…. Port11_CR	Per Port control register: BITs [0 ;1] • 00: Port Disabled • 01: Port Enabled • 10: Force Power • 11: Reserved	131A 131C 131E 1320 1322 1324 1326 1328 132A 132C 132E 1330	2'h01 Enable	2	R/W

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
Port Test Mode Force ON Command (event)					
Port_tm_force_on_reg	**Bit per port - LSB is port #0.** Formula: • "1" = Forcing port ON until RTP functions turn it OFF If "OFF" due to RTP function => Port will not turn back ON until re-writing "1"	0191	12'h0	12	R/W
Port0_CR…. Port11_CR	Per Port Control Register – BITs [0 ;1] • 00: Port Disabled • 01: Port Enabled • **10: Force Power** • 11: Reserved	131A 131C 131E 1320 1322 1324 1326 1328 132A 132C 132E 1330	2'h01 Enable	2	R/W

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Interrupt Registers (For PD64004, PD64004A/H & PD69012 Devices)

The blue text includes a description of the Interrupt registers for the PD69012 Device

Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
Interrupt Register					
Interrupt Event Register	**Each bit in this register refers to a specific event that was triggered in one or more ports in the device.** **More than one event can be trapped and flagged, simultaneously.** The events are: • [0] Power up • [1] Power down • [2] Startup completed • [3] Detection completed • [4] Class_completed • [5] Over load • [6] Disconnect • [7] Overload during start up • [8] Vmain_out of range • [9] Over Temp event • [10] port Off due to power Management Formula: • "1" = Event was detected. • "0" = Event was not detected or event was cleared	01A7	10'd000	10	RO
Port Interrupt Out Register	This 12 bits register has a bit per port indication corresponding to the port that had the interrupt out event. BIT [0 ..11] = Ports 0 to 11	13A6	12'd000	12	RO
Interrupt I/O Enable	This bit switches the LSD I/O between LED stream data functionality output to interrupt (INT) functionality output (enable the INTERRUPT OUT I/O at the LSD Pin) BIT [5] • "1" = LED Stream Data (LSD) Out • "0" = INT Out	1160 BIT 5	1 = Disable	16	R/W

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
Interrupt Event Mask Register	Each bit in this INT MASK register refers to a specific event MASKED or ENABLED to be latched in the INT register. • "1" = Event enabled (non Masked) • "0" = Masked The events are: • [0] Port power up • [1] Port power down • [2] Detection fail • [3] OVL or short • [4] UDL or disconnect • [5] OVL during start • [6] Port Off due to PM • [7] Port Off at Start Up • [8] Over Temperature • [9] Temperature Alarm • [10] Vmain < AF limit • [11] Vmain < AT limit • [12] Vmain > Lim • [13] Reserved event	13A4	16'd000	16	R/W
Interrupt Event Register	Each bit in this INT register refers to a specific event that was latched during system operation • "1" = Event Latched • "0" = Event Cleared up All Bits are automatically cleared after read operation • The events are: • [0] Port power up • [1] Port power off • [2] Detection fail • [3] OVL or short • [4] UDL or disconnect • [5] OVL during start or DVDT fail • [6] Port OFF due to PM • [7] Port Off at Start Up • [8] Over temperature • [9] Temperature alarm • [10] Vmain < AF limit	0324	16'd000	16	R/W

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
	• [11] Vmain < AT limit • [12] Vmain > Lim [13] Reserved event				
Power Up – Interrupt Event					
Port Power Up	Per Port Power Up event. Logic "1" indicates that the specific port was switched **on** (including force power command) • [0] Port #1 • [1] Port #2 • [2] Port #3 • [3] Port #4 Formula: • "1" = Event was detected • "0" = Event was not detected or event was cleared	01AE	4'd0	4	RO
Interrupt – Clear On Read Command					
Port Power Up - Clear On Read Register	Read Operation of this register clears up the specific bit in the associated interrupt register. Logic "1": clears the specific bit. • [0] Port #1 • [1] Port #2 • [2] Port #3 • [3] Port #4 Formula: "1" = Clear event operation "0" = No clear operation	01AF	4'd0	4	RO

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
Power OFF Event					
Port Power Down	Per Port Power Down event. Logic "1": indicates that the specific port was switched **off** (including power **OFF** command) • [0] Port #1 • [1] Port #2 • [2] Port #3 • [3] Port #4 Formula: • "1" = Event was detected • "0" = Event was not detected or event was cleared	01B0	4'd0	4	RO
Interrupt – Clear On Read Command					
Port Power Down - Clear On Read Register	Read Operation of this register; clears up the specific bit in the associated interrupt register. Logic "1": clears the specific bit. • [0] Port #1 • [1] Port #2 • [2] Port #3 • [3] Port #4 Formula: • "1" = Clear event operation • "0" = No clear operation	01B1	4'd0	4	RO
Port Start Up Event					
Port Start Up Completed	Per Port Start Up Completed event. Logic "1": Indicates that the specific port Start Up was completed successfully. • [0] Port #1 • [1] Port #2 • [2] Port #3 • [3] Port #4 Formula: • "1" = Event was detected • "0" = Event was not detected or event was cleared	01B2	4'd0	4	RO

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
Interrupt – Clear On Read Command					
Port Start Up - Clear On Read Register	Read Operation of this register: Clears up the specific bit in the associated interrupt register. Logic "1": Clears the specific bit. • [0] Port #1 • [1] Port #2 • [2] Port #3 • [3] Port #4 Formula: • "1" = Clear event operation • "0" = No clear operation	01B3	4'd0	4	RO
Line Detection Event					
Port Detection Completed	Per Port Detection Completed event. Logic "1": Indicates that the specific port IEEE802.3AF detection was completed successfully. • [0] Port #1 • [1] Port #2 • [2] Port #3 • [3] Port #4 Formula: • "1" = Event was detected • "0" = Event was not detected or event was cleared	01B4	4'd0	4	RO
Interrupt – Clear On Read Command					
Port Detection - Clear On Read Register	Read Operation of this register: Clears up the specific bit in the associated interrupt register. Logic "1": Clears the specific bit. • [0] Port #1 • [1] Port #2 • [2] Port #3 • [3] Port #4 Formula: • "1" = Clear event operation • "0" = No clear operation	01B5	4'd0	4	RO

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
Class Completed Event					
Port Classification Completed	Per Port Classification Completed event. Logic "1": Indicates that the specific port IEEE802.3AF classification was completed successfully. • [0] Port #1 • [1] Port #2 • [2] Port #3 • [3] Port #4 Formula: • "1" = Event was detected • "0" = Event was not detected or event was cleared	01B6	4'd0	4	RO
Interrupt – Clear On Read Command					
Port Classification - Clear On Read Register	Read Operation of this register: Clears up the specific bit in the associated interrupt register. Logic "1": Clears the specific bit. • [0] Port #1 • [1] Port #2 • [2] Port #3 • [3] Port #4 Formula: • "1" = Clear event operation • "0" = No clear operation	01B7	4'd0	4	RO
Port OVL Event					
Port Overload Register	Per Port Overload event. Logic "1": Indicates that the specific port overload condition was detected Port current above Icut level for more than Tcut value or short conditions or over temperature were detected. • [0] Port #1 • [1] Port #2 • [2] Port #3 • [3] Port #4 Formula: • "1" = Event was detected • "0" = Event was not detected or event was cleared	01B8	4'd0	4	RO

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
Interrupt – Clear On Read Command					
Port Overload - Clear On Read Register	Read Operation of this register: Clears up the specific bit in the associated interrupt register. Logic "1": Clears the specific bit. • [0] Port #1 • [1] Port #2 • [2] Port #3 • [3] Port #4 Formula: • "1" = Clear event operation • "0" = No clear operation	01B9	4'd0	4	RO
Port Disconnected Event					
Port Disconnect Register	Per Port Disconnect event. Logic "1":I Indicates that the specific port AC or DC Disconnect event was detected • [0] Port #1 • [1] Port #2 • [2] Port #3 • [3] Port #4 Formula: • "1" = Event was detected • "0" = Event was not detected or event was cleared	01BA	4'd0	4	RO
Interrupt – Clear On Read Command					
Port Overload - Clear On Read Register	Read Operation of this register: Clears up the specific bit in the associated interrupt register. Logic "1": Clears the specific bit. • [0] Port #1 • [1] Port #2 • [2] Port #3 • [3] Port #4 Formula: • "1" = Clear event operation • "0" = No clear operation	01BB	4'd0	4	RO

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
OVL during Startup Event					
Port OVL at Start Up Register	Per Port OVL at Start Up event. Logic "1": Indicates that the specific port Overload During Start Up event was detected This event is typically trapped when powering into short conditions or when an over sized capacitor is used. • [0] Port #1 • [1] Port #2 • [2] Port #3 • [3] Port #4 Formula: • "1" = Event was detected • "0" = event was not detected or event was cleared	01BC	4'd0	4	RO
Interrupt – Clear On Read Command					
Port OVL at Start Up - Clear On Read Register	Read Operation of this register. Clears Up the specific bit in the associated interrupt register. Logic "1": Clears the specific bit. • [0] Port #1 • [1] Port #2 • [2] Port #3 • [3] Port #4 Formula: • "1" = Clear event operation • "0" = No clear operation	01BD	4'd0	4	RO
Power OFF Due To PM					
Port Off Due to Power Management Register	Per Port Power Off Due to Power management event. Logic "1": Indicates that the specific port was powered down due to limited available power. • [0] Port #1 • [1] Port #2 • [2] Port #3 • [3] Port #4 Formula: • "1" = Event was detected	01C2	4'd0	4	RO

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
	• "0" = Event was not detected or event was cleared				
Interrupt – Clear On Read Command					
Port Off Due to Power Management - Clear On Read Register	Read Operation of this register. Clears up the specific bit in the associated interrupt register. Logic "1": Clears the specific bit. • [0] Port #1 • [1] Port #2 • [2] Port #3 • [3] Port #4 Formula: • "1" = Clear event operation • "0" = No clear operation	01C3	4'd0	4	RO
General System Events					
General system events Register	General system events • [0] All Ports are Powered Off due to Vmain Out Of Range Event • [1] All Ports are Powered Off due to Over Temperature Event Formula: • "1" = Event was detected • "0" = Event was not detected or event was cleared	01BE	4'd0	4	RO
Interrupt – Clear On Read Command					
General system - Clear On Read Register	Read Operation of this register: Clears up the specific bit in the associated interrupt register. Logic "1": Clears the specific bit. • [0] Clear Vmain out of range • [1] Clear Over Temp Formula: • "1" = Clear event operation • "0" = No clear operation	01BF	4'd0	4	RO

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
Interrupt – Clear On Read Command					
General Interrupt Clear On Write Register	Write Operation of this register: Clears up **ALL** Interrupt events registers. Write Operation of Logic "1" **or** "0" – clears all interrupt events registers	01C6	N/A	N/A	WO
MASK Register					
Interrupt Mask Register	Each bit in this register MASKS a specific event that was triggered in main interrupt register. The masks events are: • [0] Power up event • [1] Power down event • [2] Startup completed event • [3] Port detection completed • [4] class_completed • [5] ticut_fault • [6] Disconnect event • [7] Overload event (over tstart) • [8] Vmain_out of range • [9] Over temperature event Formula: • "1" = Event is masked (new events will not be trapped) • "0" = Event is not masked	01AB	10'dFFF All events are masked	10	R/W

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Register Name	Register Description	Address (HEX)	Default Value	Register Width	Read/ Write
General System MASK Register					
System Configuration Register and Interrupt PIN mask	System Configuration Register and Interrupt PIN mask This register includes a device configuration control bits and Interrupt PIN mask bit. Only Bit 14 can be used to mask or un-mask the interrupt pin. Other bits should not be modified. [0 to 13] Chip Internal Configuration bits **[14] Interrupt Pin Mask** [15] Chip Internal Configuration bit Formula: • "1" = Event is masked (new events will not be trapped) • "0" = Event is not masked	0040	16'd8040	16	R/W

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Appendix A: PD690xx Detailed Registers List and Description

REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
Port [0 to 11] Cut Off Current Register (I cut)	Per Port Cut Off Current (Icut) Level Port 0 = Address 1000 Port 1 = Address 1001 … Port 11 = Address 100B I cut level (current value) can range from 0 to 1.25 A Register Resolution = 4.88 mA per LSB I cut value is automatically set on Power Up according to AF and AT mode. DFLT value for AF mode = 4D = ~375 mA DFLT value for AT mode = 9D = ~770 mA Typical I cut accuracy is ±5%	1000 1001 1002 1003 1004 1005 1006 1007 1008 1009 100A 100B	4D in AF 9D in AT	[7:0]	RO
Port [0 to 11] Current Sense Register (I sense)	Per Port Current Consumption (Isense) Level Port 0 = Address 1044 Port 1 = Address 1046 … Port 11 = Address 105 A Isense level is the port real time current monitoring (value) as measured on the external Sense Resistor (Sense Pin). Register can range from 0 to 1.25 A Register Resolution = 305 uA per LSB I sense value is automatically averaged and updated every ~1 msec Reset value = 0 Typical accuracy of this Current Monitoring register is ±5%	1044 1046 1048 104A 104C 104E 1050 1052 1044 1056 1058 105A	0	[11:0]	RO
Vmain Measurement Register	Main Power Supply: Voltage Measurement Register Vmain voltage is measured on Vmain Pin	105C	0	[9:0]	RO

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
	Register can range from 0 to ~63 V Register Resolution = 61 mV per LSB Vmain value is automatically averaged and updated every ~20 msec Reset value = 0 Typical accuracy is ±3%				
I^2C External Sync Control Register	IC Interrupt Signal (PIN) is driven by an internal Interrupt Register. This register is **doubled buffered** which prevents skipping (missing) any internal event while busy with the Interrupt Handling Routine. For the host to update the Interrupt Register Microsemi recommends using the following routine: 1. Set **Register 1318** to the desired (expected) Sync Type (see below). 2. Perform **Write Command** to Register 1144 (which updates the actual Double Register). This register defines the type of the external sync Interrupt Request Signal event expected by the I^2C communication • 0x01: Detection Sync • 0x02: Startup Sync • 0x04: Update PB Sync • 0x08: Read Indications Sync • 0x10: Macro Sync • 0x20: Mode Sync • 0x40: Interrupt Out Sync • 0x80: Read PM Indications Sync 0x100: Masters Sync (for host use)	1318	0	[15:0]	R/W
Update Interrupt Event Register	Write to this register. The access operation itself to this register (address 1144) creates an internal SYNC signal which activates (Update) External Sync Type – Add 1318)	1144	0	[15:0]	WO
System Configuration and Control	Bit 0 = DC Disconnect Enable • 0: AC Disconnect Mode (all ports) • 1: DC Disconnect Mode (all ports)	1160	0	[14:0]	R/W

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
	Bit 1 = Internal Use (should be set to 0) Bit 2 = Legacy PD Detection Mode (Capacitor Det) • 0: Legacy PD Detection Enable • 1: Legacy PD Detection Disable Bit 3 = Internal Use (should be set to 0) Bit 4 = Set Icut Level • 0: Set Icut Current Level according to the Power Management and Power Budget Algorithm • 1: Set Icut Current Level to The Maximum Level according to AF and AT modes Bit 5 = Internal Use (should be set to 0) Bit 6 = Power Management Calculation Mode • 0: Static Mode. Power is allocated and total power is calculated according to pre-defined fixed power level per port • 1: Dynamic Mode. Power is allocated and total power is calculated according to port power consumption (in real time) Bit 7 = Internal Use (should be set to 0) Bit 8 = Internal Use (should be set to 0) Bit 9 = Vmain Under Voltage Protection in AT Mode • 0: AT Ports are **not** disconnected when Vmain is under 51 v (not protected) • 1: AT Ports are disconnected when Vmain drops below 51 v Bit 10 = when class 0 is detected then decide AF • 0: If Class 0 is detected – Port is configured as AT • 1: If Class 0 is detected – Port is configured as AF				

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
	Bit 11 = when port is configured to AT, then class 1 or 2 or 3 are Configured AF • 0: Classes 1 or 2 or 3 are considered AT • 1: Classes 1 or 2 or 3 are considered AF Bit 12 = Internal Use (should be set to 0) Bit 13 = Internal Use (should be set to 0) Bit 14 = Internal Use (should be set to 0)				
Software Boot State Monitoring	This register can be used to monitor and debug the IC Internal CPU Core or internal RAM or EEPROM. When the IC is powered-up, the internal CPU Core is initialized through the following boot sequence. The boot sequence is based on 10 different phases (each phase duration is ~100 usec) If, from any reason, the internal CPU core is stuck it can be easily debugged or confirmed that the boot is completed by "Boot Done" Bit 9 **Real Time Boot State Bits [7 to 0]**: • Bit 1: Verified ASIC_INI read • Bit 2: Verified I2C_INI read • Bit 3: Master configured on enhanced chip • Bit 4: Waiting for enhanced mode verification key • Bit 5: ASIC_INI configured manual mode • Bit 6: EEPROM Read • Bit 7: master held by disable ports line • Bit 8: Slave in initial config mode • Bit 9: Boot done • Internal CPU Core Register Monitoring, indicating last SW error Bits [13 to 8] 00000: No SW error since last reset	1168	0	[14:0]	RO

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
	• 00001: Empty memory space • 00010: Illegal bus access • 00100: Write in ROM space • 01000: Instruction fetch in register space Valid EEPROM Indication: Bit [14] • 0: No EEPROM found or Invalid data • 1: Valid EEPROM found and data update successfully				
Startup Completed Voltage Threshold	Voltage threshold for early start up completion phase. If Vport reaches a specific threshold then the Startup Phase is completed. The port proceeds to Ongoing State, Release Current Limit from AF lim to AT lim while activating Real Time Protections Mechanisms (Over Load, Disconnect, Power Management etc) This threshold voltage is useful for High Power PD's that would need to release Higher Current Limit as fast as possible, without waiting the standard 70 msec. Threshold is calculated by: [Vmain + 1.2 v – This register value] For example, if Vmain = 48 v and this register is set to Decimal 100, the threshold level would be 48 + 1.2 - 5.9 = 43.3 v Note that DFLT value is 0. Hence by default this Early Start Up Completion will **not** be activated. The Start Up phase will be completed only ~65 mS after the Port Power Up command. Register Range = 0 to 60 v LSB = 59.3 mv	11A8	0	[9:0]	R/W
Port [0 to 11] Status Port 0 = 11AA	Internal Status Bits [7 to 0]: Please note that these 8 bits are **not** latched (non-sticky). The value of this 8 bit field is updated momentarily (real time) by the internal logic. Therefore it does not necessarily	11AA 11AC 11AE 11B0 11B2	9 [disable]	[11:0]	RO

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
. . . Port 11 = 11C0	reflect the Port Status when the actual read command is performed. For a better Port Status Visibility, it is recommended to use bits [10 to 8] which are more stable / practical. • 0 (dec) = Port On. Port was turned on due to a valid signature (res or cap) • 1 (dec) = Force On Port. Port was turned on due to Force Power • 2 (dec) = Startup. Port is in startup • 3 (dec) = Force Power StartupTM. Port is in startup by force power • 4 (dec) = Searching Phase. Port is waiting for detection or during detection phase • 5 (dec) = Invalid Signature. Invalid signature has been detected • 6 (dec) = Class Error. Error in classification has been detected (For example Class Finger 1 is different than Finger 2) • 7 (dec) = Test Mode. Port turned on in Test Mode – Force Power • 8 (dec) = Valid Signature. A valid signature has been detected • 9 (dec) = Disabled. Port is disabled • 10 (dec) = StartupOVL. Overload during startup • 11 (dec) = StartupUDL. Underload during startup • 12 (dec) = StartupShort: Short during startup • 13 (dec) = Port Start Up Fail. Failure in the Start Up (Dv/Dt) algorithm • 14 (dec) = Test Error. Port was turned on in Test Mode and has error • 15 (dec) = OVL. Overload detected • 16 (dec) = UDL. Under-load detected • 17 (dec) = Short Circuit. Short circuit detected • 18 (dec) = Power Management Off – port was turned off due to Power Management • 19 (dec) = Sys. Disabled. Chip	11B4 11B6 11B8 11BA 11BC 11BE 11C0			

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
	level error (over voltage or over temp) • 20 (dec) = Unknown. General chip error Port Status: Bits [10 to 8] The value of this 3 bit field indicates the Real Time Port Status Change by the internal logic. These 3 bits better reflect Port Status when the actual read command is performed. • 000: Port Is Disabled (Port Off) • 001: Port is Searching for PD Detection • 010: Port is Delivering Power (Port On) • 011: Port in Test Mode • 100: Reserved • 101: Reserved • 110: Reserved • 111: Reserved AT Mode [Bit 11]: After classification this bit indicates if the port is an AF or AT • 0: port is detected as AF • 1: port is detected as AT				
Port [0 to 11] Class Status Port 0 = 11C2 . . . Port 11 = 11D8	• First Finger Class Results: Bit [3 to 0] • Second Finger Class Results: Bit [7 to 4] • Final Class Results: Bit [15 to 8] • 000: Class 0 • 001: Class 1 • 010: Class 2 • 011: Class 3 • 100: Class 4 • 101: Class Error (>50mA) or Finger 1 different than Finger 2 • 110: Reserved • 111: Class Not Defined	11C2 11C4 11C6 11C8 11CA 11CC 11CE 11D0 11D2 11D4 11D6 11D8	7 (dec)	[15:0]	RO
Per Port Class Status Register	Bit Per port: Overall result for the classification Bit 0 = Port 0 Bit 1 = Port 1 . .	11DA	0	[11:0]	RO

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
	Bit 11 = Port 11 0: class is completed ok 1: class fail				
Port Last Disconnection Event Port 0 = 11DC . . . Port 11 = 11F2	The reason for the last port disconnection • 9 (dec) = Port was disabled • 10 (dec) = Port was over-loaded during startup • 11 (dec) = Port was under-loaded during startup • 12 (dec) = Port was shorted during startup • 13 (dec) = Port Failure in the startup algorithm • 14 (dec) = Port was turned on as Test, Mode and has error • 15 (dec) = Overload detected • 16 (dec) = Under-load detected • 17 (dec) = Short circuit detected • 18 (dec) = Port was turned off due to Power Manager • 19 (dec) = Chip level error • 20 (dec) = General chip error	11DC 11DE 11E0 11E2 11E4 11E6 11E8 11EA 11EC 11EE 11F0 11F2	0	[7:0]	RO
Port Counter for Invalid Detection Events Port 0 = 11F4 . . . Port 11 = 120A	Per Port 8 Bit Counter: Counts the number of Invalid Detection Events (Wrong Signature) from the IC's last power up This Counter is cyclic: When the counter is Full (FF), it goes back to 0 and re-starts the counting.	11F4 11F6 11F8 11FA 11FC 11FE 1200 1202 1204 1206 1208 120A	0	[7:0]	RO
Port Counter for Power Denied Events Port 0 = 120C . . . Port 11 = 1222	Per Port 8 Bit Counter. Counts the number of Power Denied Events (Due To Power Management) from the IC last power up. When the counter is Full (FF) it goes back to 0 and re-starts the counting.	120C 120E 1210 1212 1214 1216 1218 121A 121C 121E 1220 1222	0	[7:0]	RO

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
Port Counter for Over Load Events Port 0 = 1224 . . . Port 11 = 123A	Per Port 8 Bit Counter. Counts the number of Overload Events from the IC last power up. When the counter is Full (FF) it goes back to 0 and re-starts the counting.	1224 1226 1228 122A 122C 122E 1230 1232 1234 1236 1238 123A	0	[7:0]	RO
Port Counter for Under Load Events Port 0 = 123C . . . Port 11 = 1252	Per Port 8 Bit Counter. Counts the number of Under Load Events from IC last power up. When the counter is Full (FF) it goes back to 0 and re-starts the counting.	123C 123E 1240 1242 1244 1246 1248 124A 124C 124E 1250 1252	0	[7:0]	RO
Port Counter for Short Events Port 0 = 1254 . . . Port 11 = 126A	Per Port 8 Bit Counter. Counts the number of Short Events from IC last power up. When the counter is Full (FF) it goes back to 0 and re-starts the counting.	1254 1246 1258 125A 125C 125E 1260 1262 1264 1266 1268 126A	0	[7:0]	RO
Port Counter for Class Error Events Port 0 = 126C . . . Port 11 = 1282	Per Port 8 Bit Counter. Counts the number of Class Error Events from IC last Power Up. When the counter is Full (FF) it goes back to 0 and re-starts the counting.	126C 126E 1270 1272 1274 1276 1278 127A 127C 127E 1280 1282	0	[7:0]	RO

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
Per Port Status Indication Port 0 = 1284 . . . Port 11 = 129A	Per Port Status Indication Sticky Bits with Double Buffer The Original Bits are cleared on read To read this register → need to perform Indication Sync 1. Write to 1364 – Port Select 2. Perform Sync Read Indication (Type) 1318 3. Write to 1144 Bit 0 = Under Load (Disconnect) Detected • 0: No under load detected • 1: Under load detected Bit 1 = Over Load Detected • 0: No overload detected • 1: Overload detected Bit 2 = Short Detected • 0: No short detected • 1: Short detected Bit 3 = invalid PD Resistor Signature Detected • 0: No Invalid signature detected • 1: Invalid signature detected Bit 4 = Valid PD Resistor Signature Detected • 0: No Valid PD signature detected • 1: Valid PD signature detected Bit 5 = Power Was Denied • 0: Power has not been denied • 1: Power has been denied Bit 6 = Valid Capacitor signature Detected • 0: No Valid Capacitor detected • 1: Valid capacitor detected Bit 7 = Backoff state has occurred • 0: No Backoff was made • 1: Backoff was done Bit 8 = Class Error has occurred • 0: No class error detected • 1: Class error detected	1284 . . . 129A	0	[8:0]	RO

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
Ports Power Management Indication	Bit per port: Indicates a power management event Bit 0 = Port 0 . . Bit 11 = Port 11 • 0: Port is not marked to be a candidate for power management disconnection in case of missing budget • 1: Port is marked to be a candidate for power management disconnection in case of missing budget	129C	0	[11:0]	RO
Port Real Time (Actual) Power Consumption Port 0 = 12B4 . . . Port 11 = 12CA	Port power consumption (Actual Real Time Power Consumption) Port Power is calculated based on: I port x V port LSB = 0.1W Range = 0 to FF For example: Register Decimal Value = 100 = 10 watt	12B4 . . 12CA	0	[15:0]	RO
ChipTotalCurrentCons	IC total port current (summary of all 12 ports); based on port actual current (load) LSB = 4.88 mA For example: Register Value = AA (hex) = 170 (dec) = 0.8 amp	12D2	0	[15:0]	RO
Total System Calculated Power Consumption	Sum of the whole system calculated power consumption (including all IC's – masters and slaves that are currently connected to this Master IC) This calculated power consumption is based on Port Requested Power by Class and AF/AT mode Note that this Register should be read from the Master only. Before reading this Register it is recommended to update it's content by writing "1" to Register Address 139C LSB = 0.1 W	12E2	0	[15:0]	RO

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
	Range = 0 to FF For example: Register Decimal Value = 500 = 50 watt				
Total System Real Time / Actual Power Consumption	Sum of the whole system real time power consumption This Power consumption is based on All Active Ports Power Consumption Note that this register should be read from the Master only. Before reading this register it is recommended to update it's content by writing "1" to Register Address 139C LSB = 0.1 W Range = 0 to FF For example: Register Decimal Value = 500 = 50 watt	12E8	0	[15:0]	RO
Active Slave List Register	First 8 LSBits [7 to 0] represent a bit per Active Slave IC Bit 0 = Slave 0 … Bit 7 = Slave 7 1 = Slave IC is active 0 = Slave IC is not active Note that this register should be read from the master IC only. Before reading this register it is recommended to update it's content by writing "1" to Register Address 139C Other 8 MSBits [15 to 8] represent a bit per Detected slave IC on power up Bit 8 = slave 0 … Bit 15 = Slave 7 • 1 = Slave IC was detected at Power Up • 0 = Slave IC was not detected	12EA	0	[15:0]	RO
Total (Actual) Power Consumption Per Slave IC Slave 0 =	Total real time / actual power consumption of slave 0 (master) Note that this register should be read from the Master only.	12EC . . 12FA	0	[15:0]	RO

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
12EC . . . Slave 7 = 12FA	Before reading this register it is recommended to update it's content by writing "1" to Register Address 139C LSB = 0.1 W Range = 0 to FF For example: Register Decimal Value = 100 = 10 watt				
Vmain High (MAX) Threshold	Maximum Vmain Threshold Above this level all ports are disconnected to protect the PD from over voltage This policy is always activated. LSB = 61 mV Range = 0 to 62 v For example: Register DFLT Value = 3BC (hex) = 956 (dec) = 58v	12FE	3BC	[9:0]	R/W
AT mode Vmain Low (MIN) Threshold	Minimum Vmain threshold for AT mode. Below this level "AT" ports are disconnected to comply with the AT standard. This policy can be activated or deactivated according to Register Address 1160 Bit 9. LSB = 61 mV Range = 0 to 62 v For example: Register DFLT Value = 313 (hex) = 787 (dec) = 48 v	1300	313	[9:0]	R/W
AF mode Vmain High (MAX) Threshold	Minimum Vmain Threshold for AF Mode. Below this level "AF" Ports are disconnected to comply with the AF standard. This policy is always activated. Range = 0 to 62 v For example: Register DFLT Value = 2B0 (hex) = 688 (dec) = 42v	1302	2B0	[9:0]	R/W

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
Junction Averaged Temperature	Junction average temperature: Based on two temperature sensors located on the Die. Temperature (deg C) = ((reg_value: 684) / (-1.514)): 40 Range = ~-200° C to ~400° C For example: Register Value = 500 (dec) = 82° C	130A	0	[9:0]	RO
Junction Max. Temperature Threshold for Ports Disconnect	Junction maximum temperature for ports operation. Above this value ports are disconnected to protect the IC from temperature damage. For example: Register DFLT Value = 184 (hex) = 155° C	130C	184	[9:0]	R/W
Junction Max. Temperature Threshold for Alarm	Junction maximum temperature for activating temperature alarm. Above this value temperature alarm is activated to protect the IC (see address 1314 bit 5). For example: Register DFLT Value = 184 (hex) = 155° C	130E	184	[9:0]	R/W
Junction Max. Temperature Capture	Junction maximum temperature that was captured and latched. This Register is Re-Set on Power Up or Reset	1312	3FF	[9:0]	RO
General System Errors Flags Register	Bit 0 = Vmain is over the upper threshold Bit 1 = The temperature is over the threshold Bit 2 = Disable ports PIN is active Bit 3 = Vmain is under AF low threshold Bit 4 = Vmain is under AT low threshold Bit 5 = The temperature is over the alarm threshold	1314	0	[5:0]	RO
Port Configuration Register Port 0 = 131A . . . Port 11 =	Bits [1:0] = Port Enable Status • 00: Port Disabled • 01: Port Enabled (DFLT) • 10: Force Power • 11: Reserved Bits [3:2] = Port Pair Control 00: Reserved • 01: Alternative A (DFLT)	131A .. 1330	21 (dec)	[7:0]	R/W

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
1330	• 10: Alternative B (Backoff Enable) • 11: Reserved Bits [5:4] = Port Type Definition • 00: AF mode enable • 01: AT mode enable (DFLT) • 10: Reserved • 11: Reserved Bits [7:6] = Port Priority Level • 00: Critical – Highest Priority (DFLT) • 01: High • 10: Low • 11: Reserved				
Port Enable / Disable Register	Bit Per Port: External disable port command Bit 0 = Port 0 … Bit 11 = Port 11 • 0: Port enabled • 1: Port disabled	1332	0	[11:0]	R/W
Port Power Allocation Limit Register Port 0 = 1334 . . . Port 11 = 134A	Port Power Allocation Limit (PPL) for Power Management Mechanism. These registers values are set automatically (write) by the Power Management Mechanism, according to a pre-defined algorithm. This algorithm monitors and distributes power for each port based on the system power budget, port priority, port status and port class. A port that exceeds this power level will be disconnected due to power management when power budget is limited. In Auto Mode the content of these registers is set periodically by Master (every ~20 mS) so it is not practical to set (write) a different value by external CPU. LSB = 0.1 W Default Value = 140 (hex) = 320 (dec) = 32 W	1334 .. 134A	140	[15:0]	R/W

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
Port Power Allocation Limit Register For Layer 2 Support Port 0 = 134C . . . Port 11 = 1362	Port Power Allocation Limit Register for Layer 2 Classification Support (TPPL). These registers can be used to set (write) by an external CPU (host) to set port power allocation for the Power Management Mechanism. When these registers are manually set by the external CPU / Host (usually after port is powered up), Power Management would use its value for Port Power Control. A port that exceeds this power level might be disconnected due to power management when power budget is limited. LSB = 0.1 W Default Value = 0 watt	134C .. 1362	0	[15:0]	R/W
Port Indication Clear	Port number to be cleared using the indications clear sync event 0000 = Port 0 is selected to clear 0001 = Port 1 is selected … 1011 = Port 11 is selected	1364	0	[4:0]	R/W
Total System Power Budget for Emergency Bank 0	System power budget for state 000 of the power good lines LSB = 0.1 W Default = 36 W * 96 = 3456 W	138C	8700	[15:0]	R/W
Total System Power Budget for Emergency Bank 1	System power budget for state 001 of the power good lines LSB = 0.1 W Default: 36 W * 12 = 432 W	138E	10E0	[15:0]	R/W
Total System Power Budget for Emergency Bank 2	System power budget for state 010 of the power good lines LSB = 0.1 W Default: 36 W * 8 = 300 W	1390	BB8	[15:0]	R/W
Total System Power Budget for Emergency Bank 3	System power budget for state 011 of the power good lines LSB = 0.1 W Default: 36 W * 6 = 220 W	1392	898	[15:0]	R/W
Total System Power Budget	System power budget for state 100 of the power good lines	1394	7D0	[15:0]	R/W

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
for Emergency Bank 4	LSB = 0.1 W Default: 200 W				
Total System Power Budget for Emergency Bank 5	System power budget for state 101 of the power good lines LSB = 0.1 W Default: 150 W	1396	5DC	[15:0]	R/W
Total System Power Budget for Emergency Bank 6	System power budget for state 110 of the power good lines LSB = 0.1 W Default: 15.4W * 8 = 120 W	1398	4B0	[15:0]	R/W
Total System Power Budget for Emergency Bank 7	System power budget for state 111 of the power good lines LSB = 0.1W Default: 15.4W * 6 = 100 W	139A	3E8	[15:0]	R/W
Updated Power Management Parameters	Parameters update request and indication 0: Parameters were updated 1: Waiting for parameters update	139C	0	[0]	R/W
General User Register	General user define byte: This register is used to detect reset events by the host or by the local CPU. User can program (write): Any value (different than 0) into this register. Upon Reset Event: This register returns to it's DFLT value (0)	13A0	0	[7:0]	R/W
Interrupt Mask Register	Interrupt Mask Register. Bit Per Event, Indicating that an Event was captured at one (or more) ports. 0 = Event is Masked (Disabled) 1 = Event is Enabled To trace the specific port location in which the event was traced, go to address 13A6 Bit 0 = port turned on Bit 1 = port turned off Bit 2 = detection failed Bit 3 = OVL or SC Bit 4 = Underload Detected Bit 5 = OVL or SC during startup or DvDt fail Bit 6 = port turned off due to PM Bit 7 = port power denied at startup Bit 8 = over temp Bit 9 = temp alarm Bit 10 = vmain low AF	13A4	0	[13:0]	R/W

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REGISTER NAME	REGISTER DESCRIPTION	ADDRESS (HEX)	DEFAULT VALUE (HEX)	REGISTER WIDTH (BITS)	READ/ WRITE
	Bit 11 = vmain low AT Bit 12 = vmain high Bit 13 = Reserved				
Interrupt Port Location Register	Bit per port indication of the port that had the interrupt out event 0 = Event was **not** captured 1 = Event was captured in this port Bit 0 = Port 0 … Bit 11 = Port 11	13A6	0	[11:0]	RO

Appendix B: Opening a Configuration Register for Write Operation

To protect the PoE system from incorrect configuration sequencing, some of the PD69012 Configuration Registers (from addr 0x1000 to 0x1314) are locked.

If you want to open the locked mechanisms, use the following sequence.

Note: It is highly recommended that PoE system configuration registers, such as AT / AF mode, Res. Detection / Legacy Detection Mode, I CUT currents levels etc. are set only when the system is initializing and ports are **OFF**.

Recommended sequence is listed herein:

1. Disable all ports (via the Disable pin or via the Disable Port Register).
2. Change mode to CONFIG mode (see instructions below).
3. Perform all the necessary changes (Registers Set).
4. Return to normal operational Auto mode.
5. Enable PoE ports power.

To enter the CONFIG mode:

1. DisPortsCmd reg (addr 0x1332) ➔ Write Data = 0x03FF

   or disable each port in the Portx_CR register (addr 0x131A to 0x1330) bits [1:0] ➔ Write Data = 00
2. Change mode:
   - SW_ConfigReg (addr 0x139E) ➔ Write Data = 0xDC03
   - I2C_ExtSyncType (addr 0x1318) ➔ Write Data = 0x0020 (Mode Event Sync)
   - EXT_EV_IRQ (addr 0x1144) ➔ Write Data = 0x0020 (Mode Event IRQ Sync)
   - To ensure that this command was properly performed, the user may read the SW_ConfigReg register (go to addr 0x139E) ➔ Expected Read Data = 0x0003
3. Note that at this point the RAM space (from addr 0x1000 to the end) is open for Write operations. In this mode the user can make changes to relevant registers
4. Upon write operation completion, it is recommended to return to the operational Auto mode:
   - SW_ConfigReg (addr 0x139E) ➔ Write Data = 0xDC00
   - I2C_ExtSyncType (addr 0x1318) ➔ Write Data = 0x0020
   - EXT_EV_IRQ (addr 0x1144) ➔ Write Data = 0x0020
   - To ensure that this command was performed properly, the user can read the SW_ConfigReg register (addr 0x139E) ➔ Expected Data = 0x0000
5. Re-Enable all PoE ports:
   - DisPortsCmd reg (addr 0x1332) ➔ Write Data = 0x0000, or enable each port in the Portx_CR register (addr 0x131A to 0x1330) bits [1:0] ➔ Write Data = 01

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Revision History

Revision Level / Date	Para. Affected	Description
1.0 / 30 December. 08	-	Initial Release – preliminary version
1.1 / 19 January 09	p2	Adding a note related to the reading / writing 16 bit registers.
1.2 / 24 Feb 09	p3	instructions describing how to get into CONFIG MODE added Section 2 – I^2C protocol MS byte and LS byte were inverted
1.3 / 20 Aug 09	Appendix A	Add Appendix A – with Detailed PD69012 Registers Description
1.4 / 11-Oct-09	Appendix A/B	Editing Appendix A – with detailed PD69012 Registers Description + Open Configuration to Write

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