



IGLOO2 FPGA, Errata

v3.1 January 2014

This Errata sheet contains information about known issues specific to the IGLOO[®]2 device family and provides available fixes and solutions.

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Table 1: Revision History

Date	Version	Changes
January 2014	3.1	Added information about ISP programming mode.
December 2013	3.0	Added additional programming support (SPI Slave). Added Power-up Digest is not supported —Item 12. Added SHA-256 Service to Usage Guidelines section.
October 2013	2.2	Added Item 12.
October 2013	2.1	Added the M2GL025, and M2GL005 devices.
August 2013	2.0	Added M2GL010 device information. Added item 8. Added " Usage Guidelines for IGLOO2 Devices " section.
June 2013	1.0	First revision

Table 2: Revisions Released per Device

Silicon Device	Revision	Device Status
M2GL050	Commercial/Industrial	Advanced
M2GL025	Commercial/Industrial	Advanced
M2GL010	Commercial/Industrial	Advanced
M2GL005	Commercial/Industrial	Advanced

Errata for the IGLOO2 Devices

Table 3 lists the issues specific to the IGLOO2 devices.

Table 3: Summary of IGLOO2 Devices Issues

No.	Issues	Affected Devices/ Software/ Revisions	Fixed in Device/Software/ Revisions
1.	MDDR and FDDR AXI interface does not support exclusive access	M2GL050	Updated information will be available in the Production version of the Errata.
2.	Apply DEVRST_N after ISP programming	M2GL050	Additional programming modes will be supported for the Production devices.
3.	AXI wrap transfers with more than 32 bytes in burst mode are not supported for MDDR and FDDR	M2GL050	Updated information will be available in the Production version of the Errata.
4.	MDDR/FDDR controller must be used with sequential burst mode; with BL = 8 and PHY = 32	M2GL050	Updated information will be available in the Production version of the Errata.
5.	HPMS may reset when ENC_DATA_AUTHENTICATION or DEVICE_INFO STAPL commands are sent	M2GL050	Updated information will be available in the Production version of the Errata.
6.	VPP must be 2.5V (as described in the datasheet) when operating in Industrial temperatures	M2GL050 M2GL025 M2GL010 M2GL005	Updated information will be available in the Production version of the Errata.
7.	Do not apply over-voltage on MISOs in Flash*Freeze mode	M2GL050 M2GL025 M2GL010 M2GL005	Updated information will be available in the Production version of the Errata.
8.	Verification of FPGA fabric at junction temperatures higher than 50°C erroneously indicates a failure	M2GL050 M2GL025 M2GL010 M2GL005	The future Production version of the Errata will have updated information regarding the issue.
9.	Design with DDR_OUT macro or I/O register may fail in the silicon	Software issue	Libero SoC v11.1 SP3 fixes the issue.
10.	Dedicated differential I/O driving the reference clock of the CCC may cause a functional issue due to a software bug	Software issue	Libero SoC v11.1 SP3 fixes the issue.
11.	NVM Ready bit in eNVM Status register can generate a false READY signal in the M2GL050 devices	M2GL050	Updated information will be available in the Production version of the Errata.

Table 3: Summary of IGLOO2 Devices Issues (continued)

No.	Issues	Affected Devices/ Software/ Revisions	Fixed in Device/Software/ Revisions
12.	Power-up Digest is not supported	M2GL050 M2GL025 M2GL010 M2GL005	The future Production version of the Errata will have updated information regarding this issue.

Issues, Descriptions, and Solutions for the IGLOO2 device

1. MDDR and FDDR AXI interface does not support exclusive access

The MDDR and FDDR AXI interface in the M2GL050 device is compliant with AMBA AXI Protocol Specification v1.0, except for the exclusive access functionality. The future version of the Errata will have updated information about the exclusive access functionality for the AXI interface in the M2GL050 commercial device.

2. Apply DEVRST_N after ISP programming

The M2GL050 device supports programming in JTAG, Slave SPI, and ISP modes. However, after ISP programming, DEVRST_N needs to be used to reset the device or power cycle the device.

3. AXI wrap transfers with more than 32 bytes in burst mode are not supported for MDDR and FDDR

Do not use wrap transfers with more than 32 bytes in the M2GL050 device.

4. MDDR/FDDR controller must be used with sequential burst mode; with BL = 8 and PHY = 32

Although the MDDR and FDDR controllers in the IGLOO2 devices support various burst modes/lengths and PHY settings, only a subset of these settings are supported in the M2GL050 devices.

Recommendation:

Only use Sequential burst with BL= 8 and PHY = 32 for MDDR and FDDR with the M2GL050 device.

5. HPMS may reset when ENC_DATA_AUTHENTICATION or DEVICE_INFO STAPL commands are sent

The HPMS may reset with certain STAPL actions.

- The HPMS will reset after executing one of the following STAPL actions:
 - ENC_DATA_AUTHENTICATION
 - DEVICE_INFO
- Additionally, if any of these actions are executed while a SmartDebug session is active, HPMS resets will be observed.

6. VPP must be 2.5V (as described in the datasheet) when operating in Industrial temperatures

When writing or programming the eNVM of M2GL050, M2GL025, M2GL010, and M2GL005 devices below 0°C, the VPP must be set to 2.5V. Refer to the [IGLOO2 FPGA](#) datasheet for the VPP minimum and maximum settings. However, the eNVM reading with the VPP set to 3.3V or 2.5V, operates as intended.

7. Do not apply over-voltage on MISOs in Flash*Freeze mode

When the input voltage is above the bank supply voltage (VIH/VDDIx), additional current can be consumed in Flash*Freeze mode.

8. Verification of FPGA fabric at junction temperatures higher than 50°C erroneously indicates a failure

In M2GL050, M2GL025, M2GL010, and M2GL005 devices, standalone verification (STAPL VERIFY action) should be run at temperatures lower than 50°C. If a VERIFY action is run at temperatures higher than 50°C, a false verify failure may be reported. Check Digest system services can be used to confirm design integrity at temperature within the recommended operation conditions.

9. Design with DDR_OUT macro or I/O register may fail in the silicon

There are two cases using Libero SoC v11.1 SP1 and v11.1 SP2, the designs will not work on the silicon but it's fine in simulation.

- If you use DDR_OUT macro in your design.
- If you combine an output or output enable register with an I/O using the PDC command `set_io <portName> -register yes`

Solution:

Libero SoC v11.1 SP3 fixes the issue.

10. Dedicated differential I/O driving the reference clock of the CCC may cause a functional issue due to a software bug

If your design has the dedicated differential I/O pair driving the reference clock of the CCC, the input clock may not propagate to CCC due to a software bug and the device will fail during silicon testing. There are several options to drive the ref clock of the CCC. One of the options is to drive from "Dedicated Input PAD x" (x = 0 to 3); this uses hardwired routing. In this option, choose single-ended I/O or differential I/O as the ref clock. This issue exists when you choose the differential I/O option, meaning the dedicated differential I/O is used as CCC reference clock input.

This issue can't be detected in any functional simulation, and can only be detected in silicon testing.

Solution:

The issue is fixed in the Libero SoC 11.1 SP3. Migrate your design to the Libero SoC 11.1 SP3, and re-run Compile and Layout.

11. NVM Ready bit in eNVM Status register can generate a false READY signal in the M2GL050 devices

If you send an instruction to the eNVM controller in the M2GL050 device and then start polling the READY signal (bit0 of the eNVM Status register) to check when the eNVM controller is ready for the next function, the first assertion of the READY signal occurs when the eNVM controller is not yet ready, resulting in generation of a false READY signal. However, the immediate next assertion of the READY signal will correctly indicate that the eNVM controller is ready.

Workaround for the M2GL050 Devices

The workaround is to add an extra eNVM Status bit read that will poll/read the eNVM Status bit twice as READY.

12. Power-up Digest is not supported

The current M2GL050, M2GL025, M2GL010, and M2GL005 device do not support the Power-up Digest feature.

Workaround

The user can use NVM Data Integrity Check System service after the device is on and check the data integrity.

Usage Guidelines for IGLOO2 Devices

Microsemi recommends the following conditions for IGLOO2 device usage:

1. Programming support

- JTAG and SPI Slave programming modes only however, after ISP programming, DEVRST_N needs to be used to reset the device or power cycle the device.
- FLASH_GOLDEN_N pin functionality is not currently supported. Contact Microsemi SoC technical support for additional information.

2. Accessing PCIe Bridge register in high speed serial interface

The PCIe Bridge registers should not be accessed before the PHY is ready. Wait for the PHY_READY signal (indicates when PHY is ready) to be asserted before updating the PCIe Bridge registers. The PHY_READY signal is normally asserted within 200 μ s after the device is powered up, so wait for 200 μ s before accessing the PCIe Bridge registers.

3. SHA-256 Service

Microsemi recommends the message required to be on byte boundary when using SHA-256 System Service for the M2GL050S (TS) devices.

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**

From the rest of the world, call **650.318.4460**

Fax, from anywhere in the world **650.318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Microsemi SoC Products Group Customer Support website for more information and support (<http://www.microsemi.com/soc/support/search/default.aspx>). Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on website.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at <http://www.microsemi.com/soc/>.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

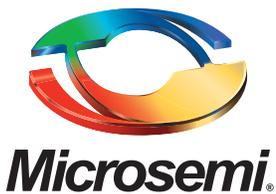
Microsemi SoC Products Group customers may submit and track technical cases online by going to [My Cases](#).

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within [My Cases](#), select Yes in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the [ITAR web page](#).



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