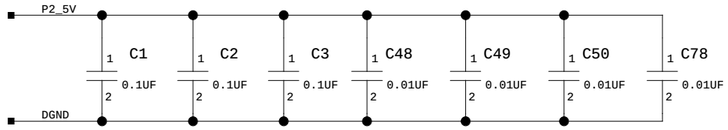
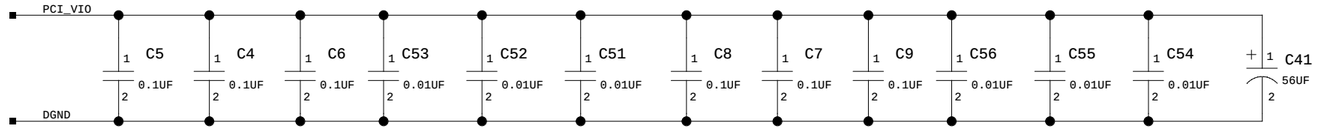
ACTEL CORE PCI DEVELOPMENT BOARD

REVISION NUMBER	DESCRIPTION
1.00	Initial Release

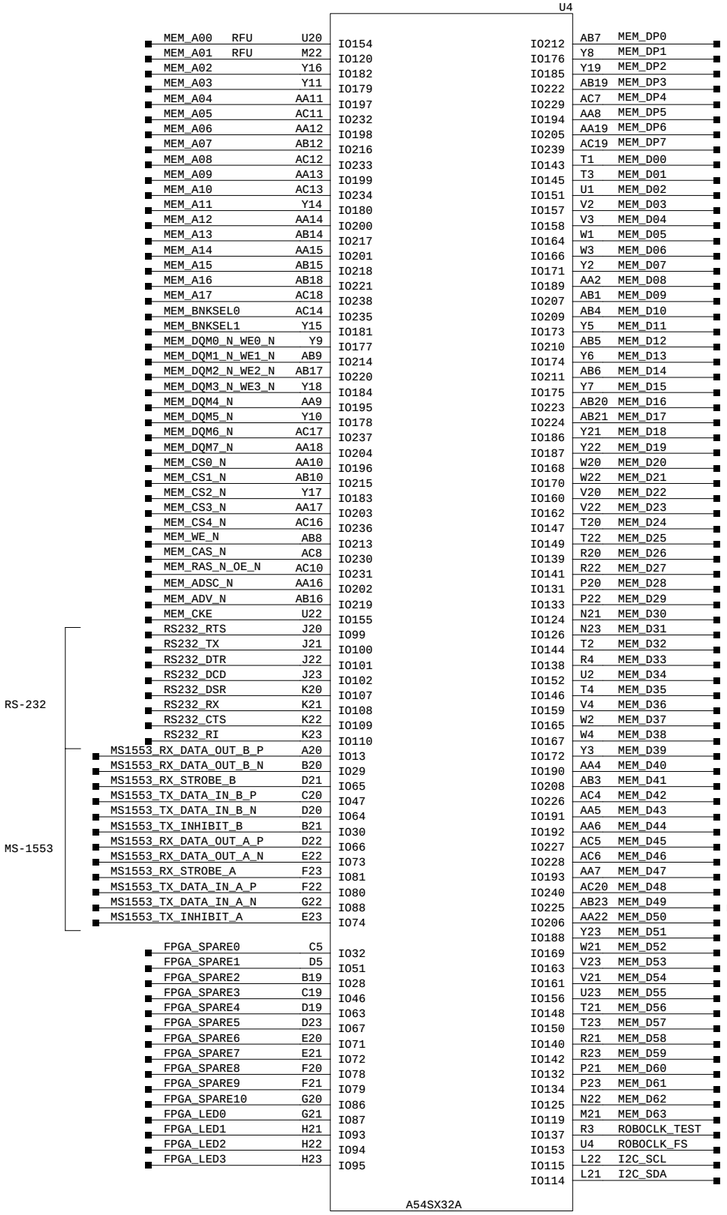
PROTOCOL DESIGN SERVICES

PROJECT:	ACTEL CORE PCI DEVELOPMENT BOARD	
PART NO:	9210-01-03	
	Sheet: 1	DATE: 7/22/02
Last edit: 7-22-2002_10:33	Rev. 1.00 of: 6	DRAWN BY: R. SCHOENBERG

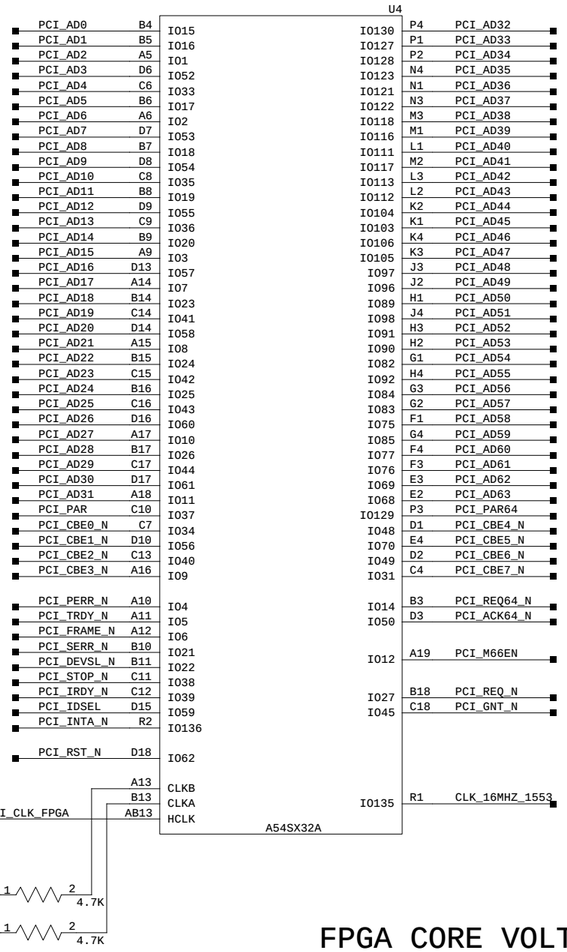




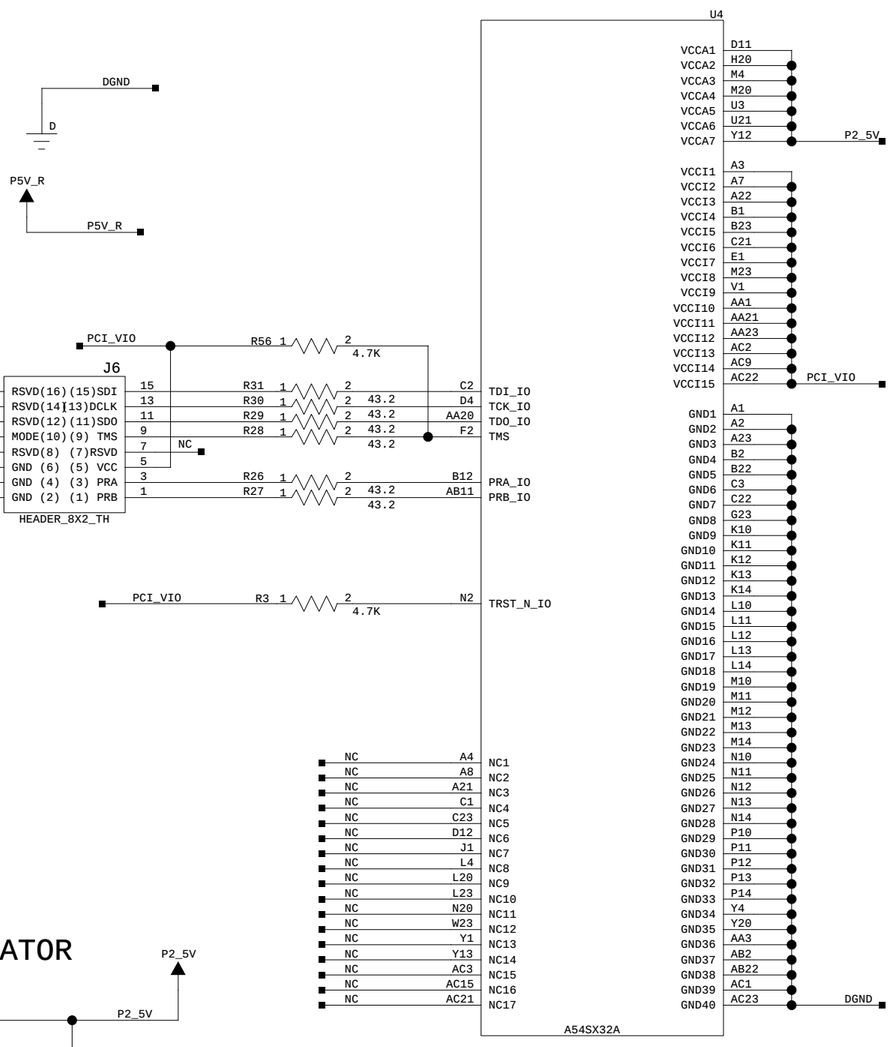
MEMORY, I/O AND SPARE



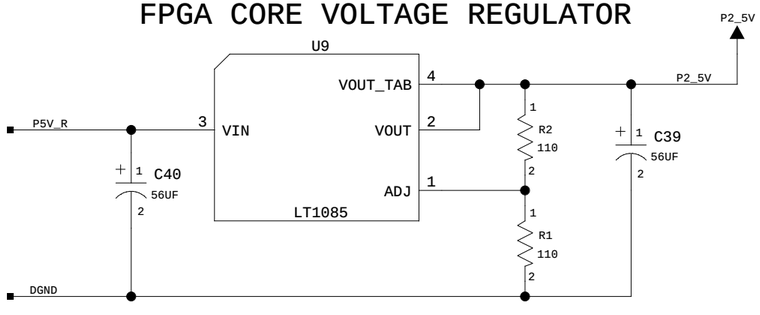
PCI CONNECTIONS



POWER AND SILICON EXPLORER



FPGA CORE VOLTAGE REGULATOR



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Actel
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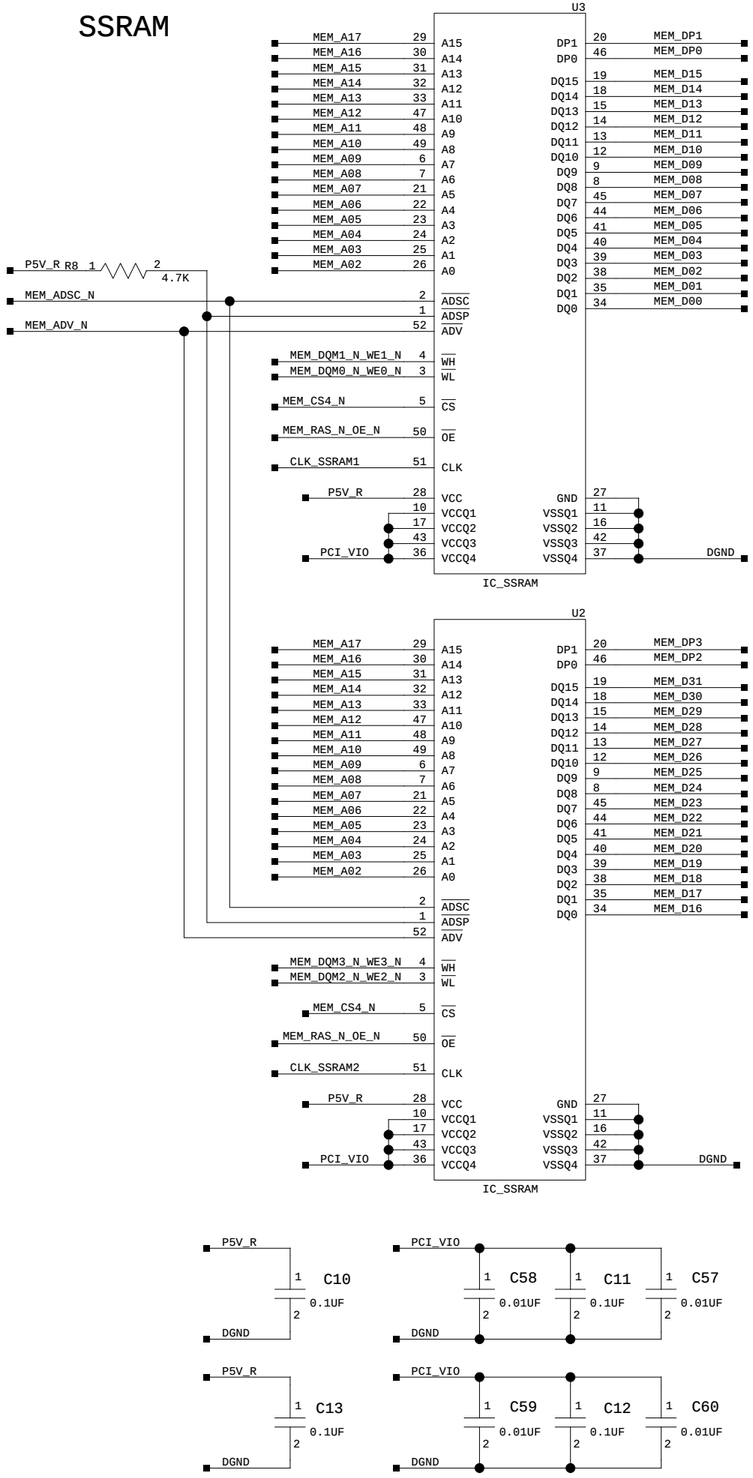
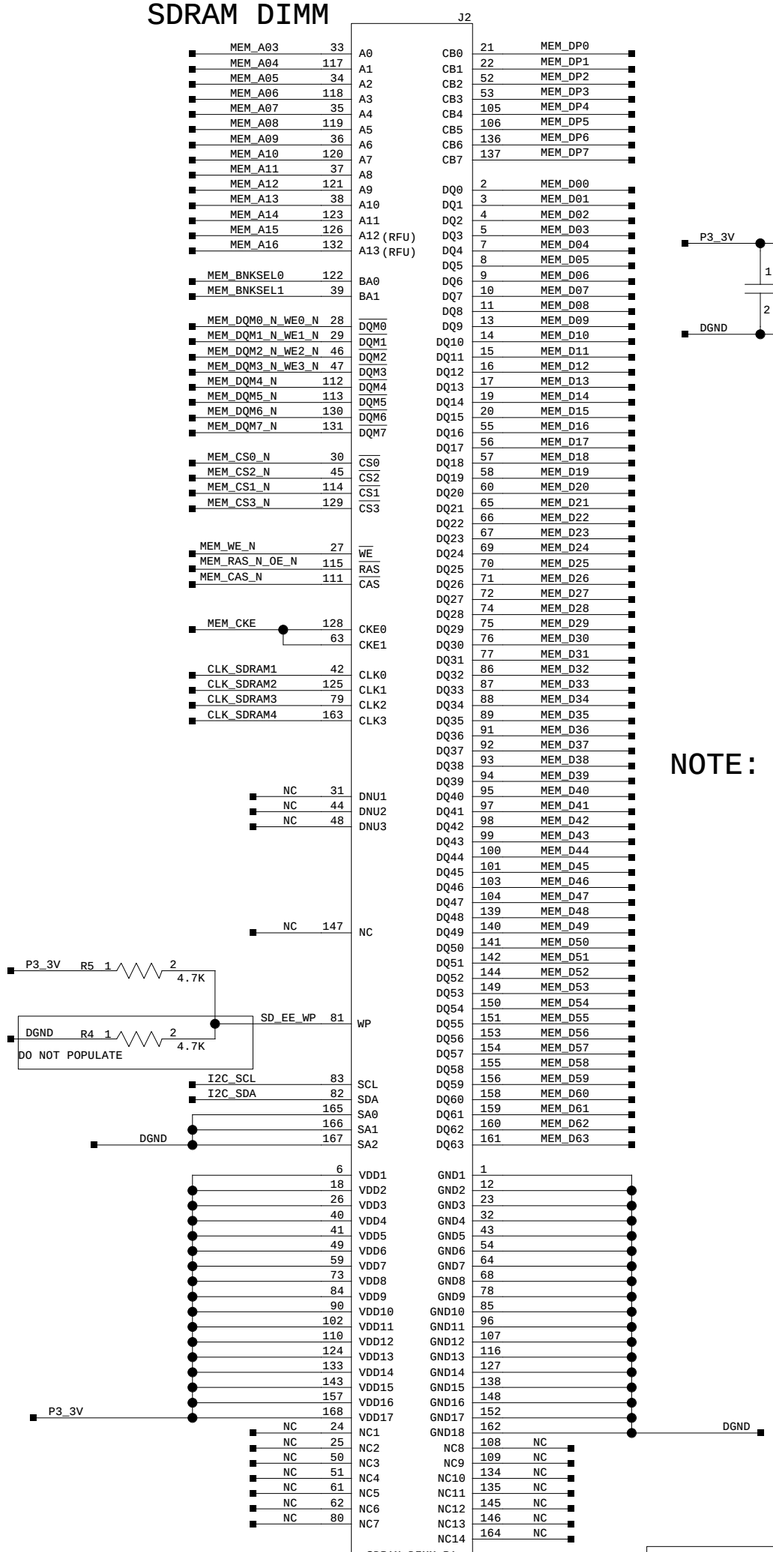
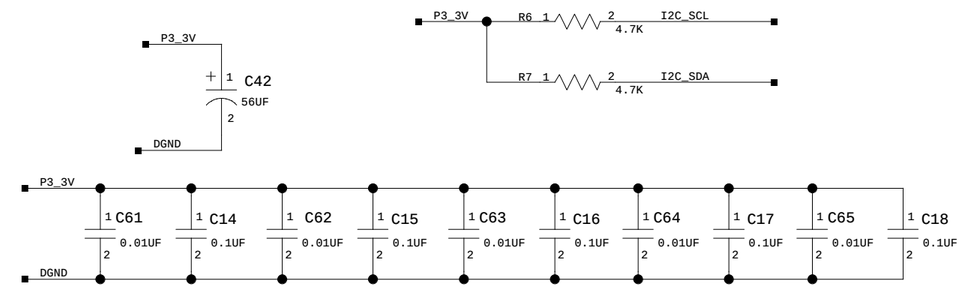
SSRAM

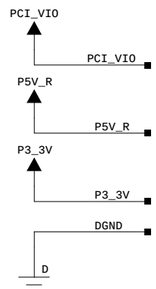


SDRAM DIMM





NOTE: DIMM MUST BE REMOVED FOR
OPERATION IN 5V PCI SYSTEM.



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CLOCK PLL AND DRIVER

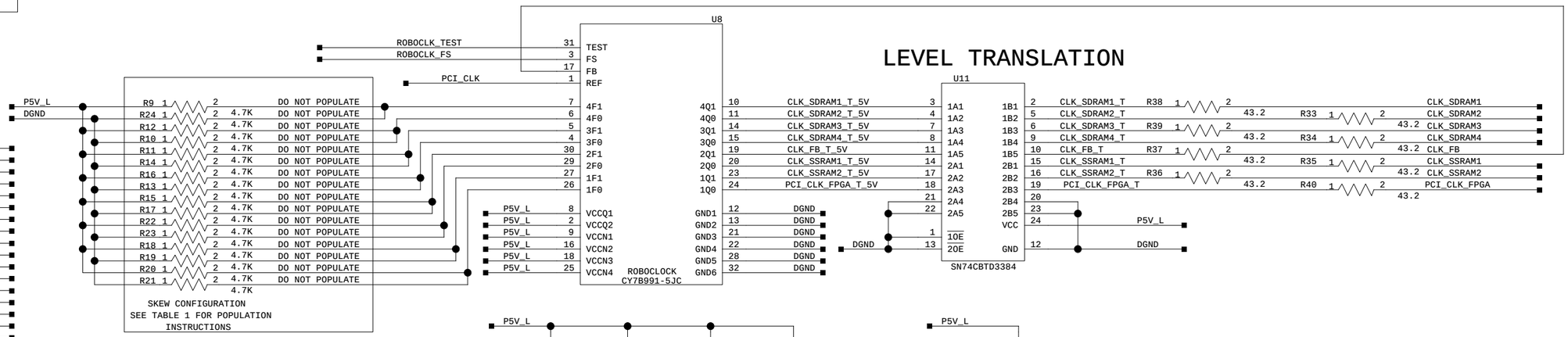
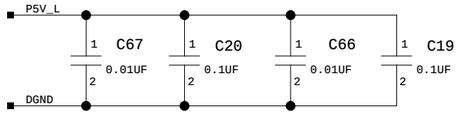


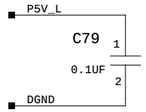
Table 1. Programmable Skew Configurations

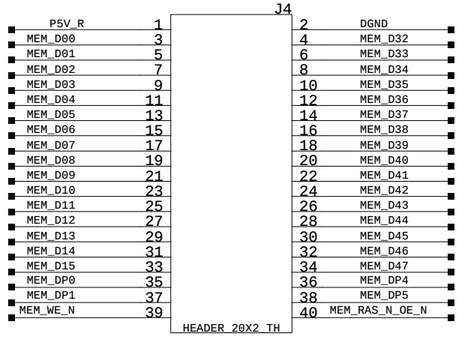
Function Selects		Output Functions		
1F1, 2F1, 3F1, 4F1	1F0, 2F0 3F0, 4F0	1Q0, 1Q1, 2Q0, 2Q1	3Q0, 3Q1	4Q0, 4Q1
LOW	LOW	$-4t_U$	Divide by 2	Divide by 2
LOW	MID	$-3t_U$	$-6t_U$	$-6t_U$
LOW	HIGH	$-2t_U$	$-4t_U$	$-4t_U$
MID	LOW	$-1t_U$	$-2t_U$	$-2t_U$
MID	MID	$0t_U$	$0t_U$	$0t_U$
MID	HIGH	$+1t_U$	$+2t_U$	$+2t_U$
HIGH	LOW	$+2t_U$	$+4t_U$	$+4t_U$
HIGH	MID	$+3t_U$	$+6t_U$	$+6t_U$
HIGH	HIGH	$+4t_U$	Divide by 4	Inverted

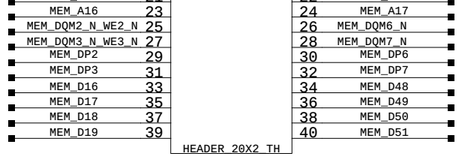
1F0 -> (R38 & R39) Low: Install R39 - Mid: Install neither - High: Install R38
1F1 -> (R36 & R37) Low: Install R37 - Mid: Install neither - High: Install R36
2F0 -> (R34 & R35) Low: Install R35 - Mid: Install neither - High: Install R34
2F1 -> (R32 & R33) Low: Install R33 - Mid: Install neither - High: Install R32
3F0 -> (R30 & R31) Low: Install R31 - Mid: Install neither - High: Install R30
3F1 -> (R28 & R29) Low: Install R29 - Mid: Install neither - High: Install R28
4F0 -> (R26 & R27) Low: Install R27 - Mid: Install neither - High: Install R26
4F1 -> (R24 & R25) Low: Install R25 - Mid: Install neither - High: Install R24

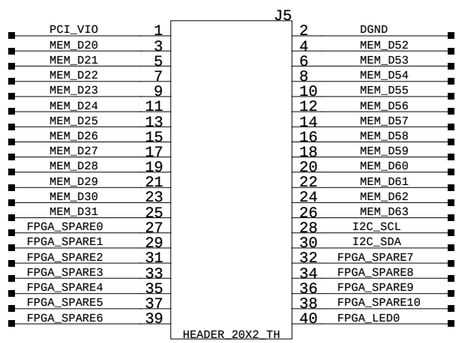
LEVEL TRANSLATION



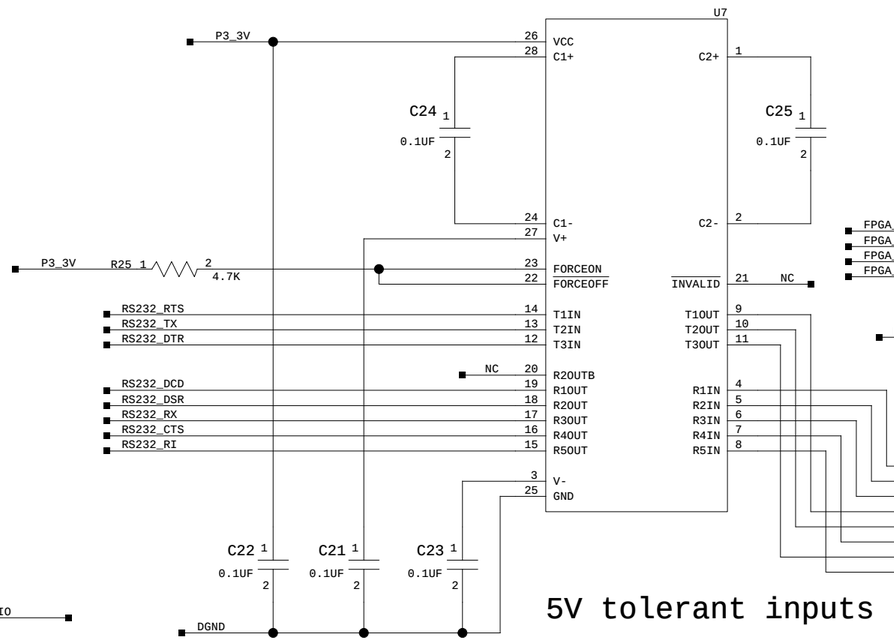




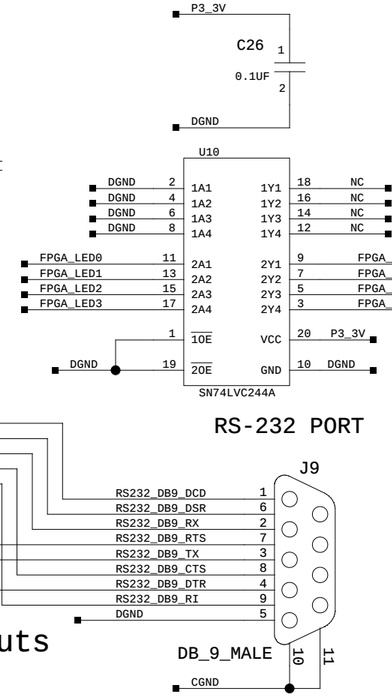




RS-232 INTERFACE

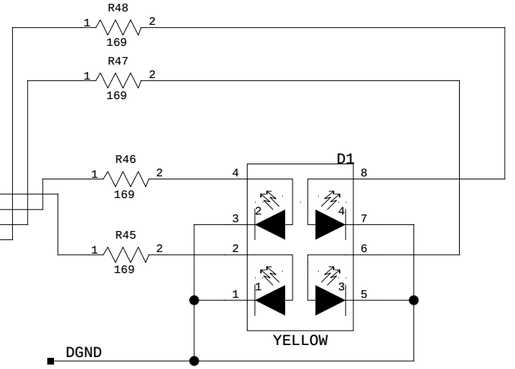


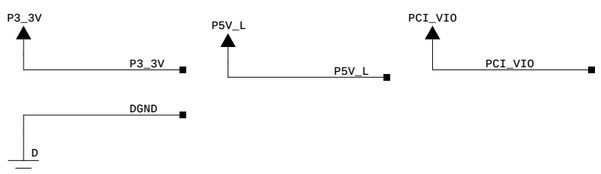
5V tolerant inputs



RS-232 PORT

GENERAL PURPOSE LEDS





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64 bit PCI edge connector

J1

N12V	B1	-12V	TRST	A1	NC	PCI_TRST_N
PCI_TCK	B2	TCK	+12V	A2		P12V
DGND	B3	GND	TMS	A3	NC	PCI_TMS
PCI_TDO	B4	TDO	TDI	A4		PCI_TDI
P5V_L	B5	+5VB5	+5VA5	A5		
	B6	+5VB6	INTA	A6		PCI_INTA_N
PCI_INTB_N NC	B7	INTB	INTC	A7	NC	PCI_INTC_N
PCI_INTD_N NC	B8	INTD	+5VA8	A8		P5V_L
R50 1 0.0 2	B9	PRSNT1	RSVDA9	A9		NC
	NC B10	RSVDB10	VIOA10	A10		PCI_VIO
DGND R49 1 0.0 2 25W DO NOT POPULATE	B11	PRSNT2	RSVDA11	A11		NC
NC	B14	RSVDB14	+3.3VAUX	A14		NC
	B15	GNDB15	RST	A15		PCI_RST_N
PCI_CLK	B16	CLK	VIOA16	A16		
	B17	GNDB17	GNT	A17		PCI_GNT_N
PCI_REQ_N	B18	REQ	GNDA18	A18		
	B19	VIOB19	PME	A19		NC
PCI_AD31	B20	AD31	AD30	A20		PCI_AD30
PCI_AD29	B21	AD29	+3.3VA21	A21		
	B22	GNDB22	AD28	A22		PCI_AD28
PCI_AD27	B23	AD27	AD26	A23		PCI_AD26
PCI_AD25	B24	AD25	GNDA24	A24		
P3_3V_EDGE_CONN	B25	+3.3VB25	AD24	A25		PCI_AD24
PCI_CBE3_N	B26	C/BE3	IDSEL	A26		PCI_IDSEL
PCI_AD23	B27	AD23	+3.3VA27	A27		
	B28	GNDB28	AD22	A28		PCI_AD22
PCI_AD21	B29	AD21	AD20	A29		PCI_AD20
PCI_AD19	B30	AD19	GNDA30	A30		
	B31	+3.3VB31	AD18	A31		PCI_AD18
PCI_AD17	B32	AD17	AD16	A32		PCI_AD16
PCI_CBE2_N	B33	C/BE2	+3.3VA33	A33		
	B34	GNDB34	FRAME	A34		PCI_FRAME_N
PCI_IRDY_N	B35	IRDY	GNDA35	A35		
	B36	+3.3VB36	TRDY	A36		PCI_TRDY_N
PCI_DEVSL_N	B37	DEVSEL	GNDA37	A37		
	B38	PCIXCAP/GND	STOP	A38		PCI_STOP_N
NC	B39	LOCK	+3.3VA39	A39		
PCI_PERR_N	B40	PERR	SMBCLK	A40		NC
	B41	+3.3VB41	SMBDAT	A41		NC
PCI_SERR_N	B42	SERR	GNDA42	A42		
	B43	+3.3VB43	PAR	A43		PCI_PAR
PCI_CBE1_N	B44	C/BE1	AD15	A44		PCI_AD15
PCI_AD14	B45	AD14	+3.3VA45	A45		
	B46	GNDB46	AD13	A46		PCI_AD13
PCI_AD12	B47	AD12	AD11	A47		PCI_AD11
PCI_AD10	B48	AD10	GNDA48	A48		
PCI_M66EN	B49	M66EN	AD9	A49		PCI_AD9
PCI_AD8	B52	AD8	C/BE0	A52		PCI_CBE0_N
PCI_AD7	B53	AD7	+3.3VA53	A53		
	B54	+3.3VB54	AD6	A54		PCI_AD6
PCI_AD5	B55	AD5	AD4	A55		PCI_AD4
PCI_AD3	B56	AD3	GNDA56	A56		
	B57	GNDB57	AD2	A57		PCI_AD2
PCI_AD1	B58	AD1	AD0	A58		PCI_AD0
	B59	VIOB59	VIOA59	A59		
PCI_ACK64_N	B60	ACK64	REQ64	A60		PCI_REQ64_N
	B61	+5VB61	+5VA61	A61		
P5V_R	B62	+5VB62	+5VA62	A62		P5V_R
NC	B63	RSVDB63	GNDA63	A63		
	B64	GNDB64	C/BE7	A64		PCI_CBE7_N
PCI_CBE6_N	B65	C/BE6	C/BE5	A65		PCI_CBE5_N
PCI_CBE4_N	B66	C/BE4	VIOA66	A66		
	B67	GNDB67	PAR64	A67		PCI_PAR64
PCI_AD63	B68	AD63	AD62	A68		PCI_AD62
PCI_AD61	B69	AD61	GNDA69	A69		
	B70	VIOB70	AD60	A70		PCI_AD60
PCI_AD59	B71	AD59	AD58	A71		PCI_AD58
PCI_AD57	B72	AD57	GNDA72	A72		
	B73	GNDB73	AD56	A73		PCI_AD56
PCI_AD55	B74	AD55	AD54	A74		PCI_AD54
PCI_AD53	B75	AD53	VIOA75	A75		
	B76	GNDB76	AD52	A76		PCI_AD52
PCI_AD51	B77	AD51	AD50	A77		PCI_AD50
PCI_AD49	B78	AD49	GNDA78	A78		
	B79	VIOB79	AD48	A79		PCI_AD48
PCI_AD47	B80	AD47	AD46	A80		PCI_AD46
PCI_AD45	B81	AD45	GNDA81	A81		
	B82	GNDB82	AD44	A82		PCI_AD44
PCI_AD43	B83	AD43	AD42	A83		PCI_AD42
PCI_AD41	B84	AD41	VIOA84	A84		
	B85	GNDB85	AD40	A85		PCI_AD40
PCI_AD39	B86	AD39	AD38	A86		PCI_AD38
PCI_AD37	B87	AD37	GNDA87	A87		
	B88	VIOB88	AD36	A88		PCI_AD36
PCI_AD35	B89	AD35	AD34	A89		PCI_AD34
PCI_AD33	B90	AD33	GNDA90	A90		
	B91	GNDB91	AD32	A91		PCI_AD32
NC	B92	RSVDB92	RSVDA92	A92		NC
NC	B93	RSVDB93	GNDA93	A93		
	B94	GNDB94	RSVDA94	A94		NC

PCICON_64

P12V — C28 1 0.1UF 2 — DGND — C27 1 0.1UF 2 — N12V

C29 1 0.1UF 2 D

PCI_TDO — R51 1 0.0 2 — PCI_TDI

PCI_VIO — C43 1 56UF 2 — DGND

P5V_L — C44 1 56UF 2 — DGND

3.3 VOLT REGULATOR

U1: VIN (P5V_R via C45 1 56UF 2 to DGND), VOUT_TAB (4) → P3_3V, VOUT (2) → P3_3V via C46 1 56UF 2, GND (1) → DGND; LT1585_3_3

P3_3V — PCI_VIO — P5V_L — P5V_R — DGND — D

P3_3V_EDGE_CONN — C68 1 0.01UF 2 — C69 1 0.01UF 2 — C70 1 0.01UF 2 — C71 1 0.01UF 2 — DGND

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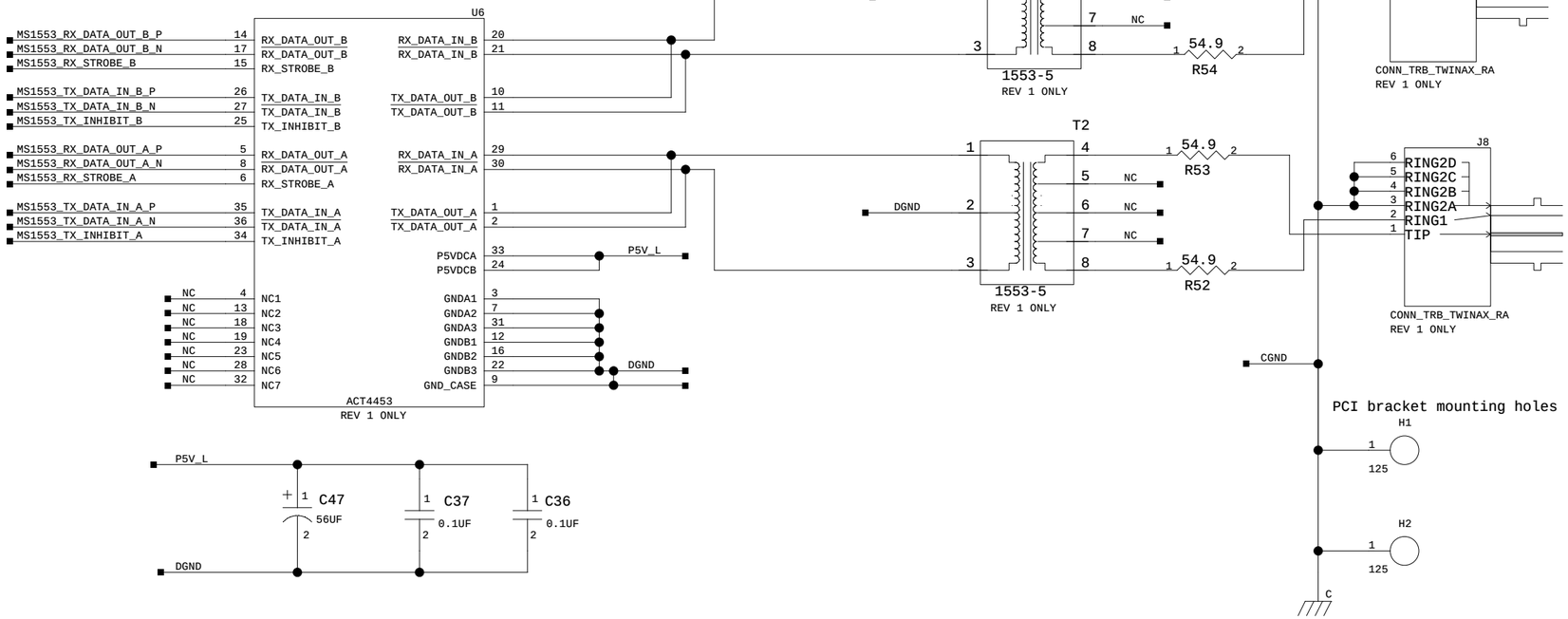
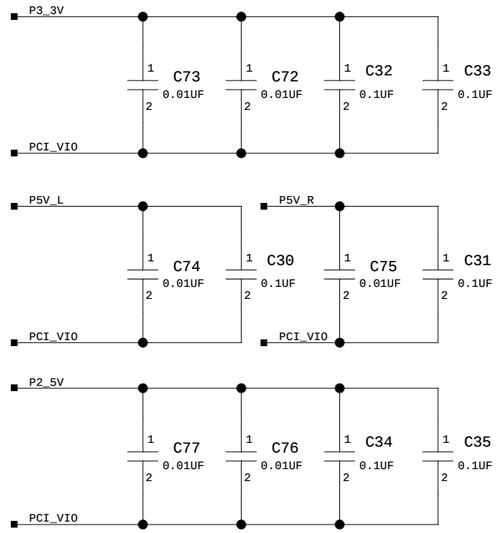
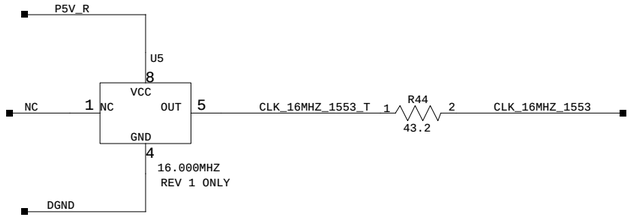
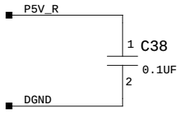
Configured for Direct coupling only.

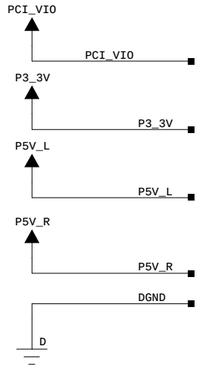


DECOUPLING FOR SPLIT VOLTAGE PLANE.









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