CorePCI 5.31 Release Notes

This document describes the new features and enhancements in the CorePCI5.31 release. CorePCI5.31 is a patch release that MUST be installed on top the CorePCI5.3 release; it provides a complete new set of VHDL source files that resolve several PCI compliance issues.

Actel recommends that all CorePCI customers using the target+DMA or target+master core upgrade to the 5.31 release; without this upgrade it is possible for the core to lock the PCI bus. Customers using just the target should also upgrade to correct various non-compliance issues.

WARNING: This patch only updates the VHDL source files; customers using Verilog source code should contact Actel customer support.

Installation Instructions

You must install the CorePCI5.3 release before installing the CorePCI 5.31 patch release. The CorePCI5.3 software and installation instructions are included on the CorePCI5.31 CD.

If you have already installed the CorePCI5.3 software, you are ready to proceed with the installation of CorePCI5.31. To do so:

1. **Copy the CorePCI5.31 update zip file from the CorePCI5.31 CD or electronic delivery (ftp or email) to a temporary location on the hard disk and unzip the files.**
2. **In the *CorePCI5.3/vhdl* directory rename the *src* directory to *src_53.***
3. **In the *CorePCI5.3/vhdl* directory rename the *wrappers* directory to *wrappers_53.***
4. **In the *CorePCI5.3* directory rename the *tbench* directory to *tbench_53.***
5. **Copy the unzipped *vhdl/src* directory to *CorePCI5.3/vhdl/src.***
6. **Copy the unzipped *vhdl/wrappers* directory to *CorePCI5.3/vhdl/wrappers.***
7. **Copy the unzipped *tbench* directory to *CorePCI5.3/tbench***

You have now updated the *vhdl/src*, *vhdl/wrappers* and *tbench* directories to the 5.31 release. You can now perform simulation and synthesis using the new VHDL files (as described in the *CorePCI5.3 Users Guide*).

Supported Tool Flows

Use Libero 2.2-SP2 or Designer R1-2002-SP2 (or later) with the CorePCI5.3 release.

Resolved Issues

Table 1 lists all the updates and fixes for the CorePCI5.31 software release.

Table 1. Software Action Requests (SARs) Resolved in the CorePCI5.31 Release

SAR No.	Description
12211	Back2back tests will fail in some cases (testbench problem)
13178	Master to Target Back-to-back Fails
21084	DMA_GNT is missing in the non-SDRAM wrappers
21085	REQn is supposed to be de-asserted for 2 cycles following a retry or disconnect
21086	REQ/GNT failure if GNT removed before FRAME
21088	Master Watchdog Timer should be off by default for Compliance
21315	Problems with BUSY and PIPE_FULL inputs
21349	PERR Pipelining Problem
21350	Testbench should stop itself properly
21773	CONFIG_RD_DATA is un-driven in the master file
21856	APA Library does not include library APA statements
21878	The 0B Test does not work in the testbench

Table 1. Software Action Requests (SARs) Resolved in the CorePCI5.31 Release

SAR No.	Description
22203	Testbench Issues ERROR messages - RAM initialization
22204	Testbench Version Numbers are not updated in the 5.3 release.
22206	Testbench cannot handle changing Backend memory widths
22210	The wrapper component package file does not contain the generics
22711	Backend Request Grant Function Fails
22740	Max Burst length logic does not handle 1024 count
22761	Bus Parking and driving CBE
22763	Simultaneous FRAMEn assertion with GNTN De-assertion
22791	Master followed by a target access fails when XX_BE_RDY is held active
22822	Core can assert STOPn at the wrong time
22873	Core can lock up if BUSY asserted in master mode
23305	Memory Read on first access, can insert >120 clock cycles
23346	Latency Timer Violates the Specification
23405	Core does not drive PERRN high after a parity error
23532	PCI State machine can enter an illegal state
24193	Core fails to handle IRDY de-assertion during burst Configuration read
24435	Configuration Cycles fail if IRDY assertion delayed or de-asserted
24447	Core should disconnect with data if transfer is not DWORD aligned
24454	The core does not report parity errors on PERR for Configuration cycles
24541	Core does not respond to Memory Read Line Commands etc
24542	Core does not disconnect at Memory (BAR) Boundaries (See note below)
24638	GNT Circuitry fails if GNTn active for only 2 clocks

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SAR No.	**Description**
24751	Array sizes for several files do not support 1024 word non-DMA transfers
24752	Write transfers that cross SDRAM page boundary corrupt data
24753	During DMA transfer, core hangs if master crosses SDRAM page boundary
24754	Long DMA transfer fails when SDRAM starting address is not 0
24770	Testbench error occurs if exhaustive tests are run twice without break

Known Issues

Table 2 lists unresolved SARs in the CorePCI5.31 release.

Table 2. Unresolved Software Action Requests (SARs) in the CorePCI5.31 Release

SAR No.	**Description**
12131	The verilog_setup.do script for MTI does not work on PC
12160	SX32A-BG329 with JTAG pins restricted causes an error with the pin file
22631	APA FG456 Pin out, INTAN at wrong end of device
23711	Technology library directories are inconsistent
24027	No Margins in Target/Master timing in the latest version of Designer using APA750
24553	MTI scripts do not compile the non DMA wrappers
24755	Pin definitions for A54SXA devices should be upward compatible to SX72A
24796	Testbench clocking may cause non-SDF netlist simulation to fail
24964	64 bit cores do not operate correctly when plugged into 32 bit buses

Only SAR24964 is a PCI compliance issue, and only effects 64 bit versions of the core when plugged into 32 bit PCI buses. All other issues relate either to the Verilog source files (not provided with this patch), pin location files (not provided with this patch), are enhancements to the simulation environment, or are corrections to the full release structure.

Timing Driven layout - Clock to Out timing fails after layout

Occasionally the core fails to meet the PCI clock-to-output delays. The constraints provided in the user guide do not take into account that the enables for the I/O buffers enable the buffers and clock cycle early and therefore the path is non-critical. If the Timer shows the clock-to-out timing failing through the I/O pad ENABLE pin then disable the path. The turnoff time is also non-critical since the PCI bus allows a complete clock cycle for the bus turnaround cycle.

In the Timer GUI go to the Breaks tab and select Global Stops. In the Filter box type “*PAD*:E” and click Set, followed by Select All and then Add. This adds all the I/O pad enable pins to the breaks, allowing the Timer to ignore the timing through the I/O pad enable pins.

Important Notes

SAR24542: Core does not disconnect at Memory (BAR) Boundaries

The core maintains the previous non-compliant behavior and does not disconnect at memory boundaries. However, if the EN_BAR_OVERFLOW constant in ADD_PHASE.VHD (line 111) is changed to '1' the core becomes PCI complaint and disconnect at memory boundaries. When enabled the core may also disconnect at address locations within 4 dwords of the actual address boundary (this may lower the PCI bus throughput).

SAR24976: Testbench clocking may cause non-SDF netlist simulation to fail

If you perform gate-level simulations then you must back-annotate SDF timing onto the netlist or the simulation will fail (due to clock skew within the testbench).

SAR24964: 64 Bit Cores

The core does not support 32 bit operations when in 64-bit mode. If a 32-bit cycle is carried out then the core treats it as 64-bit operation, even though no data is provided on the upper 32 data bits. This implies that a 64-bit core should be used only in systems that are known to operate exclusively in 64-bit mode.

Updating from 5.21

The top level generic types on the 5.3 and 5.31 core use INTEGER types, previous versions (5.21 and earlier) used std_logic. The instantiation of the core in your design needs to be updated. This change was made to make the code compatible with Synopsys Design Compiler.