Core1553BRT 2.1 Release Notes

This document describes the new features and enhancements of the Core1553BRT 2.1 release. It also contains information about system requirements, new supported families, implementations, and known limitations and workarounds.

Delivery Types

The Core1553BRT core is supplied in three variations

- Evaluation: Allows simulation of the Core1553BRT core using Modelsim
- Netlist: Complete core, enables integration into your design
- RTL: Complete core with VHDL and Verilog source code

The CD is marked with Evaluation, Netlist or RTL.

Features

- MIL-STD-1553B Compliant Remote Terminal
- Tested to RT validation Test Plan MIL-HDBK-1553, Appendix A

Supported Families

- Axcelerator
- ProASIC^{PLUS}
- RT54SX-S
- A54SX
- A54SX-A
- ACT3

Supported Tool Flows

Use Libero IDE v2.2 or Designer R1-2003 or later with the Core1553BRT 2.1 release.

Simulation for the evaluation and netlist versions require Libero IDE v2.2 OR a full version of Modelsim 5.7a or later.

Install Instructions

Copy the complete contents of the CD to the hard disk and unzip the files. This will produce a top-level directory Core1553BRT, as shown in Figure 1.

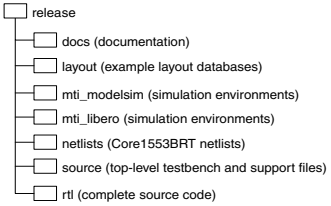

Figure 1. Core1553BRT Directory Structure

For electronic delivery (email or ftp), copy the supplied zip files to the hard disk and unzip them.

After installation the appropriate modelsim simulation directory MUST BE copied to a directory called mti.

- Libero IDE Customers: copy mti_libero to mti
- Modelsim Customers: copy mti_modelsim to mti

All the above directories are provided with the RTL version. The netlist version includes all directories apart from the *rtl* directory and the evaluation version only includes the *mti* and *docs* directories.

Refer to the Core1553BRT User's Guide (docs/Core1553BRT_UG.pdf) after installation for details on how to simulate, synthesize and run place-and-route for this core.

Documentation

The *docs* directory in the release contains a copy of the *CORE1553BRT Datasheet*, *Core1553BRT User Guide* and certification report. The datasheet describes the core functionality and the user guide gives step-by-step instructions on how to simulate, synthesize and place-and-route this core as well as implementation examples.

For updates and additional information about the software, devices, and hardware, please visit the Intellectual Property pages on the Actel web site at http://www.actel.com.

Discontinued Features and Devices

No features have been discontinued in the Core1553BRT release.

Resolved Issues in the 2.1 Release

Table 1 lists the Software Action Requests (SARs) that have been resolved in the Core1553BRT 2.1 release.

Table 1. Resolved Issues

SAR No.	Description
24740	The datasheet describes a MSGSTART output. This was omitted from the 2.0 version of the core. The CMDSYNC output behaves as the MSG-START signal not as described in the datasheet. Both of these outputs not function as per the datasheet
24741	CMDOKOUT output added. Indicates whether the legality checker has detected a legal command word. This is useful when the core USEEX-TOK is high, it allows the user to logic to know whether a received com-mand word is legal
25206	The Verilog backend model used in the user testbench did not declare enough memory for operation when CMODE=1

Table 1. Resolved Issues

SAR No.	Description
25269	The core loopback logic only verifies the data bits, an inverted SYNC pattern is not detected. The core now checks the SYNC pattern and data bits in the loopback logic

Known Limitations and Workarounds

The following problems and limitations have been found in the Core1553BRT release:

Simulation

Two sets of simulation libraries are supplied. The first, mti_libero, are compiled to run with the version of Modelsim supplied in the Libero IDE v2.2 environment. The second, mti_modelsim, are compiled to run with the full version of Modelsim. These libraries will run on Modelsim 5.7a or later.

The verification testbenches only work on systems with a VHDL Modelsim license. For systems with a Verilog Modelsim license you can use only the customizable Verilog testbench.

Libero IDE v2.3

- You may encounter the following error message when you refresh the simulation libraries with the refresh.do script:

  ```
  # ** Error: (vcom-1004) Dependencies have changed since the
  last compilation.
  ```

  Use the following command instead

  ```
  vcom -refresh -force_refresh -work Core1553B
  ```

- You may encounter the following error message when you invoke simulation:

  ```
  # ** Warning: (vsim-3473) Component 'xxxhxldxxxxxx' is not
  bound.
  ```

  The VITAL simulation libraries provided in the Libero IDE v2.3 release are incorrect. Please contact Actel customer support to obtain updated Vital simulation libraries. This applies to both the standalone Vital libraries and the pre-complied Libero IDE simulation libraries.