

A

B

C

D

THIS DRAWING AND SPECIFICATION, HEREIN, ARE THE PROPERTY OF ACTEL CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION.

REVISION NUMBER

DESCRIPTION

1.00

Initial Release

ACTEL CORE PCI DEVELOPMENT BOARD

1

1

2

2

3

3

4

4

TABLE OF CONTENTS

2	FPGA & CORE REGULATION
3	MEMORIES: SDRAM DIMM & SSRAM
4	TEST HEADERS, CLOCK GENERATION & RS-232
5	PCI INTERFACE
6	MLL-STD 1553 INTERFACE



PROJECT: ACTEL CORE PCI DEVELOPMENT BOARD
PART NO: 9210-01-03

Sheet: 1 of 6 DATE: 7/22/02
DRAWN BY: R. SCHOENBERG

Last edit: 7-22-2002_10:33

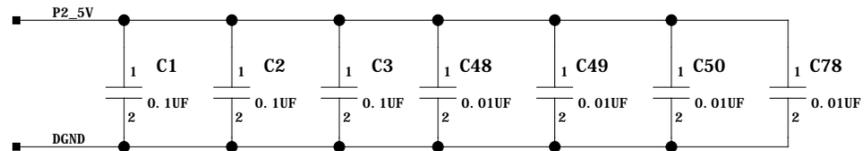
A

B

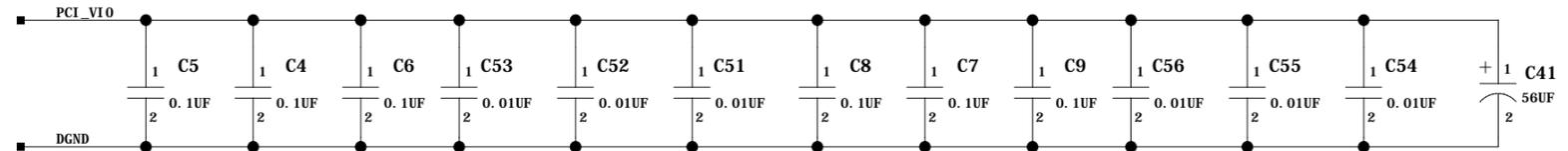
C

D

THIS DRAWING AND SPECIFICATION, HEREIN, ARE THE PROPERTY OF ACTEL CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION.



MEMORY, I/O AND SPARE



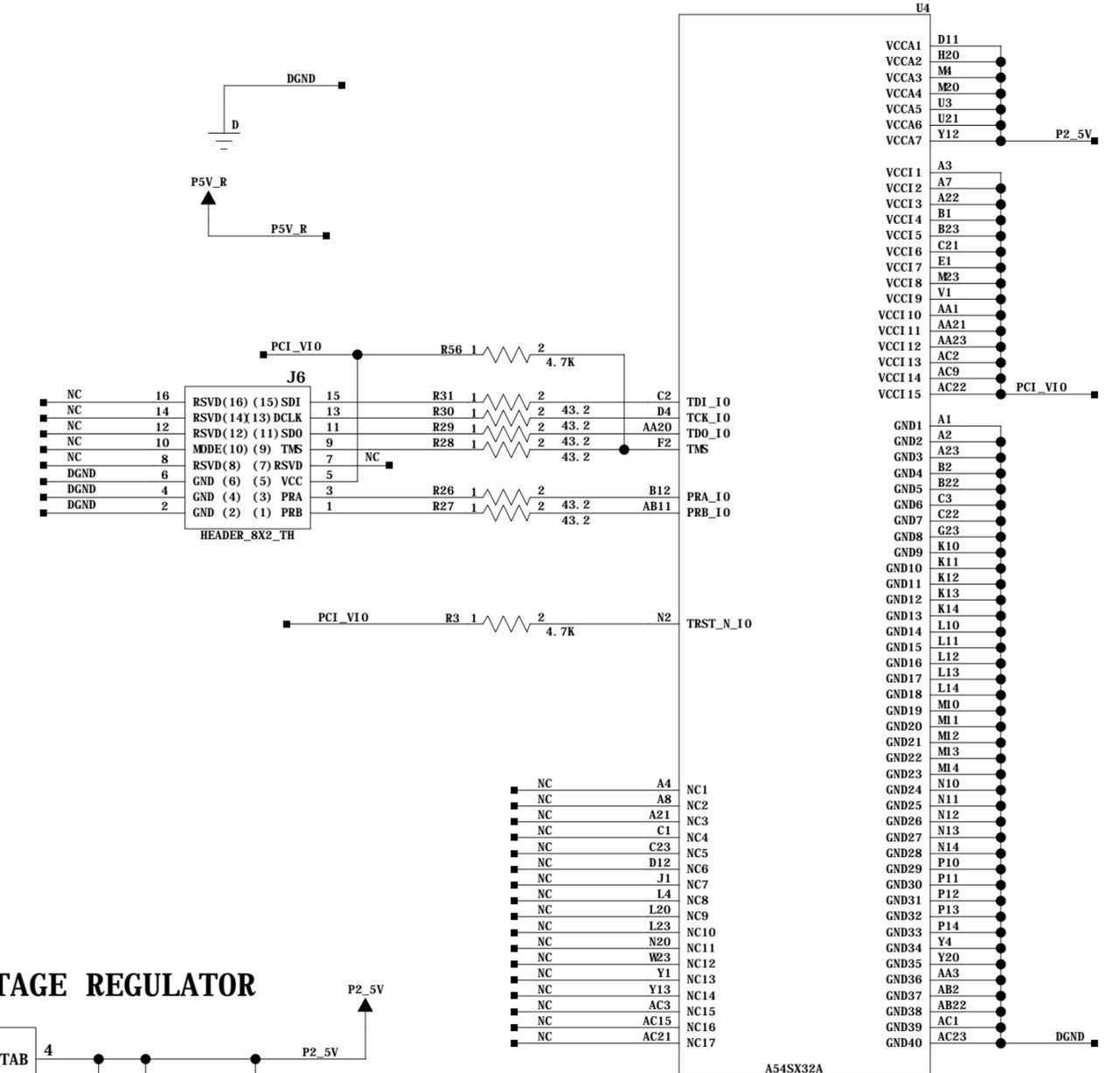
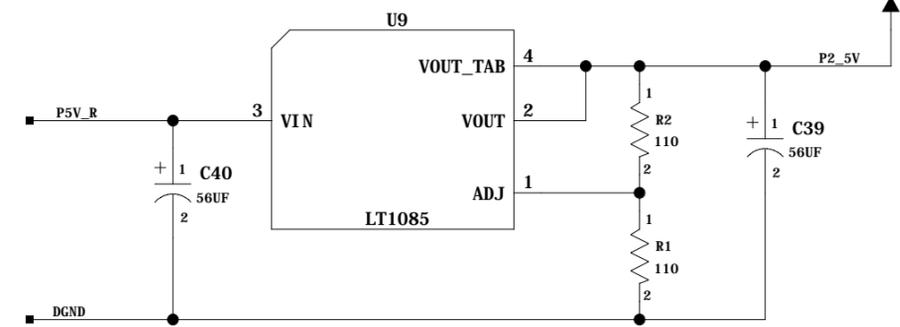
PCI CONNECTIONS

POWER AND SILICON EXPLORER

MEM_A00 RFU	U20	10154	AB7 MEM_DP0	10212
MEM_A01 RFU	M22	10176	Y8 MEM_DP1	10120
MEM_A02	Y16	10182	Y19 MEM_DP2	10185
MEM_A03	Y11	10179	AB19 MEM_DP3	10222
MEM_A04	AA11	10197	AC7 MEM_DP4	10229
MEM_A05	AC11	10232	AA8 MEM_DP5	10194
MEM_A06	AA12	10198	AA19 MEM_DP6	10205
MEM_A07	AB12	10216	AC19 MEM_DP7	10239
MEM_A08	AC12	10233	T1 MEM_DP0	10143
MEM_A09	AA13	10199	T3 MEM_DP1	10145
MEM_A10	AC13	10234	U1 MEM_DP2	10151
MEM_A11	Y14	10180	V2 MEM_DP3	10157
MEM_A12	AA14	10200	V3 MEM_DP4	10158
MEM_A13	AB14	10217	W1 MEM_DP5	10164
MEM_A14	AA15	10201	W3 MEM_DP6	10166
MEM_A15	AB15	10218	Y2 MEM_DP7	10171
MEM_A16	AB18	10221	AA2 MEM_DP8	10189
MEM_A17	AC18	10238	AB1 MEM_DP9	10207
MEM_BNKSELO	AC14	10235	AB4 MEM_DP10	10209
MEM_BNKSEL1	Y15	10181	Y5 MEM_DP11	10173
MEM_DQ0M_N_WE0_N	Y9	10177	AB5 MEM_DP12	10210
MEM_DQ0M_N_WE1_N	AB9	10214	Y6 MEM_DP13	10174
MEM_DQ0M_N_WE2_N	AB17	10220	AB6 MEM_DP14	10211
MEM_DQ0M_N_WE3_N	Y18	10184	Y7 MEM_DP15	10175
MEM_DQ0M_N	AA9	10195	AB20 MEM_DP16	10223
MEM_DQ05_N	Y10	10178	AB21 MEM_DP17	10224
MEM_DQ06_N	AC17	10237	Y21 MEM_DP18	10186
MEM_DQ07_N	AA18	10204	Y22 MEM_DP19	10187
MEM_CS0_N	AA10	10196	W20 MEM_DP20	10168
MEM_CS1_N	AB10	10215	W22 MEM_DP21	10170
MEM_CS2_N	Y17	10183	V20 MEM_DP22	10160
MEM_CS3_N	AA17	10203	V22 MEM_DP23	10162
MEM_CS4_N	AC16	10236	T20 MEM_DP24	10147
MEM_WE_N	AB8	10213	T22 MEM_DP25	10149
MEM_CAS_N	AC8	10230	R20 MEM_DP26	10139
MEM_RAS_N_OE_N	AC10	10231	R22 MEM_DP27	10141
MEM_ADSC_N	AA16	10202	P20 MEM_DP28	10131
MEM_ADV_N	AB16	10219	P22 MEM_DP29	10133
MEM_CKE	U22	10155	N21 MEM_DP30	10124
RS232_RTS	J20	10099	N23 MEM_DP31	10126
RS232_TX	J21	10100	T2 MEM_DP32	10144
RS232_DTR	J22	10101	R4 MEM_DP33	10138
RS232_DCD	J23	10102	U2 MEM_DP34	10152
RS232_DSR	K20	10107	T4 MEM_DP35	10146
RS232_RX	K21	10108	V4 MEM_DP36	10159
RS232_CTS	K22	10109	W2 MEM_DP37	10165
RS232_RI	K23	10110	W4 MEM_DP38	10167
MS1553_RX_DATA_OUT_B_P	A20	1013	Y3 MEM_DP39	10172
MS1553_RX_DATA_OUT_B_N	B20	1029	AA4 MEM_DP40	10190
MS1553_RX_STROBE_B	D21	1065	AB3 MEM_DP41	10208
MS1553_TX_DATA_IN_B_P	C20	1047	AC4 MEM_DP42	10226
MS1553_TX_DATA_IN_B_N	D20	1064	AA5 MEM_DP43	10191
MS1553_TX_INHIBIT_B	B21	1030	AA6 MEM_DP44	10192
MS1553_RX_DATA_OUT_A_P	D22	1066	AC5 MEM_DP45	10227
MS1553_RX_DATA_OUT_A_N	E22	1073	AC6 MEM_DP46	10228
MS1553_RX_STROBE_A	F23	1081	AA7 MEM_DP47	10193
MS1553_TX_DATA_IN_A_P	F22	1080	AC20 MEM_DP48	10240
MS1553_TX_DATA_IN_A_N	G22	1088	AB23 MEM_DP49	10225
MS1553_TX_INHIBIT_A	E23	1074	AA22 MEM_DP50	10206
FPGA_SPARE0	C5	1032	Y23 MEM_DP51	10188
FPGA_SPARE1	D5	1051	W21 MEM_DP52	10169
FPGA_SPARE2	B19	1028	V23 MEM_DP53	10163
FPGA_SPARE3	C19	1046	V21 MEM_DP54	10161
FPGA_SPARE4	D19	1063	U23 MEM_DP55	10156
FPGA_SPARE5	D23	1067	T21 MEM_DP56	10148
FPGA_SPARE6	E20	1071	T23 MEM_DP57	10150
FPGA_SPARE7	E21	1072	R21 MEM_DP58	10140
FPGA_SPARE8	F20	1072	R23 MEM_DP59	10142
FPGA_SPARE9	F21	1079	P21 MEM_DP60	10134
FPGA_SPARE10	G20	1086	N22 MEM_DP61	10132
FPGA_LED0	G21	1087	M21 MEM_DP62	10125
FPGA_LED1	H21	1093	R3 ROBOCLK_TEST	10119
FPGA_LED2	H22	1094	U4 ROBOCLK_FS	10137
FPGA_LED3	H23	1095	L22 I2C_SCL	10153
			L21 I2C_SDA	10114

PCI_AD0	B4	1015	P4	PCI_AD32	10130
PCI_AD1	B5	1016	P1	PCI_AD33	10127
PCI_AD2	A5	101	P2	PCI_AD34	10128
PCI_AD3	D6	1052	N4	PCI_AD35	10123
PCI_AD4	C6	1033	N1	PCI_AD36	10121
PCI_AD5	B6	1017	N3	PCI_AD37	10122
PCI_AD6	A6	102	M3	PCI_AD38	10118
PCI_AD7	D7	1053	M1	PCI_AD39	10116
PCI_AD8	B7	1018	L1	PCI_AD40	10111
PCI_AD9	D8	1054	M2	PCI_AD41	10117
PCI_AD10	C8	1035	L3	PCI_AD42	10113
PCI_AD11	B8	1019	L2	PCI_AD43	10112
PCI_AD12	D9	1055	K2	PCI_AD44	10104
PCI_AD13	C9	1036	K1	PCI_AD45	10103
PCI_AD14	B9	1020	K4	PCI_AD46	10106
PCI_AD15	A9	103	K3	PCI_AD47	10106
PCI_AD16	D13	1057	J3	PCI_AD48	10105
PCI_AD17	A14	107	J2	PCI_AD49	1097
PCI_AD18	B14	1023	H1	PCI_AD50	1098
PCI_AD19	C14	1041	J4	PCI_AD51	1098
PCI_AD20	D14	1058	H3	PCI_AD52	1091
PCI_AD21	A15	108	H2	PCI_AD53	1090
PCI_AD22	B15	1024	G1	PCI_AD54	1082
PCI_AD23	C15	1042	H4	PCI_AD55	1092
PCI_AD24	B16	1025	G3	PCI_AD56	1084
PCI_AD25	C16	1043	G2	PCI_AD57	1083
PCI_AD26	D16	1060	F1	PCI_AD58	1075
PCI_AD27	A17	1010	G4	PCI_AD59	1085
PCI_AD28	B17	1026	F4	PCI_AD60	1077
PCI_AD29	C17	1044	F3	PCI_AD61	1076
PCI_AD30	D17	1061	E3	PCI_AD62	1069
PCI_AD31	A18	1011	E2	PCI_AD63	1068
PCI_PAR	C10	1037	P3	PCI_PAR64	10129
PCI_CBE0_N	C7	1034	D1	PCI_CBE4_N	1048
PCI_CBE1_N	D10	1056	E4	PCI_CBE5_N	1070
PCI_CBE2_N	C13	1040	D2	PCI_CBE6_N	1049
PCI_CBE3_N	A16	109	C4	PCI_CBE7_N	1031
PCI_PERR_N	A10	104	B3	PCI_REQ64_N	1014
PCI_TRDY_N	A11	105	B3	PCI_ACK64_N	1050
PCI_FRAME_N	A12	106			
PCI_SERR_N	B10	1021	A19	PCI_MB6EN	1012
PCI_DEVSL_N	B11	1022			
PCI_STOP_N	C11	1038	B18	PCI_REQ_N	1027
PCI_IRDY_N	C12	1039	C18	PCI_GNT_N	1045
PCI_IDSEL	D15	1059			
PCI_INTA_N	R2	10136			
PCI_RST_N	D18	1062	R1	CLK_16MHZ_1553	10135
CLKB	A13				
CLKA	B13				
HCLK	AB13				

FPGA CORE VOLTAGE REGULATOR



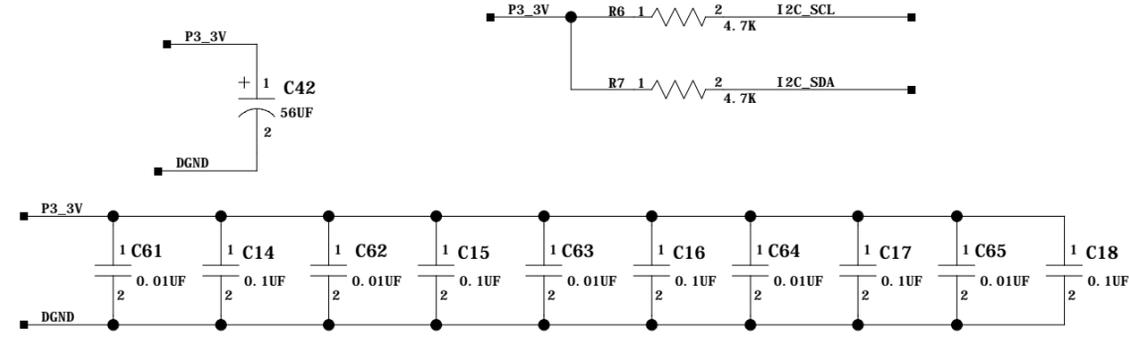
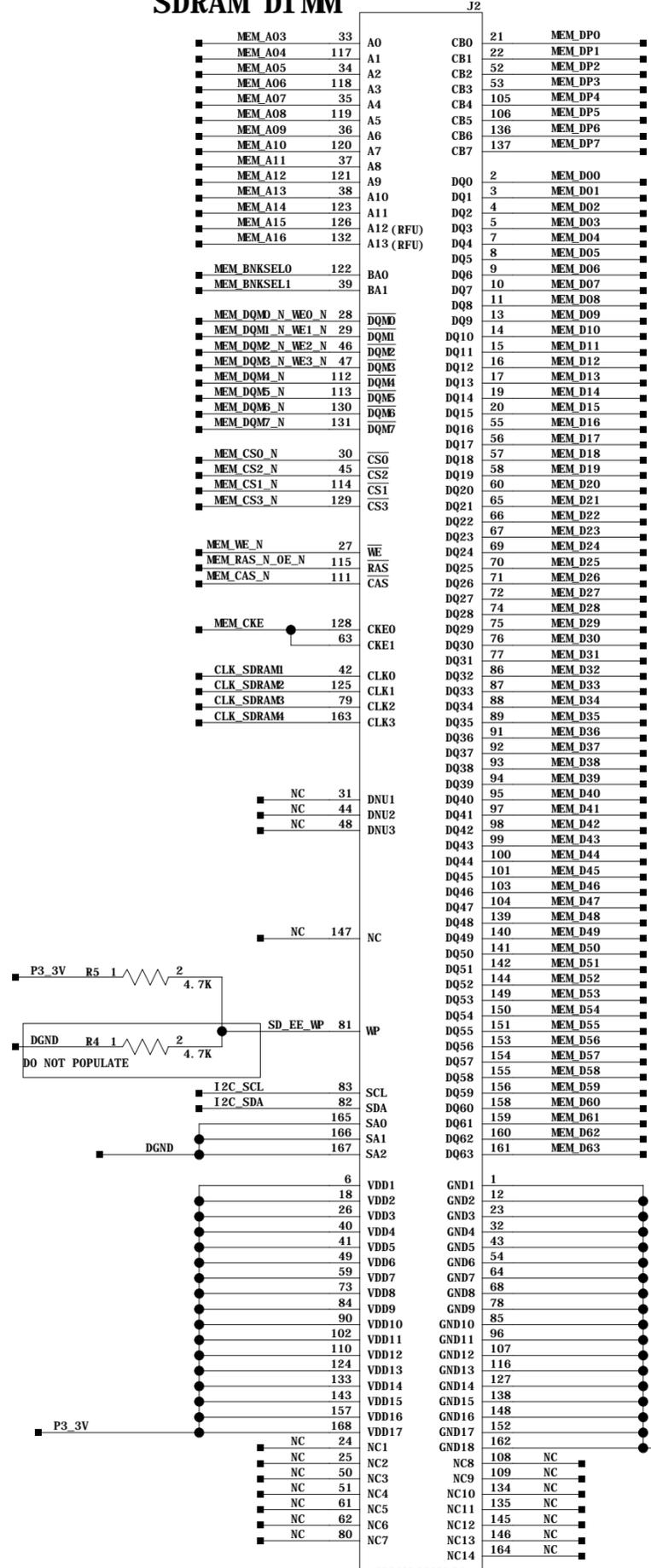
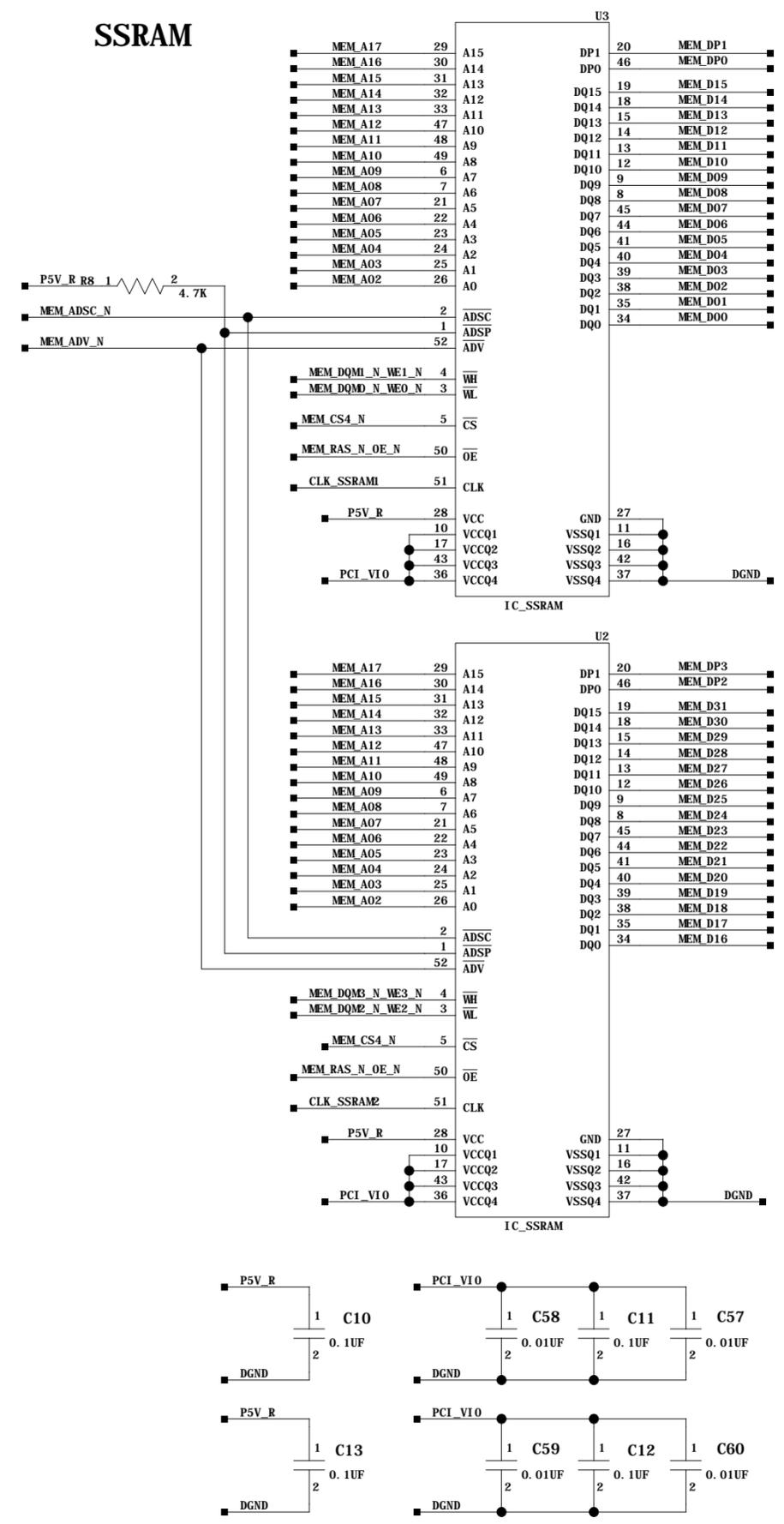
PROJECT:	ACTEL CORE PCI DEVELOPMENT BOARD		
PART NO:	9210-01-03		
Sheet:	2	DATE:	7/22/02
Rev.	1.00	of:	6
		DRAWN BY:	R. SCHOENBERG

Last edit: 7-5-2002_16:23

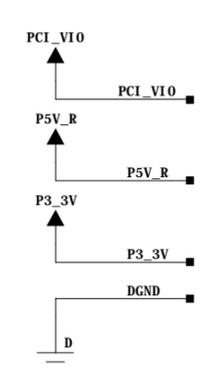
THIS DRAWING AND SPECIFICATION, HEREIN, ARE THE PROPERTY OF ACTEL CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION.

SDRAM DIMM

SSRAM



NOTE: DIMM MUST BE REMOVED FOR OPERATION IN 5V PCI SYSTEM





ACTEL
PROTOCOL DESIGN SERVICES

PROJECT: ACTEL CORE PCI DEVELOPMENT BOARD	
PART NO: 9210-01-03	
Sheet: 3	DATE: 7/22/02
Rev. 1.00	of: 6
DRAWN BY: R. SCHOENBERG	

Last edit: 9-11-2002_10:52

1

2

3

4

1

2

3

4

THIS DRAWING AND SPECIFICATION, HEREIN, ARE THE PROPERTY OF ACTEL CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION.

CLOCK PLL AND DRIVER

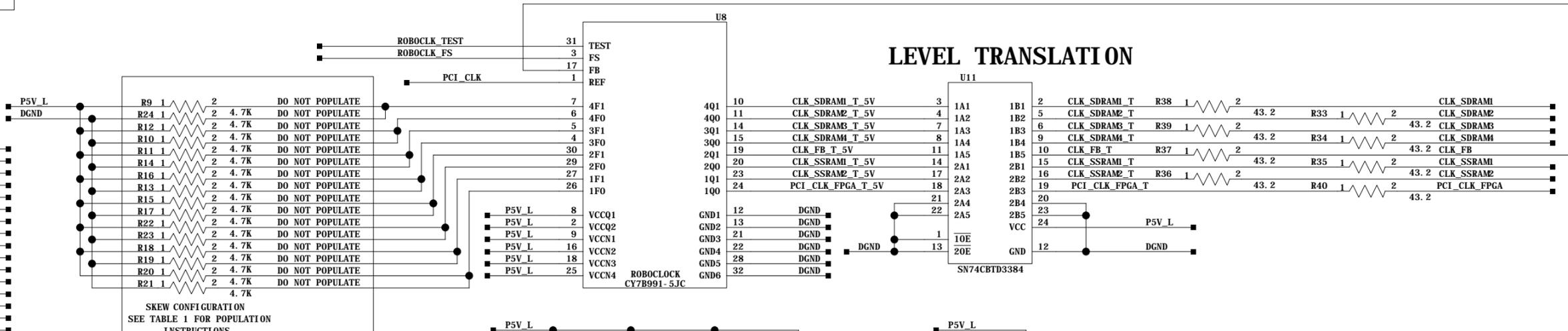
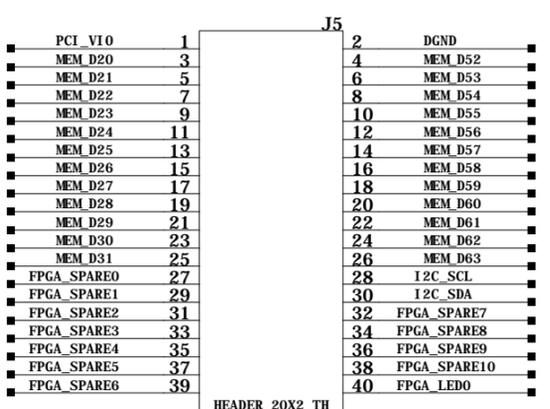
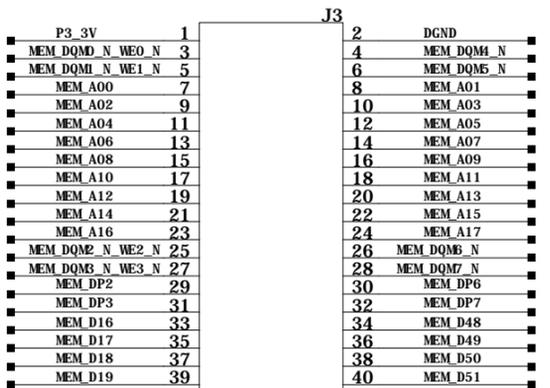
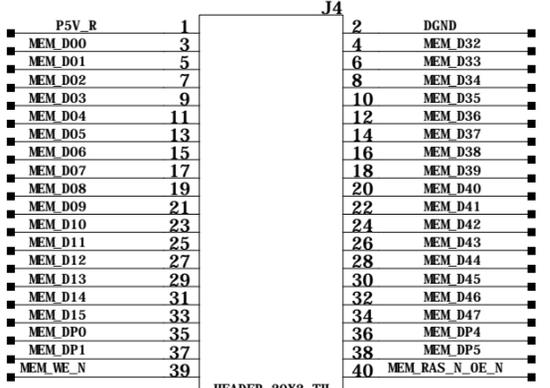
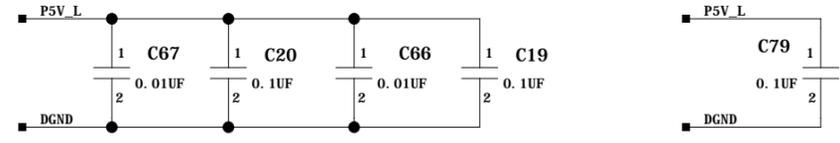


Table 1. Programmable Skew Configurations

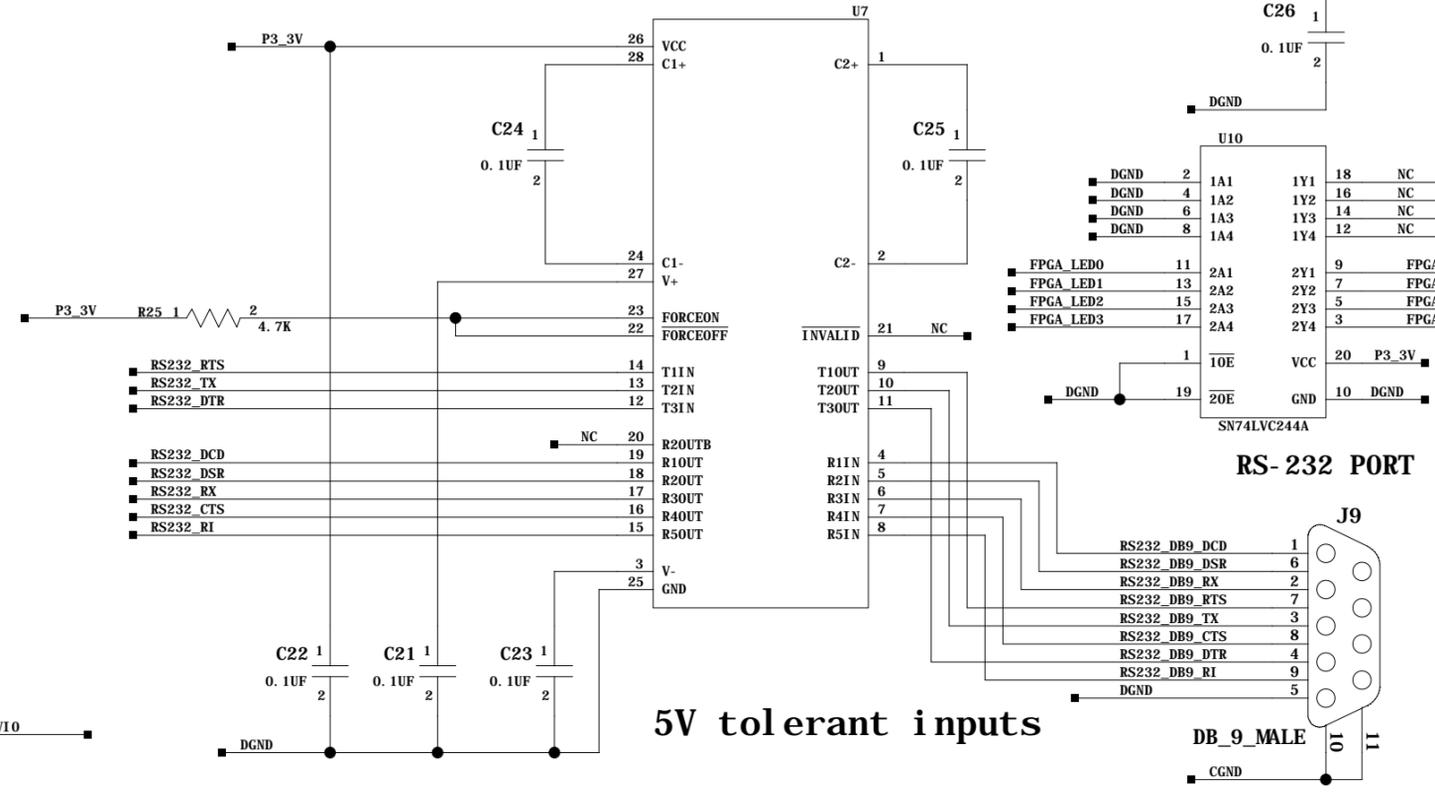
Function Selects	Output Functions			
1F1, 2F1, 3F1, 4F1	1F0, 2F0, 3F0, 4F0	1Q0, 1Q1, 2Q0, 2Q1	3Q0, 3Q1	4Q0, 4Q1
LOW	LOW	-4t _U	Divide by 2	Divide by 2
LOW	MID	-3t _U	-6t _U	-6t _U
LOW	HIGH	-2t _U	-4t _U	-4t _U
MID	LOW	-1t _U	-2t _U	-2t _U
MID	MID	0t _U	0t _U	0t _U
MID	HIGH	+1t _U	+2t _U	+2t _U
HIGH	LOW	+2t _U	+4t _U	+4t _U
HIGH	MID	+3t _U	+6t _U	+6t _U
HIGH	HIGH	+4t _U	Divide by 4	Inverted

- 1F0 -> (R38 & R39) Low: Install R39 - Mid: Install neither - High: Install R38
- 1F1 -> (R36 & R37) Low: Install R37 - Mid: Install neither - High: Install R36
- 2F0 -> (R34 & R35) Low: Install R35 - Mid: Install neither - High: Install R34
- 2F1 -> (R32 & R33) Low: Install R33 - Mid: Install neither - High: Install R32
- 3F0 -> (R30 & R31) Low: Install R31 - Mid: Install neither - High: Install R30
- 3F1 -> (R28 & R29) Low: Install R29 - Mid: Install neither - High: Install R28
- 4F0 -> (R26 & R27) Low: Install R27 - Mid: Install neither - High: Install R26
- 4F1 -> (R24 & R25) Low: Install R25 - Mid: Install neither - High: Install R24

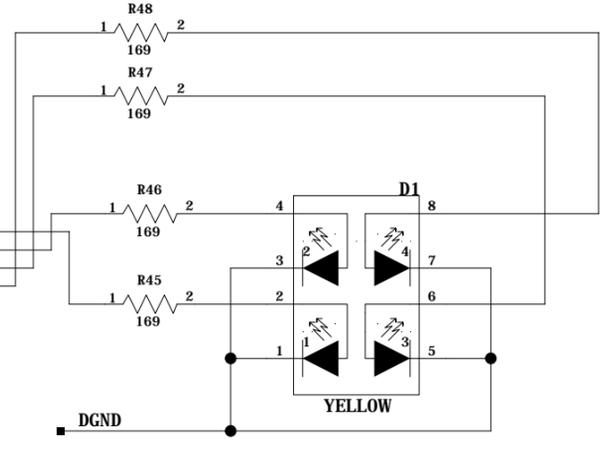
LEVEL TRANSLATION



RS-232 INTERFACE



GENERAL PURPOSE LEDs



5V tolerant inputs



PROJECT:	ACTEL CORE PCI DEVELOPMENT BOARD		
PART NO:	9210-01-03		
Sheet:	4	DATE:	7/22/02
Rev.	1.00	of:	6
		DRAWN BY:	R. SCHOENBERG

Last edit: 7-22-2002_11:03

THIS DRAWING AND SPECIFICATION, HEREIN, ARE THE PROPERTY OF ACTEL CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION.

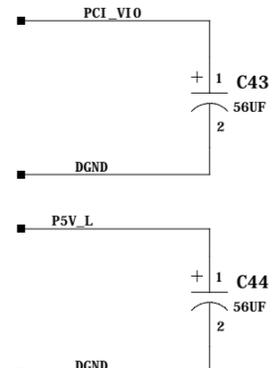
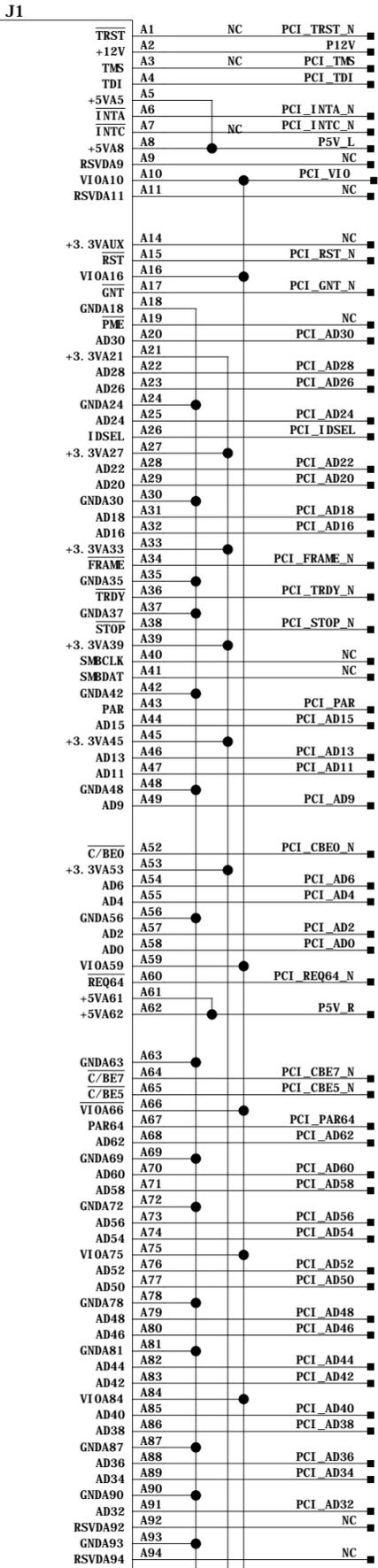
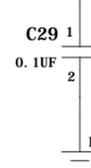
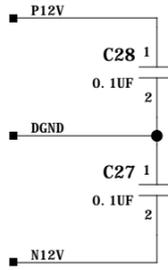
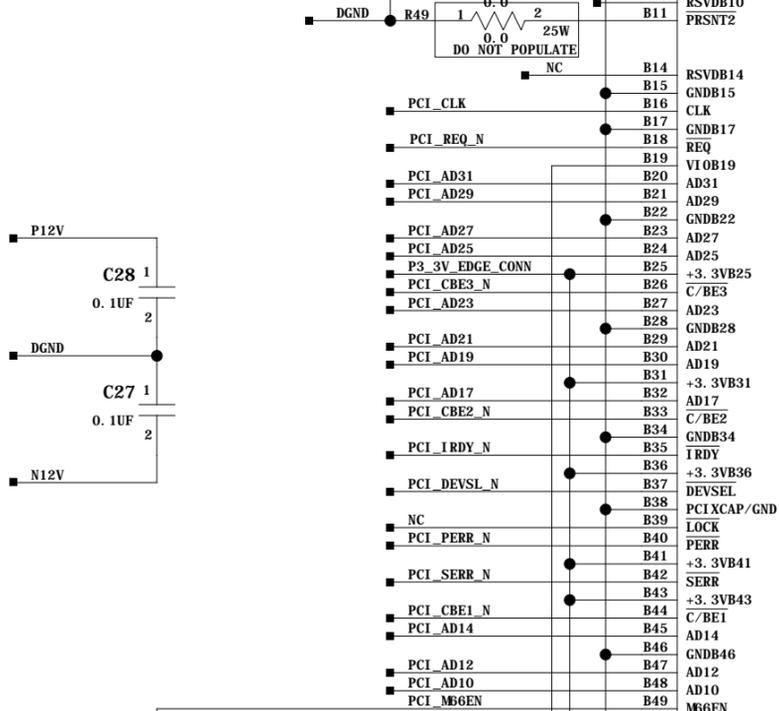
64 bit PCI edge connector

A

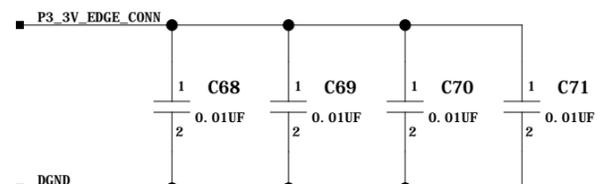
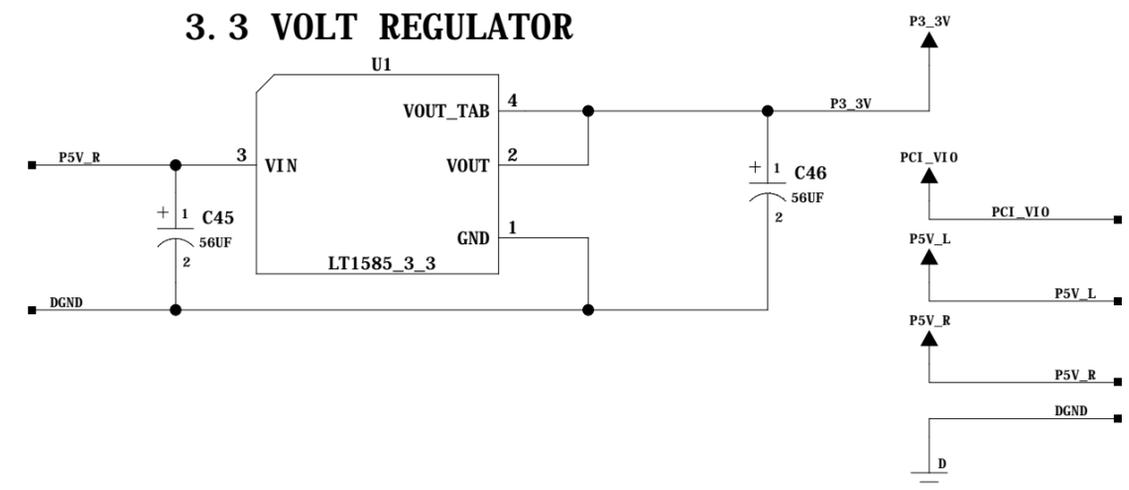
B

C

D



3.3 VOLT REGULATOR



PROJECT:	ACTEL CORE PCI DEVELOPMENT BOARD		
PART NO:	9210-01-03		
Sheet:	5	DATE:	7/22/02
Rev. 1.00	of: 6	DRAWN BY:	R. SCHOENBERG

Last edit: 7-22-2002_11:03

A

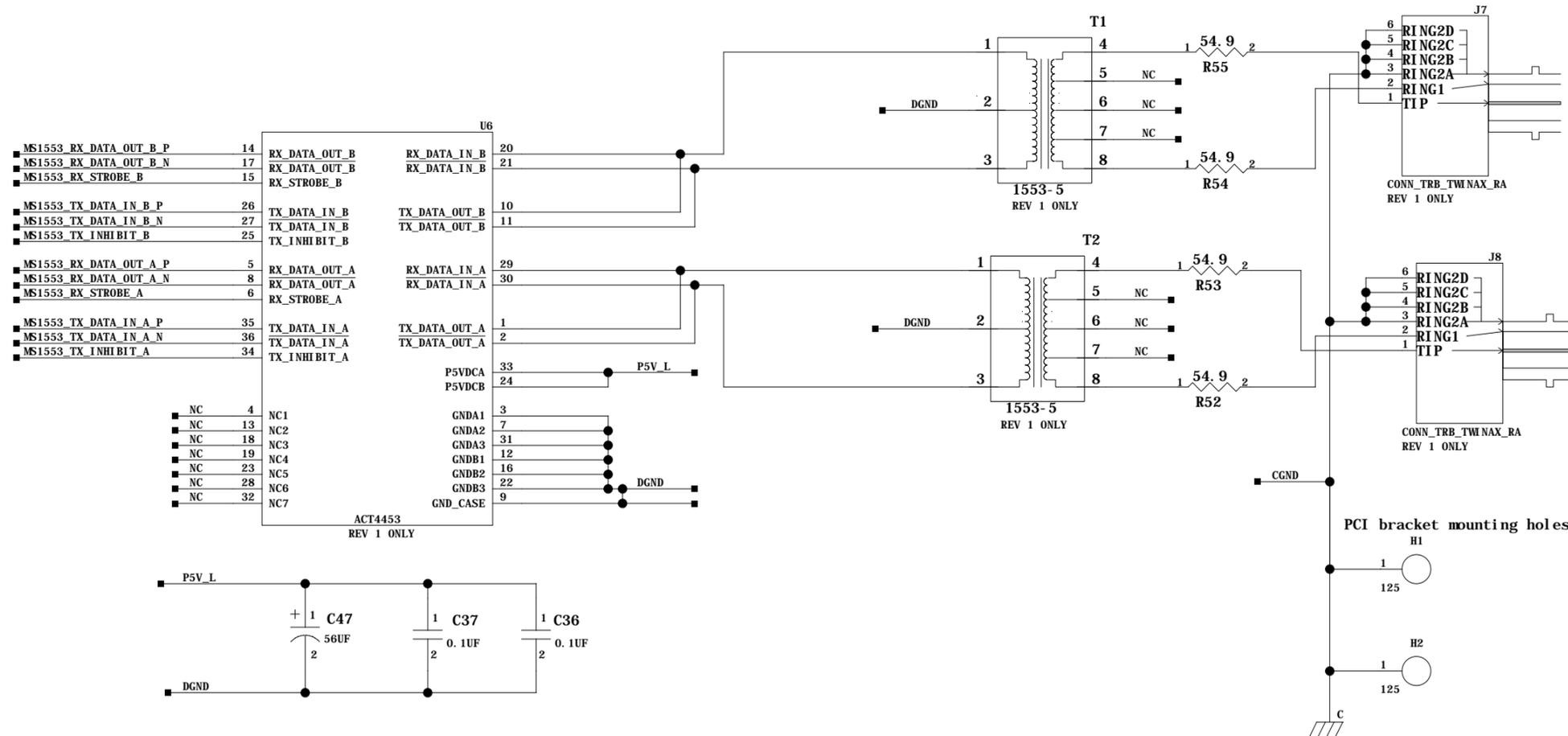
B

C

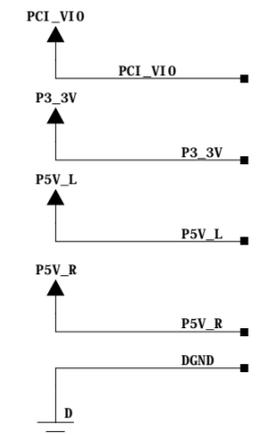
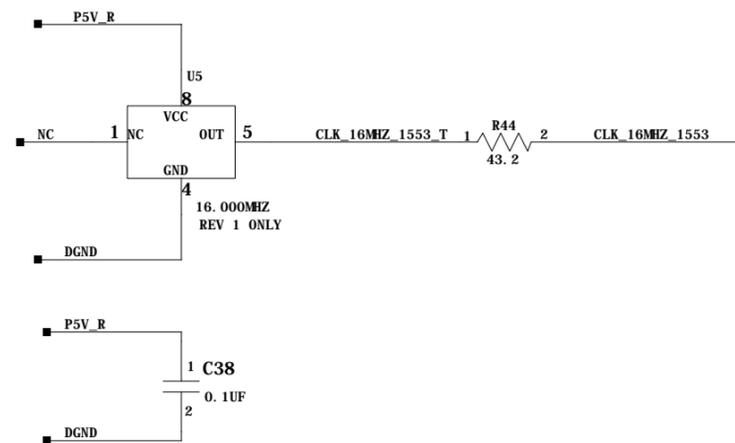
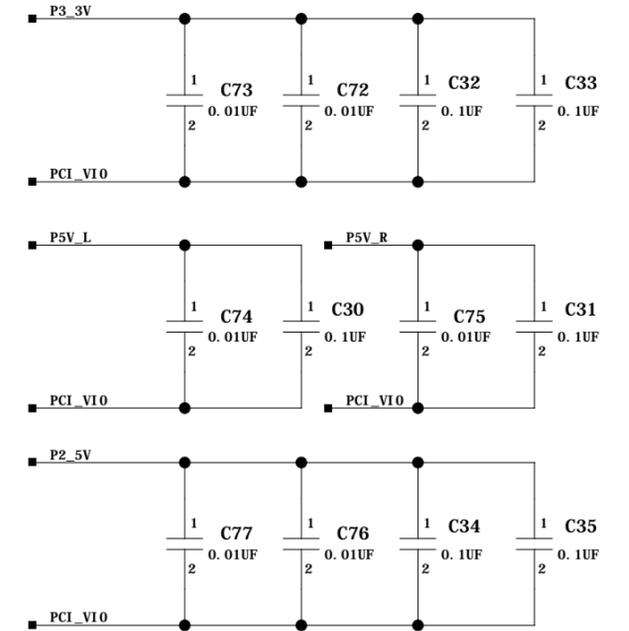
D

THIS DRAWING AND SPECIFICATION, HEREIN, ARE THE PROPERTY OF ACTEL CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION.

Configured for Direct coupling only.



DECOUPLING FOR SPLIT VOLTAGE PLANE.



PROJECT: ACTEL CORE PCI DEVELOPMENT BOARD
 PART NO: 9210-01-03
 Sheet: 6 of: 6 DATE: 7/22/02
 DRAWN BY: R. SCHOENBERG

Last edit: 9-11-2002_10:52