CorePCI 5.3 Release Notes

This document describes the new features and enhancements of the Core PCI 5.3 release. It also contains information about sytem requirements, new supported families, implementations, and known limitations and workarounds.

System Requirements

Solaris

- Solaris 2.6 (last version supporting this platform)
- Solaris 2.7
- Solaris 2.8

HP

- HP-UX 10.2
- HP-UX 11.0

PC

- Windows 98 Second Edition
- Windows NT 4.0 SP6
- Windows 2000 SP1 or SP2
- Windows XP 5.1

New Features

- ProASIC^{PLUS} family support
- Axcelerator family support
- Source code supports with Synopsys Design Compiler
- Release Directory Structure enhanced to support multiple families and devices

Supported Families

- A54SXP
- A54SXA
- RT54SXS
- ProASIC
- ProASIC PLUS
- Axcelerator

Supported Tools Flows

Use Libero 2.2 or Designer R1-2002 with the CorePCI 5.3 release.

Install Instructions

Copy the complete contents of the CD to the hard disk and unzip the files. This will produce a top-level directory CorePCI_5.3, as shown in Figure 1.

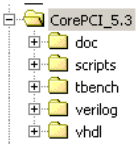

Figure 1. CorePCI 5.3 Directory Structure

For electronic delivery (email or ftp), copy the supplied zip files to the hard disk and unzip them.

Refer to the CorePCI 5.3 User's Guide (doc/usersguide.pdf) after installation for details on how to simulate, synthesize and run place-and-route for this core.

Documentation

The doc directory in the release contains a copy of the CorePCI 5.3 datasheet and *Users Guide*. The datasheet describes the core functionality and the user's guide gives a step-by-step guide on how to simulate, synthesize and place-and-route this core.

For updates and additional information about the software, devices, and hardware, please visit the Intellectual Property pages on the Actel web site at http://www.actel.com.

Implementations Contained in this Release

You can implement the CorePCI Target, Master, Target+DMA and Target+Master cores on the six Actel families listed above in either 32- or 64-bit versions with either 33 or 66 MHz clock rates (the SX-A or Axcelerator family is required for 66 MHz clock rates). You can target the PCI cores to multiple device size and package combinations in each of these families. Finally, Actel supplies VHDL and Verilog source code as well as supports various synthesis tools. In total, there are over 1,000 possible implementation variations.

The CorePCI 5.3 release contains example runs for various cores using a particular tool flow and device package combinations. This release contains eighteen example run directories (Table 1-1).

Table 1-1. Sample Run Directories

Core	Size	MHz	Language	Flow	Family	Device	Speed	Package
Master	32	33	VHDL	Synplicity	AX	AX500	Std	FG484
Master	64	66	VHDL	Synplicity	AX	AX1000	-1	FG484
Target	32	33	VHDL	Synopsys	SXA	A54SX16A	-3	PQ208
Target	32	33	Verilog	Synplicity	SXA	A54SX16P	-3	PQ208
Target	32	33	VHDL	Synplicity	RTSXS	RT54SX32S	-1	CQ208
Target	32	33	VHDL	Synplicity	APA	APA750	Std	BG456

Table 1-1. Sample Run Directories (Continued)

Core	Size	MHz	Language	Flow	Family	Device	Speed	Package
Target	32	33	VHDL	Synplicity	AX	AX500	Std	FG484
Target	64	66	VHDL	Synplicity	AX	AX1000	-1	FG484
Target+DMA	32	33	VHDL	Synopsys	ProASIC	A500K130	Std	BG456
Target+DMA	32	33	Verilog	Synplicity	ProASIC	A500K130	Std	BG456
Target+DMA	32	33	VHDL	Synplicity	AX	AX500	Std	FG484
Target+DMA	64	66	Verilog	Synopsys	SXA	A54SX32A	-3	BG329
Target+DMA	64	66	VHDL	Synplicity	SXA	A54SX32A	-3	BG329
Target+DMA	64	66	VHDL	Synplicity	AX	AX1000	-1	FG484
Target+Master	32	33	Verilog	Synopsys	APA	APA750	Std	BG456
Target+Master	32	33	VHDL	Synplicity	APA	APA750	Std	BG456
Target+Master	32	33	VHDL	Synplicity	AX	AX500	Std	FG484
Target+Master	64	66	VHDL	Synplicity	AX	AX1000	-1	FG484

You can implement the cores in any of the devices listed in the datasheet. For instance, the Target 32-bit 33MHz core version can be implemented using Verilog with Synplicity in a SX72A/PQ208. You can then re-layout the SX16A/PQ208 database, changing the device to a SX72A. If you used a SX72A/FG484 device, you would need to create a new pin file. Please check with the Actel IP support (ip_support@actel.com) to see whether the pin file for a specific combination has been created since this release.

Discontinued Features and Devices

No features have been discontinued in the 5.3 release.

Known Limitations and Workarounds

The following problems and limitations have been found in the 5.3 release.

General

The 5.3 release does not support the RT54SX72S device.

All Cores

- The PIPE_FULL_CNT input only supports values 000 to 110, it must not be set to “111”.
- When in 64 bit mode the core does not support 32 bit operations. If a 32 bit cycle is carried out then the core will treat it as 64 bit operation even though no data is provided on the upper 32 data bits. This implies that a 64 bit core should only be used in systems that are known to operate only in 64 bit mode.

Target Cores

No known problems.

Master Cores

- The core only de-asserts REQn for a single clock cycle if there are pending PCI transfers. This does not cause a problem in most PCI systems. The PCI specification requires that REQn is de-asserted for two clock cycles. Please contact Actel support for details on how to correct this problem.
- If an arbiter grants the bus to core and then removes the GNT before the core asserts FRAME (allowed by the PCI specification) then the core may still start a bus transfer. This could lead to bus contention. Please contact Actel support for details on how to correct this problem.
- The REQn/GNTn circuitry does not support bus parking. If the arbiter parks the bus on the core and the core then requests the bus, the PCI transfer may fail. The Actel CorePCI arbiter does not park the bus. Hence, the problem only occurs when a third-party arbiter is used. Please contact Actel support for the details on how to correct this problem.