Core1553BBC Release Notes

This document accompanies the first production release for Core1553BBC. It describes new features and enhancements and contains information about system requirements, new supported families, implementations, and known limitations and workarounds.

Delivery Types

The Core1553BBC is supplied in three variations:

- Evaluation: Allows simulation of the Core1553BBC core using ModelSim
- Netlist: Complete core, enables integration into your design
- RTL: Complete core with VHDL and Verilog source code

The CD is marked with Evaluation, Netlist or RTL.

Features

- MIL-STD-1553B Compliant Remote Terminal
- Fully Automated Message Scheduling

Supported Families

- Axcelerator
- RTAX-S
- ProASIC^{PLUS}
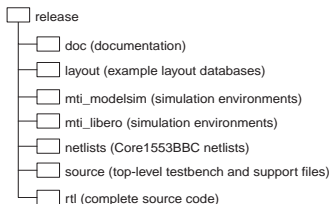- SX-A
- RT54SX-S
- ACT3
- MX

Supported Tool Flows

Use Libero IDE v2.3 Service Pack 2 (SP 2) or Designer R1-2003 Service Pack 2 or later with the Core1553BBC release.

Simulation for the evaluation and netlist versions require Libero IDE v2.3 Service Pack 2 OR a full version of Modelsim 5.7a or later.

Install Instructions

Copy the complete contents of the CD to the hard disk and unzip the files. This will produce a top-level directory Core1553BBC, as shown in Figure 1.

```
release
    doc (documentation)
    layout (example layout databases)
    mti_modelsim (simulation environments)
    mti_libero (simulation environments)
    netlists (Core1553BBC netlists)
    source (top-level testbench and support files)
    rtl (complete source code)
```

Figure 1. Core1553BBC Directory Structure

For electronic delivery (email or ftp), copy the supplied zip files to the hard disk and unzip them.

All the above directories are provided with the RTL version. The netlist version includes all directories apart from the *rtl* directory. The evaluation version only includes the *sim* and *doc* directories.

Refer to the *Core1553BBC User's Guide* (*doc/Core1553BBC_UG.pdf*) after installation for details on how to simulate, synthesize and run place-and-route for this core.

Documentation

The *doc* directory in the release contains a copy of the *CORE1553BBC Datasheet* and *Core1553BBC User Guide*. The datasheet describes the core functionality

and the user guide gives step-by-step instructions on how to simulate, synthesize and place-and-route this core as well as implementation examples.

For updates and additional information about the software, devices, and hardware, please visit the Intellectual Property pages on the Actel web site at http://www.actel.com.

Discontinued Features and Devices

No features have been discontinued in the Core1553BBC release.

Known Limitations and Workarounds

The following problems and limitations have been found in the Core1553BBC release.

Simulation

Two sets of simulation libraries are supplied. The first, mti_libero, are compiled to run with the version of Modelsim supplied in the Libero IDE v2.3 environment. The second, mti_modelsim, are compiled to run with the full version of ModelSim. These libraries will run on ModelSim 5.7a or later.

The verification testbenches only work on systems with a VHDL ModelSim license. For systems with a Verilog ModelSim license you can use only the customizable Verilog testbench.