Core1553BRT DevKit

Quick Start Guide

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Core1553BRT DevKit

Quick Start Guide

Actel

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Introduction

The 1553BRT DevKit is a starter kit for working with Actel Core1553BRT products and is intended to help you get your 1553BRT product to market faster. The kit consists of a 1553BRT board, example design, and software drivers to exercise the board.

Core1553BRT DevKit Documentation

The Core1553BRT DevKit includes a printed and online version of the *Core1553BRT DevKit Quick Start Guide,* which contains information and procedures for using the Core1553BRT. The guide is in PDF format on the CD-ROM in the "\doc" directory. To view the online manual, you must have Adobe® Acrobat Reader® installed. Actel provides Reader on the Designer CD-ROM.

Core1553BRT DevKit Quick Start Guide

The Core 1553BRT DevKit is a starter kit for working with Actel Core1553BRT products and is intended to help you get your 1553BRT product to market faster. Intended uses are as follows:

1. To provide a hardware platform for software driver development specific to your system.

2. To provide hardware functionality to complement the simulation test bench.

3. To provide the ability to test modifications and enhancements made to the Core1553BRT core (IP and additional devices sold separately).

Overview

The 1553B RT development kit contains an Actel Core1553BRT Demonstration Board, reference design and software to support the card.

The board implements a PCI to 1553B remote terminal function, the block diagram is shown in Figure 1-1.
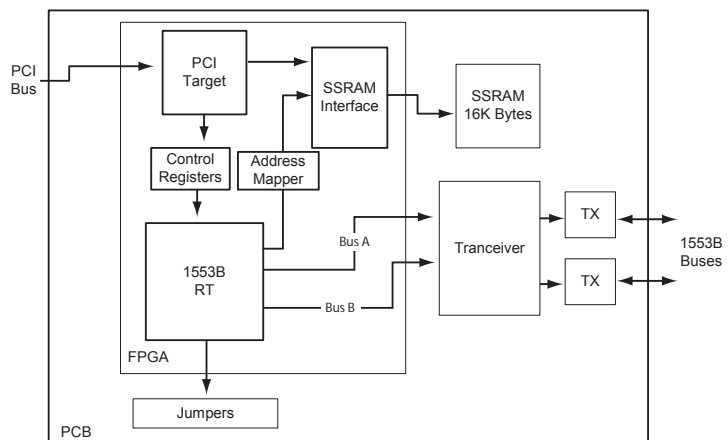
Figure 1-1. PCI to 1553B Remote Terminal Function Block Diagram

The FPGA contains five main blocks: the PCI Target, Control registers, 1553B RT, address mapper and the SSRAM interface.

The PCI target is a standard implementation of the Actel CorePCI Target IP core (version 5.3). The Control registers control the operating mode inputs on the 1553BRT core (see "Using the Remote Terminal" on page 17). The address mapper allows the RT to operate with an enhanced memory map. Finally, the SSRAM interface allows both the CorePCI and Core1553BRT to access the same external memory.

What's Included

The following is included with your new Core1553BRT Development Kit.

Core1553BRT Demo Board

- 1553BRT card
- Socketed 54SX32A device implementing the Core1553BRT and CorePCI function
- 1533B transceivers and transformers wired for direct coupling
- Header strips for backend observation
- Silicon Explorer connector for viewing internal nodes

CD with Software Drivers and Design Files

- Actel 1553BRT Demo application software for either Win98, NT, XP, or Windows 2000 systems
- VHDL source code for the chip-level wrapper, refer to Appendix A for more information

IP Cores (CorePCI and Core1553BRT) are sold separately.

Software Installation

Note: **You must install your software before you install the PCI Demo Card.**

To install the 1553BRT demonstration driver and software:

1. **Log in as Administrator.**

2. **Insert the Core1553BRT software CD; installation starts automatically.** Follow the instructions on the screen. If installation does not start automatically, run

   ```
   <CDdrive>:\DEMO software\Setup.EXE
   ```

Installing the 1553BRT Demo Card

Before installing the 1553BRT demo card, **Make sure that the RT Address jumpers are fitted correctly ("RT Address Jumpers" on page 25)**. You can also set the RT address using the supplied software.

> **WARNING: An SDRAM memory must not be fitted to the SDRAM DIMM socket.**

To install the hardware:

1. **Turn the computer power off.**

2. **Install PCI Development Card using static-safe procedures.**

3. **Boot your PC and login as Administrator if required.** When/if the New Hardware Wizard pops up click "Next" and then select "Display list of the known drivers". Click "Next" again.

4. **Select "Show compatible hardware drivers".**

5. **Select "Actel Development Board".** Click "Next" and "Next" again.

6. **Click "Finish".** Installation is now complete.

Refer to "Core1553BRT DevKit Contents" on page 37 for instructions on how to remove the 1553B demo card.

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Using the Core1553BRT Demo Card

The 1553BRT development PCB is supplied with a basic Windows utility that enables you to peek, poke, fill, and display the PCI/RT memory.

Exercising the 1553BRT Demo Card

This development kit provides you a demo application to exercise basic PCI access to the 1553BRT memory. The demo application allows basic reads and writes to the SSRAM.

Run Demo Software

To execute the demo application, select the ActelPCI program from the Start menu (from the Start menu, select Programs -> Actel -> ActelPCI).

Demo Application Operations Window

The Operations window of the demo application is shown in Figure 2-1.
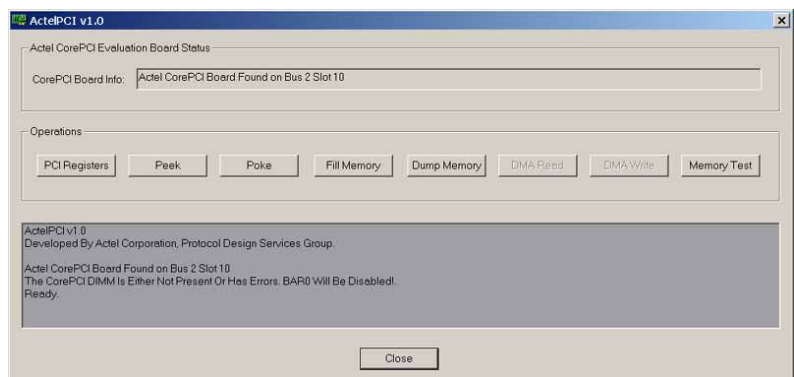
Figure 2-1. Demo Program Operations Window

PCI Configuration Space

To access the PCI configuration space click the PCI Registers button in the Operations window (Figure 2-1). The PCI Configuration Register dialog box appears, as shown in Figure 2-2. Click OK to continue.
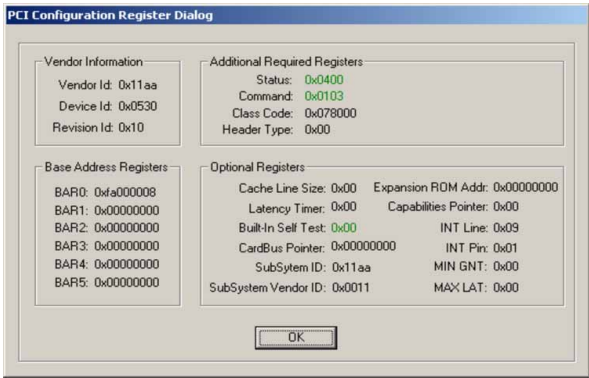
Figure 2-2. PCI Configuration Register Dialog

BAR0 is used for the Core1553BRT memory space. If you click the Status or Command registers the Demo displays the register settings.

Memory Test

Click the Memory Test button in the Operations window to perform a memory test (Figure 2-1). The Memory Test button opens a dialog box (Figure 2-3). Set the Memory Device/Range to BAR0.

Figure 2-3. Memory Test Dialog Box

The memory test fails at addresses 4000 and upwards since these locations are used by the control registers and do not return what was written.

Warning: When you run the memory test it corrupts the 1553B registers. You must set them back to their correct values after you run the memory test. For more information, see "Setting Registers to Defaults" on page 34.

Poke

To write a specific value to a specified location inside the memory, click the Poke button in the in the Operations window (Figure 2-1). This displays the Memory Value Dialog box, as shown in Figure 2-4.
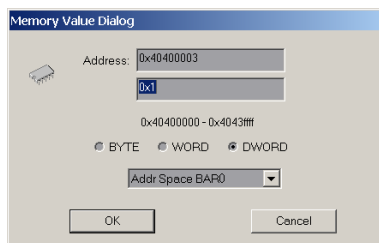
Figure 2-4. Memory Value Dialog Box - Poke

Provide the addresses, value, and the address space, then click OK to perform a memory write.

Peek

Click the Peek button in the Operations window to read a specified memory location (Figure 2-1). The Memory Value Dialog box appears.
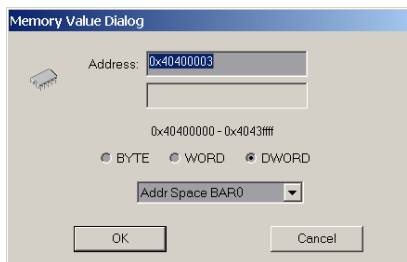
Figure 2-5. Memory Value Dialog Box - Peek

Provide the read address and specify the address space, then click OK. The message box appears to report the data for all the requested addresses.

Memory Fill

Use the Memory Fill button in the Operations window to write a specified value to a consecutive memory location. Click the Memory Fill button to open the Memory Fill Dialog box (Figure 2-6).
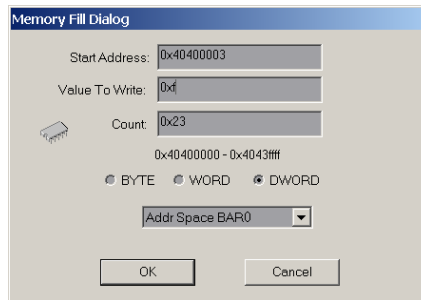
Figure 2-6. Memory Fill Dialog Box

Provide a starting address, location numbers, value and address space, and then click OK to write the specified value.

Memory Dump

Click the Memory Dump button in the Operations window to dump consecutive memory locations. The Memory Dialog box appears (Figure 2-7).
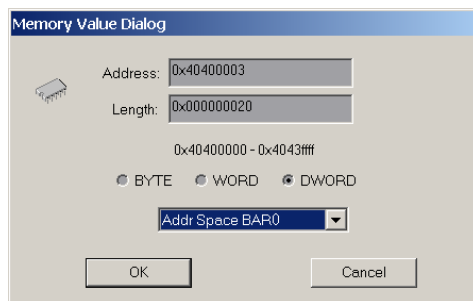
Figure 2-7. Memory Value Dialog Box - Memory Dump

To read out the serial memory (dump memory), provide the starting address, the length, and the address space, then click OK.

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Using the Remote Terminal

The Core1553BRT DevKit can be used to test modifications you made to the core or can be used to test custom backends using a daughter card strategy. For either case, a new device can be programmed and inserted into the socket.

For the daughter card strategy, it is essential to ensure that the synchronous SSRAMs are configured so that they will not drive data. The simplest mechanism for doing this is to ensure that the signal "RAM_CEn" be held high by the macro. A daughter card can then be connected through the backend header pins and will not be affected by the SSRAM devices.

Board Description

The 1553BRT demo board is illustrated in Figure 3-1. The main components on the board are the socketed FPGA 1553B transceivers and transformers, the backend SSRAM, the Silicon Explorer connector, and the backend header strips. The RS-232 translator and SDRAM DIMM interface are not used in the 1553BRT design. The board includes the 64-bit PCI extension; however, the extension is not used.
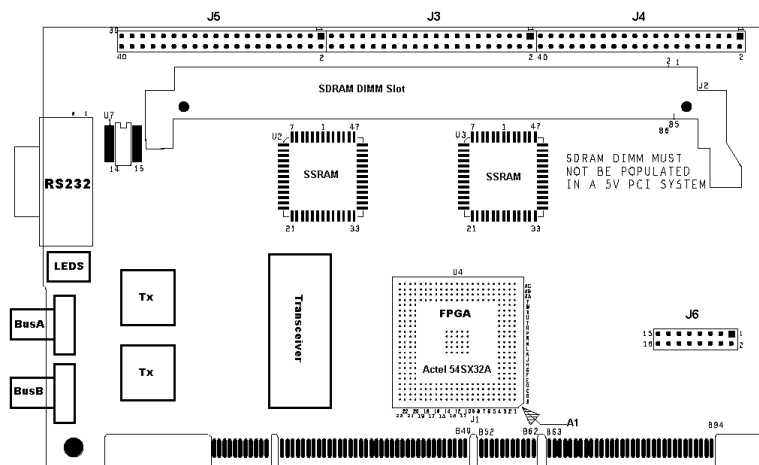
Figure 3-1. 1553BRT Demo Board

The following table describes the 1553BRT demo board components.

Table 3-1. 1553BRT Demo Board Legend

J2	SDRAM DIMM INTERFACE - DO NOT FIT AN SDRAM!
J3	Header strip
J4	Header strip
J5	Header strip
U4	Actel 54SX32A FPGA
U2	SSRAM
U3	SSRAM
U6	1553B Transceiver
T1/T2	1553B Transformers
U7	RS-232 Transceiver
J6	Silicon Explorer Connection

1553BRT Demo Card Back Panel Connections

Four LEDs on the 1553BRT demo card are shown in Figure 3-2.
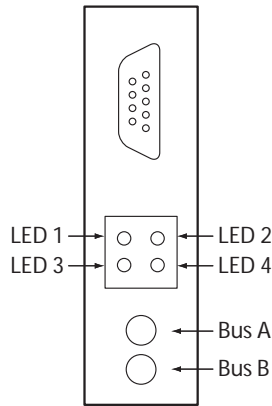
Figure 3-2. LEDs on the PCI Demo Card

See Table 3-2 for a summary.

Table 3-2. LED Function Summary

LED	Function	Description
1	ACTIVE	Indicates that the 1553BRT is responding to a 1553B message
2	AUTOLOOP	Indicates that the AUTOLOOP function is enabled (bit 17 of the control register)
3	Memory fail	Indicates that the 1553BRT core failed to access the memory
4	RT address error	Indicates that the RT address and parity bit are set incorrectly. This represents the RTADDER output from the Core1553BRT

Signals and Connections

The tables on the following pages provide connection information among the FPGA, the 1553BRT bus, and the backend header strips. When applicable, SSRAM signals are included.

This is the PCI Bus Signal Connections table.

Table 3-3. PCI Bus Signal Connection Table

PCI Signal	SX32A Pin Number	PCI Signal	SX32A Pin Number
CLK	AB13	AD23	C15
RST	D18	AD24	B16
AD0	B4	AD25	C16
AD1	B5	AD26	D16
AD2	A5	AD27	A17
AD3	D6	AD28	B17
AD4	C6	AD29	C17
AD5	B6	AD30	D17
AD6	A6	AD31	A18
AD7	D7	CBE0	C7
AD8	B7	CBE1	D10
AD9	D8	CBE2	C13
AD10	C8	CBE3	A16
AD11	B8	DEVSELN	B11
AD12	D9	FRAMEN	A12
AD13	C9	GNTN	C18

Table 3-3. PCI Bus Signal Connection Table (Continued)

PCI Signal	SX32A Pin Number	PCI Signal	SX32A Pin Number
AD14	B9	IDSEL	D15
AD15	A9	INTAN	R2
AD16	D13	IRDYN	C12
AD17	A14	PAR	C10
AD18	B14	PERRN	A10
AD19	C14	REQN	B18
AD20	D14	SERRN	B10
AD21	A15	STOPN	C11
AD22	B15	TRDYN	A11

Table 3-4. Header Strip J3

Header Pin	Signal	FPGA Pin	Header Pin	Signal	FPGA Pin
1	P3_3V	na	2	GND	na
3	Unused	Y9	4	Unused	AA9
5	Unused	AB9	6	Unused	Y10
7	Unused	U20	8	Unused	M22
9	Unused	Y16	10	Unused	Y11
11	Unused	AA11	12	Unused	AC11
13	Unused	AA12	14	Unused	AB12
15	Unused	AC12	16	Unused	AA13
17	Unused	AC13	18	Unused	Y14
19	Unused	AA14	20	Unused	AB14
21	Unused	AA15	22	Unused	AB15
23	Unused	AB18	24	Unused	AC18
25	Unused	AB17	26	Unused	AC17
27	Unused	Y18	28	Unused	AA18
29	Unused	Y19	30	Unused	AA18
31	Unused	AB19	32	Unused	AA19
33	Unused	AB20	34	Unused	AC19
35	Unused	AB21	36	Unused	AB23
37	Unused	Y21	38	Unused	AA22
39	Unused	Y22	40	Unused	Y23

Table 3-5. Header Strip J4 (RT Address Setting)

Header Pin	Signal	FPGA Pin	Header Pin	Signal	FPGA Pin
1	P5V_R	na	2	GND	na
3	Unused	T1	4	Link1	T2
5	Unused	T3	6	Logic1	R4
7	Unused	U1	8	Logic1	U2
9	Unused	V2	10	Link2	T4
11	Unused	V3	12	Logic0	V4
13	Unused	W1	14	Logic0	W2
15	Unused	W3	16	Link3	W4
17	Unused	Y2	18	Logic1	Y3
19	Unused	AA2	20	Logic1	AA4
21	Unused	AB1	22	Link4	AB3
23	Unused	AB4	24	Logic0	AC4
25	Unused	Y5	26	Logic0	AA5
27	Unused	AB5	28	Link5	AA6
29	Unused	Y6	30	Logic1	AC5
31	Unused	AB6	32	Logic1	AC6
33	Unused	Y7	34	Link6	AA7
35	Unused	AB7	36	Logic0	AC7
37	Unused	Y8	38	Unused	AA8
39	Unused	AB8	40	Unused	AC10

Table 3-6. Header Strip J5

Header Pin	Signal	FPGA Pin	Header Pin	Signal	FPGA Pin
1	PCI_VI0	na	2	GND	na
3	Unused	W20	4	Unused	W21
5	Unused	W22	6	Unused	V23
7	Unused	V20	8	Unused	V21
9	Unused	V22	10	Unused	U23
11	Unused	T20	12	Unused	T21
13	Unused	T22	14	Unused	T23
15	Unused	R20	16	Unused	R21
17	Unused	R22	18	Unused	R23
19	Unused	P20	20	Unused	P21
21	Unused	P22	22	Unused	P23
23	Unused	N21	24	Unused	N22
25	Unused	N23	26	Unused	M21
27	Unused	C5	28	Unused	na
29	Unused	D5	30	Unused	na
31	Unused	B19	32	Unused	E21
33	Unused	C19	34	Unused	F20
35	Unused	D19	36	Unused	F21
37	Unused	D23	38	Unused	G20
39	Unused	E20	40	Unused	G21

RT Address Jumpers

The RT address is set via jumpers fitted to J4. Table 3-7 shows jumper settings for RT 0 to RT 4 (you can also set RT addresses 5 to 30, though they are not shown). The jumpers set the RTADDR and RTADDRP inputs on the Core1553BRT core. The PCB is shipped with the jumpers set to RT 1. If the jumpers are set incorrectly the 1553B RT core does not respond to any 1553B messages and the RT Address error back panel LED lights up.

Table 3-7. RT Address Jumpers

J4			RT0	RT1	RT2	RT3	RT4
2	GND						
4	Link 1	RTADDR 0	0	1	0	1	0
6	VCC						
8	VCC						
10	Link 2	RTADDR 1	0	0	1	1	0
12	GND						
14	GND						
16	Link 3	RTADDR 2	0	0	0	0	1
18	VCC						
20	VCC						
22	Link4	RTADDR 3	0	0	0	0	0
24	GND						
26	GND						
28	Link 5	RTADDR 4	0	0	0	0	0
30	VCC						
32	VCC						
34	Link 6	RTADDR P	1	0	0	1	0
36	GND						

You can override the RT number with the control register.

1553BRT Bus Connections

The 1553BRT development card uses DIRECT 1553B connections. You can convert the card to a Transformer coupling by removing the four 50R resistors and fitting links to connect the transformers directly to the 1553B connectors. Please contact Actel customer support for help if this is required.

1553BRT Demo Card Address Map

The 1553B RT demo card uses a single PCI BAR register, BAR0, and requires 32K bytes of memory (0000hex-7FFFhex). The lower half of this address directly addresses the 16K bytes of SSRAM memory. The upper 16K access the four control registers.

The 1553B RT demo design supports two RT memory maps, in standard mode the memory is mapped in the default mode as defined in the *Core1553BRT Data Sheet*. In extended mode and address mapper function is implemented as described in the *Core1553BRT User Guide* (these documents are available in the *docs* directory on the CD). The ADDRMAPPER bit in the control register enables the extended address mode.

Standard Address Map

Only the first 4K bytes (0000 hex-0fff hex) of memory is used. This memory is split into sixty-four data buffers. Each buffer holds 64 bytes and has a receive and a transmit buffer, as shown in .

The memory allocated to the unused receive sub-addresses 0 and 31 is used to provide status information back to the rest of the system. At the end of every

transfer, the 1553B command word or the transfer status word, TSW, is written to these locations.

Table 3-8. Standard Address Map Summary

Address	RAM contents	
000	RX transfer status words	The core only writes to these addresses
040	Receive subaddress 1	
	…	
780	Receive subaddress 30	
7C0	TX transfer status words	
800	Not used	The core only reads from these addresses
840	Transmit subaddress 1	
	…	
E40	Transmit subaddress 30	
FC0	Not used	

Extended Address Map

The extended address map uses 16K-byte of memory. Each sub-address is allocated 64 words and separate buffers are provided for non-broadcast receive, transmit and broadcast, receive and transmit (as shown in Table 3-9).

Table 3-9. Extended Mode Address Map

Byte Address	
0000-007F	Mode Code SA=00 T/R=0
0080-00FF	Receive Sub-address 1
….	….
0F00-0F7F	Receive Sub-address 30
0F80-0FFF	Mode Code SA=31 T/R=0
1000-107F	Mode Code SA=00 T/R=1
1080-10FF	Transmit Sub-address 1
….	….
1F00-1F7F	Transmit Sub-address 30
1F80-1FFF	Mode Code SA=31 T/R=1
2000-207F	Mode Code SA=00 T/R=0
2080-20FF	Broadcast Receive Sub-address 1
….	….
2F00-2F7F	Broadcast Receive Sub-address 30
2F80-2FFF	Broadcast Mode Code SA=31 T/R=0
3000-307F	Broadcast Mode Code SA=00 T/R=1
3080-30FF	Broadcast Transmit Sub-address 1
….	….
3F00-3F7F	Broadcast Transmit Sub-address 30
3F80-3FFF	Broadcast Mode Code SA=31 T/R=1

Each non-mode code sub-address consists of 64 words, the command word or TSW value is written to location 0, and the associated data words are stored at locations 32 to 63 (as in Table 3-10).

Table 3-10. Extended Mode Non Mode Code Address Map

Byte Address	
0000	CMDWORD or TSWVALUE
0002	Not used
….	…
003E	Not used
0040	Data Word 0
0042	Data Word 1
….	…
007C	Data Word 30
007E	Data Word 32

The command word or TSW value is written to location 0 plus the mode code value, and the data word is stored at location 64 plus the mode code value. For example:

- Synchronize with data command - the command word is stored at location 17 (22 hex) and the data written to location 49 (62 hex).

- Transmit vector word command - the command word is stored in location 16 (1020 hex) and the vector word read from location 48 (1060 hex).

Note: Separate address spaces exists for transmit and receive mode codes and broadcast transmit and receive mode codes. Table 3-11 shows the mode code address mapping for non-broadcast sub-address 0.

Table 3-11. Extended Mode Code Address Map

RX Byte Address T/R=0 SA=00		TX Byte Address T/R=1 SA=00
0000	CMDWord or TSWVALUE for Modecode WC=00000	1000
0002	CMDWord or TSWVALUE for Modecode WC=00001	1002
…		…
003C	CMDWord or TSWVALUE for Modecode WC=11110	103C
003E	CMDWord or TSWVALUE for Modecode WC=11111	103E
0040-005F	Not used (data storage for mode codes without data)	1040-105F
	Modecode Data WC=10000 (Txt Vector Word)	1060
0062	Modecode Data WC=10000 (Synchronize with data)	
….	…	….
007C	Modecode Data WC=11110	107C
007E	Modecode Data WC=11111	107E

Control Registers

Six 32-bit control registers are provided, these are mapped to PCI addresses 4000 hex to 4017 hex (as shown in Table 3-12).

Table 3-12. Control Register Description

Address	Register	Description
4000-4003	Control	This register sets the control inputs on the 1553BRT core
4004-4007	RTStatus	This register sets the values of the 1553B status bits used by the 1553B RT.
4008-400B	Interrupt Vector and Vector Word	This register allows the PCI interface to read the INVECT output from the 1553B RT core and set the vector word input
400C-400F	Transmit Sub-address enables	This allows the transmit sub-addresses to be illegalized
4010-4013	Receive Sub-address enables	This allows the receive sub-addresses to be illegalized
4014-4017	Message Count	Counts the number of 1553B messages received

Table 3-13. 1553BRT Control Register, 4000 hex

Bits	Type	Reset Value	Function
31:17	RO	0	Reserved, returns '0'
18	RO	0	Memory Fail, this should never be set
17	RW	1	AUTOLOOP. When enabled the SSRAM interface automatically copies received 1553B data from the receive sub-address to the transmit sub-address after a 1553B message has been received.
16	RW	0	ADDRMAPPER. When '0' the 1553BRT uses the standard memory map. When '1' the 1553BRT uses the extended memory map

Table 3-13. 1553BRT Control Register, 4000 hex (Continued)

Bits	Type	Reset Value	Function
15	RO	0	Reserved, returns '0'
14	RW	0	INTENBBR (Core1553BRT input, refer to the Core1553B datasheet)
13	RW	0	SA30LOOP (Core1553BRT input, refer to the Core1553B datasheet)
12	RW	0	EXTMDATA (Core1553BRT input, refer to the Core1553B datasheet)
11	RW	0	WRTCMD (Core1553BRT input, refer to the Core1553B datasheet)
10	RW	1	WRTTSW (Core1553BRT input, refer to the Core1553B datasheet)
9	RW	1	BCASTEN (Core1553BRT input, refer to the Core1553B datasheet)
8	RW	0	CLRERR (Core1553BRT input, refer to the Core1553B datasheet)
7	RO	0	RT Address Error (Core1553BRT output, refer to the Core1553B datasheet)
6	RW	0	Use RT Address - When '0' the RT address is set by the RT address jumpers on the PCB; When '1' the RT address is set by bits 5:0 below
5	RW	0	RT Address Parity (Core1553BRT input, refer to the Core1553B datasheet)
4:0	RW	00000	RT Address (Core1553BRT input, refer to the Core1553B datasheet)

Table 3-14. 1553B RT Status Word Setting, 4004 hex

Bits	Type	Reset Value	Function
31:4	RO	0	Reserved, return '0'
3	RW	0	Service Request (Core1553BRT input, refer to the Core1553B datasheet)
2	RW	0	Subsystem Flag, (Core1553BRT input, refer to the Core1553B datasheet)
1	RW	0	Busy, (Core1553BRT input, refer to the Core1553B datasheet)

Table 3-14. 1553B RT Status Word Setting, 4004 hex

Bits	Type	Reset Value	Function
0	RW	0	Terminal Flag, (Core1553BRT input, refer to the Core1553B datasheet)

Table 3-15. 1553B RT Interrupt and Vector Word Register, 4008 hex

Bits	Type	Reset Value	Function
31	RW	0	Interrupt Pending, writing a '1' will clear
30	RW	0	Interrupt Enable
29	RO	0	Good Block Received
28	RO	0	Broadcast Received
27	RO	0	Mode Code Received
26	RO	0	Transmit '1' or Receive '0'
25:21	RO	00000	Sub Address
20:16	RO	00000	Word Count
15:0	RW	0000	Vector Word Value

Table 3-16. 1553B RT Transmit Sub-Address Enables Register, 400C hex

Bits	Type	Reset Value	Function
31	RW	1	Reserved
30:1	RW	1	Enables transmits from sub-address 30 to 1. Bit 1 enables sub-address 1 etc.
0	RW	1	Reserved

Table 3-17. 1553BRT Receive Sub-Address Enables Register, 4010 hex

Bits	Type	Reset Value	Function
31	RW	1	Reserved
30:1	RW	1	Enables receives from sub-address 30 to 1. Bit 1 enables sub-address 1 etc.
0	RW	1	Reserved

Table 3-18. 1553B Message Count Register, 4014 hex

Bits	Type	Reset Value	Function
31:0	RW	00000000	Counts the number of good 155B messages received; the count values are reset by writing zero

Setting Registers to Defaults

To set the 1553B RT to operate as RT 1, set up the control registers as shown in Table 3-19.

Table 3-19. Setting the Default Register

Register	Address	Value (hex)
Control	4000	00020641 hex
RTStatus	4004	00000000 hex
Interrupt/VW	4008	00001234 hex
TXEnable	400C	FFFFFFFF hex
RXEnable	4010	FFFFFFFF hex

These setting also enable the AUTOLOOP function with the TSW word written to memory. The RT vector word is set to 1234 hex and all sub-addresses are enabled.

Note: After you run the memory test procedure from the GUI you need to reset the control registers to the desired values.

Core1553BRT DevKit Contents

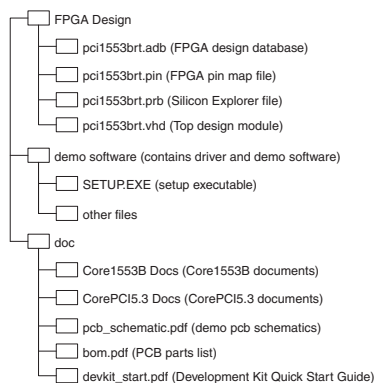The contents of the Core1553BRT Development Kit are shown in Figure A-1.

```
┌── FPGA Design
│       ├── pci1553brt.adb (FPGA design database)
│       ├── pci1553brt.pin (FPGA pin map file)
│       ├── pci1553brt.prb (Silicon Explorer file)
│       └── pci1553brt.vhd (Top design module)
├── demo software (contains driver and demo software)
│       ├── SETUP.EXE (setup executable)
│       └── other files
└── doc
        ├── Core1553B Docs (Core1553B documents)
        ├── CorePCI5.3 Docs (CorePCI5.3 documents)
        ├── pcb_schematic.pdf (demo pcb schematics)
        ├── bom.pdf (PCB parts list)
        └── devkit_start.pdf (Development Kit Quick Start Guide)
```

Figure A-1. Core1553BRT DevKit Contents

Removing the 1553BRT Demo Card

To uninstall the demo card:

1. **Shut down your PC.**

2. **Remove the PCI Development Card using static-safe procedures.**

3. **Boot your PC.** Login as Administrator (if required).

4. **Remove the software.** Go to Control Panel -> Add Remove Programs and select "Actel CorePCI Device Driver and Application" and click "Remove".

5. **Reboot if required.**

B

Product Support

Actel backs its products with various support services including Customer Service, a Customer Applications Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Actel U.S. Toll-Free Line

Use the Actel toll-free line to contact Actel for sales information, technical support, requests for literature about Actel and Actel products, Customer Service, investor information, and using the Action Facts service.

The Actel toll-free line is (888) 99-ACTEL.

Customer Service

Contact Customer Service for nontechnical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call (408) 522-4480.
From Southeast and Southwest U.S.A., call (408) 522-4480.
From South Central U.S.A., call (408) 522-4434.
From Northwest U.S.A., call (408) 522-4434.
From Canada, call (408) 522-4480.
From Japan, call (408) 522-4743.
From the rest of the world, call (408) 522-4743.
Fax, from anywhere in the world (408) 522-8044.

European customers should contact their local sales representative. See the Actel website at http://www.actel.com/contact/offices/index.html for a complete list of local offices.

Customer Applications Center

Actel staffs its Customer Applications Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Applications Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your question(s).

Guru Automated Technical Support

Guru is a web-based automated technical support system accessible through the Actel home page (**http://www.actel.com/guru/**). Guru provides answers to technical questions about Actel products. Many answers include diagrams, illustrations, and links to other resources on the Actel web site. Guru is available 24 hours a day, seven days a week.

Web Site

Actel has a World Wide Web home page where you can browse a variety of technical and nontechnical information. Use a Net browser (Netscape recommended) to access Actel's home page.

The URL is **http://www.actel.com**. You are welcome to share the resources provided on the Internet.

Please visit the Intellectual Property portion of our web site. It lists supported cores, documentation, and development boards for use with these cores.

There is also a Technical Documentation area on our website that contains information regarding products, technical services, current manuals, and release notes.

You can visit the Product Support area of the Actel website from your Designer software. Click the Product Support button in your Designer Main Window to access the latest datasheets, application notes, and more.

FTP Site

Actel has an anonymous FTP site located at **ftp://ftp.actel.com**. Here you can obtain library updates, software patches, design files, and data sheets.

Contacting the Customer Applications Center

Highly skilled engineers staff the Customer Applications Center from 7:30 A.M. to 5:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Electronic Mail

You can communicate your technical questions to our e-mail address and receive answers back by e-mail, fax, or phone. Also, if you have design problems, you can e-mail your design files to receive assistance. We constantly monitor the e-mail account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support e-mail address is **tech@actel.com**.

Telephone

Our Technical Message Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:30 A.M. to 5:00 A.M., Pacific Time, Monday through Friday.

The Customer Applications Center number is (800) 262-1060.

If you are a European customer, contact your local sales office. Visit the actel website at http://www.actel.com/contact/offices/index.html for information on your local sales office.

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