SmartFusion2 SoC FPGA, Errata

v2.1 February 2014

This Errata sheet contains information about known issues specific to the SmartFusion®2 device family and provides available fixes and solutions.

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Table 1: **Revision History**

Date	Version	Changes
February 2014	2.1	Updated information about ISP programming mode and clarified MDDR/FDDR usage in the M2S050 device.
December 2013	2.0	Updated USB ULPI – Item 5. Added Item 13. Power-up Digest is not supported. Updated additional programming support (SPI Slave and M3 ISP). Added SHA-256 System Service to Usage Guidelines section.
October 2013	1.1	Added Item12.
October 2013	1.0	Removed Package Errata section. Removed all ES and PP devices.*
*Contact Microsemi SoC technical support for information on ES and PP devices.		

Table 2: **Revisions Released per Device**

Silicon Devices	Revisions	Device Status
M2S050	Commercial/Industrial	Advanced
M2S025	Commercial/Industrial	Advanced
M2S010	Commercial/Industrial	Advanced
M2S005	Commercial/Industrial	Advanced

Device Errata for SmartFusion2 Commercial and Industrial Devices

Table 3 lists the specific device issues and the affected SmartFusion2 Commercial and Industrial devices.

Table 3: **Summary of SmartFusion2 Devices Errata**

No.	Issues	Affected Devices/ Revisions / Software	Fixed in Device/Software/Revisions
1.	The MDDR and FFDR AXI interface does not support exclusive access in the M2S050 devices	M2S050	The future Production version of the Errata will have updated information regarding this issue for the M2S050 device.
2.	Apply DEVRST_N after ISP programming	M2S050	Additional programming modes will be supported in future Production devices.
3.	AXI wrap transfers with more than 32 bytes in burst mode are not supported for MDDR and FDDR in the M2S050 devices	M2S050	The future Production version of the Errata will have updated information regarding this issue for the M2S050 device.
4.	The MDDR/FDDR controller must be used with the sequential burst mode with BL = 8 and PHY = 32 or PHY = 16	M2S050	The future Production version of the Errata will have updated information regarding this issue for the M2S050 device.
5.	Use USBD I/O group for USB-ULPI mode in the M2S050-FG896 devices	M2S050	The future Production version of the Errata will have updated information regarding this issue for the M2S050 device.
6.	VPP must be set to 2.5 V when programming/writing at Industrial temperatures range	M2S050 M2S025 M2S010 M2S005	The future Production version of the Errata will have updated information regarding this issue.
7.	Over-voltage support on MSIOs during the Flash*Freeze mode	M2S050 M2S025 M2S010 M2S005	The future Production version of the Errata will have updated information regarding this issue.
8.	Verification of the FPGA fabric at junction temperatures higher than 50°C erroneously indicates a failure	M2S050 M2S025 M2S010 M2S005	The future Production version of the Errata will have updated information regarding this issue.
9.	DDR_OUT and I/O-Reg functional issue due to a software bug	Software issue	Libero SoC v11.1 SP3 fixes the issue.
10.	Dedicated differential I/O driving the reference clock of the CCC may cause a functional issue due to a software bug	Software issue	Libero SoC v11.1 SP3 fixes the issue.
11.	NVM Ready bit in eNVM Status register can generate a false READY signal in the M2S050 devices	M2S050	Updated information will be available in the Production version of the Errata.
12.	Standby IDD and Flash*Freeze IDD for devices currently shipping, may be up to 30% higher than the corresponding datasheet specification	M2S050 M2S025 M2S010 M2S005	The IDD vlaue of future silicon devices will correlate with the Production datasheet.

Table 3: **Summary of SmartFusion2 Devices Errata (continued)**

No.	Issues	Affected Devices/ Revisions / Software	Fixed in Device/Software/Revisions
13.	Power-up Digest is not supported	M2S050 M2S025 M2S010 M2S005	The future Production version of the Errata will have updated information regarding this issue.

Errata Descriptions and Solutions

Look at the new pin assignment and make sure that your board follows the new pin assignment. Contact Microsemi SoC technical support if you have additional questions.

1. The MDDR and FFDR AXI interface does not support exclusive access in the M2S050 devices

The MDDR and FDDR AXI interface in the M2S050 device is compliant with AMBA AXI Protocol Specification v1.0, except for the exclusive access functionality. The future version of the Errata will have updated information about the exclusive access functionality for the AXI interface in the M2S050 Commercial device. This issue is fixed in the M2S010 and M2S025 devices.

2. Apply DEVRST_N after ISP programming

Commercial and Industrial devices support device programming in JTAG, Slave SPI, and ISP programming modes. However, after ISP programming, DEVRST_N needs to be used to reset the device or power cycle the device.

3. AXI wrap transfers with more than 32 bytes in burst mode are not supported for MDDR and FDDR in the M2S050 devices

Do not use wrap transfers with more than 32 bytes in the M2S050 devices. Future versions of the Errata will have more information.

4. The MDDR/FDDR controller must be used with the sequential burst mode with BL = 8 and PHY = 32 or PHY = 16

Although the MDDR and FDDR controllers in the M2S050 devices support various burst modes/lengths and PHY settings (as specified in the *SmartFusion2 SoC FPGA High Speed Serial and DDR Interfaces User's Guide*), only a subset of these settings are supported in the M2S050 devices.

Recommendation for M2S050 Devices

Only use sequential burst mode with BL = 8 for PHY16 or PHY32 modes for the MDDR or FDDR.

5. Use USBD I/O group for USB-ULPI mode in the M2S050-FG896 devices

For interfacing the USB OTG controller with ULPI PHY, the USB MSIO signals are connected to four separate mutually exclusive I/O groups: USBA, USBB, USBC, and USBD I/O. In the M2S050-F896 devices, only the USBD I/O group should be used.

This issue does not apply to the M2S010, M2S025, M2S005 COM/IND devices.

Excluding the M2S050-FG896, other SmartFusion2 devices' availability of the USB ULPI I/O group are package specific and some of the packages do not have any USB ULPI I/O group, refer to the SmartFusion2 Product Brief. In addition, USB is not supported in the VF400, FG484, and FCS325 packages for the M2S050 device.

Solution for M2S050-FG896 Devices

Use channel D for USB I/Os with the M2S050-FG896 devices. For example, The USB_DATA6 can be connected to the I/O through USB_DATA6_A, USB_DATA6_B, and USB_DATA6_C. Use only USB_DATA6_D in the M2S050-FG896 COM/IND device.

6. VPP must be set to 2.5 V when programming/writing at Industrial temperatures range

VPP can be set to 2.5 V or 3.3 V. However, when writing or programming the eNVM of M2S050, M2S025, M2S010, and M2S005 devices below 0°C, VPP must be set to 2.5 V. Refer to the SmartFusion2 System-on-Chip FPGAs datasheet for VPP minimum and maximum settings. Note that the eNVM reading with VPP set to 3.3 V or 2.5 V operates as intended.

7. Over-voltage support on MSIOs during the Flash*Freeze mode

When the input voltage is driven above the reference voltage for that bank, additional current can be consumed in the Flash*Freeze mode for the M2S050, M2S025, M2S010, and M2S005 devices.

8. Verification of the FPGA fabric at junction temperatures higher than 50°C erroneously indicates a failure

In the M2S050, M2S025, M2S010, and M2S005 devices, standalone verification (STAPL VERIFY action) should be run at temperatures lower than 50°C. If a VERIFY action is run at temperatures higher than 50°C, a false verify failure may be reported. Check Digest system services can be used to confirm design integrity at temperatures within the recommended operation conditions.

9. DDR_OUT and I/O-Reg functional issue due to a software bug

This issue only applies if you created or updated your design using Libero SOC v11.1 SP1 or v11.1 SP2. If you have one of the following in your design, the corresponding I/O will not function properly in the silicon due to the wrong software implementation of the I/O macro.

- If you use DDR_OUT macro in your design.
- If you combine an output or output enable register with an I/O using the PDC command set_io <portName> -register yes

Solution:

Both the issues are fixed in Libero SOC v11.1 SP3. Please migrate your design to Libero SOC v11.1 SP3, and re-run Compile and Layout.

10. Dedicated differential I/O driving the reference clock of the CCC may cause a functional issue due to a software bug

If your design has the dedicated differential I/O pair driving the reference clock of the CCC, the input clock may not propagate to CCC due to a software bug and the device will fail during silicon testing. There are several options to drive the ref clock of the CCC. One of the options is to drive from “Dedicated Input PAD x” (x = 0 to 3); this uses hardwired routing. In this option, choose single-ended I/O or differential I/O as the ref clock. This issue exists when you choose the differential I/O option, meaning the dedicated differential I/O is used as CCC reference clock input.

This issue can’t be detected in any functional simulation, and can only be detected in silicon testing.

Solution:

The issue is fixed in the Libero SoC 11.1 SP3. Migrate your design to the Libero SoC 11.1 SP3, and re-run Compile and Layout.

11. NVM Ready bit in eNVM Status register can generate a false READY signal in the M2S050 devices

If you send an instruction to the eNVM controller in the M2S050 device and then start polling the READY signal (bit0 of the eNVM Status register) to check when the eNVM controller is ready for the next function, the first assertion of the READY signal occurs when the eNVM controller is not yet ready, resulting in the generation of a false READY signal. However, the immediate next assertion of the READY signal will correctly indicate that the eNVM controller is ready.

Workaround for M2S050 Devices

The workaround is to add an extra eNVM Status bit read that will poll/read the eNVM Status bit twice as READY.

12. Standby IDD and Flash*Freeze IDD for devices currently shipping, may be up to 30% higher than the corresponding datasheet specification

Standby IDD and Flash*Freeze IDD for the current shipping production (COM and IND) silicon may be up to 30% higher than the corresponding datasheet specification. The IDD value of future silicon devices will correlate with the Production datasheet.

13. Power-up Digest is not supported

The current M2S050, M2S025, M2S010, and M2S005 devices do not support the Power-up Digest feature.

Workaround

The user can use NVM Data Integrity Check System service after the device is on and check the data integrity.

Usage Guidelines for SmartFusion2 Devices

1. Programming support

Microsemi recommends the following conditions for the SmartFusion2 device usage:

- JTAG, SPI Slave, and ISP programming modes only however, after ISP programming use DEVRST_N to reset the device or power cycle the device
- FLASH_GOLDEN_N pin functionality is not currently supported. Contact Microsemi SoC technical support for additional information.

2. SHA-256 System Service

Microsemi recommends the message required to be on byte boundary when using SHA-256 System Service for the SmartFusion2 devices.

3. MSS reset mode

To keep the MSS in reset during normal operation, it is necessary to wait for the device to power up, and then apply the reset. The US_POR_B signal from the MSS (the power-on-reset for the FPGA fabric) can be used to check the device's powered up state.

4. Accessing the PCIe Bridge register in the high speed serial interface

The PCIe® Bridge registers should not be accessed before the PHY is ready. Wait for the PHY_READY signal (which indicates when PHY is ready) to be asserted before updating the PCIe Bridge registers.

The PHY_READY signal is normally asserted within 200 µs after the device is powered up, so wait for 200 µs before accessing the PCIe Bridge registers.

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world **650.318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Microsemi SoC Products Group Customer Support website for more information and support (http://www.microsemi.com/soc/support/search/default.aspx). Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on website.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/soc/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR webpage.

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